TFT LCD Preliminary Specification

MODEL NO.: V470H1 - L01

LCD TV Head Division

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- CONTENTS -

1. GENERAL DESCRIPTION ---------- 3
1.1 OVERVIEW
1.2 FEATURES
1.3 APPLICATION
1.4 GENERAL SPECIFICATIONS
1.5 MECHANICAL SPECIFICATIONS

2. ABSOLUTE MAXIMUM RATINGS ---------- 4
2.1 ABSOLUTE RATINGS OF ENVIRONMENT
2.2 ELECTRICAL ABSOLUTE RATINGS
2.2.1 TFT LCD MODULE
2.2.2 BACKLIGHT INVERTER UNIT

3. ELECTRICAL CHARACTERISTICS ----------6
3.1 TFT LCD MODULE
3.2 BACKLIGHT UNIT
3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS
3.2.2 INVERTER CHARACTERISTICS
3.2.3 INVERTER INTERTFACE CHARACTERISTICS

4. BLOCK DIAGRAM ----------12
4.1 TFT LCD MODULE

5. V470H1-L01 LCD INPUT TERMINAL PIN ASSIGNMENT ----------13
5.1 TFT LCD MODULE LVDS input
5.2 TFT LCD MODULE Power input
5.3 BACKLIGHT UNIT
5.4 INVERTER UNIT
5.5 BLOCK DIAGRAM OF INTERFACE
5.6 LVDS INTERFACE
5.7 COLOR DATA INPUT ASSIGNMENT

6. INTERFACE TIMING ----------21
6.1 INPUT SIGNAL TIMING SPECIFICATIONS
6.2 POWER ON/OFF SEQUENCE

7. OPTICAL CHARACTERISTICS ----------24
7.1 TEST CONDITIONS
7.2 OPTICAL SPECIFICATIONS

8. PRECAUTIONS ----------28
8.1 ASSEMBLY AND HANDLING PRECAUTIONS
8.2 SAFETY PRECAUTIONS

9. MECHANICAL CHARACTERISTICS ----------29

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V470H1-L01 is a 47" thin-film-transistor liquid-crystal (TFT-LCD) module with 32-CCFL Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit/color). The inverter module for backlight is built-in.

1.2 FEATURES

- High brightness (620 nits)
- High contrast ratio (1000:1)
- Fast response time (8 ms)
- High color saturation (NTSC 75%)
- HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
-Optimized response time for 50/60 Hz frame rate
-Ultra wide viewing angle : Super MVA technology
-180 degree rotation display option

1.3 APPLICATION

- TFT LCD TVs

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1042.56(H) x 586.44(V) (47" diagonal)	mm	(1)
Bezel Opening Area	1050.6(H) x 594.4(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch (Sub Pixel)	0.543(H) x 0.543(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-reflective coating Hard coating (3H) Reflection rate: < 2%	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	-	1127	-	mm	Module Size
	Vertical (V)	-	670.8	-	mm	
	Depth (D)	-	55.2	-	mm	-
Weight		-	15000	17000	g	-

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol		Value		Unit	Note
			Min.	Max.		
Storage Temperature	T_{ST}		-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}		0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	X, Y axis	-	50	G	(3), (5)
		Z axis	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}		-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

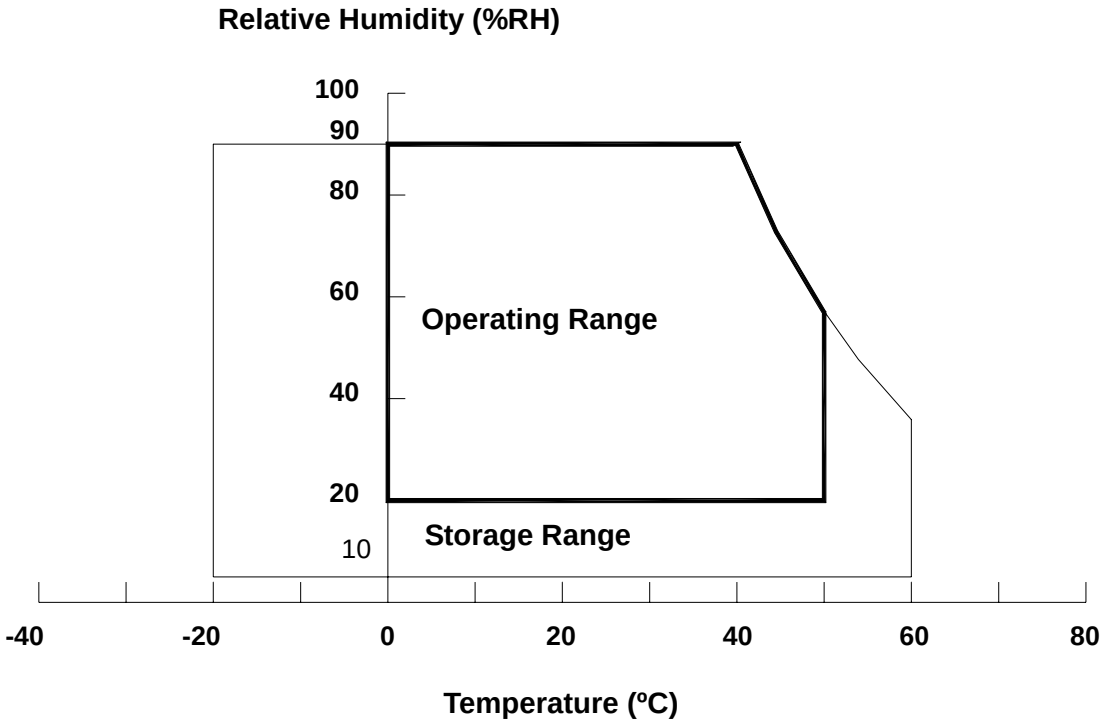
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 60 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in your product design to prevent the surface temperature of display area from being over 60 ºC. The range of operating temperature may degrade in case of improper thermal management in your product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, and ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture. The module would not be twisted or bent by the fixture.



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	20	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT INVERTER UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	5000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	140	V	(1)
Auxiliary Power Supply Voltage	V_{AUX}	0	23	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control, Internal PWM Control, External PWM Control and Internal/External PWM Selection.

3. ELECTRICAL CHARACTERISTICS

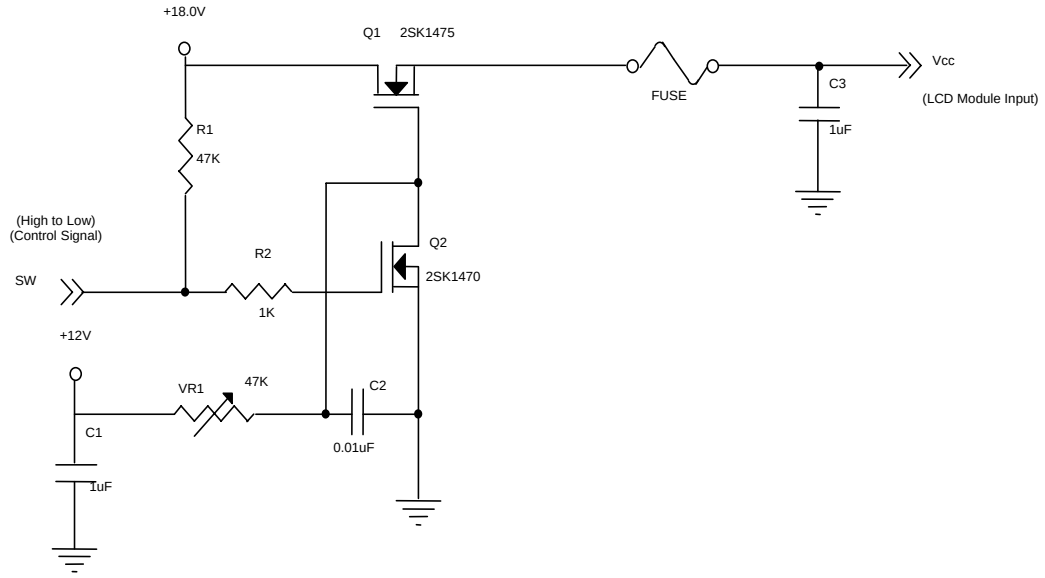
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

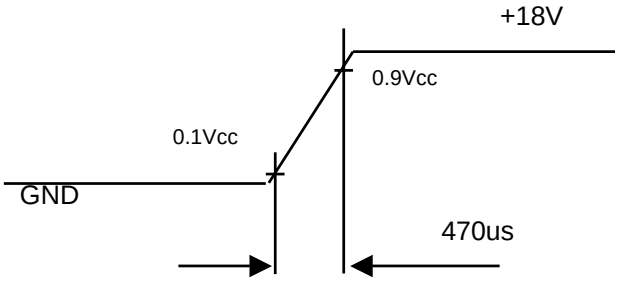
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	16.2	18	19.8	V	(1)
Power Supply Ripple Voltage		V_{RP}	-	-	200	mV	
Rush Current		I_{RUSH}	-	-	4.5	A	(2)
Power Supply Current	White	I_{CC}	-	1	-	A	(3)
	Black		-	0.42	-	A	
	Vertical Stripe		-	TBD	-	A	
LVDS Interface	Differential Input High Threshold Voltage	V_{LVTH}	-	-	+100	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-100	-	-	mV	
	Common Input Voltage	V_{LVC}	1.125	1.25	1.375	V	
	Terminating Resistor	R_T	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc = 18 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

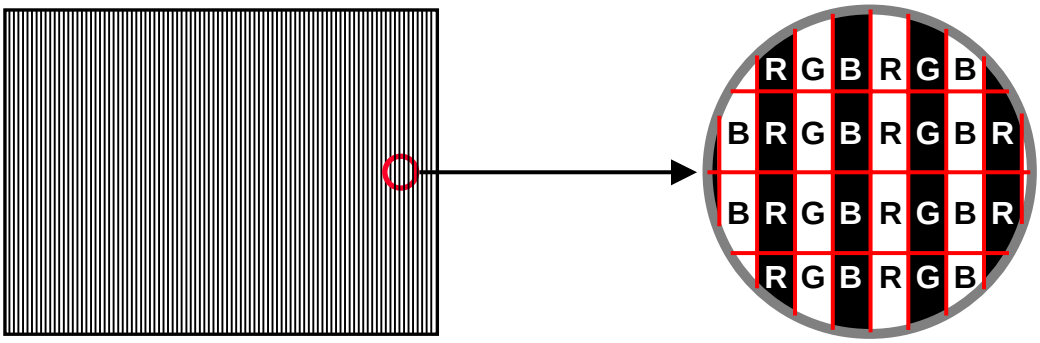
a. White Pattern

Active Area

b. Black Pattern

Active Area

c. Vertical Stripe Pattern



Active Area

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3.2 BACKLIGHT UNIT

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1590	-	V_{RMS}	I_L = 4.5 mA
Lamp Current	I_L	4.0	4.5	5.0	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	2650	-	V_{RMS}	(2), Ta = 0 ºC
		-	2100	-	V_{RMS}	(2), Ta = 25 ºC
Operating Frequency	F_L	40	-	70	KHz	(3)
Lamp Life Time	L_{BL}	50,000	-	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power consumption	P_{BL}	-	216	-	W	(5), I_L = 4.5mA
Power Supply Voltage	V_{BL}	114	120	126	V_{DC}	
Power Supply Current	I_{BL}	-	1.8	-	A	Non Dimming
Auxiliary Power Supply Voltage	V_{AUX}	16	18	20	V_{DC}	
Auxiliary Power Supply Current	I_{AUX}	-	-	650	mA	
Input Ripple Noise	-	-	-	2.5	V_{P-P}	VBL=114V
Backlight Turn on Voltage	V_{BS}	2820	-	5000	V_{RMS}	Ta = 0 ºC
		2090	-	5000	V_{RMS}	Ta = 25 ºC
Oscillating Frequency	F_W	43	46	49	kHz	
Dimming Frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	-	20	-	%	

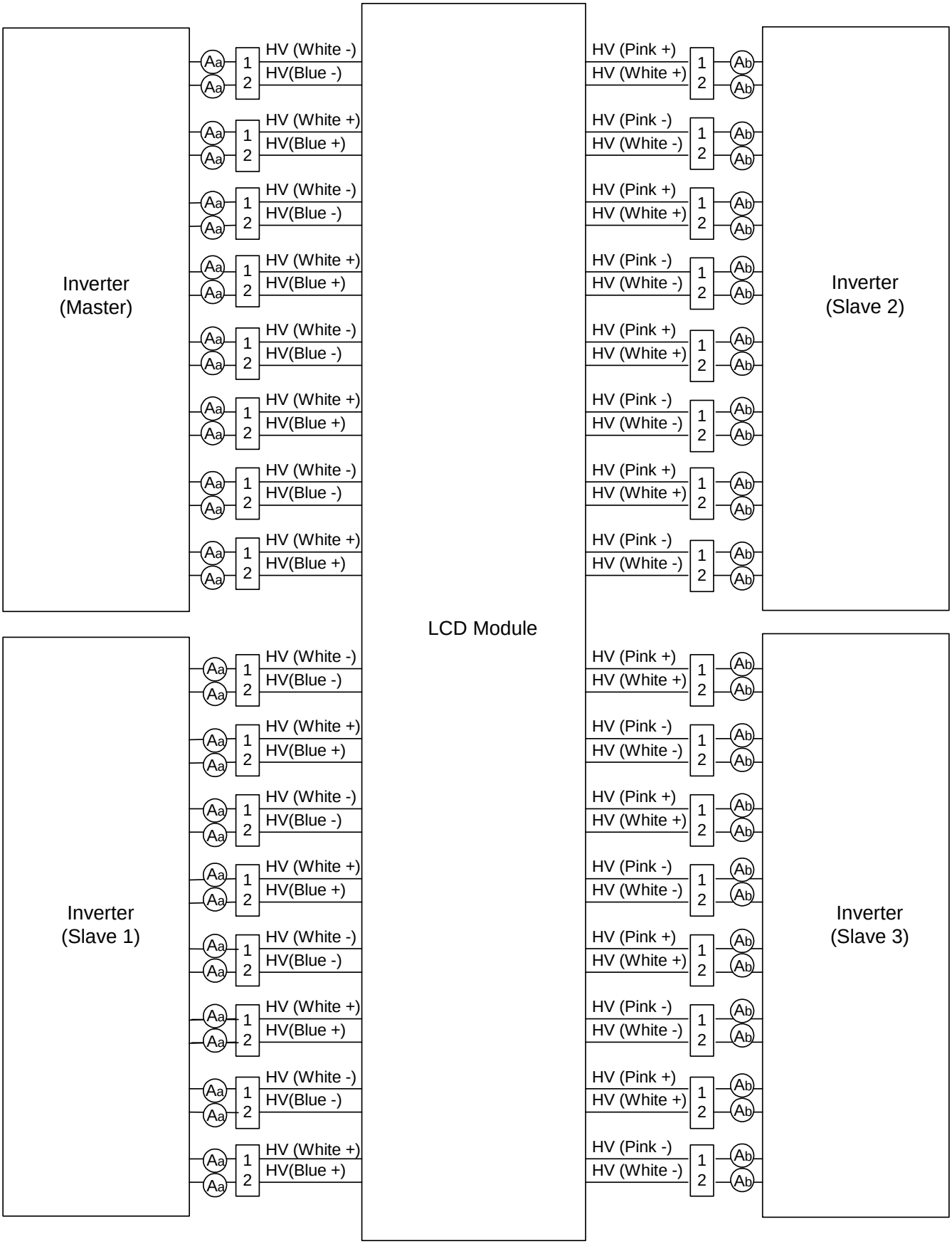
Note (1) Lamp current is measured by utilizing high frequency current meters as shown below:

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 4.0 ~ 5.0 mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.



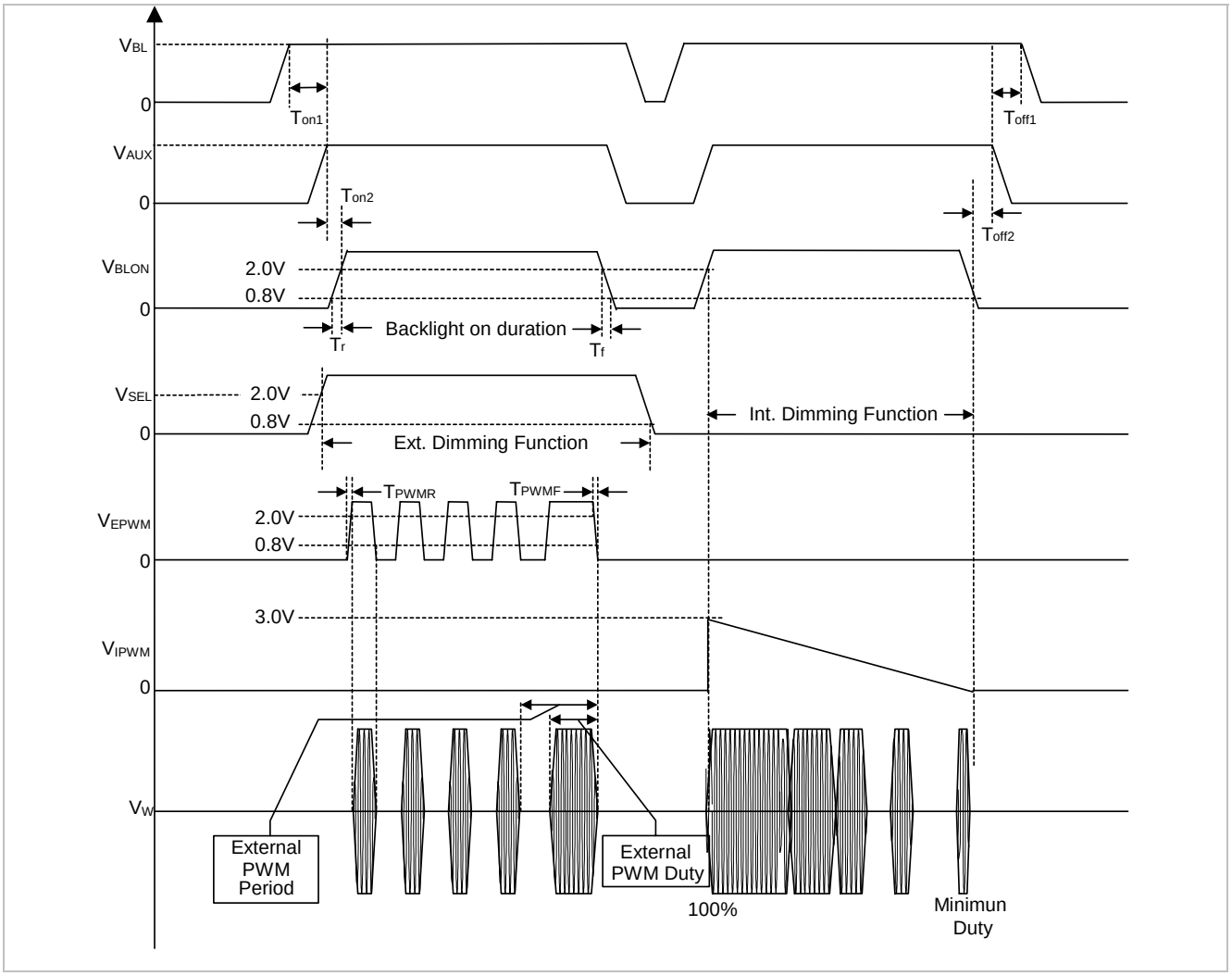
3.2.3 INVERTER INTERTFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
Inverter Good Signal	HI	V_{IG}	V_{IG} = High	2.0	—	5.0	V	Normal Output Voltage
	LO		V_{IG} =Low	0	—	0.8	V	Abnormal Output Voltage
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V	
	OFF		—	0	—	0.8	V	
Internal/External PWM Select Voltage	HI	V_{SEL}	—	2.0	—	5.0	V	
	LO		—	0	—	0.8	V	
Internal PWM Control Voltage	MAX	V_{IPWM}	V_{SEL} = L	—	—	3.0	V	Maximum duty ratio
	MIN			—	0	—	V	Minimum duty ratio
External PWM Control Voltage	HI	V_{EPWM}	V_{SEL} = H	2.0	—	5.0	V	Duty on
	LO			0	—	0.8	V	Duty off
Control Signal Rising Time		Tr	—	—	—	100	ms	
Control Signal Falling Time		Tf	—	—	—	100	ms	
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us	
Input impedance		R_{IN}	—	1	—	—	MΩ	
BLON Delay Time1		T_{on1}	—	1	—	—	ms	
BLON Off Time1		T_{off1}	—	1	—	—	ms	
BLON Delay Time2		T_{on2}	—	1	—	—	ms	
BLON Off Time2		T_{off2}	—	1	—	—	ms	

Note (1) The SEL signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM selection (SEL) during backlight turn on period.

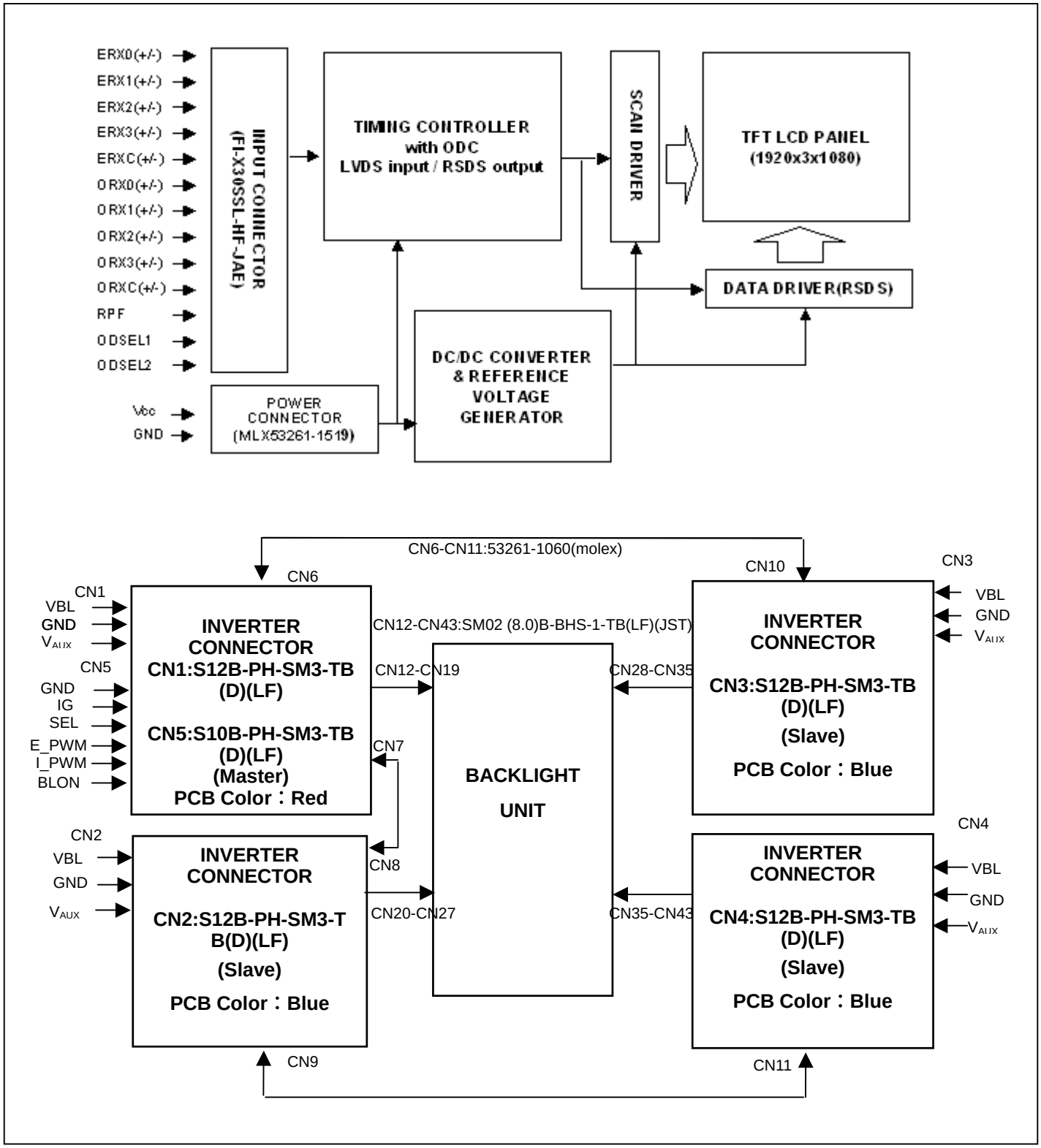
Note (2) The power sequence and control signal timing are shown in the following figure.

Note (3) The power sequence and control signal timing must follow the figure below. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control signal timing.



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE LVDS input

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	GND	Ground	
2	RPF	Display Rotation	(3)
3	NC	No Connection	(4)
4	NC	No Connection	
5	NC	No Connection	
6	ODSEL1	Overdrive Lookup Table Selection	(5)
7	ODSEL2	Overdrive Lookup Table Selection	
8	GND	Ground	
9	ERX0-	Negative transmission data of Even pixel 0	
10	ERX0+	Positive transmission data of Even pixel 0	
11	ERX1-	Negative transmission data of Even pixel 1	
12	ERX1+	Positive transmission data of Even pixel 1	
13	ERX2-	Negative transmission data of Even pixel 2	
14	ERX2+	Positive transmission data of Even pixel 2	
15	ECLK-	Negative of Even clock	
16	ECLK+	Positive of Even clock	
17	ERX3-	Negative transmission data of Even pixel 3	
18	ERX3+	Positive transmission data of Even pixel 3	
19	GND	Ground	
20	ORX0-	Negative transmission data of Odd pixel 0	
21	ORX0+	Positive transmission data of Odd pixel 0	
22	ORX1-	Negative transmission data of Odd pixel 1	
23	ORX1+	Positive transmission data of Odd pixel 1	
24	ORX2-	Negative transmission data of Odd pixel 2	
25	ORX2+	Positive transmission data of Odd pixel 2	
26	OCLK-	Negative of Odd clock	
27	OCLK+	Positive of Odd clock	
28	ORX3-	Negative transmission data of Odd pixel 3	
29	ORX3+	Positive transmission data of Odd pixel 3	
30	GND	Ground	

5.2 TFT LCD MODULE Power input

J1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	VCC	+18.0V power supply	
2	VCC	+18.0V power supply	
3	VCC	+18.0V power supply	
4	VCC	+18.0V power supply	
5	VCC	+18.0V power supply	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	No Connection	(4)
12	NC	No Connection	
13	NC	No Connection	
14	NC	No Connection	
15	NC	No Connection	

Note (1) CNF1 Connector part no.: FI-X30SSL-HF (JAE) or equivalent.

Note (2) CNF2 Connector part no.: 53261-1519 (Molex) or equivalent.

Note (3) Low : normal display (default), High : display with 180 degree rotation

Note (4) Reserved for internal use. Left it open.

Note (5) Overdrive lookup table selection. The overdrive lookup table should be selected in accordance to the frame rate to optimize image quality.

ODSEL2	ODSEL1	Note
L	L	Lookup table was optimized for 60 Hz frame rate.
L	H	Lookup table was optimized for 50 Hz frame rate.
H	L	Reserved. Do not use.
H	H	Reserved. Do not use.

5.3 BACKLIGHT UNIT

The pin configuration for the housing and the leader wire is shown in the table below.

CN12-CN43 (Housing): BHR-03VS-1

Pin	Name	Description	Wire Color
1	HV	High Voltage	Pink
2	HV	High Voltage	White

Note (1) The backlight interface housing for high voltage side is a model BHR-03VS-1, manufactured by JST. The mating header on inverter part number is SM02 (8.0) B-BHS-1-TB (LF)(JST).

5.4 INVERTER UNIT

CN1-CN4 (Header): S12B-PH-SM3-TB (D)(LF)

Pin	Name	Description
1	VBL	+120V Power input
2		
3		
4	NC	NC
5		
6	GND	GND
7		
8		
9		
10		
11	V_{AUX}	+18V
12		

CN5 (Header): S10B-PH-SM3-TB (D)(LF)

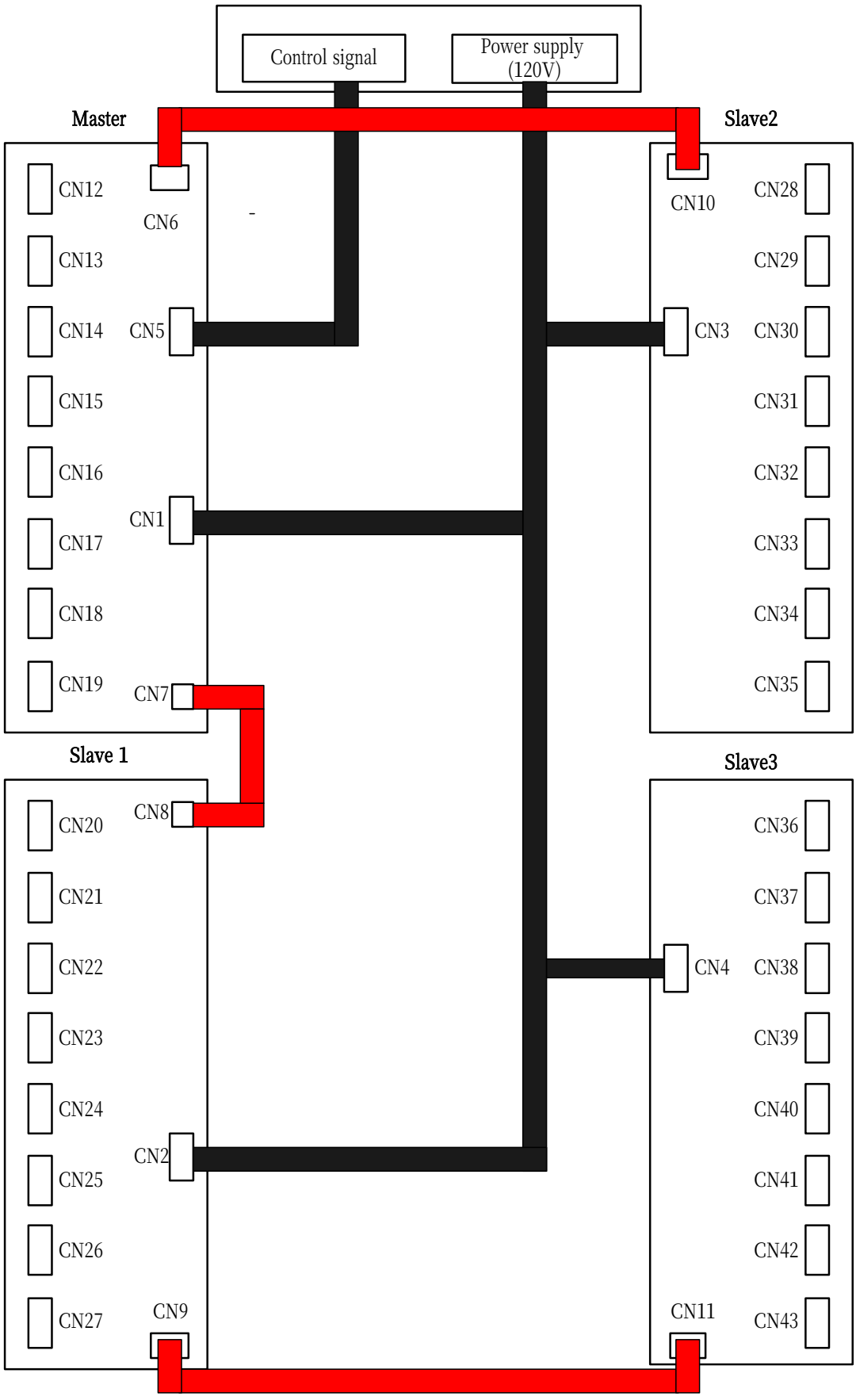
Pin	Name	Description
1	GND	GND
2		
3		
4	NC	NC
5	IG	Inverter Good Signal
6	NC	NC
7	SEL	Internal/external PWM selection High : external dimming Low : internal dimming
8	E_PWM	External PWM control signal E_PWM should be connected to low when internal PWM was selected (SEL = High).
9	I_PWM	Internal PWM control signal I_PWM should be connected to ground when external PWM was selected (SEL = Low).
10	BLON	Backlight on/off control

CN6-CN11 (Header): 53261-1060 (Molex)

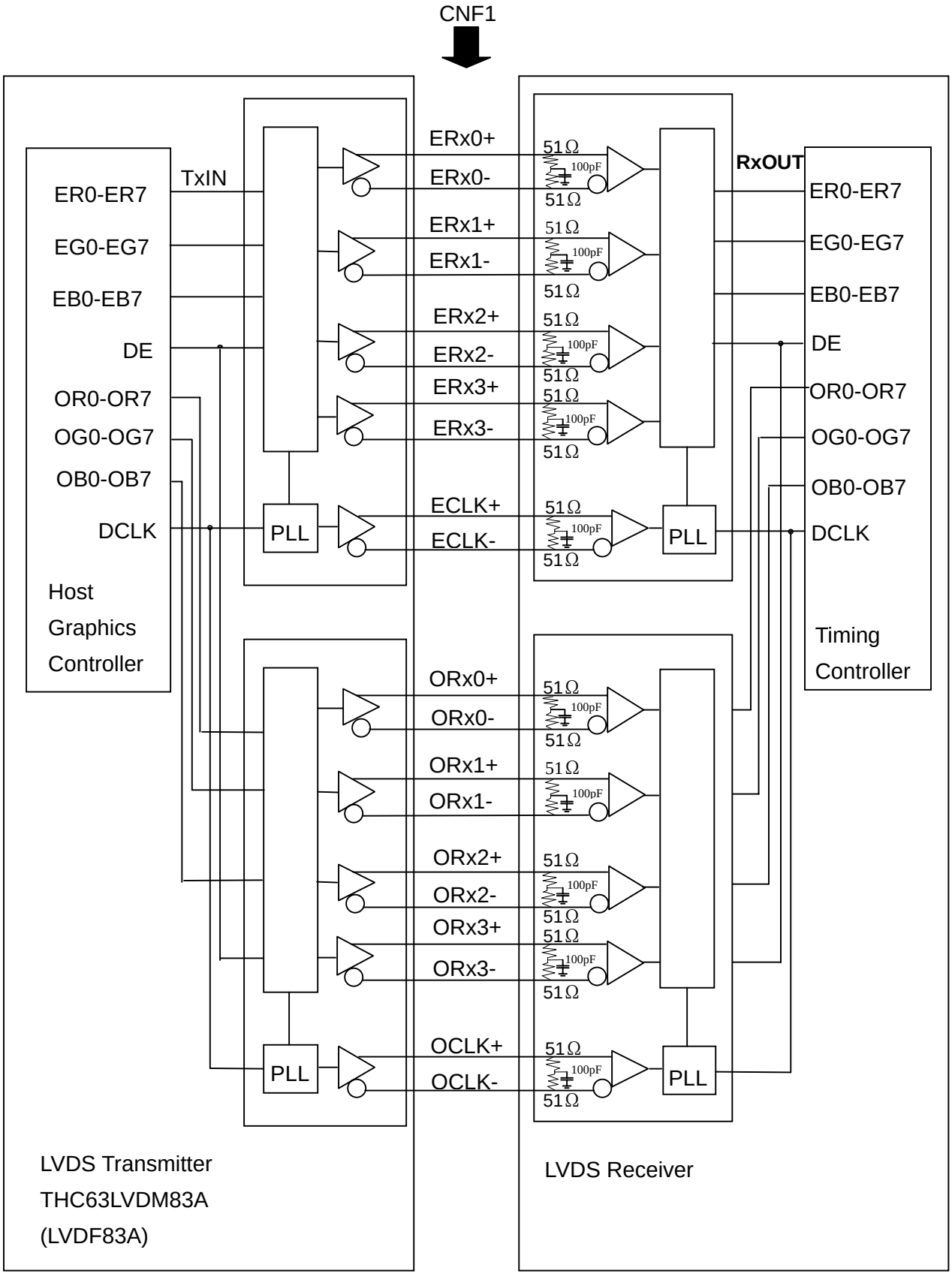
Pin	Name	Description
1	Control Signal	Board to Board
2		
3		
4		
5		
6		
7		
8		
9		
10		

CN12-CN43 (Header): SM02 (8.0) B-BHS-1-TB (LF)(JST)

Pin	Name	Description
1	CCFL HOT	CCFL high voltage
2	CCFL HOT	CCFL high voltage



5.5 BLOCK DIAGRAM OF INTERFACE



ER0~ER7 : Even pixel R data
EG0~EG7 : Even pixel G data
EB0~EB7 : Even pixel B data
OR0~OR7 : Odd pixel R data
OG0~OG7: Odd pixel G data
OB0~OB7 : Odd pixel B data
DE : Data enable signal
DCLK : Data clock signal

Notes: (1) The system must have the transmitter to drive the module.
(2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.
(3) Two pixel data send into the module for every clock cycle. The first pixel of the frame is even pixel and the second pixel is odd pixel.

5.6 LVDS INTERFACE

	SIGNAL	TRANSMITTER THC63LVDM83A		INTERFACE CONNECTOR		RECEIVER THC63LVDF84A		TFT CONTROL INPUT
		PIN	INPUT	Host	TFT-LCD	PIN	OUTPUT	
24bit	R0	51	TxIN0	TA OUT0+	Rx 0+	27	Rx OUT0	R0
	R1	52	TxIN1			29	Rx OUT1	R1
	R2	54	TxIN2			30	Rx OUT2	R2
	R3	55	TxIN3			32	Rx OUT3	R3
	R4	56	TxIN4	TA OUT0-	Rx 0-	33	Rx OUT4	R4
	R5	3	TxIN6			35	Rx OUT6	R5
	G0	4	TxIN7			37	Rx OUT7	G0
	G1	6	TxIN8	TA OUT1+	Rx 1+	38	Rx OUT8	G1
	G2	7	TxIN9			39	Rx OUT9	G2
	G3	11	TxIN12			43	Rx OUT12	G3
	G4	12	TxIN13			45	Rx OUT13	G4
	G5	14	TxIN14	TA OUT1-	Rx 1-	46	Rx OUT14	G5
	B0	15	TxIN15			47	Rx OUT15	B0
	B1	19	TxIN18			51	Rx OUT18	B1
	B2	20	TxIN19			53	Rx OUT19	B2
	B3	22	TxIN20	TA OUT2+	Rx 2+	54	Rx OUT20	B3
	B4	23	TxIN21			55	Rx OUT21	B4
	B5	24	TxIN22			1	Rx OUT22	B5
	DE	30	TxIN26	TA OUT2-	Rx 2-	6	Rx OUT26	DE
	R6	50	TxIN27			7	Rx OUT27	R6
	R7	2	TxIN5			34	Rx OUT5	R7
	G6	8	TxIN10	TA OUT3+	Rx 3+	41	Rx OUT10	G6
	G7	10	TxIN11			42	Rx OUT11	G7
	B6	16	TxIN16			49	Rx OUT16	B6
	B7	18	TxIN17			50	Rx OUT17	B7
	RSVD 1	25	TxIN23	TA OUT3-	Rx 3-	2	Rx OUT23	Not connect
	RSVD 2	27	TxIN24			3	Rx OUT24	Not connect
	RSVD 3	28	TxIN25			5	Rx OUT25	Not connect
	DCLK	31	TxCLK IN	TxCLK OUT+ TxCLK OUT-	RxCLK IN+ RxCLK IN-	26	RxCLK OUT	DCLK

R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.7 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

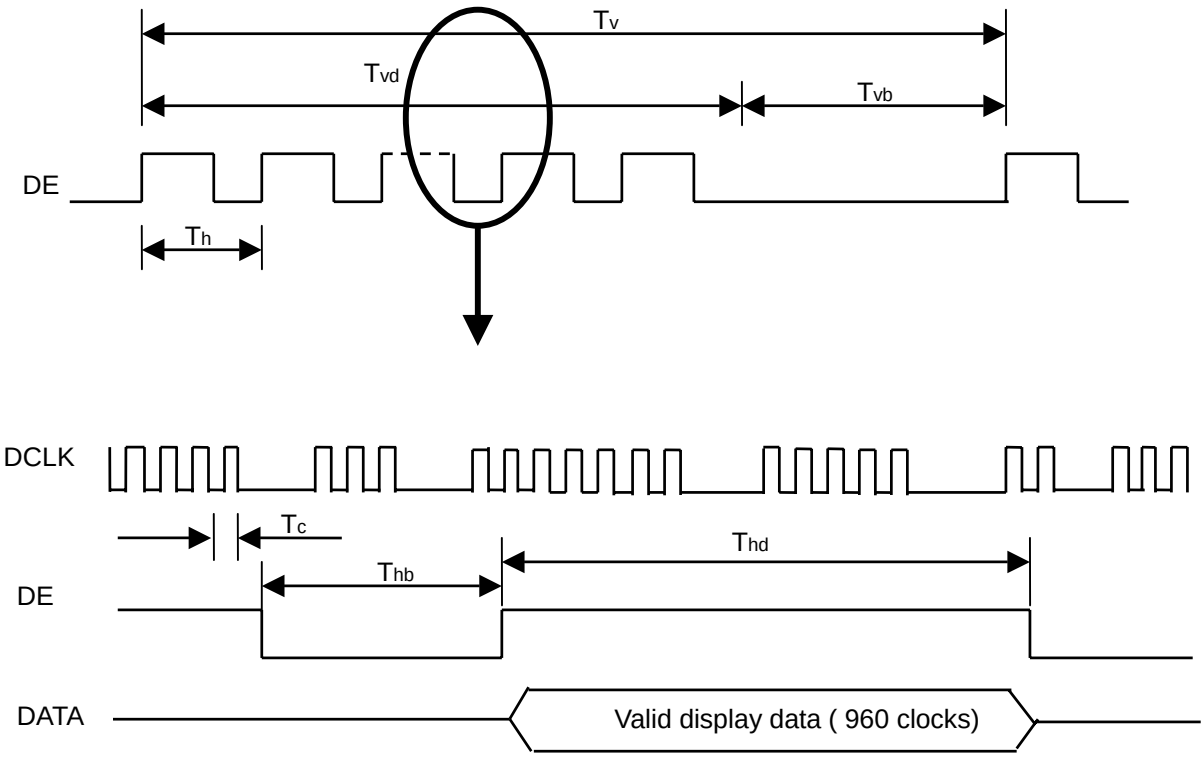
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	1/Tc	(60)	74	(80)	MHz	-
	Input cycle to cycle jitter	Trcl	-	-	200	ps	-
LVDS Receiver Data	Setup Time	Tlvsu	600	-	-	ps	
	Hold Time	Tlvhd	600	-	-	ps	
Vertical Active Display Term	Frame Rate	Fr_5	47	50	53	Hz	(2)
		Fr_6	57	60	63	Hz	(3)
	Total	Tv	(1115)	1125	(1135)	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	-
	Blank	Tvb	(35)	45	(55)	Th	-
Horizontal Active Display Term	Total	Th	(2100)	2200	(2300)	Tc	Th=Thd+Thb
	Display	Thd	1920	1920	1920	Tc	-
	Blank	Thb	(180)	280	(380)	Tc	-

Note (1) Since this module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

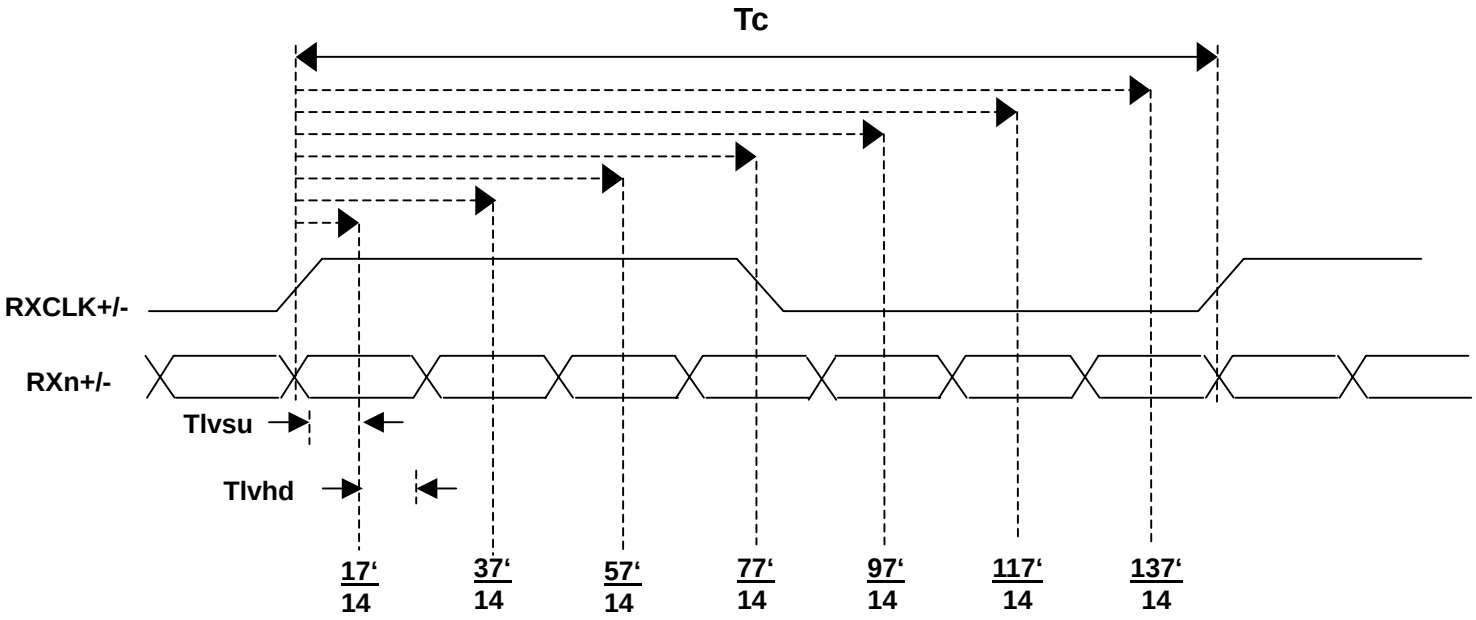
(2) (ODSEL2, ODSEL1) = (L, H). Please refer to 5.1 for detail information.

(3) (ODSEL2, ODSEL1) = (L, L). Please refer to 5.1 for detail information.

INPUT SIGNAL TIMING DIAGRAM

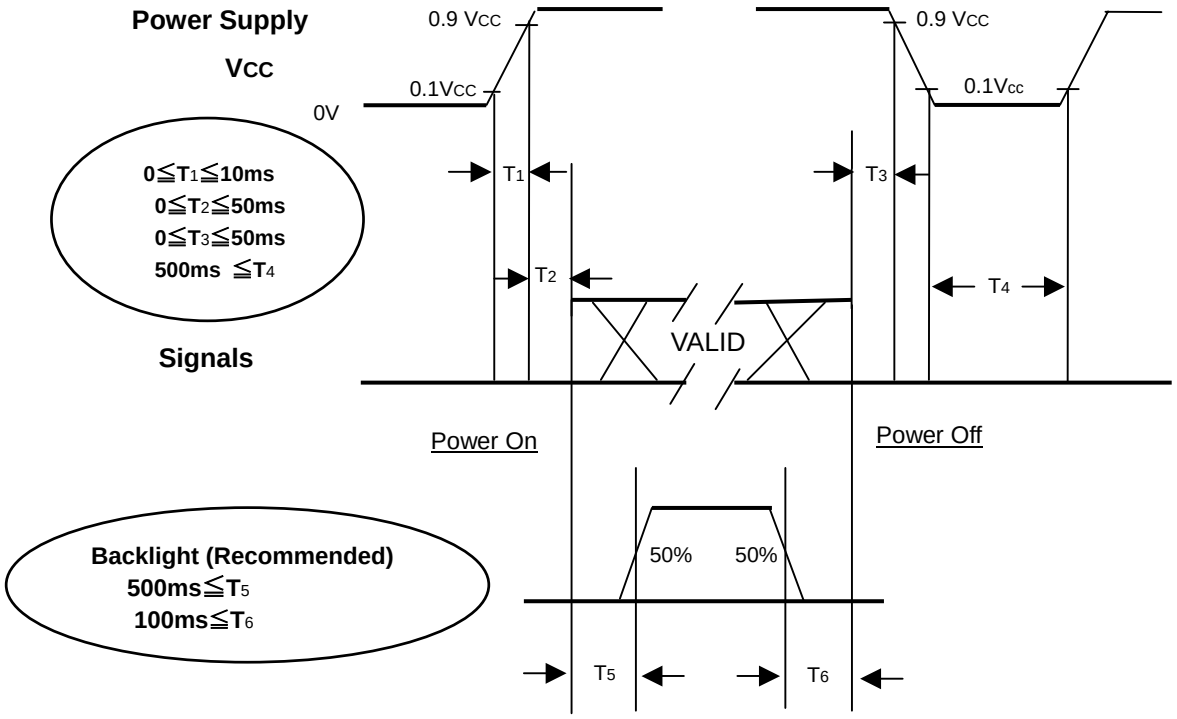


LVDS INPUT INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note.

(1) The supply voltage of the external system for the module input should follow the definition of Vcc.

(2) (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

(3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

(4) T4 should be measured after the module has been fully discharged between power off and on period.

(5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	5.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	4.5±0.5	mA
Oscillating Frequency (Inverter)	F_W	46±3	KHz

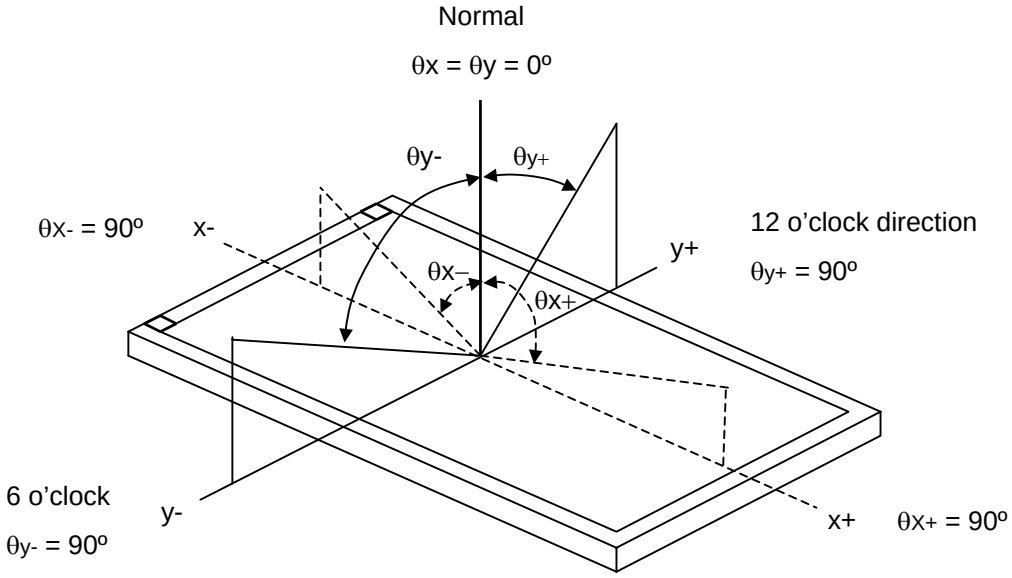
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Normal Angle		(1000)		-	Note (2)
Response Time		Gray to gray			(8)		ms	Note (3)
Center Luminance of White		L_C			(620)		cd/m^2	Note (4)
White Variation		δW				(1.6)	-	Note (7)
Cross Talk		CT				(4)	%	Note (5)
Color Chromaticity	Red	Rx			(0.652)		-	Note (6)
		Ry			(0.331)		-	
	Green	Gx			(0.273)		-	
		Gy			(0.592)		-	
	Blue	Bx			(0.142)		-	
		By			(0.068)		-	
	White	Wx			(0.281)		-	
		Wy			(0.288)		-	
	Color Gamut				75		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	(80)	(88)		Deg.	Note (1)
		θ_x-		(80)	(88)			
	Vertical	θ_Y+		(80)	(88)			
		θ_Y-		(80)	(88)			

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Eldim EZ-Contrast 160R



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

Contrast Ratio (CR) = L255 / L0

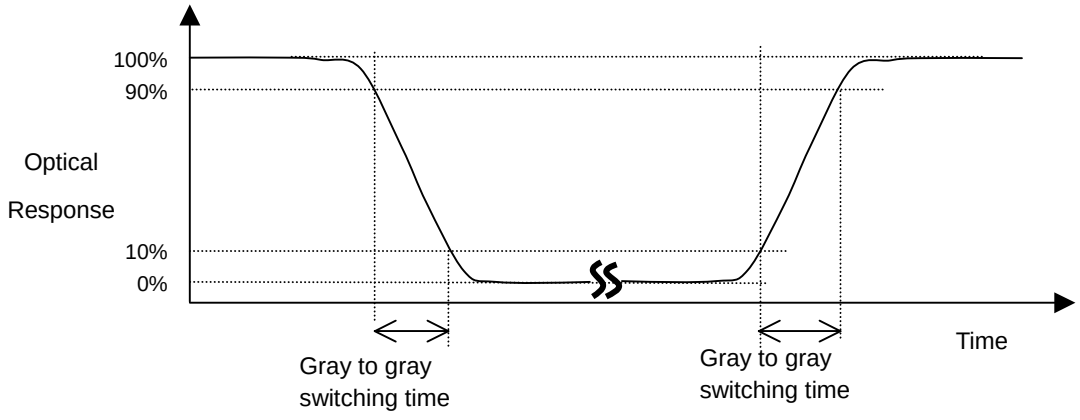
L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5)

CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 63, 127, 191, 255.

Gray to gray average time means the average switching time of gray level 0 ,63,127,191,255 to each other .

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

L (x) is corresponding to the luminance of the point X at the figure in Note (7).

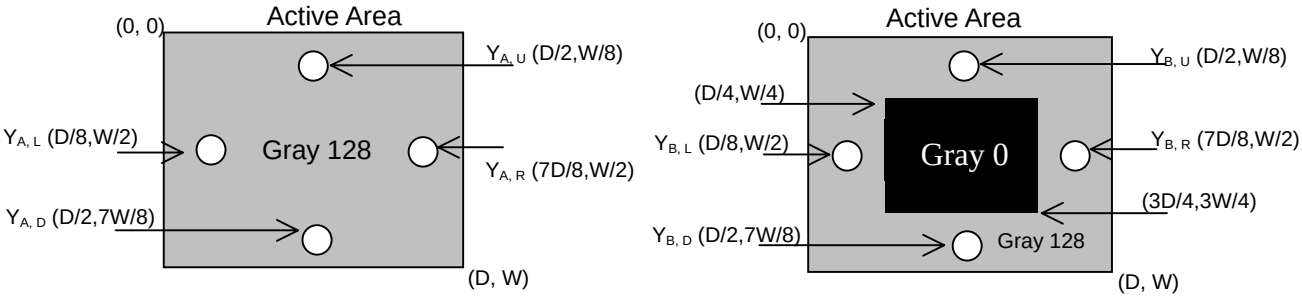
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B – Y_A | / Y_A \times 100$ (%)

Where:

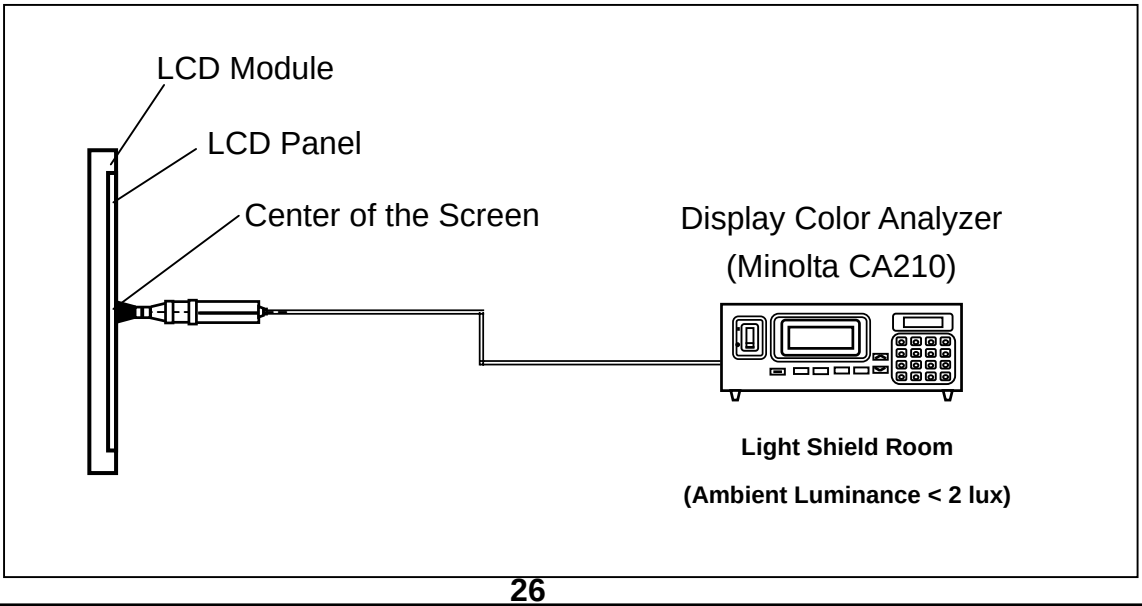
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

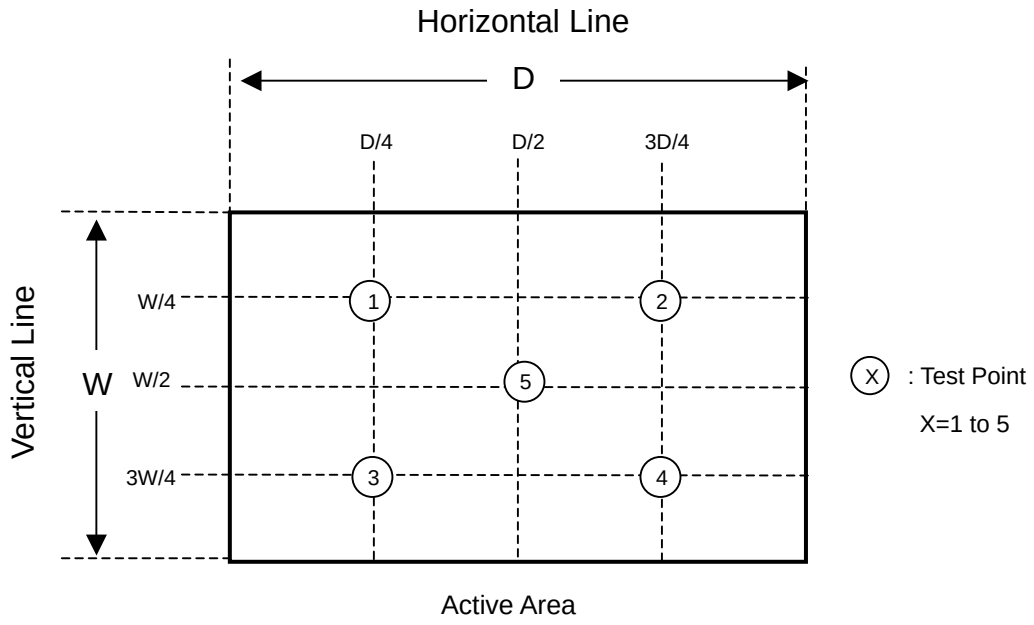
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

9. MECHANICAL CHARACTERISTIC