□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V500DK1
SUFFIX: KS1

Customer:

APPROVED BY SIGNATURE

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Carlos Lee	Archer Chang

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver.1.0	Aug.09,12	All	All	The preliminary specification was first issued.
Ver.2.0	Oct. 11,12	5	1.1	Update OVERVIEW
			1.2	Update FEATURES
		9	2.3.2	Update BACKLIGHT CONVERTER UNIT
		10-11	3.1	Update TFT LCD MODULE
		12-16	3.2	Update BACKLIGHT UNIT
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1. GENERAL DESCRIPTION

1.1 OVERVIEW

V500DK1-KS1 is a 50" TFT Liquid Crystal Display module with LED Backlight unit and 16Lane V-by-one interface. This module supports 3840 x 2160 QFHDTV format and can display true 1.07G colors (8-bit+FRC /color). The driving board module for backlight is built-in.

1.2 FEATURES

- High brightness 400 nits
- High contrast ratio 5000:1
- Fast response time Gray to Gray typical 6.5ms
- High color saturation 72% NTSC
- QFHDTV (3840 x 2160 pixels) resolution, true QFHDTV format
- DE (Data Enable) only mode
- V-by-One interface
- Optimized response time for 120 Hz frame rate
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- 3D Application.

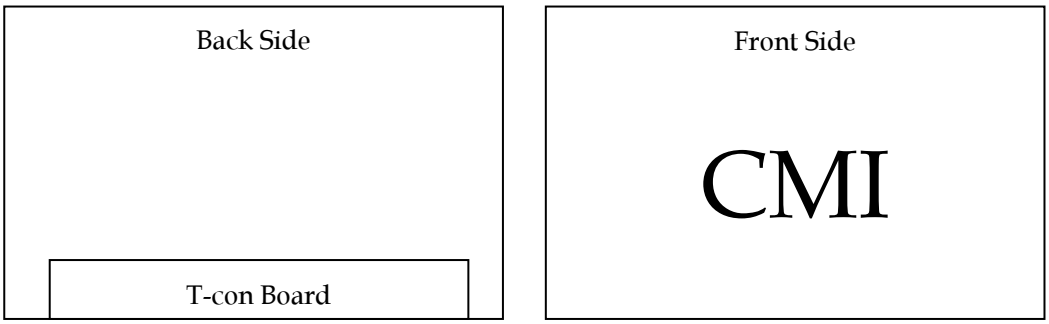
1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1095.84(H) x (V) 616.41 (50" diagonal)	mm	(1)
Bezel Opening Area	1103.04(H) x 622.41(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2160	pixel	-
Pixel Pitch(Sub Pixel)	0.0955(H) x 0.2865(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 1%),Hardness 3H	-	(2)
Rotation Function	Unachievable		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

Note (3)



1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1114.04	1115.04	1116.04	mm	Module Size
	Vertical (V)	637.41	638.41	639.41	mm	
	Depth (D)	15.2	16.2	17.2	mm	To Rear
		26.6	27.6	28.6	mm	To converter cover
	Weight		12900		G	Weight

Note (1)Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

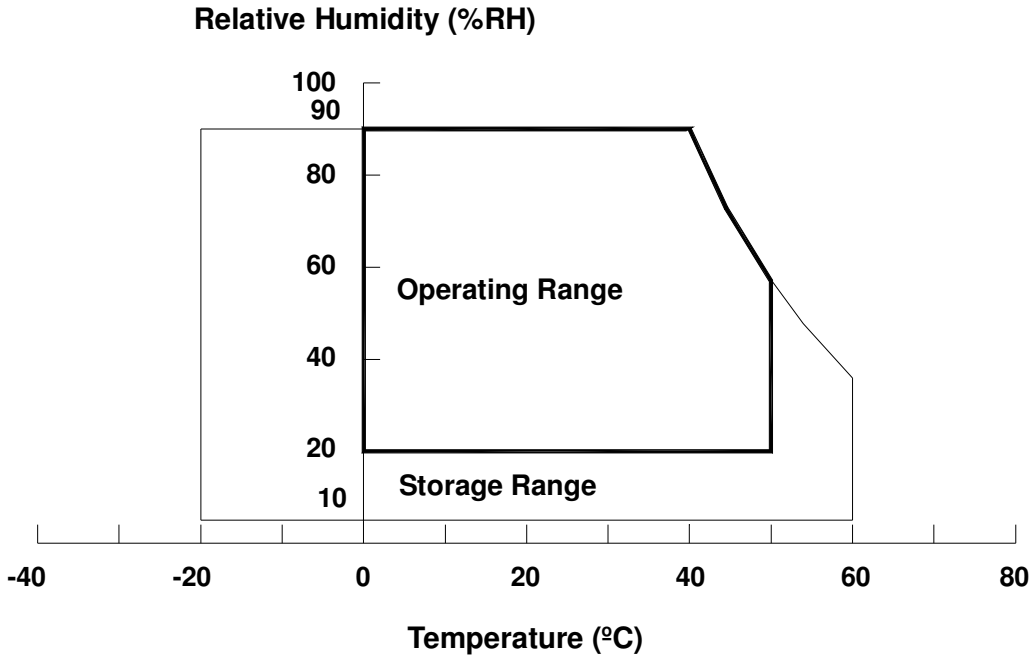
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5)At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note (1)(2)(3)
Light Bar Voltage	V_W	Ta = 25 ℃	-	-	60	V_{RMS}	
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

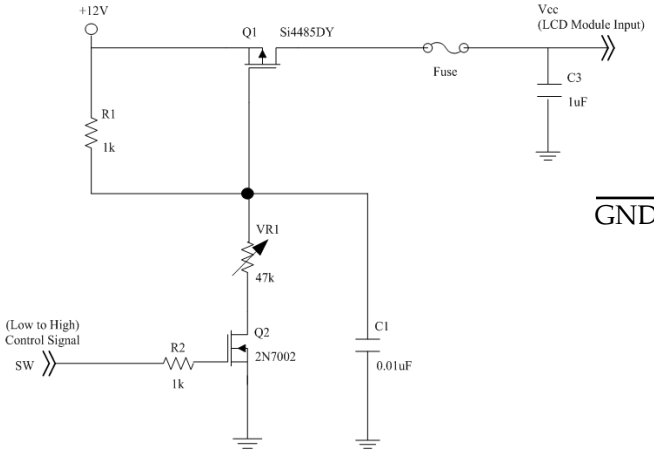
3.1 TFT LCD MODULE

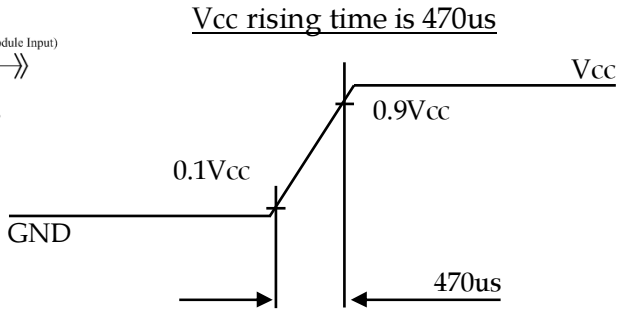
(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		VCC	10.8	12	13.2	V	(1)
Rush Current		IRUSH	—	—	7	A	(2)
Power Consumption	White Pattern	PT	—	16.1	21	W	(3)
	Black Pattern		—	16.2	21		
	Horizontal Pattern		—	34.2	51		
Power Supply Current	White Pattern	—	—	1.37	1.7	A	(3)
	Black Pattern	—	—	1.35	1.7		
	Horizontal Pattern	—	—	2.85	4.2		
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	+300	mV	
	Differential Input Low Threshold Voltage	V_{LVTL}	-300	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
CMOS interface	Input High Threshold Voltage	VIH	2.7	—	3.3	V	
	Input Low Threshold Voltage	VIL	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.)

Note (2) Measurement condition :





Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

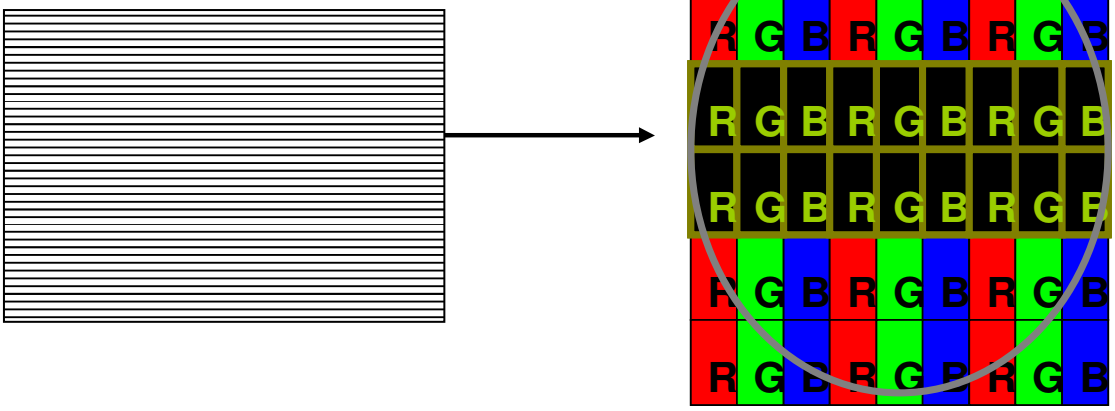
a. White Pattern

Active Area

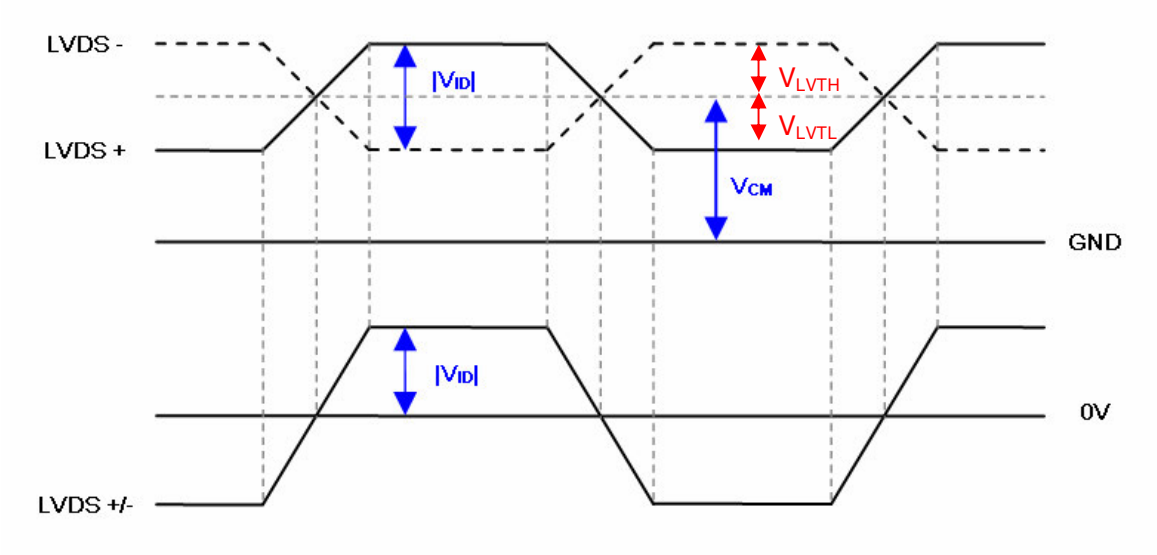
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 LED LIGHT BARCHARACTERISTICS (Ta = 25 ± 2 ºC)

The backlight unit contains 2 pcs LED light bar, and each light bar has 8 string LED

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
One String Current	$I_{L(2D)}$	117.5	125	133	mA	(1)
	$I_{L(3D)}$	376	400	424	mApeak	3D ENA=ON
One String Voltage	V_W	40	-	47	V_{DC}	I_L =125mA
One String Voltage Variation	$\triangle V_W$	-	-	2	V	
Life time	-	30,000	-	-	Hrs	(2)

Note (1) Dimming Ratio=100%

Note (2) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2℃, I_L =125mA.

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	$P_{BL(2D)}$	—	94.7	105	W	(1), (2), IL=125 mA
	$P_{BL(3D)}$	—	85	96	W	(1), (2), IL=400 mA
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	$I_{BL(2D)}$	—	3.95	4.37	A	Non Dimming
	$I_{BL(3D)}$	—	3.54	4	A	
Input Inrush Current	$I_{R(2D)}$	—	—	7.7	Apeak	V_{BL}=22.8V, (IL=typ.) (3), (6)
	$I_{R(3D)}$	—	—	14	Apeak	V_{BL}=22.8V,(IL= 360 mA.) (3), (6)
Dimming Frequency	FB	170	180	190	Hz	(5)
Dimming Duty Ratio	DDR	5	-	100	%	(4), (5)

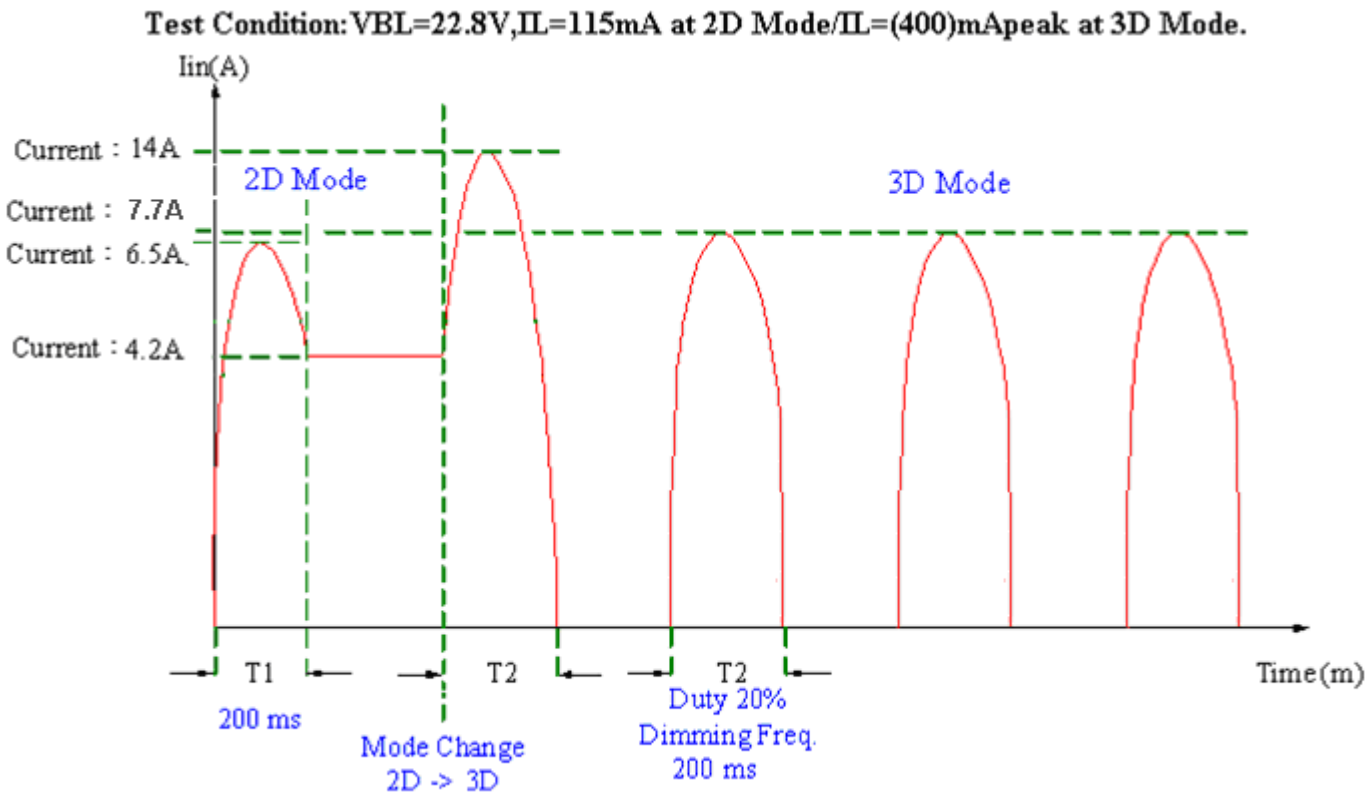
Note (1) The power supply capacity should be higher than the total converter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 50" backlight unit under input voltage 24V, average LED current 133 mA at 2D Mode (LED current 424 mA_{peak} at 3D Mode) and lighting 1 hour later.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) FB and DDR are available only at 2D Mode.

Note (5) Below diagram is only for power supply design reference.



3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on	(5) (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		F_{EPWM}	—	95	—	200	Hz	Normal mode	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		Tr1	—	20	—	—	ms	10%-90%V_{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time		T_{on}	—	300	—	—	ms		
		T_{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

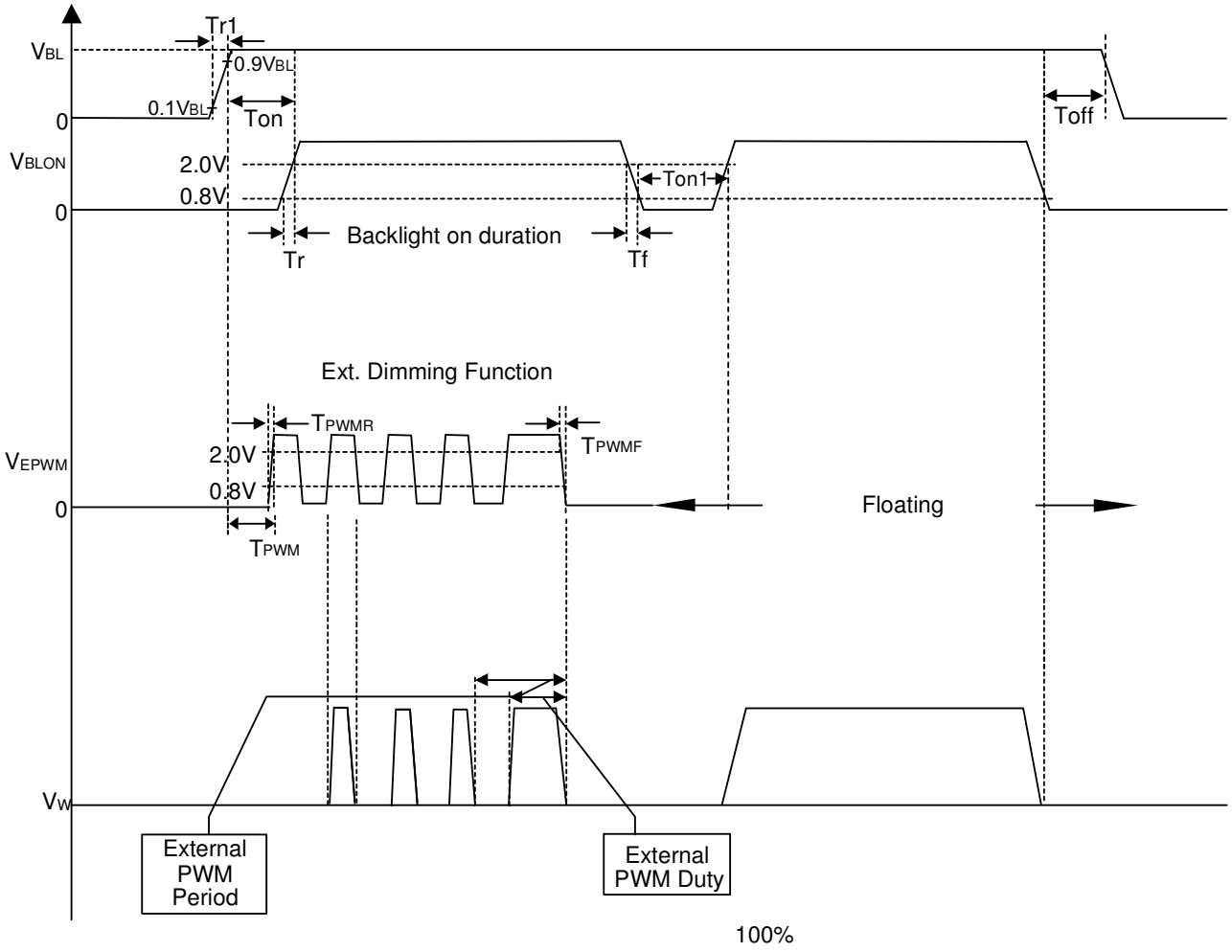
Note (4) When converter protective function is triggered, ERR will output open collector status. Please refers to Fig.2.

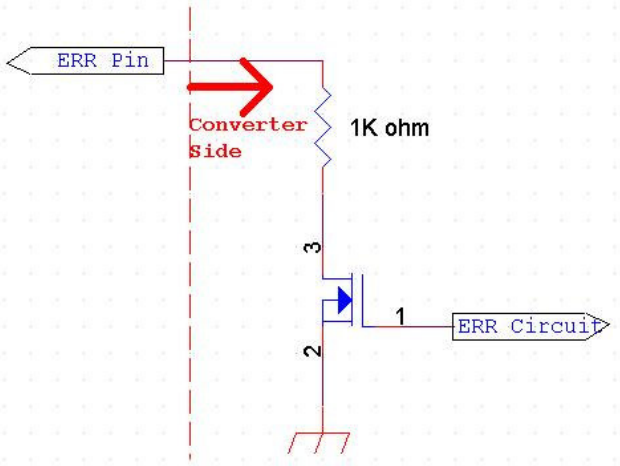
Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

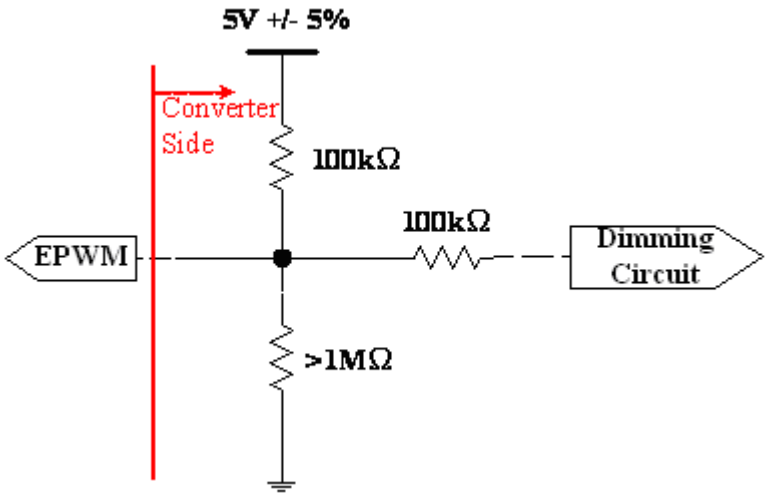
Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

Note (8) [Recommend] EPWM duty ratio is set at 100%(Max. Brightness) in 3D Mode.

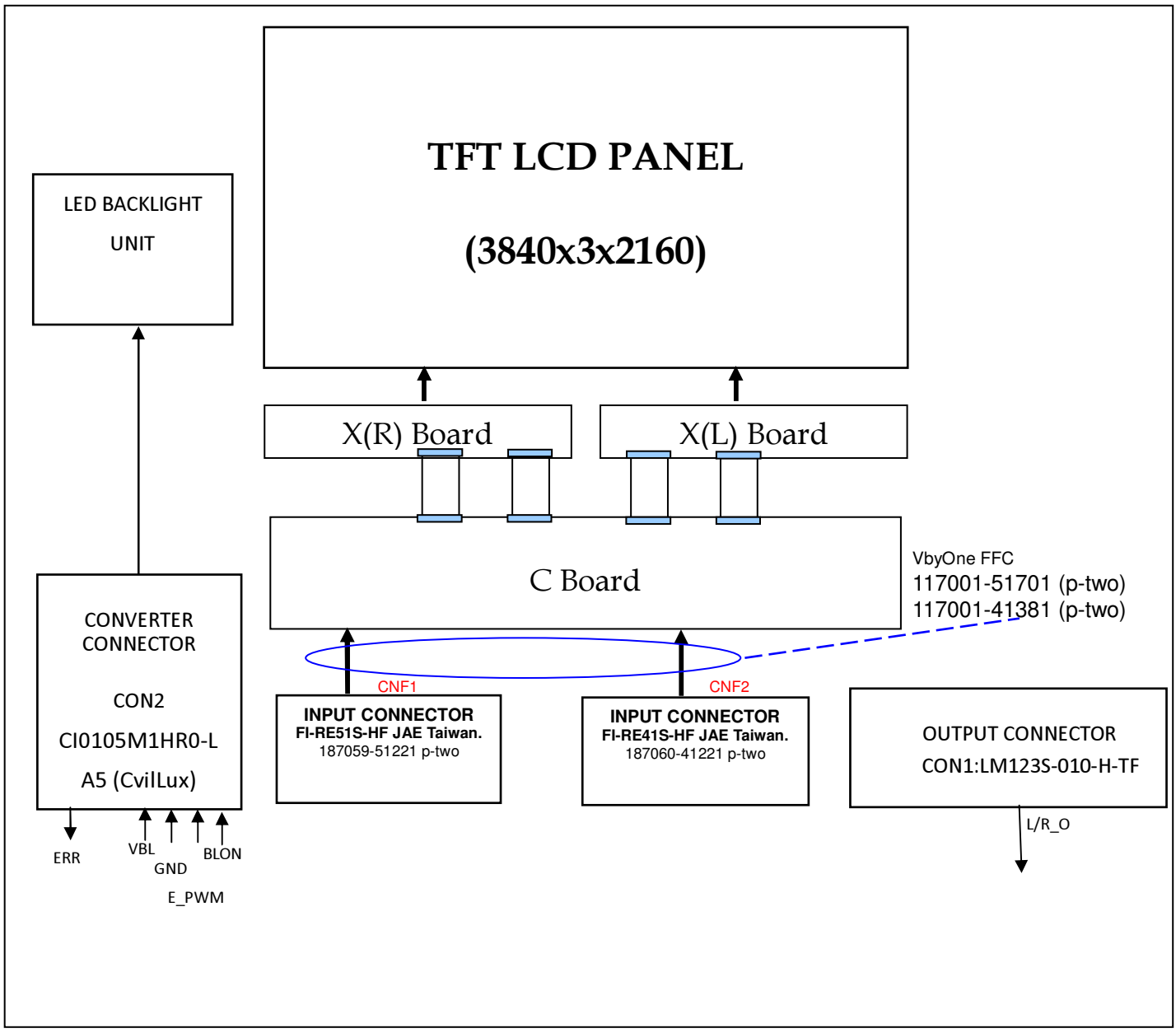






4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE VbyOne HS INPUT

CNF1 Connector Pin Assignment (P-TWO 187059-51221 or JAE FI-RE51S-HF、FI-RE51S-HF-J)

Pin	Name	Description	Note
1	Vin	Power input (+12V)	
2	Vin	Power input (+12V)	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	
6	Vin	Power input (+12V)	
7	Vin	Power input (+12V)	
8	Vin	Power input (+12V)	
9	Vin	Power input (+12V)	
10	Vin	Power input (+12V)	
11	Vin	Power input (+12V)	
12	Vin	Power input (+12V)	
13	Vin	Power input (+12V)	
14	Vin	Power input (+12V)	
15	N.C.	No Connection	
16	GND	Ground	
17	GND	Ground	
18	GND	Ground	
19	GND	Ground	
20	Rev	CMI internal use, please keep it in open and don't floating.	
21	SCN_EN	Scanning mode enable.	(5) (8)
22	LD_EN	Local Dimming Mode Enable.	(4) (7)
23	N.C.	No Connection	(11)
24	N.C.	No Connection	
25	HTPDN	Hot plug detect output, Open drain.	
26	LOCKN	Lock detect output, Open drain.	
27	GND	Ground	
28	RX0N	First Pixel Negative VbyOne differential data input in area A. Lan 0.	(1)
29	RX0P	First Pixel Positive VbyOne differential data input in area A. Lan 0.	
30	GND	Ground	
31	RX1N	Second Pixel Negative VbyOne differential data input in area A. Lan 1.	(1)
32	RX1P	Second Pixel Positive VbyOne differential data input in area A. Lan 1.	
33	GND	Ground	
34	RX2N	Third Pixel Negative VbyOne differential data input in area A. Lan 2.	(1)
35	RX2P	Third Pixel Positive VbyOne differential data input in area A. Lan 2.	

36	GND	Ground	
37	RX3N	4.th Pixel Negative VbyOne differential data input in area A. Lan 3.	(1)
38	RX3P	4.th Pixel Positive VbyOne differential data input in area A. Lan 3.	
39	GND	Ground	
40	RX4N	First Pixel Negative VbyOne differential data input in area B. Lan 4.	(1)
41	RX4P	First Pixel Positive VbyOne differential data input in area B. Lan 4.	
42	GND	Ground	
43	RX5N	Second Pixel Negative VbyOne differential data input in area B. Lan 5.	(1)
44	RX5P	Second Pixel Positive VbyOne differential data input in area B. Lan 5.	
45	GND	Ground	
46	RX6N	Third Pixel Negative VbyOne differential data input in area B. Lan 6.	(1)
47	RX6P	Third Pixel Positive VbyOne differential data input in area B. Lan 6.	
48	GND	Ground	
49	RX7N	4.th Pixel Negative VbyOne differential data input in area B. Lan 7.	(1)
50	RX7P	4.th Pixel Positive VbyOne differential data input in area B. Lan 7.	
51	GND	Ground	

CNF2 Connector Pin Assignment (P-TWO 187060-41221 or JAE FI-RE41S-HF **)**

Pin	Name	Description	Note
1	GND	Ground	
2	RX8N	First Pixel Negative VbyOne differential data input in area C. Lan 8.	(1)
3	RX8P	First Pixel Positive VbyOne differential data input in area C. Lan 8.	
4	GND	Ground	
5	RX9N	Second Pixel Negative VbyOne differential data input in area C. Lan 9.	(1)
6	RX9P	Second Pixel Positive VbyOne differential data input in area C. Lan 9.	
7	GND	Ground	
8	RX10N	Third Pixel Negative VbyOne differential data input in area C. Lan 10.	(1)
9	RX10P	Third Pixel Positive VbyOne differential data input in area C. Lan 10.	
10	GND	Ground	
11	RX11N	4.th Pixel Negative VbyOne differential data input in area C. Lan 11.	(1)
12	RX11P	4.th Pixel Positive VbyOne differential data input in area C. Lan 11.	
13	GND	Ground	
14	RX12N	First Pixel Negative VbyOne differential data input in area D. Lan 12.	(1)
15	RX12P	First Pixel Positive VbyOne differential data input in area D. Lan 12.	
16	GND	Ground	
17	RX13N	Second Pixel Negative VbyOne differential data input in area D. Lan 13.	(1)

18	RX13P	Second Pixel Positive VbyOne differential data input in area D. Lan 13.	
19	GND	Ground	
20	RX14N	Third Pixel Negative VbyOne differential data input in area D. Lan 14.	(1)
21	RX14P	Third Pixel Positive VbyOne differential data input in area D. Lan 14.	
22	GND	Ground	
23	RX15N	4.th Pixel Negative VbyOne differential data input in area D. Lan 15.	(1)
24	RX15P	4.th Pixel Positive VbyOne differential data input in area D. Lan 15.	
25	GND	Ground	
26	N.C.	No Connection	
27	L/R_O	Output signal for Glasses Left Right signal,	(6)
28	L/R	Input signal for Left/Right synchronous signal.	(3) (8)
29	2D/3D	2D/3D Enable	(2) (8)
30	N.C.	No Connection	(11)
31	N.C.	No Connection	
32	N.C.	No Connection	
33	N.C.	No Connection	
34	N.C.	No Connection	
35	N.C.	No Connection	
36	N.C.	No Connection	
37	N.C.	No Connection	
38	N.C.	No Connection	
39	N.C.	No Connection	
40	N.C.	No Connection	
41	N.C.	No Connection	

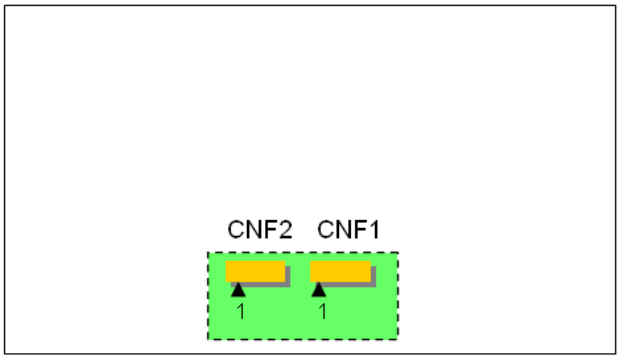
CON1 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE))

1	N.C.	No Connection	(11)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	–
5	N.C.	No Connection	(11)
6	L/R_O	Output signal for Left Right Glasses control	(6)
7	N.C.	No Connection	(11)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

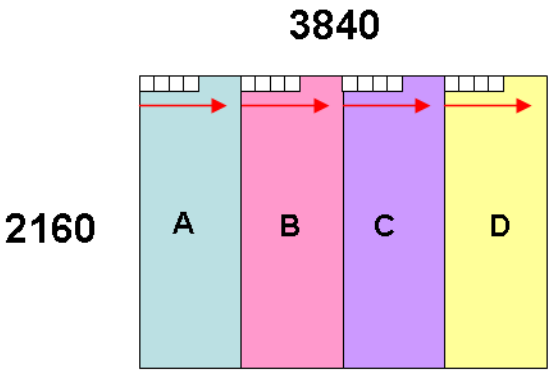
Note (1) V-by-One® HS Data Mapping

Area	Lan	Data Stream
A	Lan 0	1, 5, 9, ..., 953, 957
	Lan 1	2, 6, 10, ..., 954, 958
	Lan 2	3, 7, 11, ..., 955, 959
	Lan 3	4, 8, 12, ..., 956, 960
B	Lan 4	961, 965, 969, ..., 1913, 1917
	Lan 5	962, 966, 970, ..., 1914, 1918
	Lan 6	963, 967, 971, ..., 1915, 1919
	Lan 7	964, 968, 972, ..., 1916, 1920
C	Lan 8	1921, 1925, 1929, ..., 2873, 2877
	Lan 9	1922, 1926, 1930, ..., 2874, 2878
	Lan 10	1923, 1927, 1931, ..., 2875, 2879
	Lan 11	1924, 1928, 1932, ..., 2876, 2880
D	Lan 12	2881, 2885, 2889, ..., 3833, 3837
	Lan 13	2882, 2886, 2890, ..., 3834, 3838
	Lan 14	2883, 2887, 2891, ..., 3835, 3839
	Lan 15	2884, 2888, 2892, ..., 3836, 3840

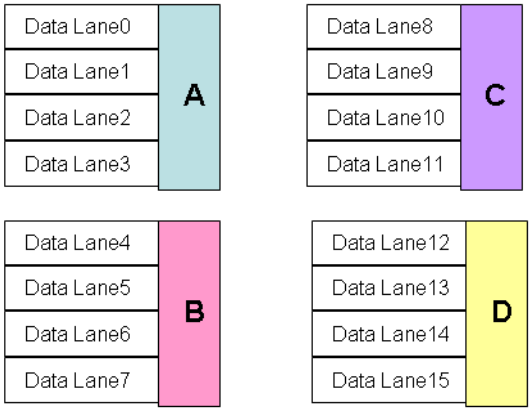
Front View



Pixel arrangement



Display



Note (2) 2D/3D mode selection.

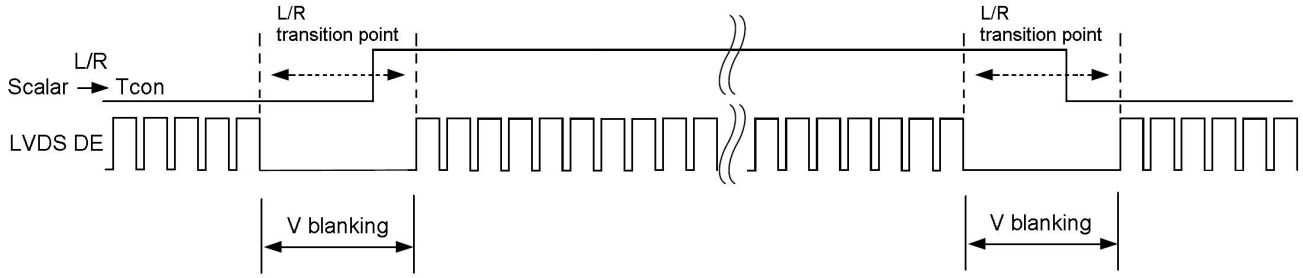
L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (3) Input signal for Left Right eye frame synchronous

V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal



Note (4) Local dimming enable selection. (Default: enable)

L= Connect to GND, H=Connect to +3.3V or Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

LD_EN enable pin should be set in power on stage.

Backlight should be turned off in the period of changing original setting after power on.

Note (5) Scanning enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

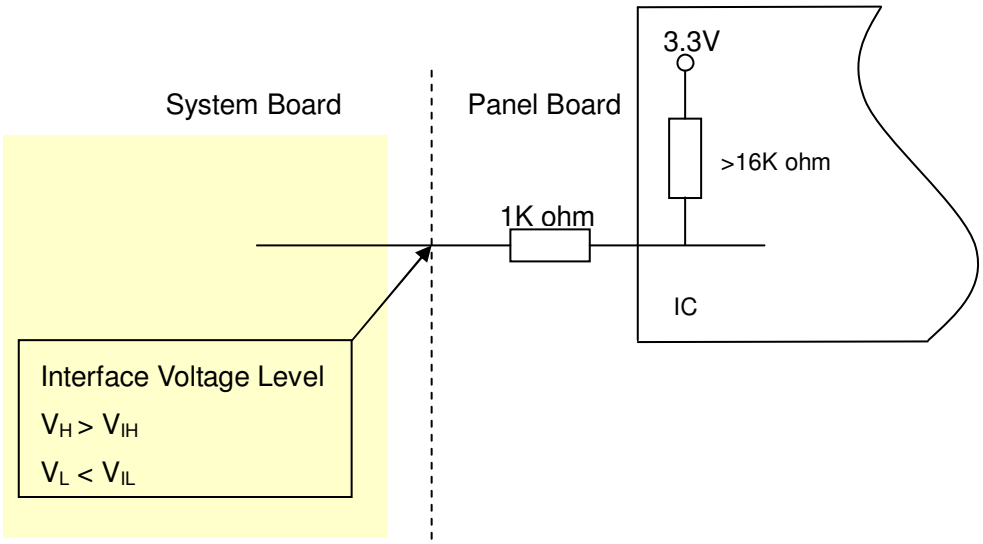
SCN_EN	Note
L or Open	Scanning Disable
H	Scanning Enable

Note (6) The definition of L/R_O signal as follows

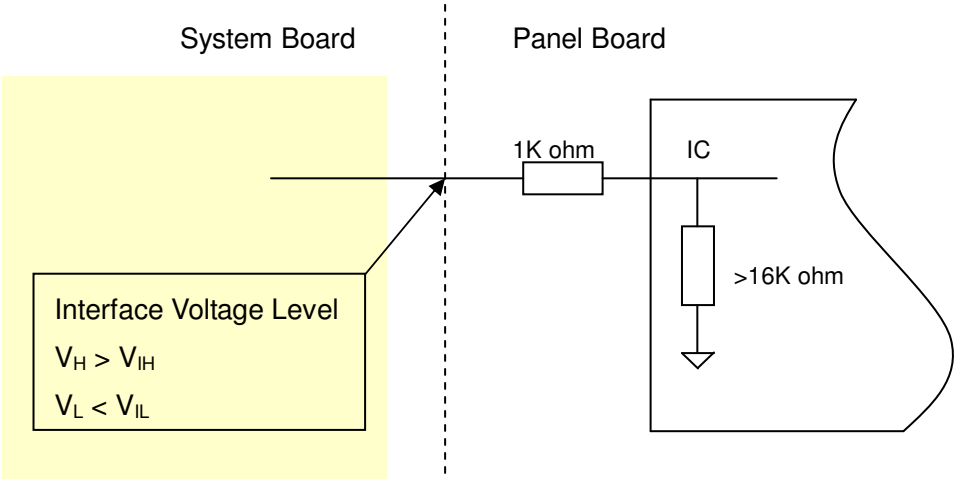
L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

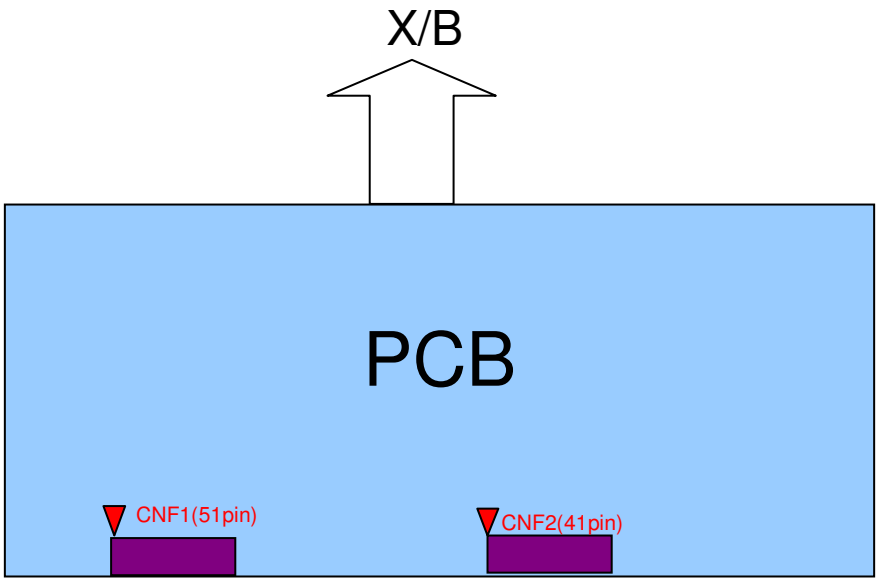
Note (7) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



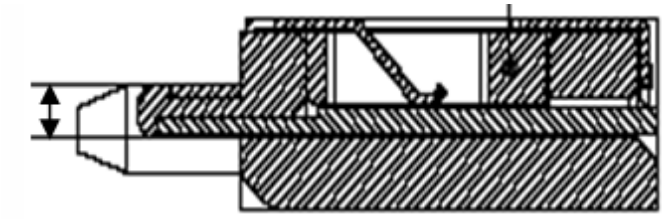
Note (8) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (9) VbyOne HS connector pin order defined as follows



Note (10) LVDS connector mating dimension range request is 0.93mm~1.0mm as below



Note (11) Reserved for internal use. Please leave it open.

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3

Connector Type : 196388-12041-3(P-TWO) or FF01-431-123A(FCN)

Pin No.	Symbol	Description
1	VLED+	Positive of LED string
2	VLED+	
3	VLED+	
4	NC	NC
5	N-	Negative of LED string
6	N-	
7	N-	
8	N-	
9	N-	
10	N-	
11	N-	
12	N-	

CN6

Connector Type : 196388-12041-3(P-TWO) or FF01-431-123A(FCN)

Pin No.	Symbol	Description
12	VLED+	Positive of LED string
11	VLED+	
10	VLED+	
9	NC	NC
8	N-	Negative of LED string
7	N-	
6	N-	
5	N-	
4	N-	
3	N-	
2	N-	
1	N-	

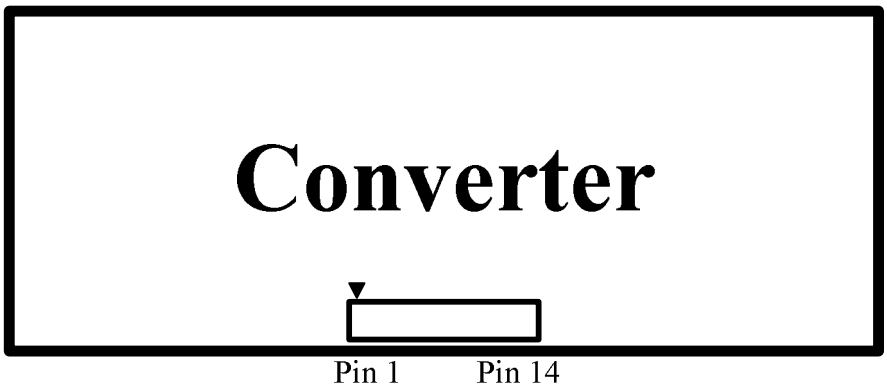
5.3 DRIVING BOARD UNIT

CN1(Header): CI0114M1HR0-LA (CvilLux) or JH2-D4-143N (FCN)

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Note (1) If Pin14 is open, E_PWM is 100% duty.

Note (2) Input connector pin order defined as follows



Input Connector

5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

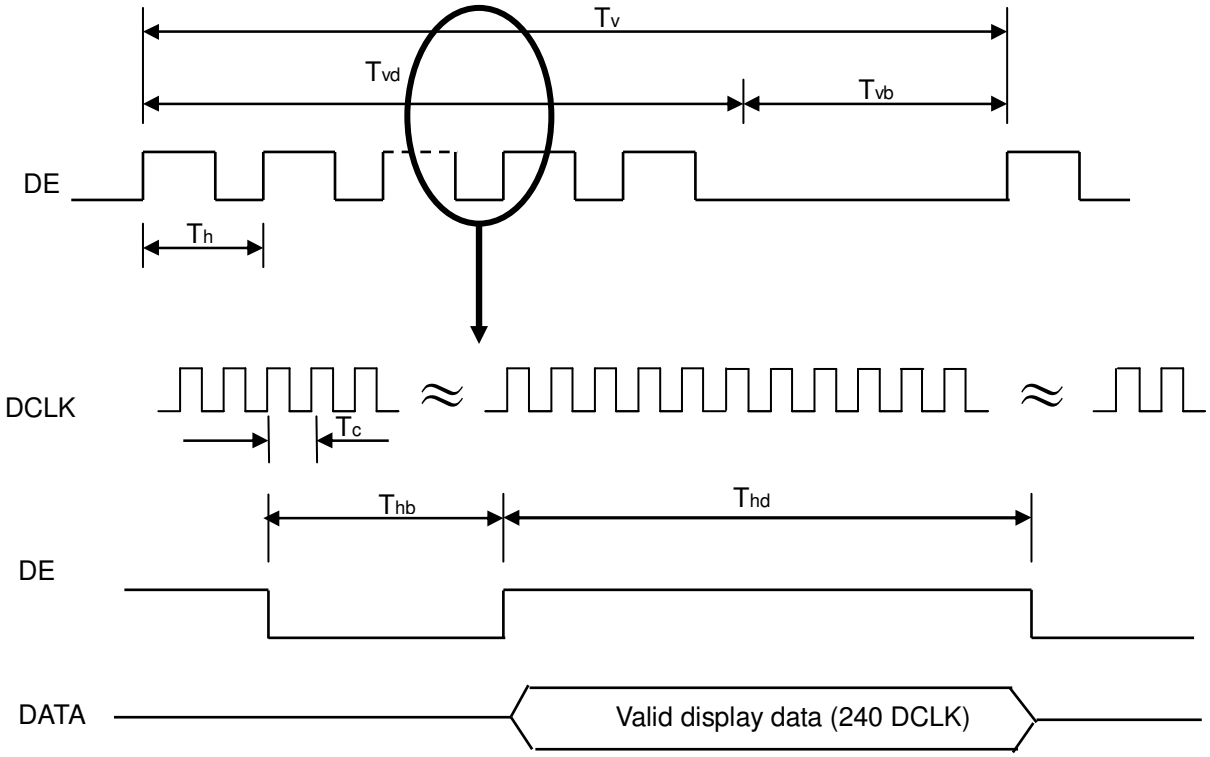
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	Data Clock		1/Tc	60	74.25	80	MHz	(1)
Frame rate	2D mode		Fr	—	120	—	Hz	
VbyOne Receiver	Data skew between each area (A/B/C/D)		Tblock			0.06	H	(2)
	Intra-Pair skew			-0.3		0.3	UI	(3)
	Inter-pair skew			-15		15	UI	(4)
	Spread spectrum		F_{clkin_mod}	F_{clkin}-0.5	—	F_{clkin}+0.5	MHz	(5)
	Spread spectrum		F_{SSM}	—	—	30	KHz	
Vertical Active Display Term (4 Lan,960X2160 Active Area)	2D Mode	Total	Tv	2250		3160	Th	Tv=Tvd+Tvb
		Display	Tvd	—	2160	—	Th	
		Blank	Tvb	90		1000	Th	
Horizontal Active Display Term (4 Lan,960X2160 Active Area)	2D Mode	Total	Th	275		450	Tc	Th=Thd+Thb
		Display	Thd	—	240	—	Tc	
		Blank	Thb	35		210	Tc	

Note (1) Please make sure the range of pixel clock has follow the below equation：

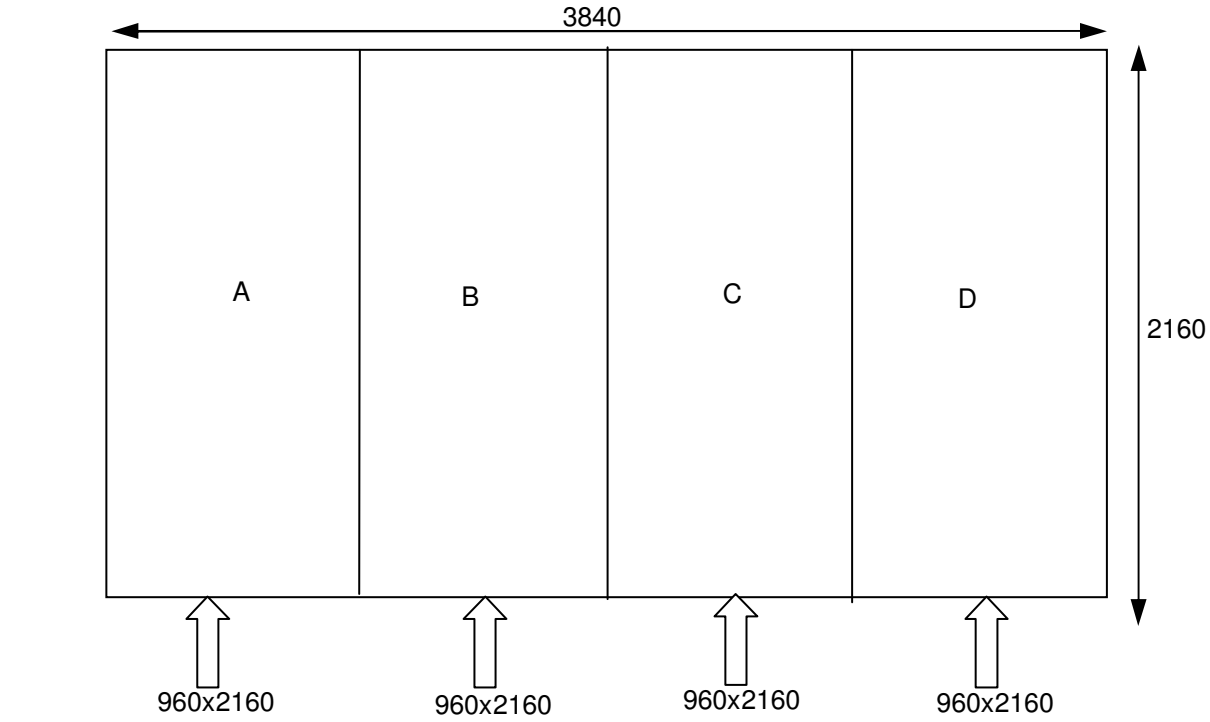
Fclkin(max) ≧ Fr × Tv × Th

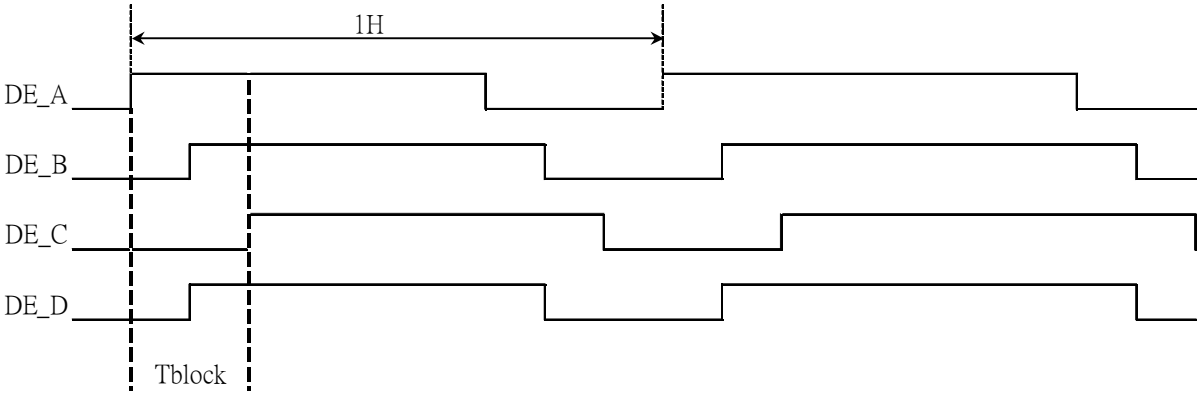
Fr × Tv × Th ≧ Fclkin (min)

INPUT SIGNAL TIMING DIAGRAM

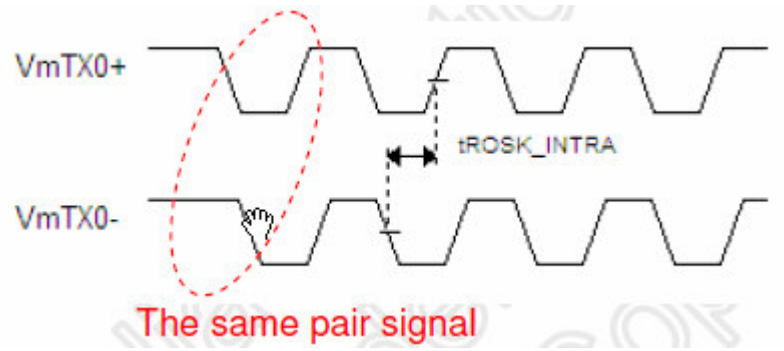


Note (2) Data skew between areas

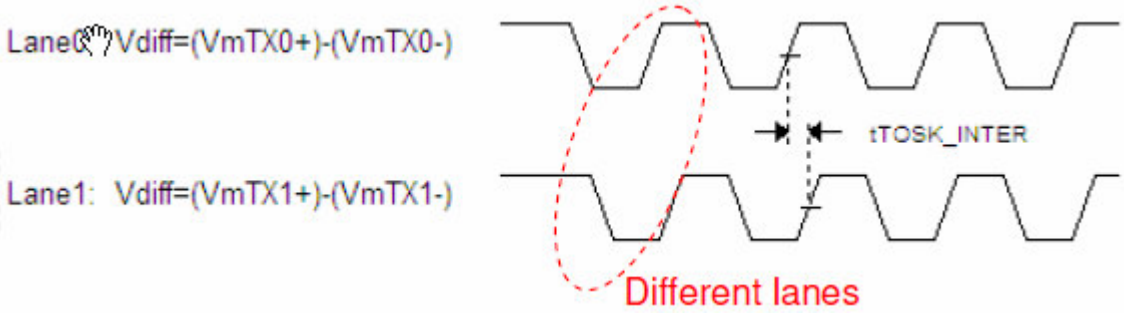




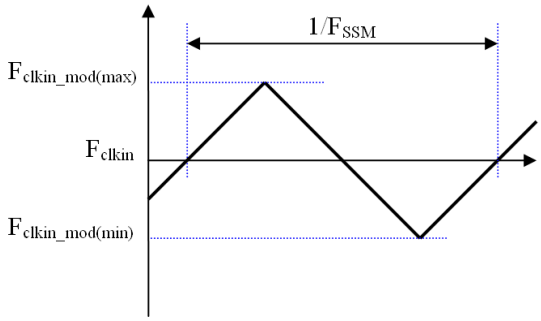
Note (3) VbyOne HS Intra-pair skew



Note (4) VbyOne HS Inter-pair skew.



Note (5) The SSCG (Spread spectrum clock generator) is defined as below figures.



6.2 V by One Input Signal Timing Diagram

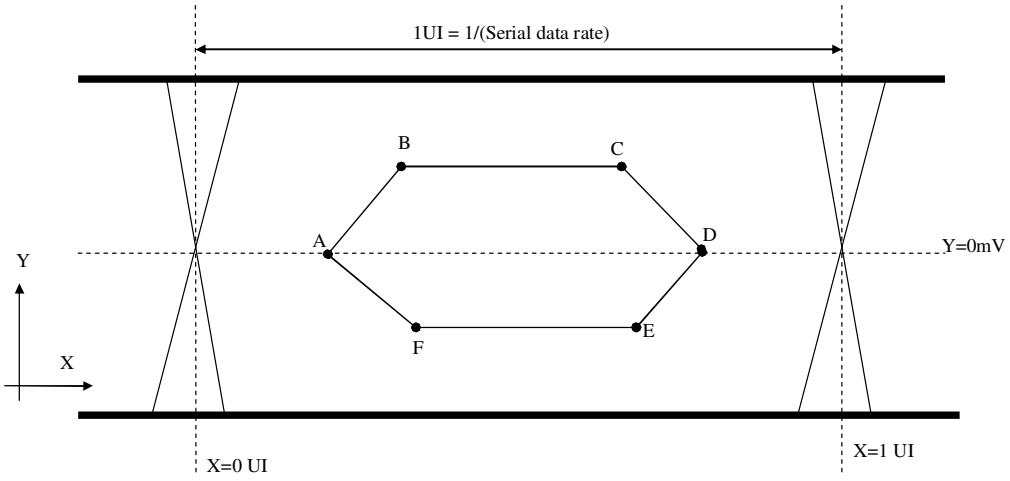


Table 1 Eye Mask Specification

	X [UI]	Y [mV]	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)
D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

Note (1) Input levels of V-by-One HS signals are comes from “V-by-One HS Stander Ver.1.4”

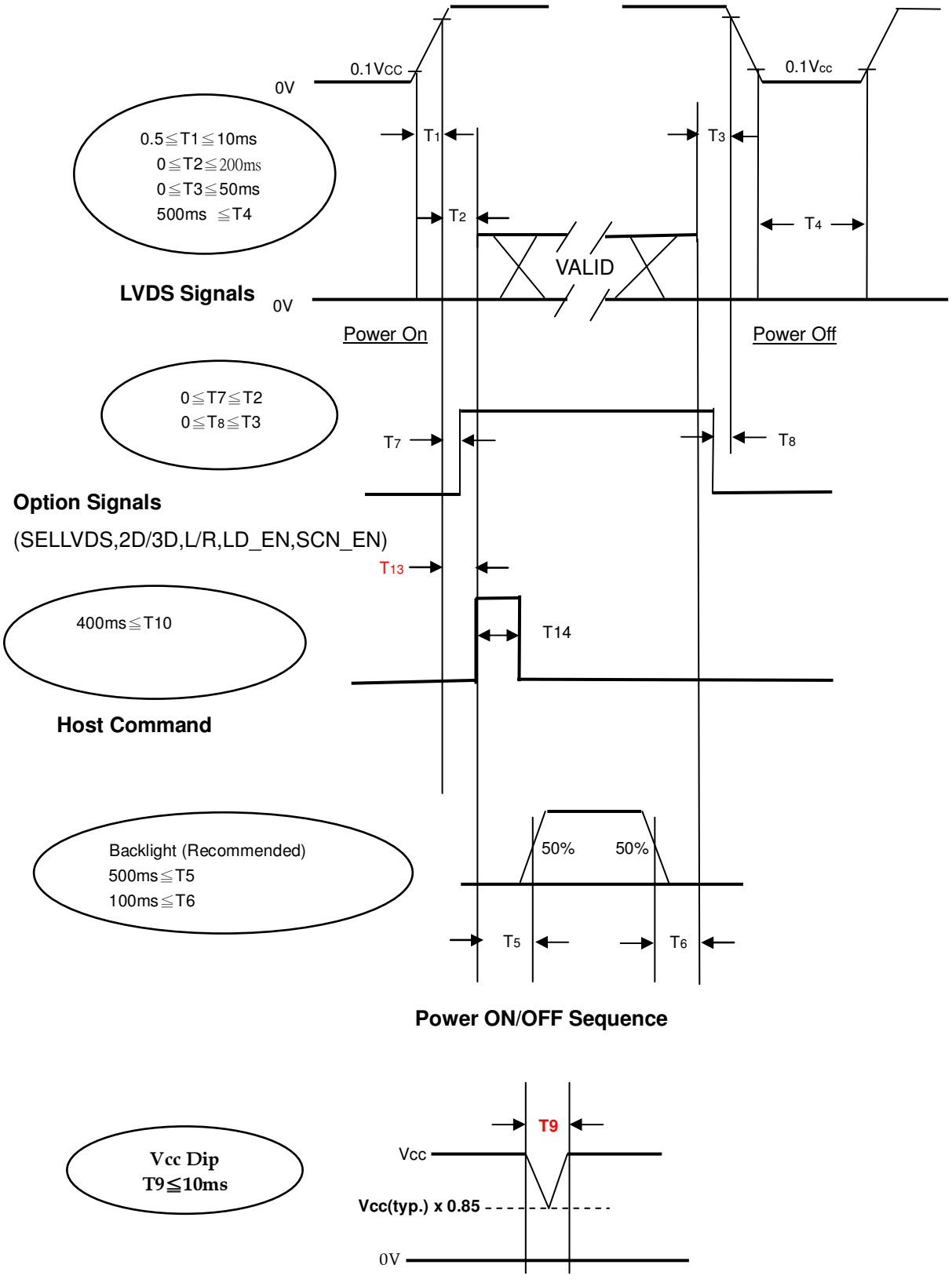
6.3 Byte Length and Color mapping of V-by-One HS

Packer input & Unpacker output		30bpp RGB (10bit)
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]

	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

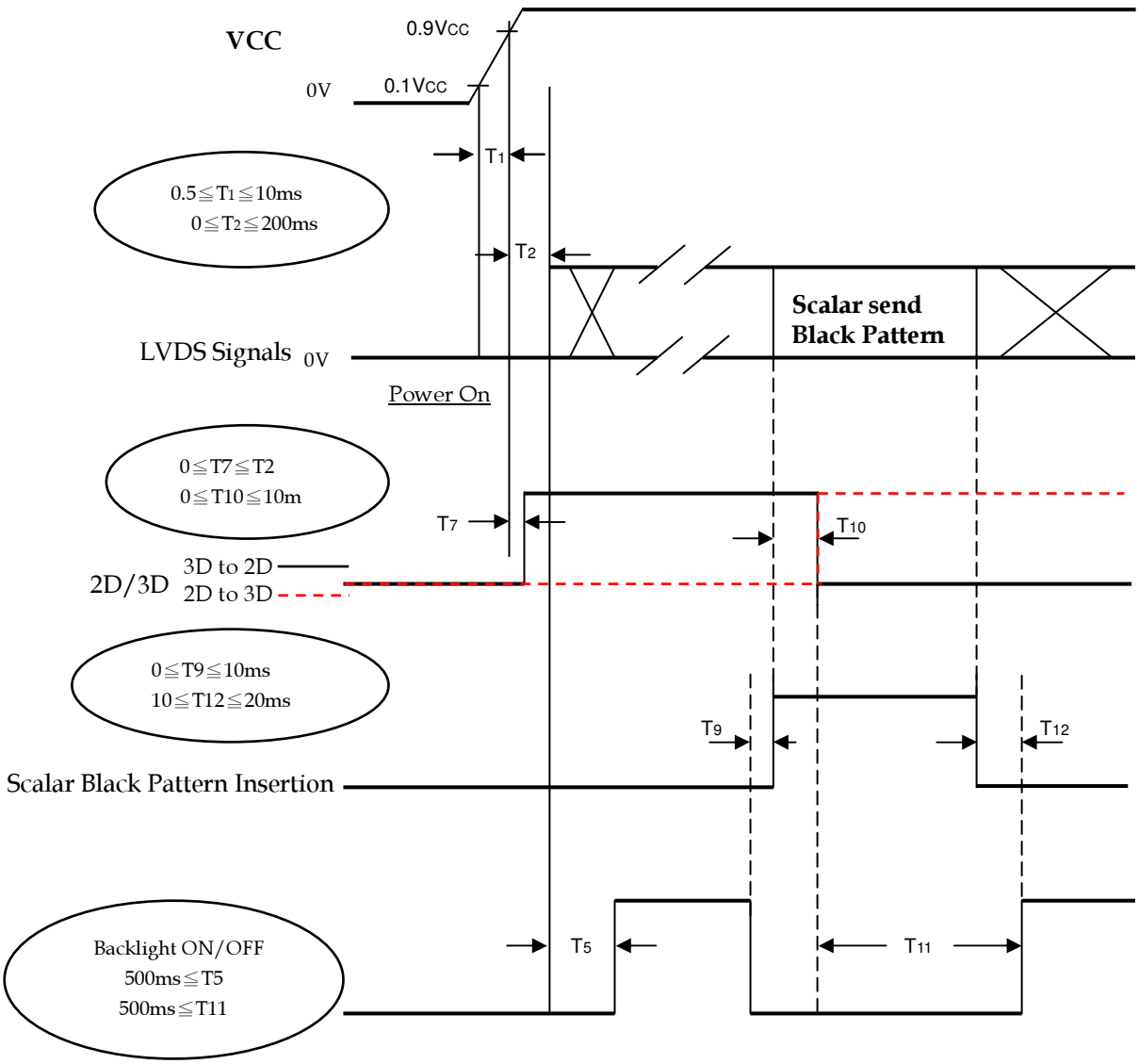
6.4 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

6.5 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

Note (7) Vcc must decay smoothly when power-off.

Note (8) T5 Backlight turn on time depend on T14 command length+T13

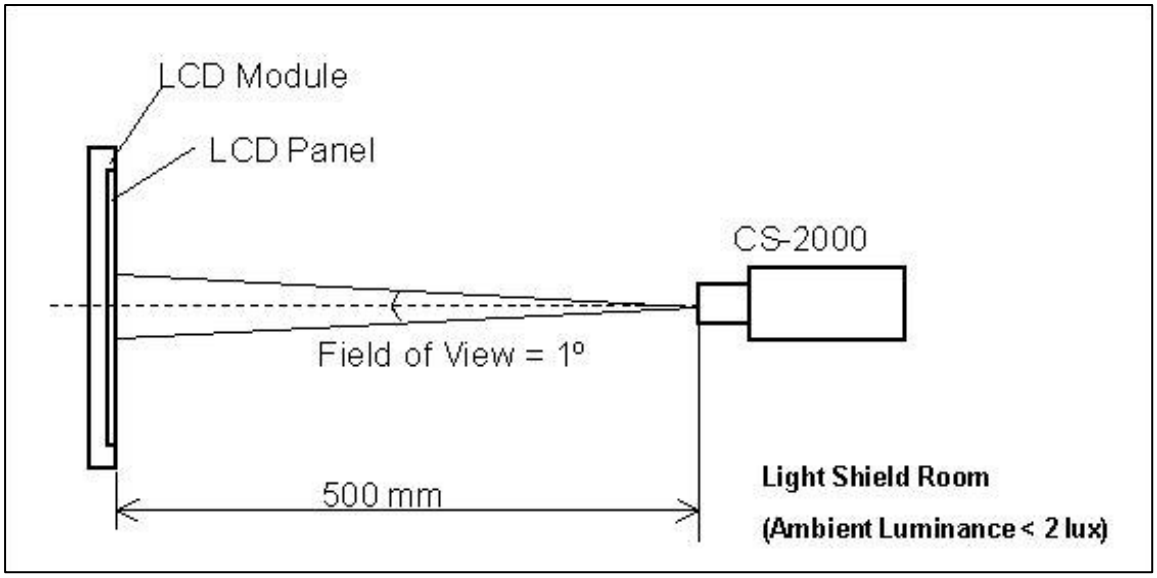
7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I_L	125± 3.45	mA
Vertical Frame Rate	Fr	120	Hz

Local Dimming Function should be Disable before testing to get the steady optical characteristics (According to 5.1 CNF1 Connector Pin Assignment, Pin no. “42”)

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



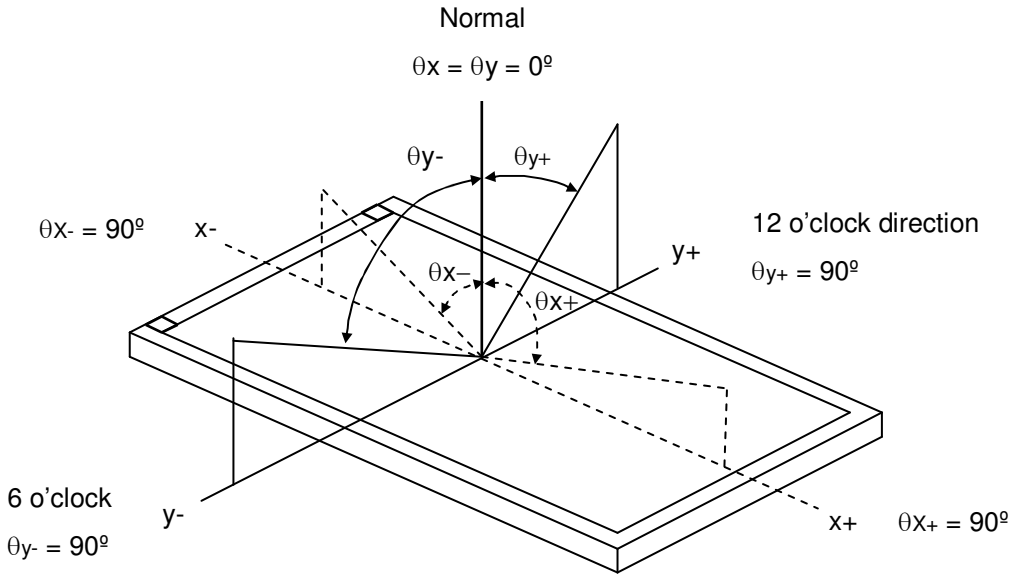
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		θ_x=0°, θ_Y =0° Viewing angle at normal direction	3500	5000	-	-	Note (2)
Response Time		Gray to gray				6.5	13	ms	Note (3)
CenterLuminance of White		L_C	2D		320	400	-	cd/m^2	Note (4)
			3D			65		cd/m^2	Note (8)
White Variation		δW					1.3	-	Note (6)
Cross Talk		CT	2D				4	%	Note (5)
			3D-W			4	-	%	Note (8)
			3D-D		-	11	-	%	Note (8)
Color Chromaticity	Red	Rx			Typ.- 0.03	0.642	Typ.+ 0.03	-	
		Ry				0.332		-	
	Green	Gx				0.306		-	
		Gy				0.619		-	
	Blue	Bx				0.152		-	
		By				0.051		-	
	White	Wx				0.280		-	
		Wy				0.290		-	
	Correlated color temperature					9800		K	
	Color Gamut	C.G.			-	72	-	%	NTSC
Viewing Angle	Horizontal	θ_x+		CR≥20	80	88	-	Deg.	(1)
		θ_x-			80	88	-		
	Vertical	θ_Y+			80	88	-		
		θ_Y-			80	88	-		
Transmission direction of the up polarizer		$\Phi_{up\text{-}P}$		-	-	90	-	Deg.	(7)

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

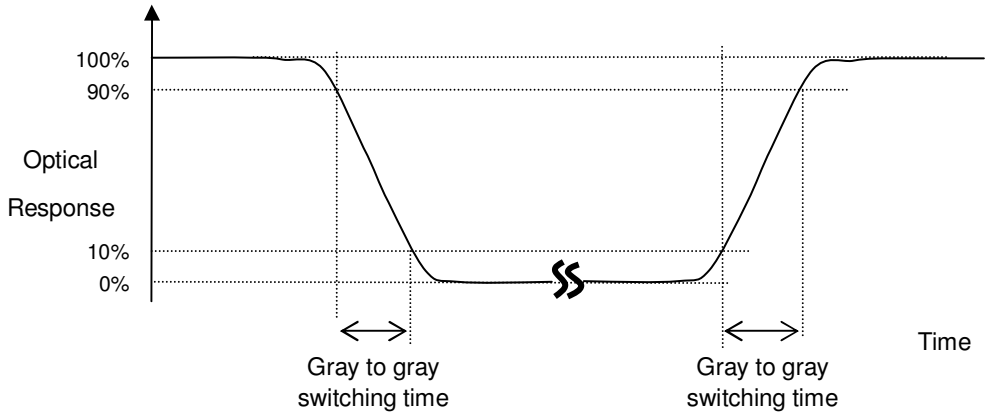
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 1023 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (6).

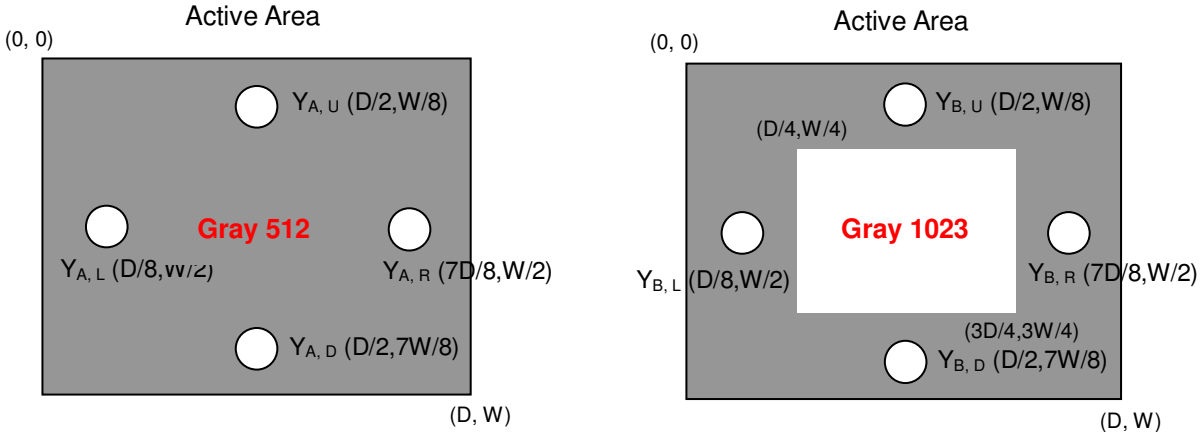
Note (5) Definition of Cross Talk (CT):

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where:

Y_A = Luminance of measured location without gray level 1023 pattern (cd/m2)

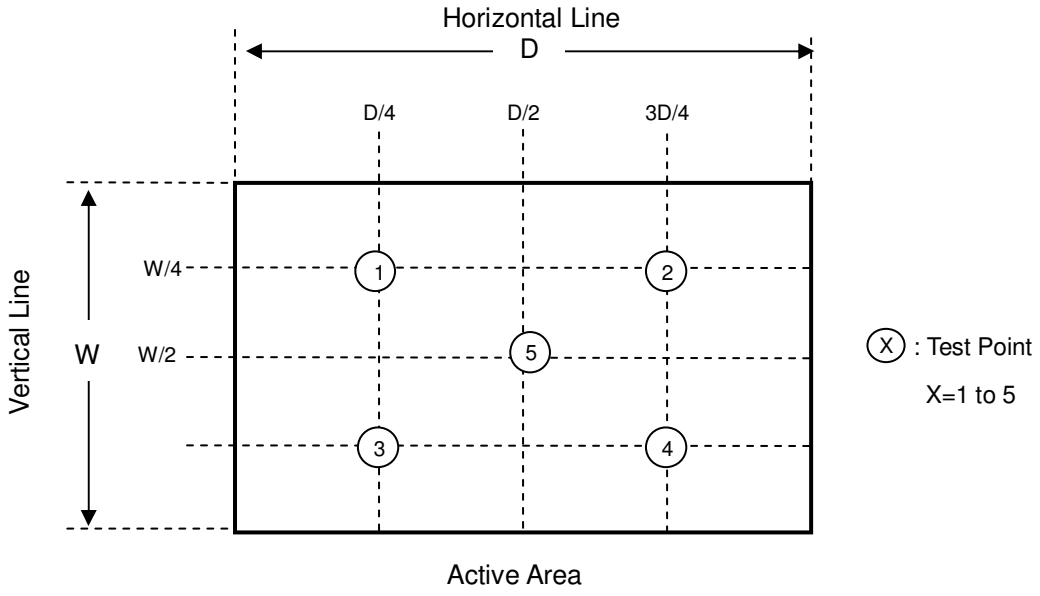
Y_B = Luminance of measured location with gray level 1023 pattern (cd/m2)



Note (6) Definition of White Variation (δW):

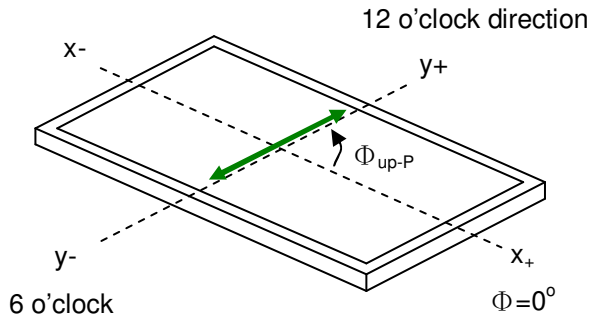
Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



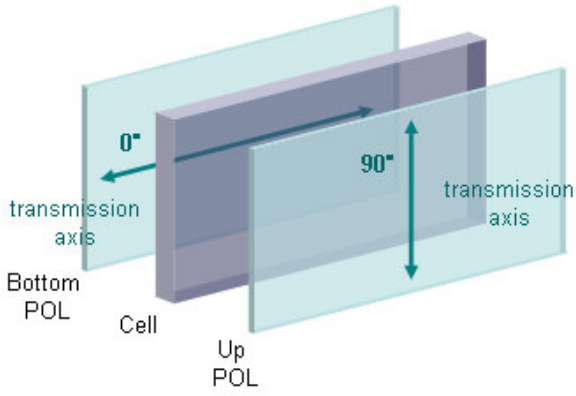
Note (7) This is a reference for designing the shutter glasses of 3D application.

Definition of the transmission direction of the up polarizer($\Phi_{up\text{-}P}$) on LCD Module:

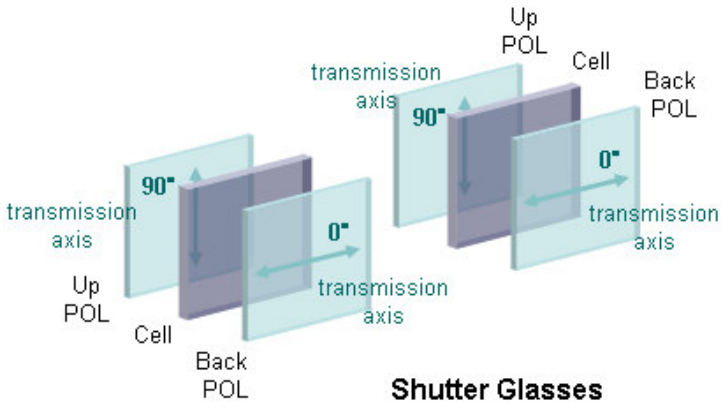


Up Polarizer

The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



LCD Module

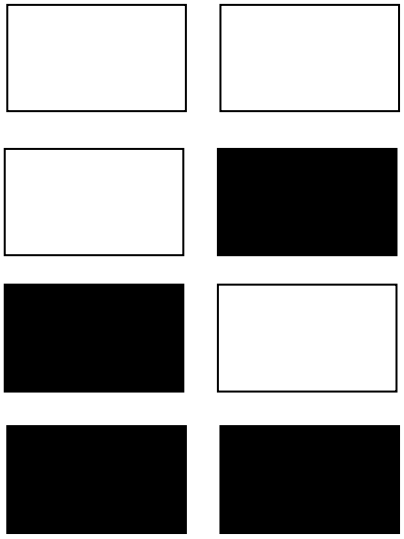


Shutter Glasses

Note(8) Definition of the 3D mode performance (measured under 3D mode, use CMI's shutter glass):

a. Test pattern

Left eye image and right eye image are displayed alternated



WW

Left eye image: W1023; Right eye image: W1023

WB

Left eye image: W1023; Right eye image: W0

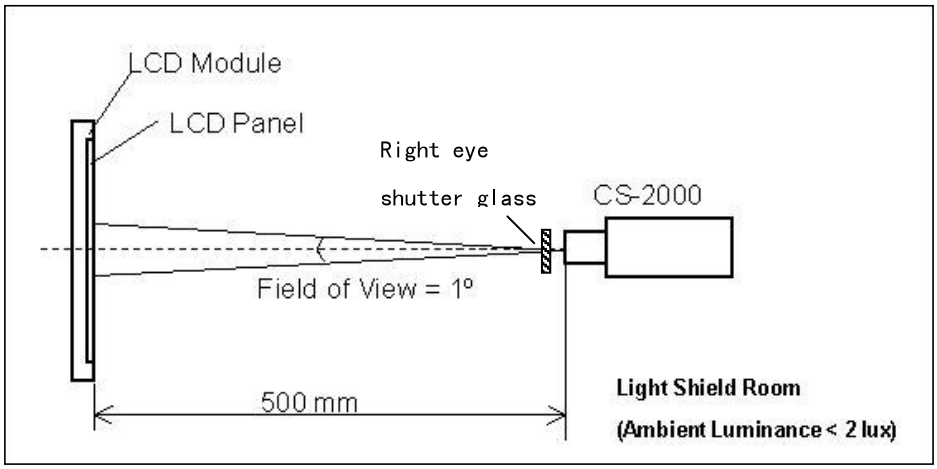
BW

Left eye image: W0; Right eye image: W1023

BB

Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern "WW", denoted L(WW); the luminance of the test pattern "WB", denoted L(WB); the luminance of the test pattern "BW", denoted L(BW); the luminance of the test pattern "BB", denoted "L(BB)

c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

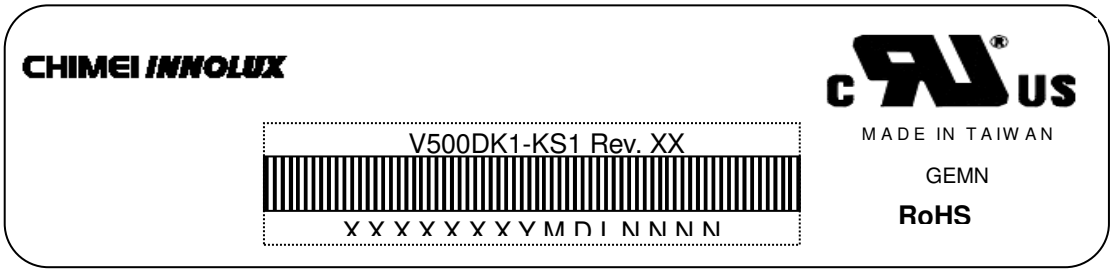
d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \left| \frac{L(WB) - L(BB)}{L(WW) - L(BB)} \right|$

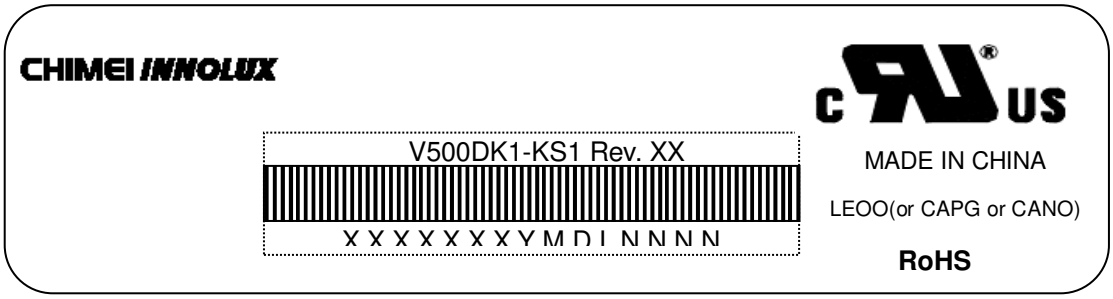
e. Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \left| \frac{L(WW) - L(BW)}{L(WW) - L(BB)} \right|$

8. DEFINITION OF LABELS

8.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

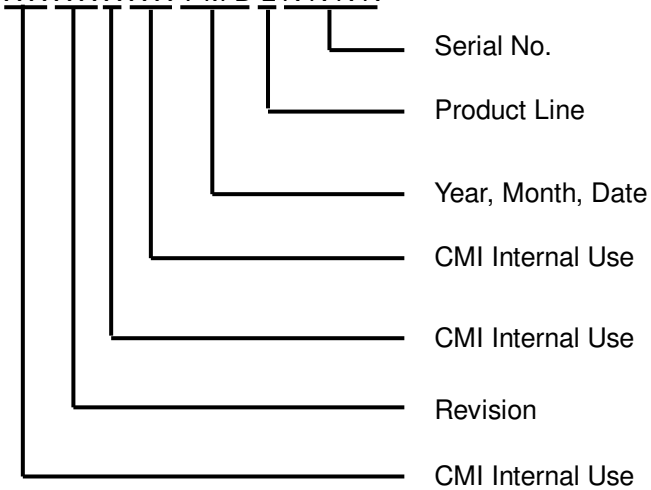




Model Name: V500DK1-KS1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

9. Packaging

9.1 PACKING SPECIFICATIONS

(1) 4 LCD TV modules / 1 Box

(2) Box dimensions: 1235(L) X 258 (W) X 751 (H)

(3) Weight: approximately 56.1 Kg (4 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

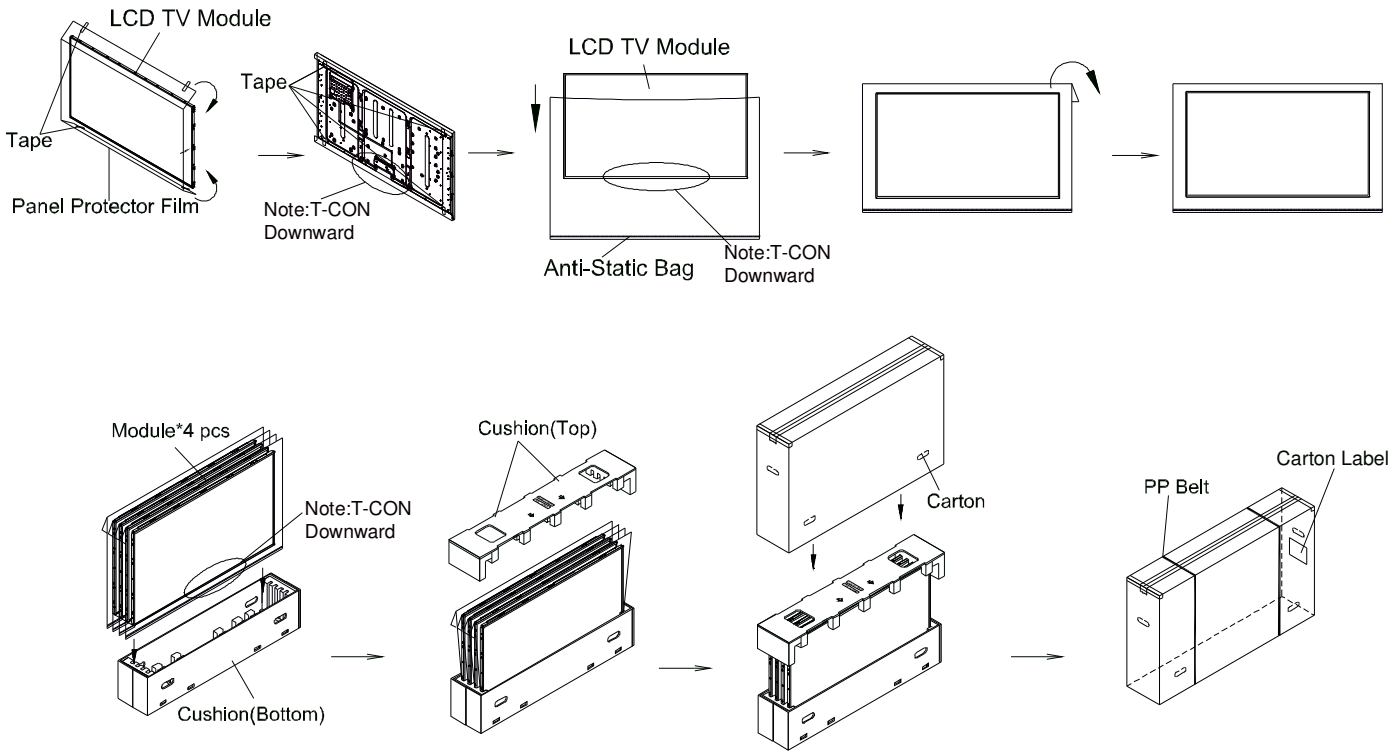
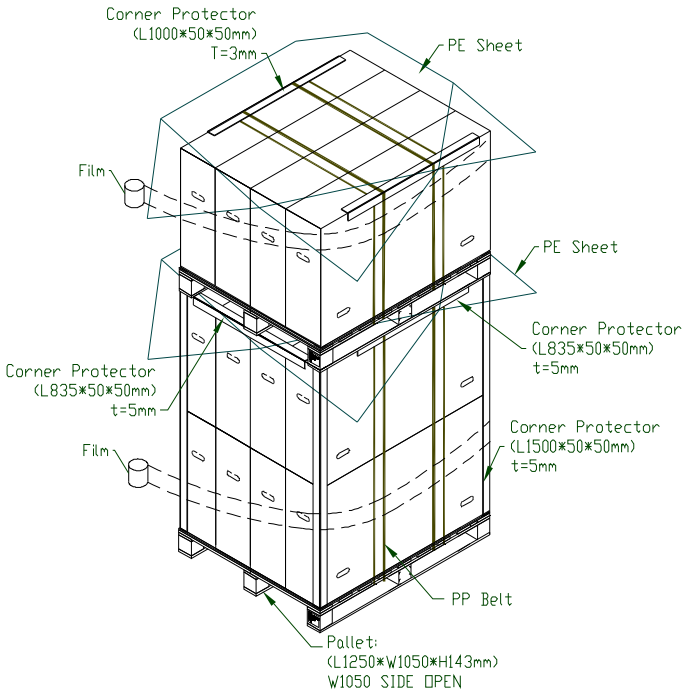
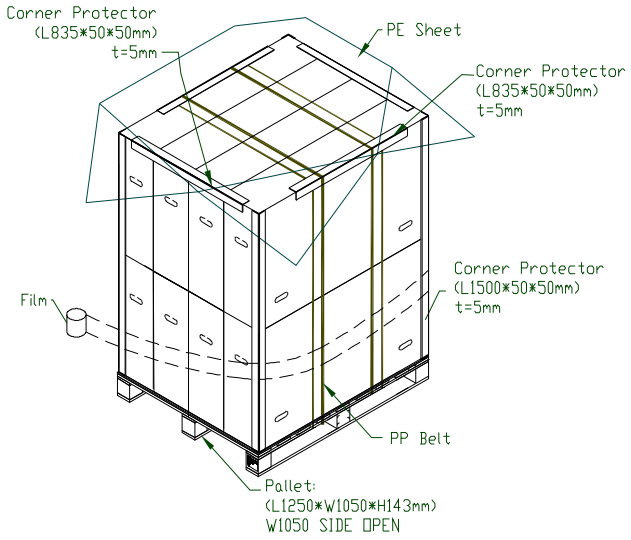


Figure.9-1 packing method

Sea / Land Transportation (40ft HQ Container)



Sea / Land Transportation (40ft/20ft Container)



Air Transportation

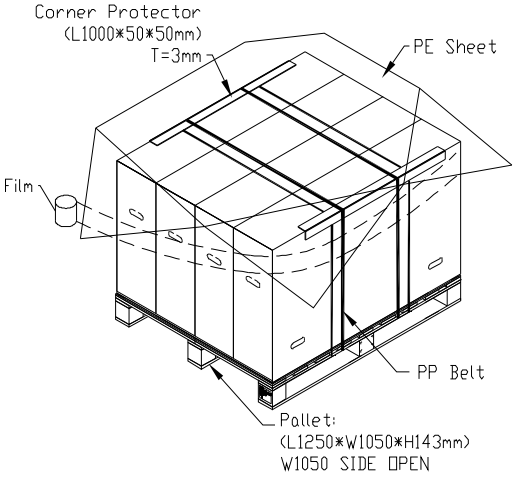


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

10.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2nd Ed.,2011
	cUL	CAN/CSA C22.2 No.60950-1-07,2nd Ed.,2011
	CB	IEC60950-1:2005+A1:2009 / EN60950-1:2006+ A11:2009+A1:2010+A12:2011
Audio/Video Apparatus	UL	UL60065: 7th Ed.,2007
	cUL	CAN/CSA C22.2 No.60065-03,1st Ed.,2006+A1:2006

	CB	IEC60065:2001+ A1:2005 +A2:2010 / EN60065:2002 + A1:2006 + A11:2008+A2:2010+A12:2011

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTIC