

- Tentative Specification
- Preliminary Specification
- Approval Specification

# MODEL NO.: V500HJ1

## SUFFIX: LE1

Customer:	
APPROVED BY	SIGNATURE
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Name / Title _____	
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
0.0	Jan.19,12	all	all	Tentative Specification Ver 0.0 was first issued.
1.3	Mar. 20,12	5 9 15 16-18 22 23 25 28 30 35 38~39	1.4 3.1 4.1 5.1 5.5 5.6 6.1 6.2 7.2 9.1 11	Update GENERAL SPECIFICATIONS Update TFT LCD MODULE Update TFT LCD MODULE Update TFT LCD MODULE Update LVDS INTERFACE Update COLOR DATA INPUT ASSIGNMENT Update INPUT SIGNAL TIMING SPECIFICATIONS Update POWER ON/OFF SEQUENCE Update OPTICAL SPECIFICATIONS Update PACKING SPECIFICATIONS Update MECHANICAL CHARACTERISTIC

## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V500HJ1-LE1 is a 50" TFT Liquid Crystal Display module with LED Backlight unit and 2ch-LVDS interface. This module supports 1920 x 1080 HDTV format and can display true 16.7M colors (8-bit /color). The driving board module for backlight is built-in.

### 1.2 FEATURES

- High brightness 350 nits
- High contrast ratio 5000:1
- Fast response time Gray to Gray typical 8ms
- High color saturation 72% NTSC
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 60 Hz frame rate
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance

### 1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

### 1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1095.84(H) x (V) 616.41 (50" diagonal)	mm	(1)
Bezel Opening Area	1102.84(H) x 623.41(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.1903(H) x 0.5708(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	16.7M	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 1%),Hardness 3H	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

**1.5 MECHANICAL SPECIFICATIONS**

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1121.14	1122.64	1124.14	mm	Module Size
	Vertical (V)	643.81	645.31	646.81	mm	
	Depth (D)	14.1	15.1	16.1	mm	To Rear
		23	24	25	mm	To converter cover
	Weight		13000		G	Weight

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

**2. ABSOLUTE MAXIMUM RATINGS**

**2.1 ABSOLUTE RATINGS OF ENVIRONMENT**

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	50	°C	(1), (2)
Shock (Non-Operating)	S <sub>NOP</sub>	-	35	G	(3), (5)
Vibration (Non-Operating)	V <sub>NOP</sub>	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

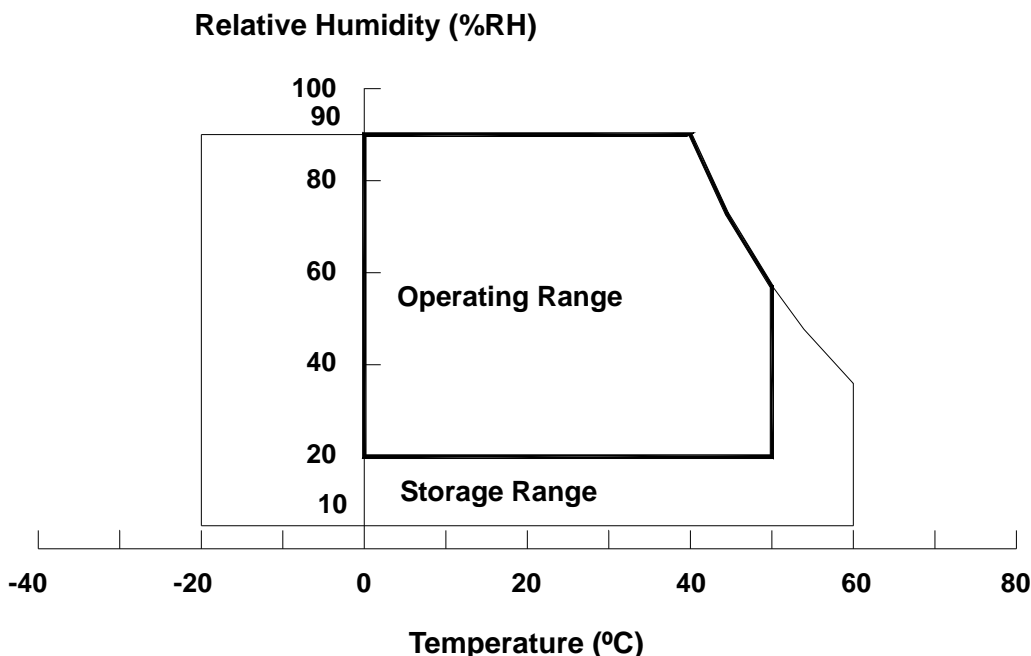
- (a) 90 %RH Max. ( $T_a \leq 40$  °C).
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40$  °C).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for  $\pm X$ ,  $\pm Y$ ,  $\pm Z$ .

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



## 2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 °C at normal humidity without condensation.
- (b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

## 2.3 ELECTRICAL ABSOLUTE RATINGS

### 2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	$V_{CC}$	-0.3	13.5	V	(1)
Logic Input Voltage	$V_{IN}$	-0.3	3.6	V	

### 2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	$V_W$	$T_a = 25\text{ }^\circ\text{C}$	-	-	46.9	$V_{RMS}$	
Converter Input Voltage	$V_{BL}$	-	0	-	30	V	(1)
Control Signal Level	-	-	-0.3	-	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.



### 3. ELECTRICAL CHARACTERISTICS

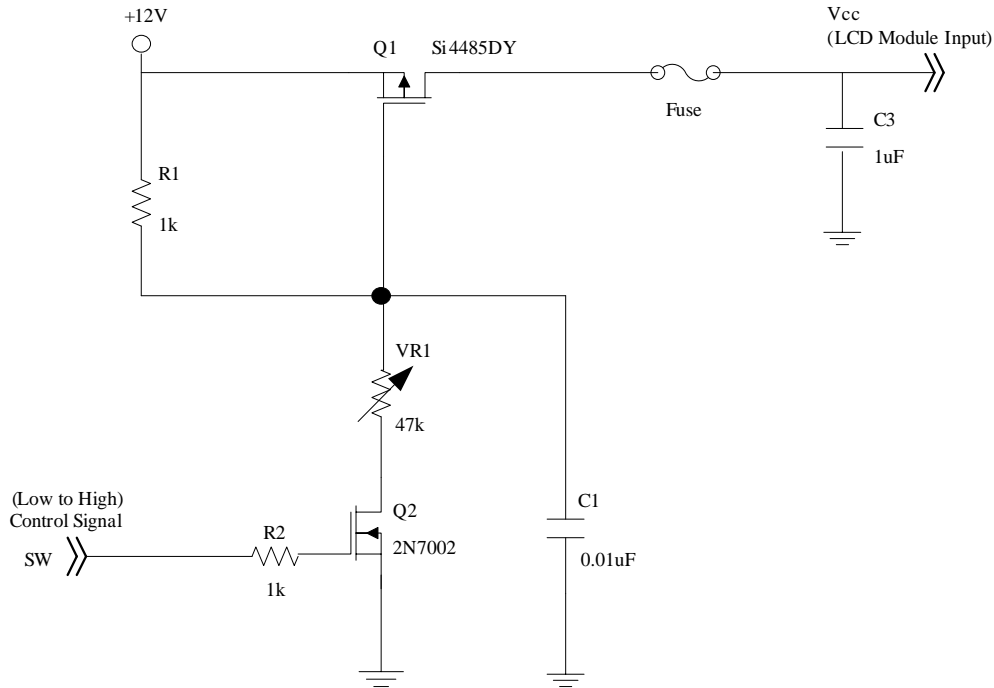
#### 3.1 TFT LCD MODULE

(Ta = 25 ± 2 °C)

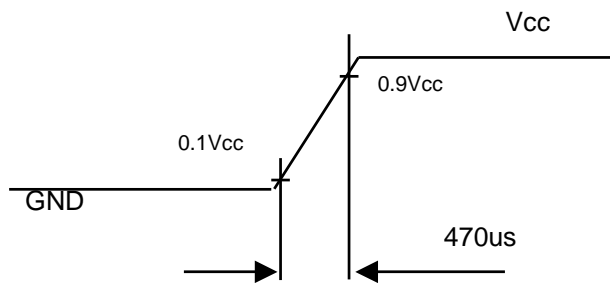
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V <sub>CC</sub>	10.8	12	13.2	V	(1)
Rush Current		I <sub>RUSH</sub>	—	—	(2.34)	A	(2)
Power Consumption	White Pattern	—	—	(5.76)	(6.86)	W	(3)
	Horizontal Stripe	—	—	(9.6)	(11.62)	W	
	Black Pattern	—	—	(5.64)	(6.73)	W	
Power Supply Current	White Pattern	—	—	(0.48)	(0.52)	A	
	Horizontal Stripe	—	—	(0.8)	(0.88)	A	
	Black Pattern	—	—	(0.47)	(0.51)	A	
LVDS interface	Differential Input High Threshold Voltage	V <sub>LVTH</sub>	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V <sub>LVTL</sub>	—	—	-100	mV	
	Common Input Voltage	V <sub>CM</sub>	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	V <sub>ID</sub>	200	—	600	mV	
	Terminating Resistor	R <sub>T</sub>	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	—	3.3	V	
	Input Low Threshold Voltage	V <sub>IL</sub>	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



**Vcc rising time is 470us**



Note (3) The specified power consumption and power supply current is under the conditions at  $V_{cc} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^\circ\text{C}$ ,  $f_v = 60\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



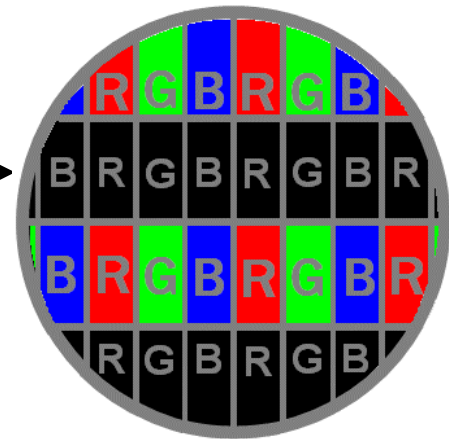
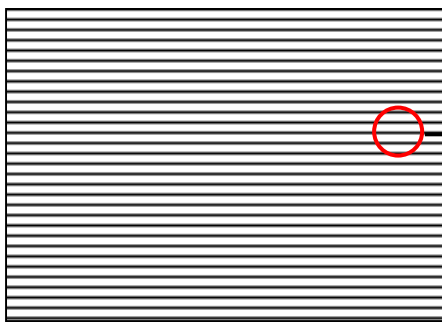
Active Area

b. Black Pattern

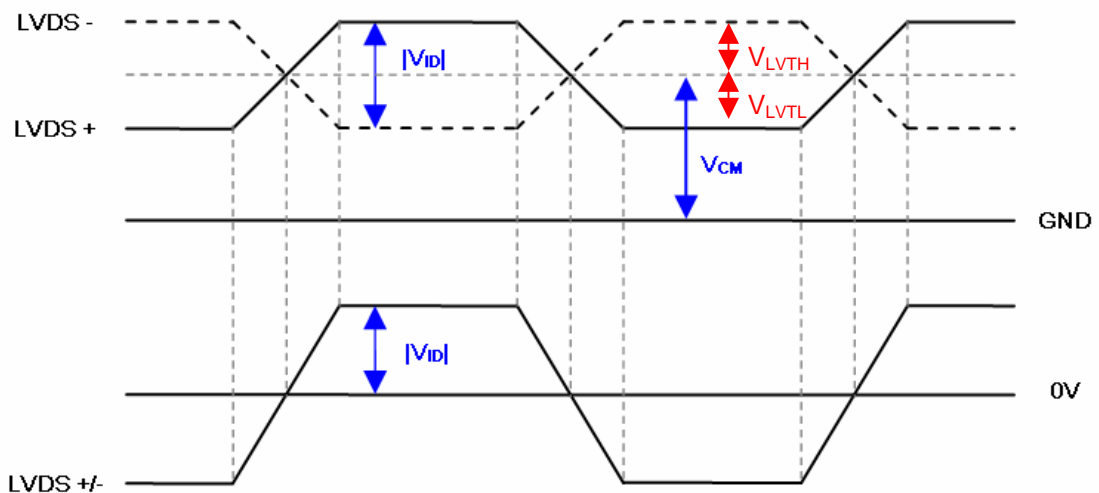


Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 BACK  
3.2.1 LED LI

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current (8 String)	I <sub>f</sub>	-	1240	1320	mA	
One String Current	I <sub>L</sub>	-	155	165	mA	
LED Forward Voltage	V <sub>f</sub>	5.7	6.3	6.7	V <sub>DC</sub>	I <sub>L</sub> =155mA
One String Voltage	V <sub>w</sub>	39.9	-	46.9	V <sub>DC</sub>	I <sub>L</sub> =155mA
One String Voltage Variation	ΔV <sub>w</sub>	-	-	1	V	
Life time	-	30,000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2°C, I<sub>L</sub> =115mA.

### 3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P <sub>BL</sub>	-	60.72	69.84	W	(1), (2) I <sub>L</sub> = 155mA
Converter Input Voltage	V <sub>BL</sub>	22.8	24.0	25.2	V <sub>DC</sub>	
Converter Input Current	I <sub>BL</sub>	-	2.53	2.91	A	Non Dimming
Input Inrush Current	I <sub>R</sub>	-	-	3.94	A <sub>peak</sub>	V <sub>BL</sub> =22.8V,(I <sub>L</sub> =typ.) (3)
Dimming Frequency	FB	150	160	170	Hz	
Minimum Duty Ratio	D <sub>MIN</sub>	5	10	-	%	(4)

Note (1) The power supply capacity should be higher than the total converter power consumption P<sub>BL</sub>.

Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 50" backlight unit under input voltage 24V, average LED current 165mA and lighting 1 hour later.

Note (3) For input inrush current measure, the V<sub>BL</sub> rising time from 10% to 90% is about 30ms.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.0	V	Duty on	(5)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		$F_{EPWM}$	—	150	160	170	Hz	Normal mode	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		Tr1	—	30	—	—	ms	10%-90% $V_{BL}$	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us		
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms		
BLON Delay Time		$T_{on}$	—	300	—	—	ms		
		$T_{on1}$	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. (Fig.2)

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

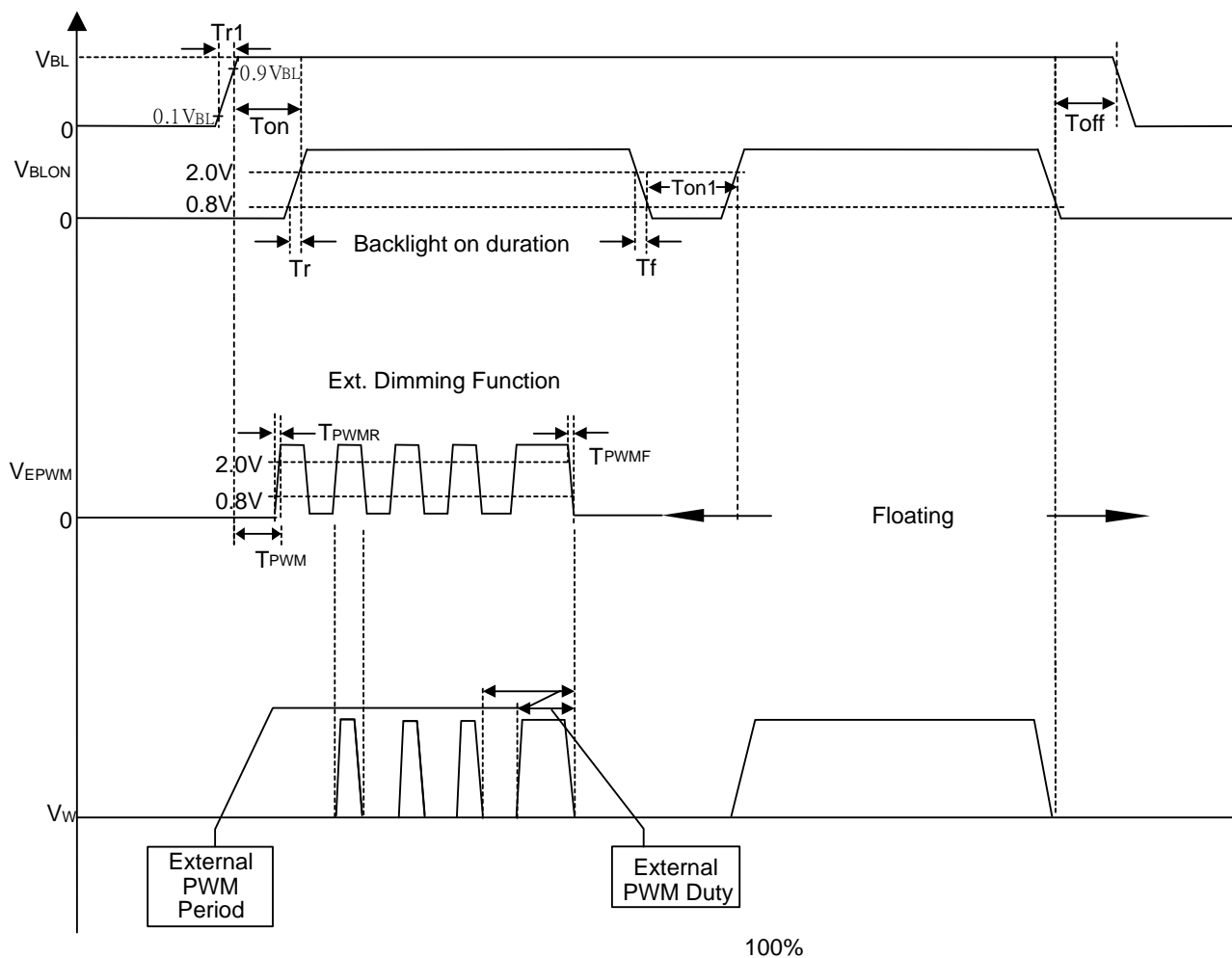


Fig. 1

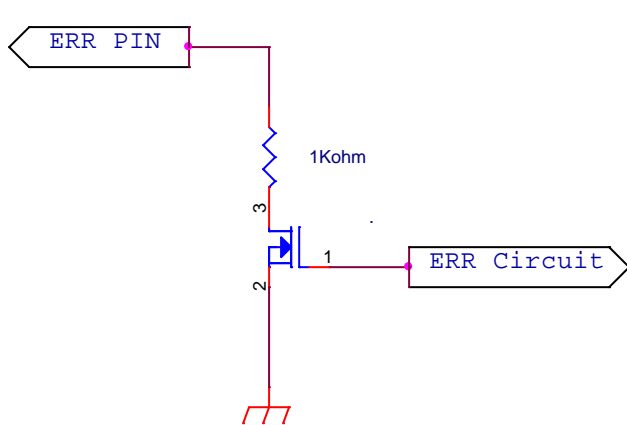


Fig. 2

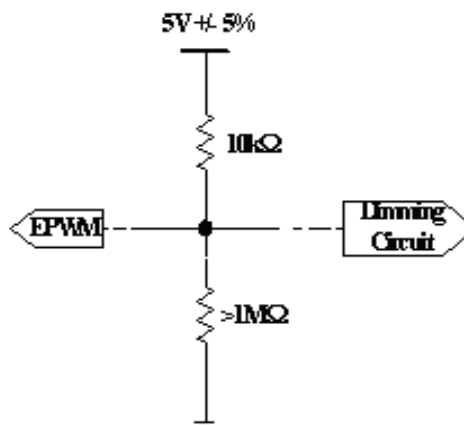
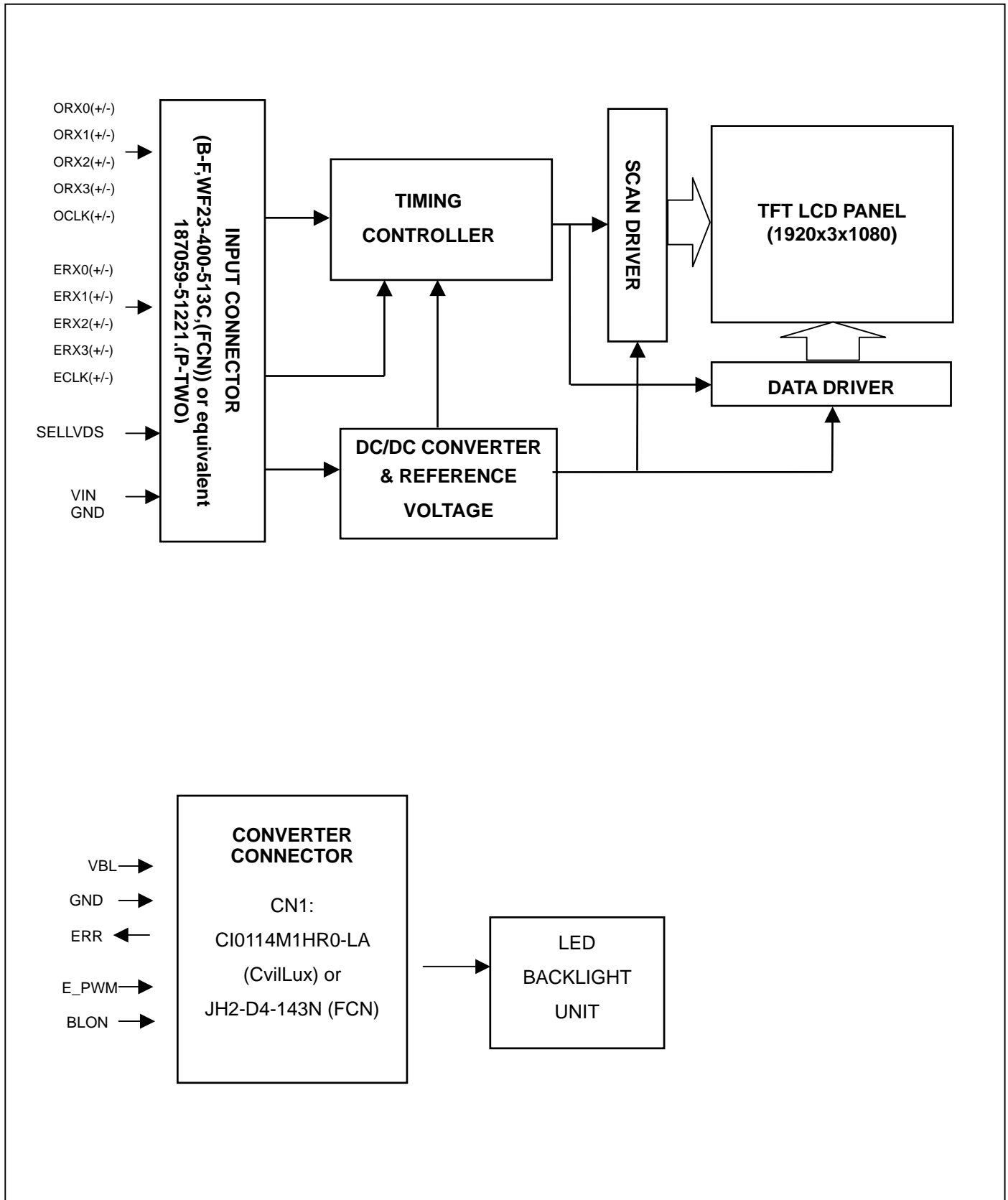


Fig. 3

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



**5 .INPUT TERMINAL PIN ASSIGNMENT**

**5.1 TFT LCD MODULE**

CNF1 Connector Pin Assignment: (WF23-400-513C-FCN) or 187059-51221,(P-TWO)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	(1)
3	N.C.	No Connection	
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS data format Selection	(3)(4)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(2)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input	(2)
20	OCLK+	Odd pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)
28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(2)



29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input.	(2)
36	ECLK+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(2)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	GND	Ground	
43	GND	Ground	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS 2-Port Data Mapping

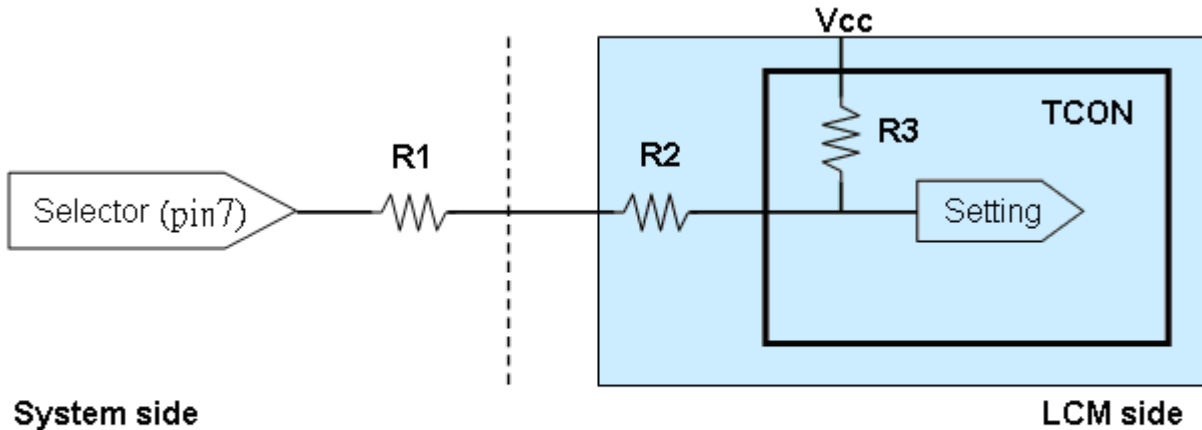
Port	CH of LVDS	Data Stream
1st Port	First pixel	1, 3, 5, ....., 1917, 1919
2nd Port	Second pixel	2, 4, 6, ....., 1918, 1920

Note (3)

SELLVDS	Mode
L	JEIDA
H(default)	VESA

L: Connect to GND, H: Connect to Open or +3.3V

Note (4) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. ( $R1 < 1K \text{ Ohm}$ )



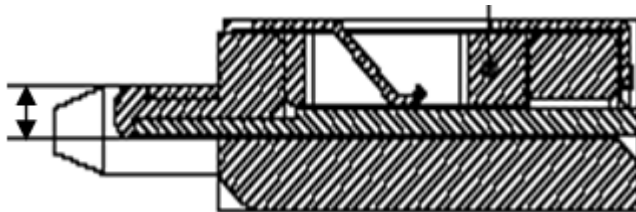
**System side**

**LCM side**

System side  
 $R1 < 1K$

Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (6) LVDS connector mating dimension range request is 0.93mm~1.0mm as follow:



**5.2 BACKLIGHT UNIT**

The pin configuration for the housing and leader wire is shown in the table below.

CN2,3: 196388-12041-3 (P-TWO) B-F or FF01-431-123A (FCN)

Pin No	Symbol	Feature
1	VLED	Positive of LED String
2	VLED	
3	VLED	
4	VLED	
5	NC	NC
6	NC	
7	NC	
8	NC	
9	N4	Negative of LED String
10	N3	
11	N2	
12	N1	

**5.3 DRIVING BOARD UNIT**

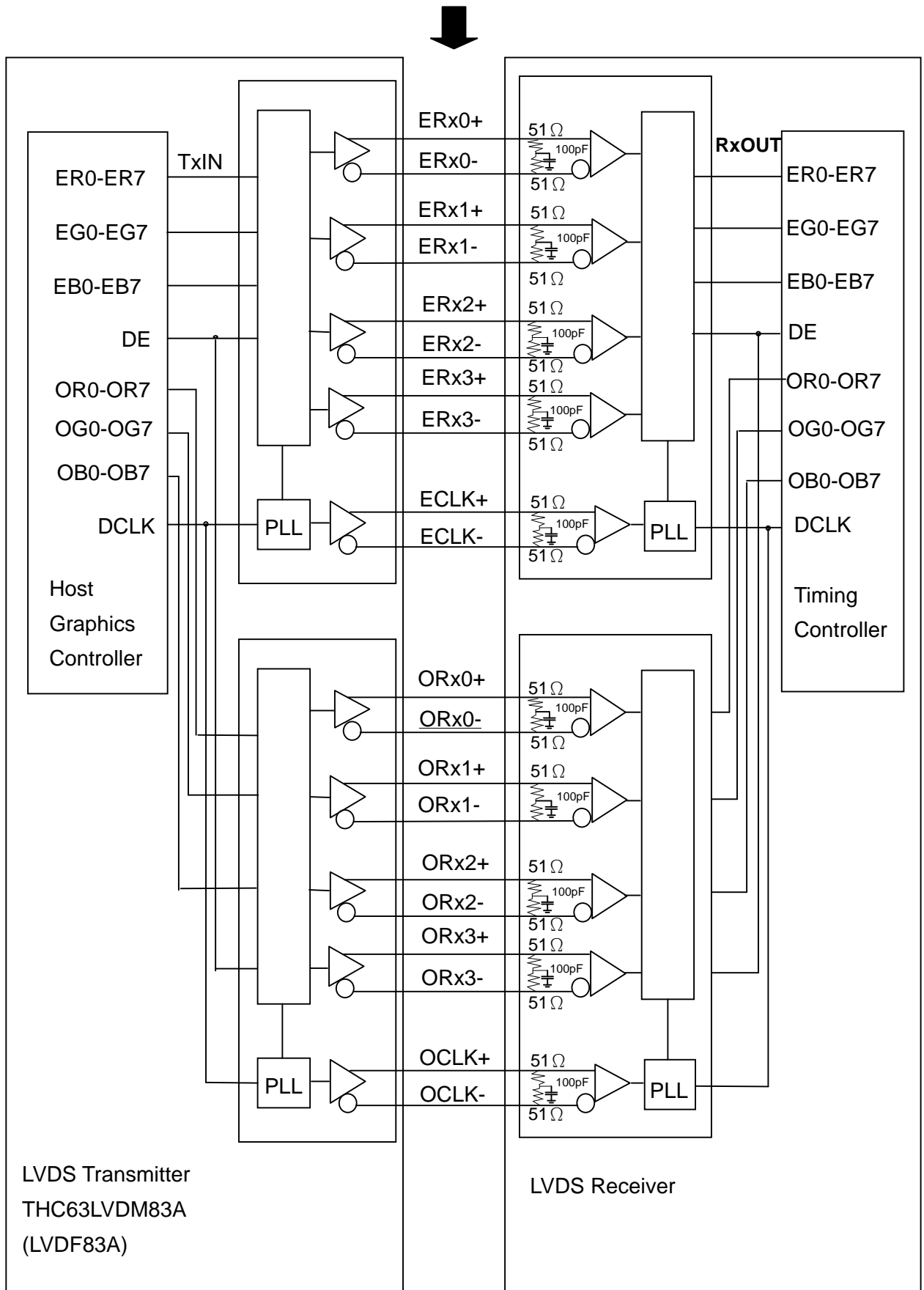
CN1(Header): CI0114M1HR0-LA (CviiLux) or JH2-D4-143N (FCN)

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Notice

1. If Pin14 is open, E\_PWM is 100% duty.

5.4 BLOCK DIAGRAM OF INTERFACE



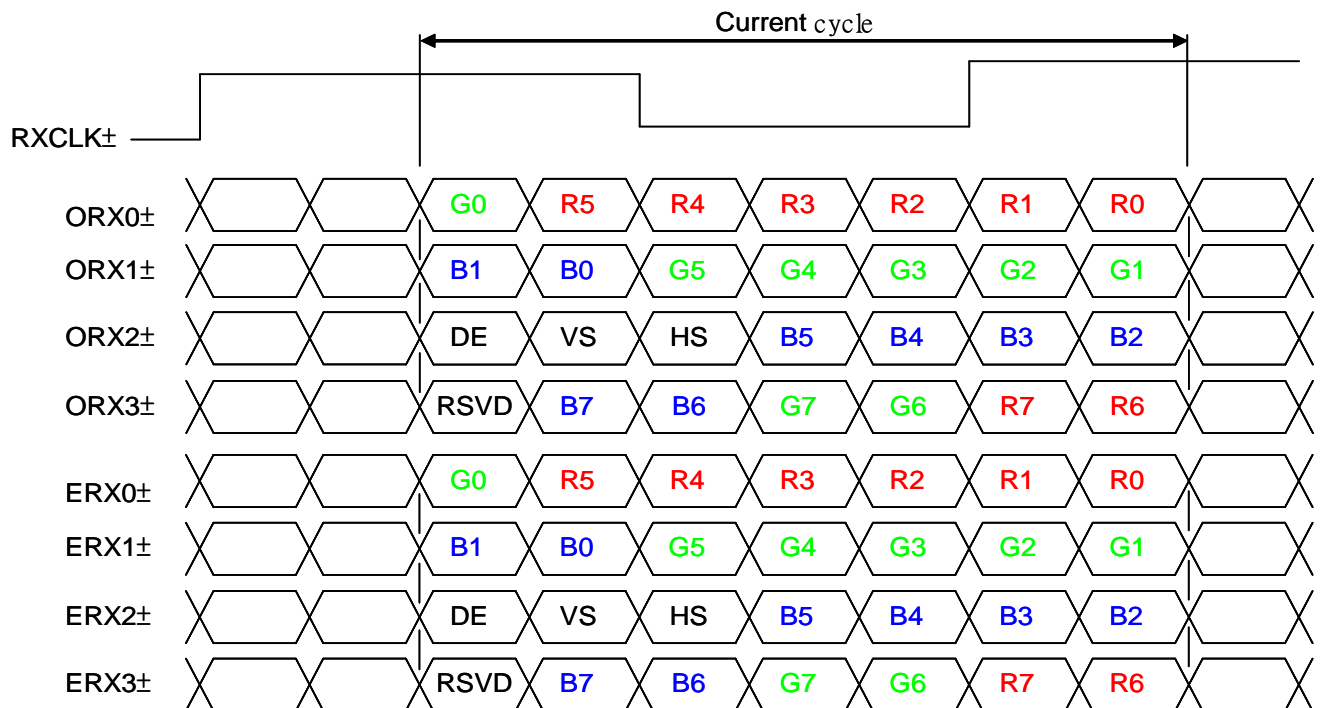
ER0~ER7: Even pixel R data  
 EG0~EG7: Even pixel G data  
 EB0~EB7: Even pixel B data  
 OR0~OR7: Odd pixel R data  
 OG0~OG7: Odd pixel G data  
 OB0~OB7: Odd pixel B data  
 DE: Data enable signal  
 DCLK: Data clock signal

Note (1) The system must have the transmitter to drive the module.

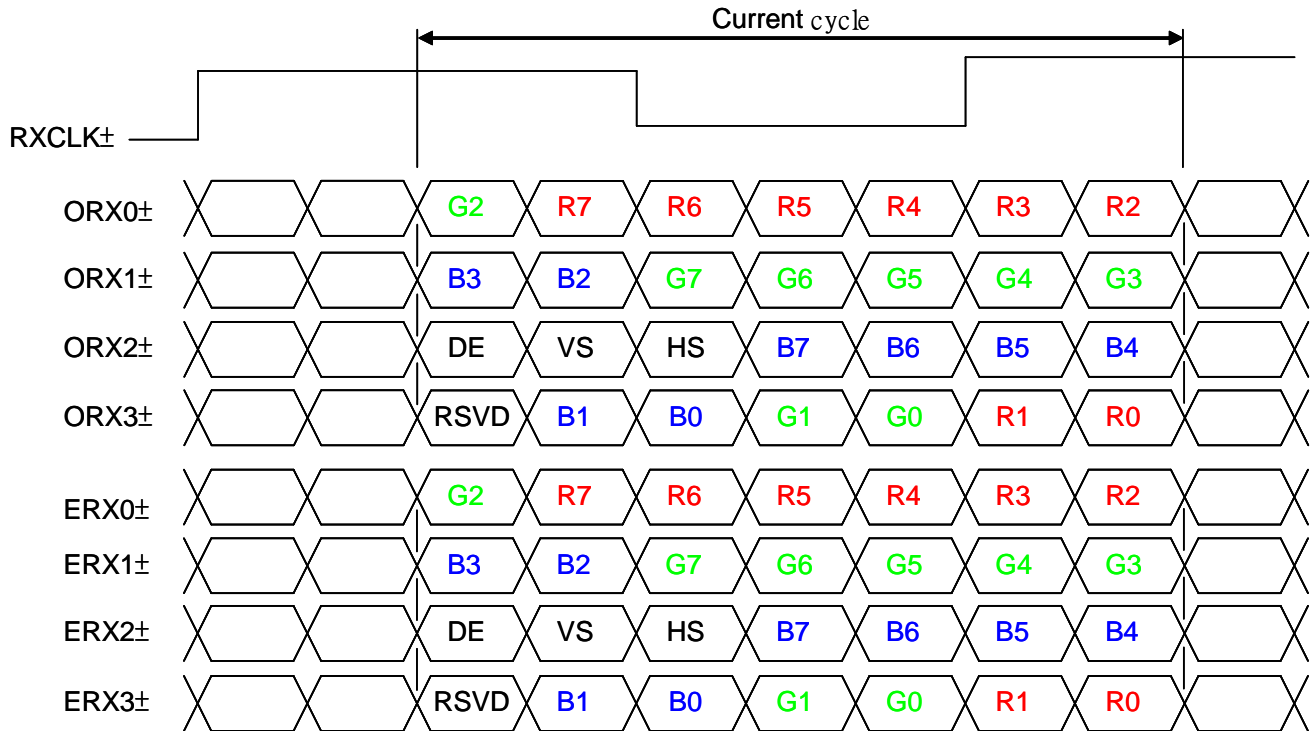
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

### 5.5 LVDS INTERFACE

VESA Format : SELLVDS = H or Open



JEIDA Format : SELLVDS = L



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE: Data enable signal

DCLK : Data clock signal

Note: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

**5.6 COLOR DATA INPUT ASSIGNMENT**

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0		
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0		
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0		
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0		
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1		
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:		
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1		

Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0
Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage



**6. INTERFACE TIMING**

**6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 °C)**

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{clk_{in}}$ (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	$T_{rcj}$	—	—	200	ps	(3)
	Spread spectrum modulation range	$F_{clk_{in\_mod}}$	$F_{clk_{in}}-2\%$	—	$F_{clk_{in}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	$F_{SSM}$	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	$T_{RSKM}$	-400	—	400	ps	(5)
Vertical Active Display Term	Frame Rate	$F_{r5}$	47	50	53	Hz	(6)
		$F_{r6}$	57	60	63	Hz	
	Total	$T_v$	1115	1125	1320	Th	$T_v=T_{vd}+T_{vb}$
	Display	$T_{vd}$	1080	1080	1080	Th	
	Blank	$T_{vb}$	35	45	240	Th	
Horizontal Active Display Term	Total	$T_h$	1050	1100	1150	$T_c$	$T_h=T_{hd}+T_{hb}$
	Display	$T_{hd}$	960	960	960	$T_c$	
	Blank	$T_{hb}$	90	140	190	$T_c$	

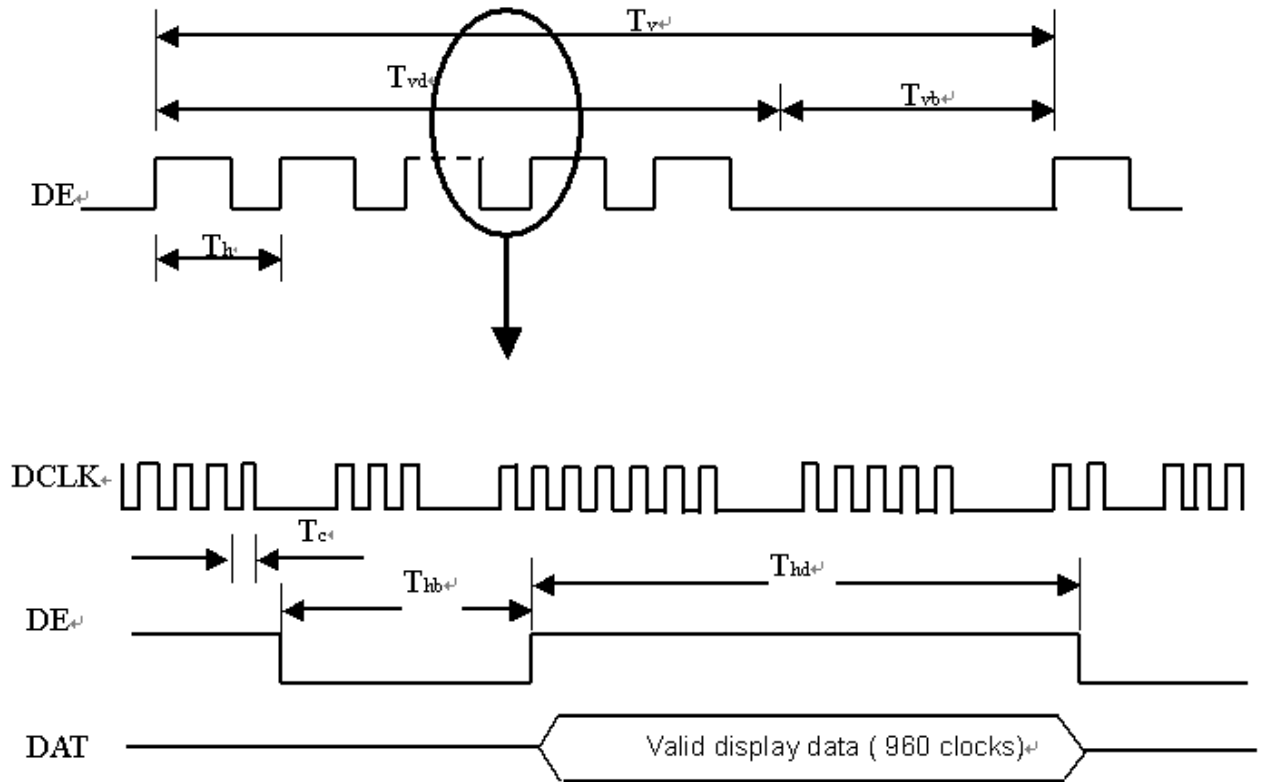
Note (1) Please make sure the range of pixel clock has follow the below equation :

$$F_{clk_{in}(max)} \geq F_{r6} \times T_v \times T_h$$

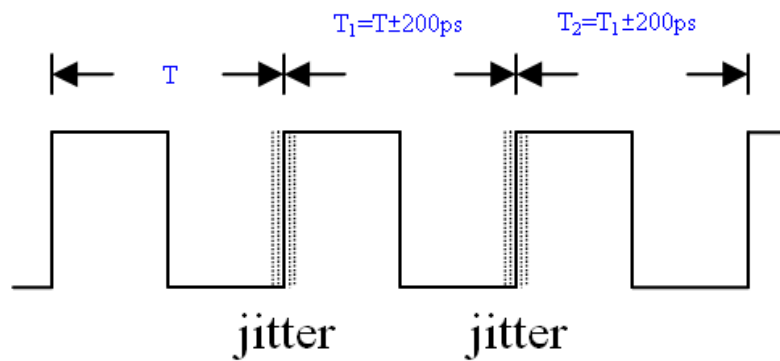
$$F_{r5} \times T_v \times T_h \geq F_{clk_{in}(min)}$$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

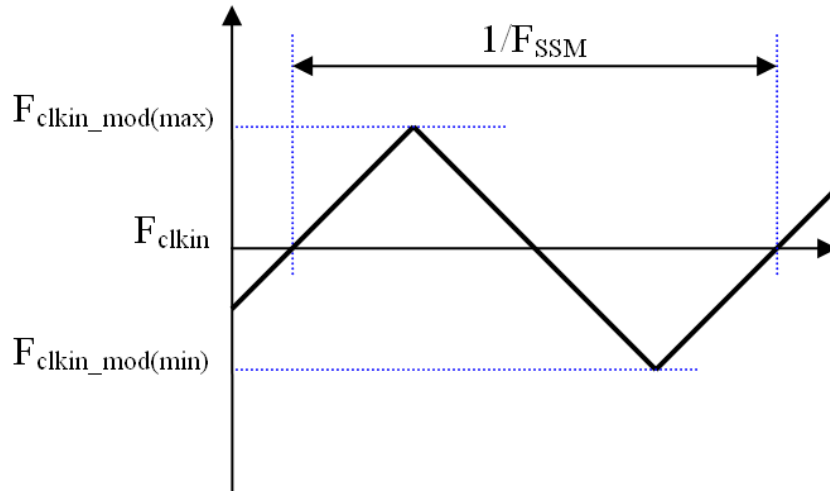
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T_1|$

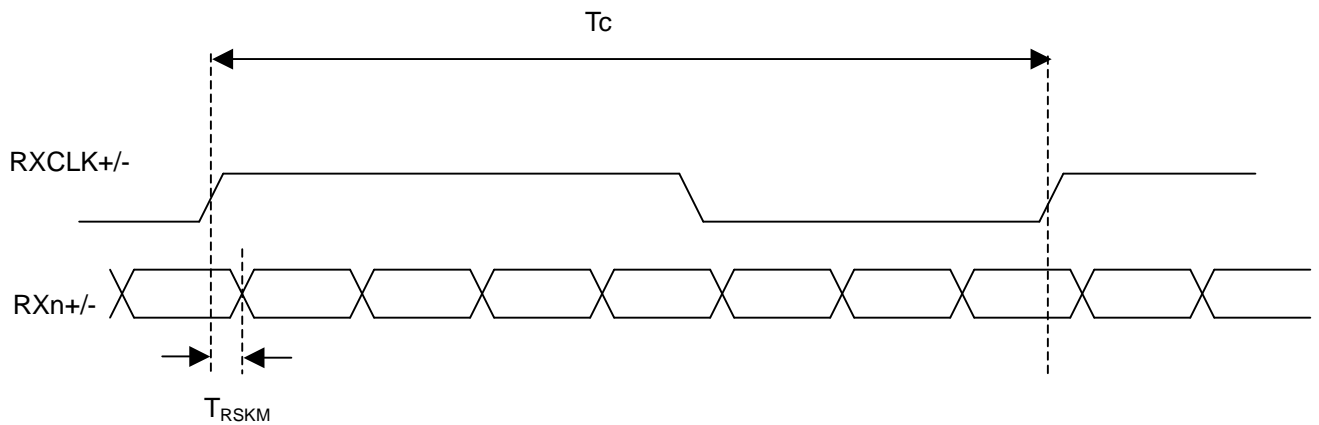


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) LVDS receiver skew margin is defined and shown as below.

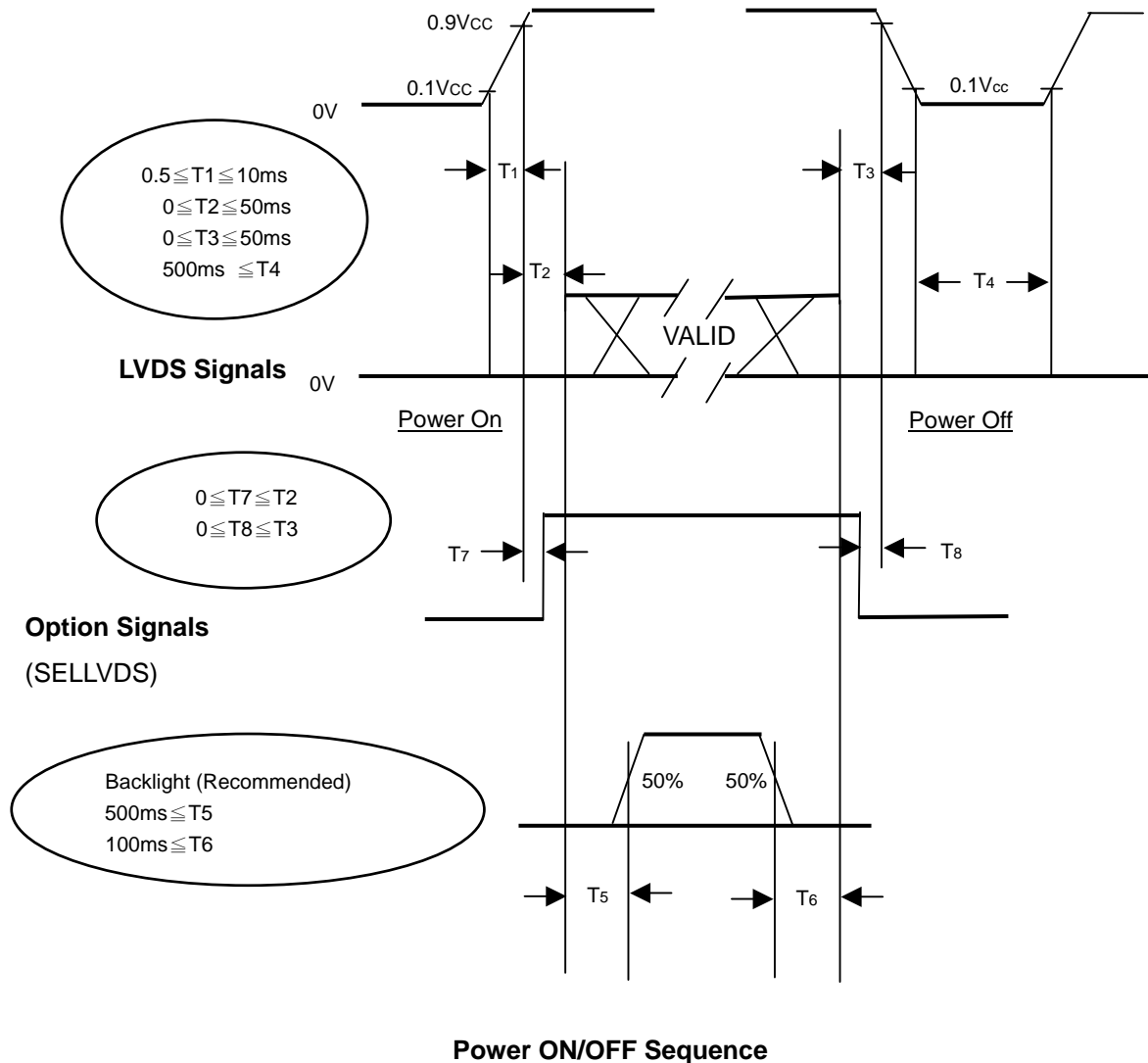
**LVDS RECEIVER INTERFACE TIMING DIAGRAM**



**6.2 POWER ON/OFF SEQUENCE**

( $T_a = 25 \pm 2 \text{ }^\circ\text{C}$ )

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.  
If  $T2 < 0$ , that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

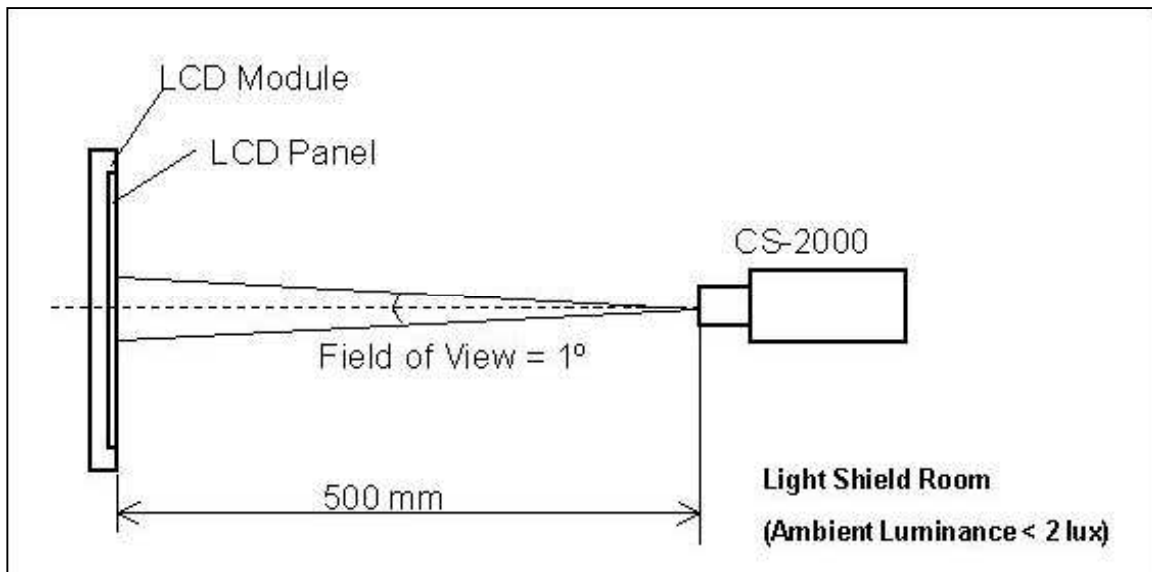
Note (5) Interface signal shall not be kept at high impedance when the power is on.

**7. OPTICAL CHARACTERISTICS**

**7.1 TEST CONDITIONS**

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V <sub>CC</sub>	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I <sub>L</sub>	155	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.

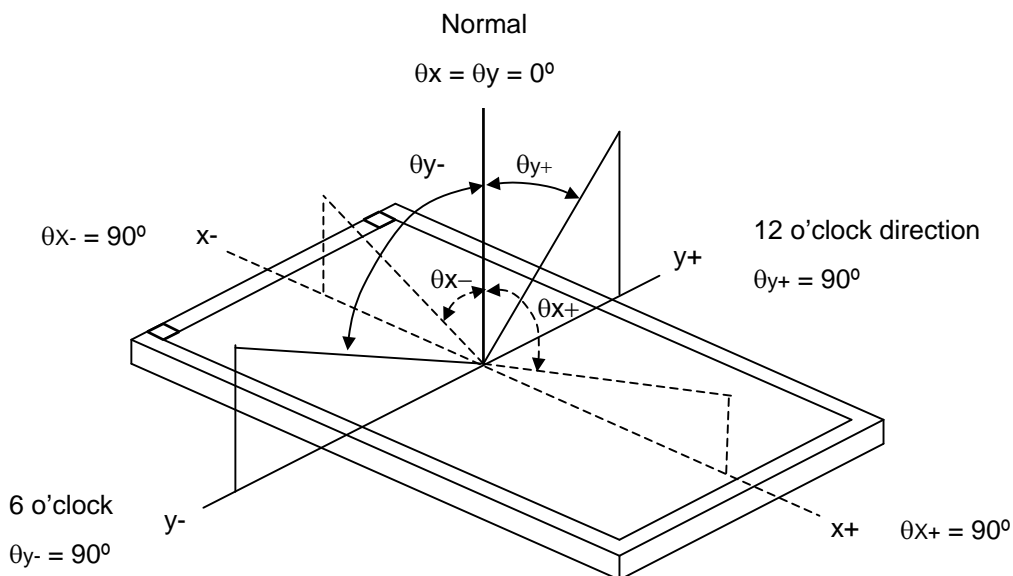


**7.2 OPTICAL SPECIFICATIONS**

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note	
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	(3500)	(5000)	-	-	Note (2)	
Response Time		Gray to gray			(8)	(15)	ms	Note (3)	
CenterLuminance of White		$L_C$		TBD	(350)	-	cd/m <sup>2</sup>	Note (4)	
White Variation		$\delta W$				(1.3)	-	Note (6)	
Cross Talk		CT		-	-	(4)	%	Note (5)	
Color Chromaticity	Red	Rx		Viewing angle at normal direction	Typ.- 0.03	(0.645)	Typ.+ 0.03	-	
		Ry				(0.329)		-	
	Green	Gx				(0.300)		-	
		Gy				(0.600)		-	
	Blue	Bx				(0.152)		-	
		By	(0.050)			-			
	White	Wx	(0.280)			-			
		Wy	(0.290)			-			
	Correlated color temperature					(9800)			
Color Gamut		C.G.	-	72	-	%	NTSC		
Viewing Angle	Horizontal	$\theta_{x+}$	CR $\geq$ 20	80	88	-	Deg.	(1)	
		$\theta_{x-}$		80	88	-			
	Vertical	$\theta_{y+}$		80	88	-			
		$\theta_{y-}$		80	88	-			

Note (1) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):  
Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR) :  
The contrast ratio can be calculated by the following expression.

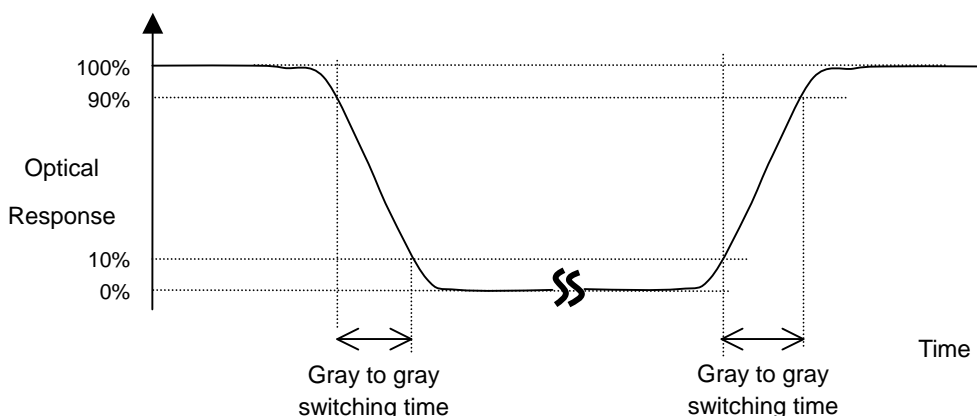
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White ( $L_C$ ):

Measure the luminance of gray level 1023 at center point.

$L_C = L(5)$ , where  $L(x)$  is corresponding to the luminance of the point X at the figure in Note (6).

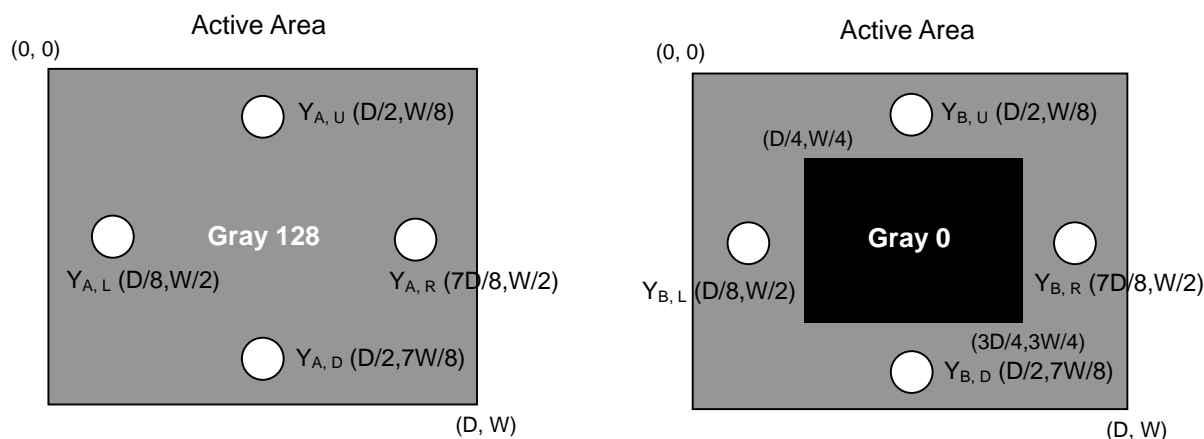
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

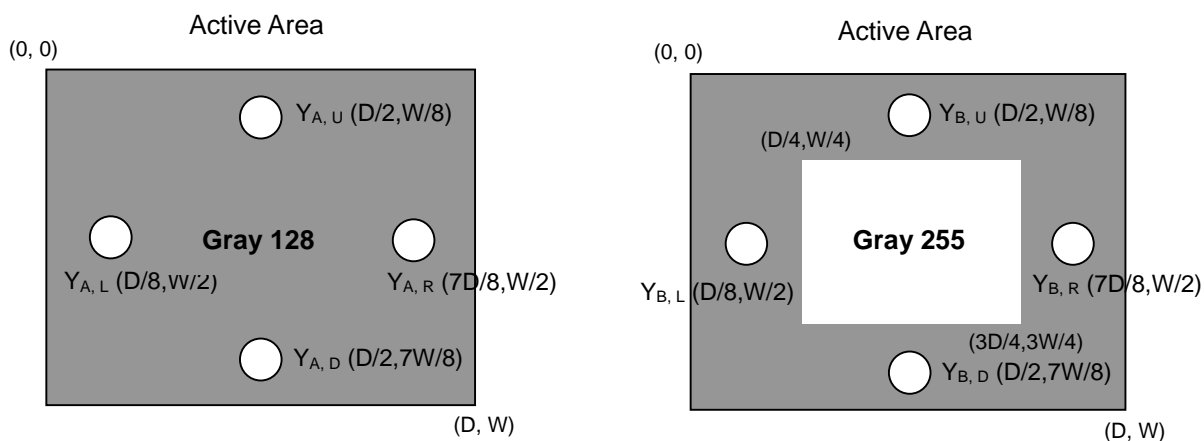
$Y_A$  = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



$Y_A$  = Luminance of measured location without gray level 255 pattern (cd/m<sup>2</sup>)

$Y_B$  = Luminance of measured location with gray level 255 pattern (cd/m<sup>2</sup>)

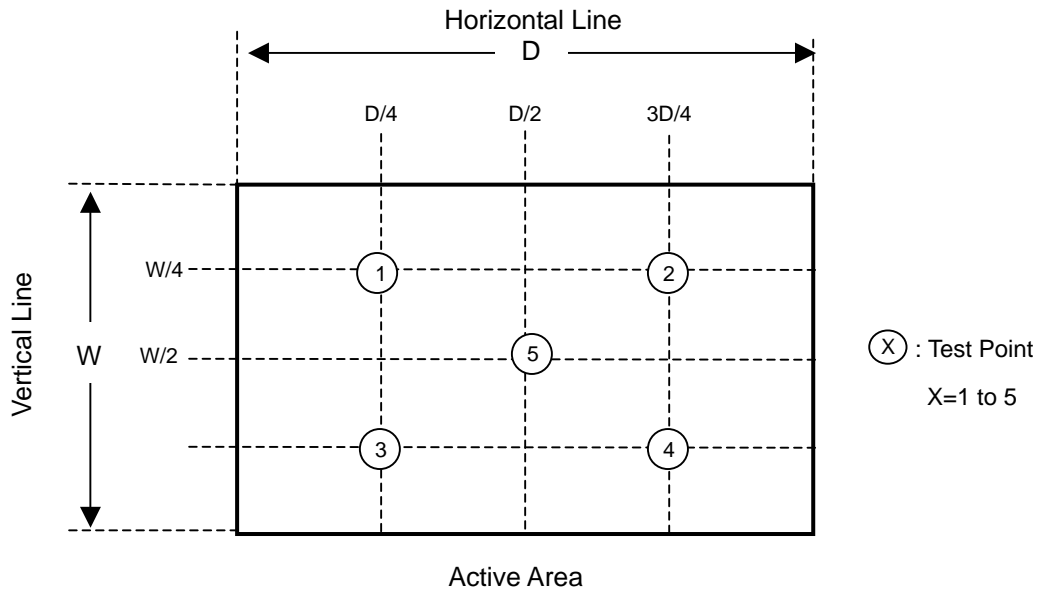


Note (6) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$

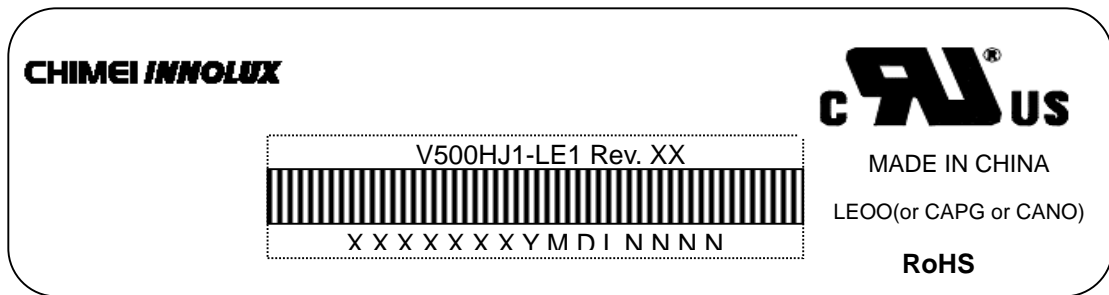
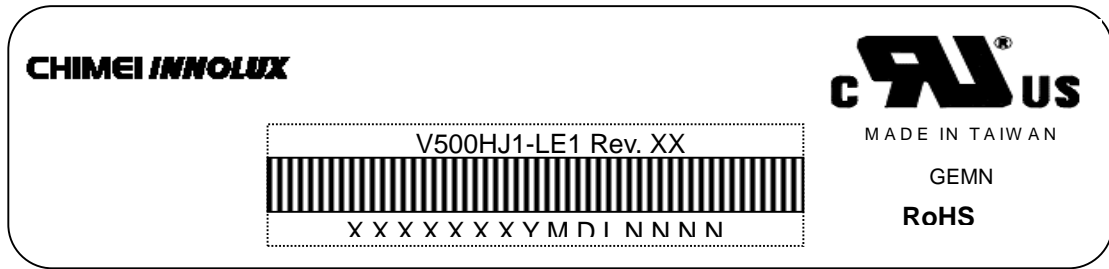




**8. DEFINITION OF LABELS**

**8.1 CMI MODULE LABEL**

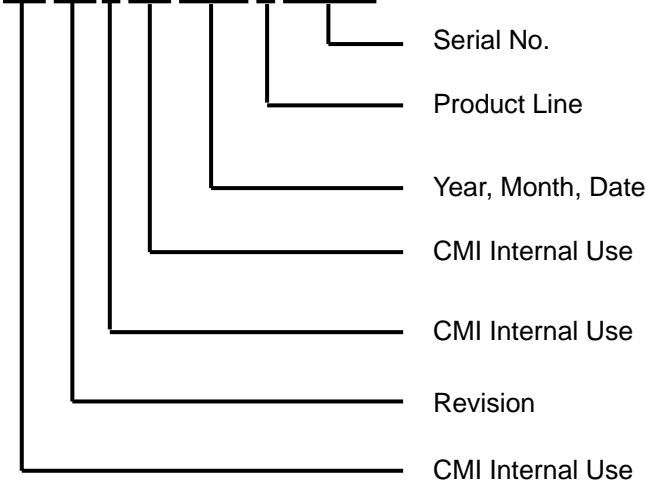
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V500HJ1-LE1

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: XXXXXXYMDLNNNN



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4...2010=0, 2011=1, 2012=2...

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, ...etc.

**9. Packaging**

**9.1 PACKING SPECIFICATIONS**

- (1) 4 LCD TV modules / 1 Box
- (2) Box dimensions: 1235(L) X 258 (W) X 751 (H)
- (3) Weight: approximately 53.6 Kg (4 modules per box)

**9.2 PACKING METHOD**

Figures 9-1 and 9-2 are the packing method

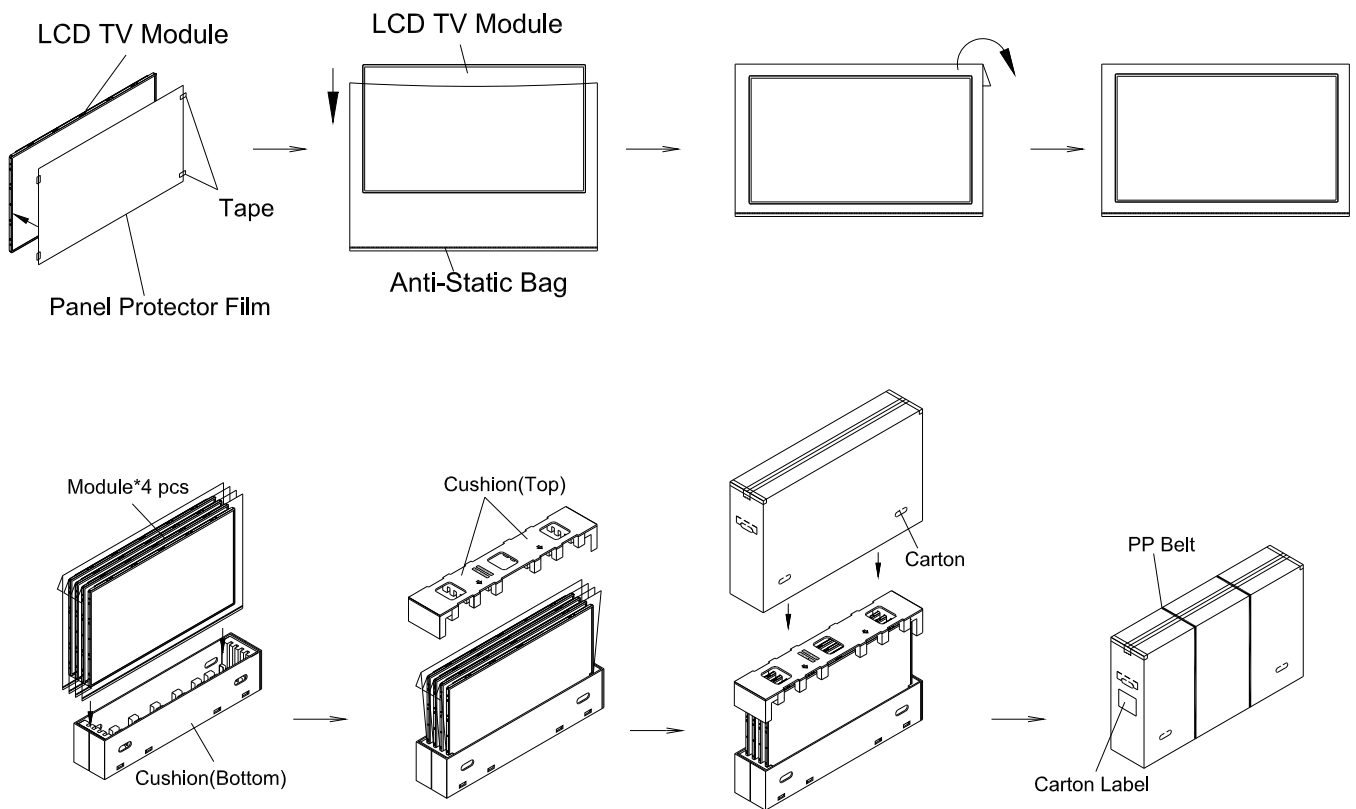
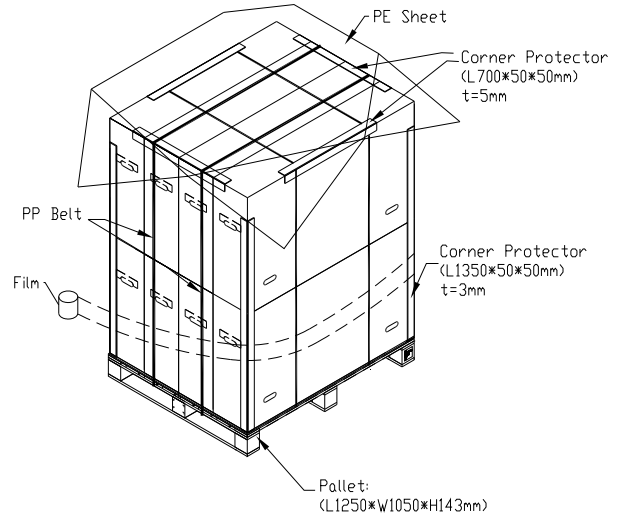
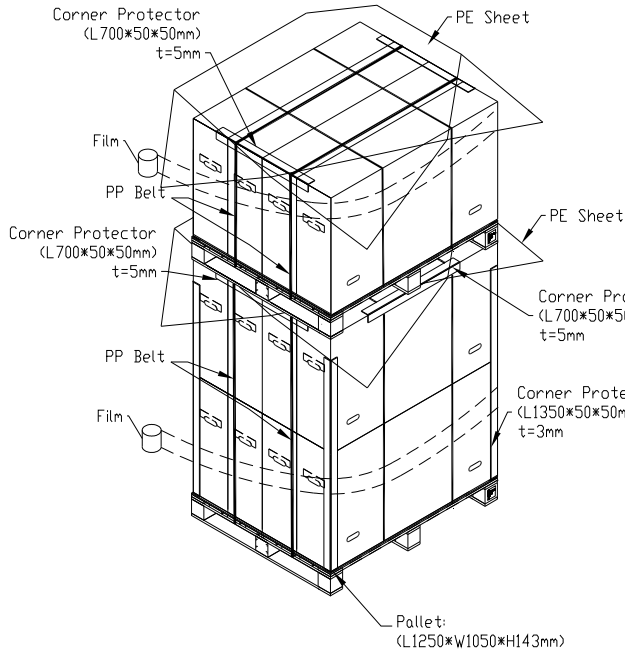


Figure.9-1 packing method

Sea / Land Transportation  
(40ft HQ Container)

Sea / Land Transportation  
(40ft/20ft Container)



Air Transportation

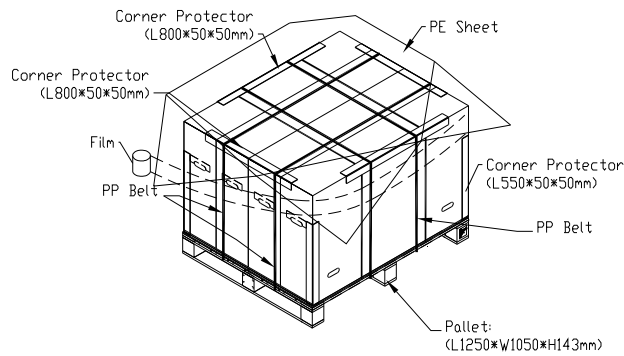


Figure. 9-2 Packing method

**10. PRECAUTIONS**

**10.1 ASSEMBLY AND HANDLING PRECAUTIONS**

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

**10.2 SAFETY PRECAUTIONS**

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

**10.3 SAFETY STANDARDS**

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTIC

