□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V500HK1

SUFFIX: PS1

50.0” FHD_60Hz_Open Cell
Source Board+Control Board+FFC Cable

Customer:

APPROVED BY SIGNATURE

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Use 60 Hz C/B . Part no : 35-D076641

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	YuYin Tsai

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.1	Jul . 31, 2012	All	All	The Approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V500HK1-PS1 is a 50" TFT Liquid Crystal Display product with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 HDTV format and can display true 1.07G colors (8-bit + Hi-FRC /color). The backlight unit is not built in.

1.2 FEATURES

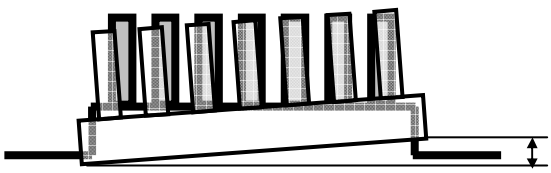
CHARACTERISTICS ITEMS	SPECIFICATIONS
Pixels [lines]	1920 × 1080
Active Area [mm]	1095.84(H) x (V) 616.41
Sub-Pixel Pitch [mm]	0.1903(H) x 0.5708(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	2190
Physical Size [mm]	1110.44 (W) x 631.61(H) x 1.705(D) Typ
Display Mode	Transmissive mode / Normally black
Contrast Ratio	6000:1 Typ. (Typical value measured at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H),+88/-88(V) Typ. (Typical value measured at CMI's module)
Color Chromaticity	Rc=0.662, 0.321 Gc=0.264, 0.563 Bc=0.135, 0.100 Wc=0.302, 0.346 * Please refer to "color chromaticity" on 7.2
Cell Transparency [%]	5.1%Typ. (Typical value measured at CMI's module)
Polarizer Surface Treatment	Anti-Glare coating (3.5% Low Haze) Hardness (3H)

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	-	2190	-	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2), (3)

Note (1)Temperature and relative humidity range is shown in the figure below.

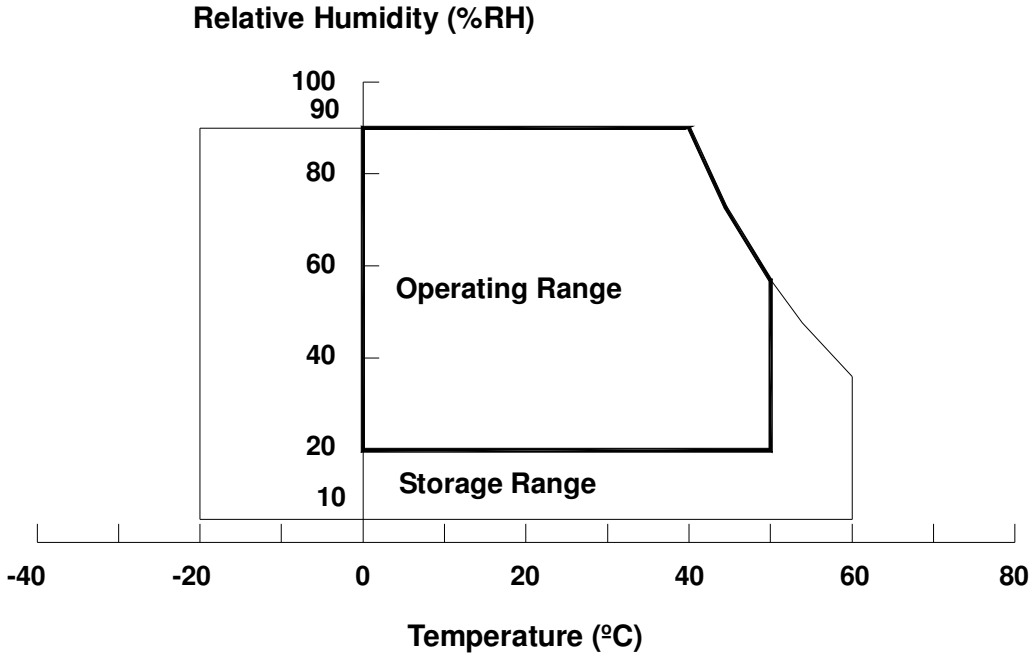
(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.



2.2 ELECTRICAL ABSOLUTE RATINGS(OPEN CELL)

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

3. ELECTRICAL CHARACTERISTICS

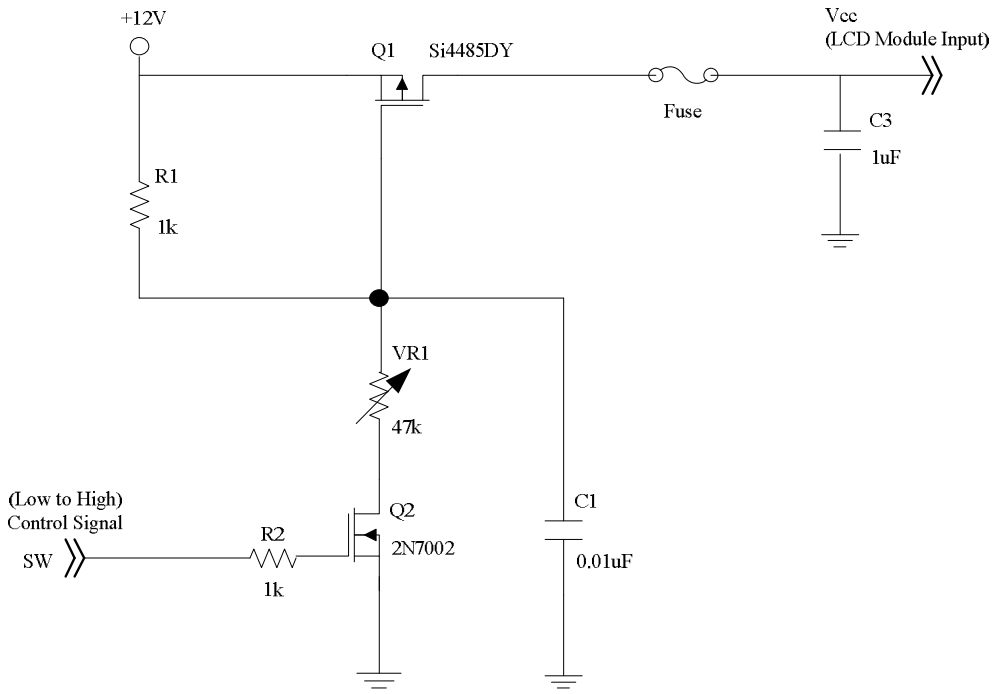
3.1 TFT LCD Module

(Ta = 25 ± 2 ºC)

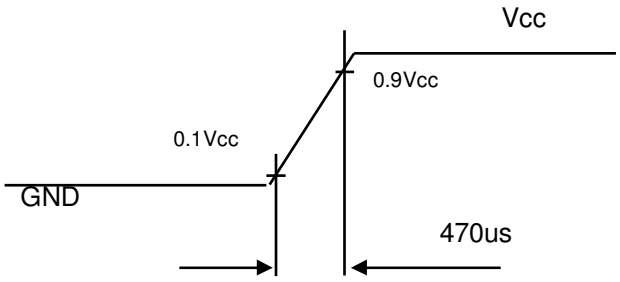
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	3.8	A	(2)
Power Consumption	White Pattern	—	—	4.75	5.77	W	(3)
	Horizontal Stripe	—	—	7.77	8.42	W	
	Black Pattern	—	—	4.03	4.99	W	
Power Supply Current	White Pattern	—	—	0.33	0.43	A	
	Horizontal Stripe	—	—	0.54	0.7	A	
	Black Pattern	—	—	0.28	0.37	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMIS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Vcc rising time is 470us



Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

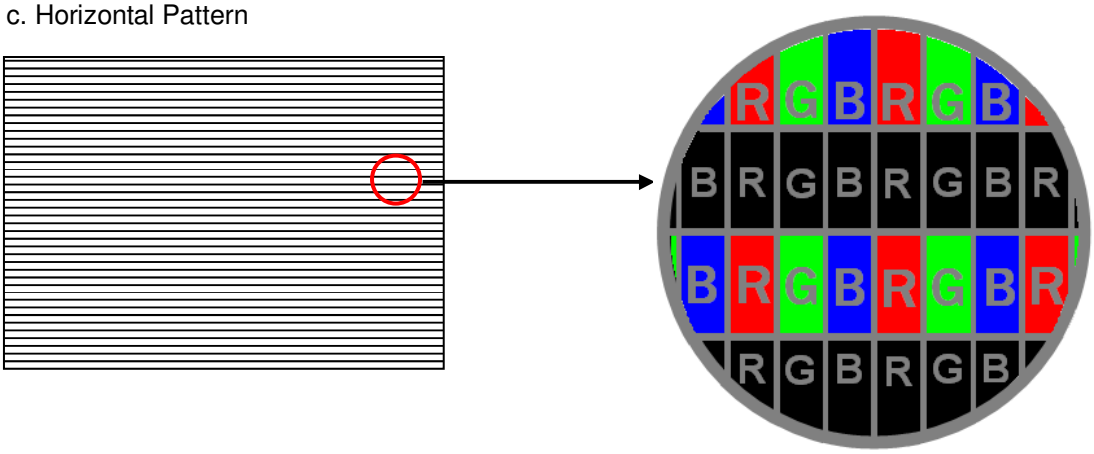
a. White Pattern

Active Area

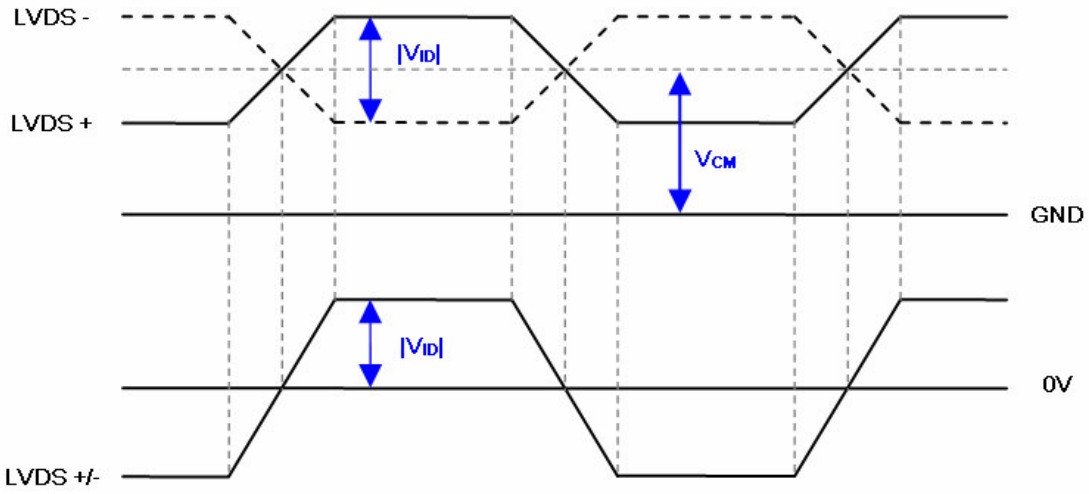
b. Black Pattern

Active Area

c. Horizontal Pattern

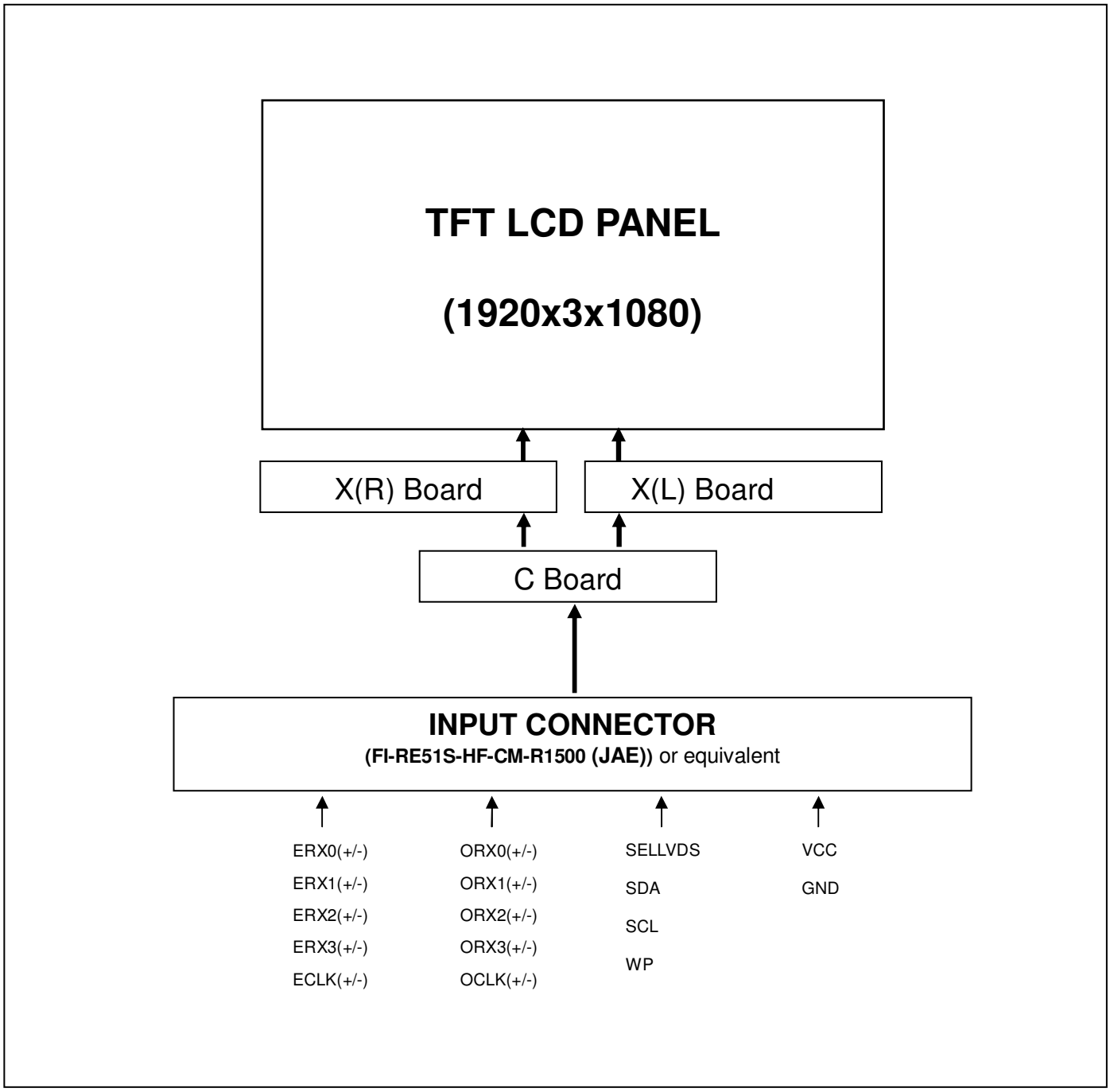


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



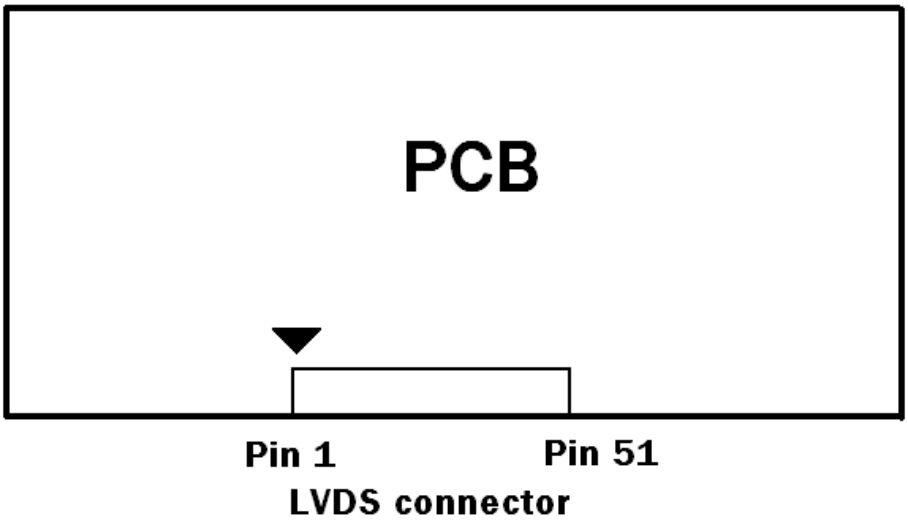
5. INPUT TERMINAL PIN ASSIGNMENT

CNF1 Connector Part No.: JAE Taiwan (台灣航空電子) FI-RE51S-HF-CM-R1500 or equivalent.

Pin	Name	Description	Note
1	VCC	Power input (+12V)	
2	VCC	Power input (+12V)	
3	VCC	Power input (+12V)	
4	VCC	Power input (+12V)	
5	VCC	Power input (+12V)	
6	N.C.	No Connection	(2)
7	GND	Ground	(6)
8	GND	Ground	
9	GND	Ground	
10	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(5)
11	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
12	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
13	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
14	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
15	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
16	GND	Ground	(6)
17	OCLK-	Odd pixel Negative LVDS differential clock input	(5)
18	OCLK+	Odd pixel Positive LVDS differential clock input	
19	GND	Ground	(6)
20	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	(5)
21	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	
22	N.C.	No Connection	(2)
23	N.C.	No Connection	
24	GND	Ground	(6)
25	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(5)
26	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
27	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
28	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
29	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
30	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
31	GND	Ground	(6)
32	ECLK-	Even pixel Negative LVDS differential clock input.	(5)
33	ECLK+	Even pixel Positive LVDS differential clock input.	
34	GND	Ground	(6)

35	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(5)
36	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
37	N.C.	No Connection	(2)
38	N.C.	No Connection	
39	GND	Ground	(6)
42	SCL	EEPROM Serial Clock	
41	N.C.	No Connection	(2)
42	N.C.	No Connection	
43	W.P	Write protection (0V~0.7V/Open→Disable, 2.7V~3.3V→Enable,for auto Vcom)	
44	SDA	EEPROM Serial Data	
45	SELLVDS	LVDS data format Selection	(3)(4)
46	N.C	No Connection	(2)
47	N.C.	No Connection	
48	N.C.	No Connection	
49	N.C.	No Connection	
50	N.C.	No Connection	
51	N.C.	No Connection	

Note (1) LVDS connector pin order defined as follows



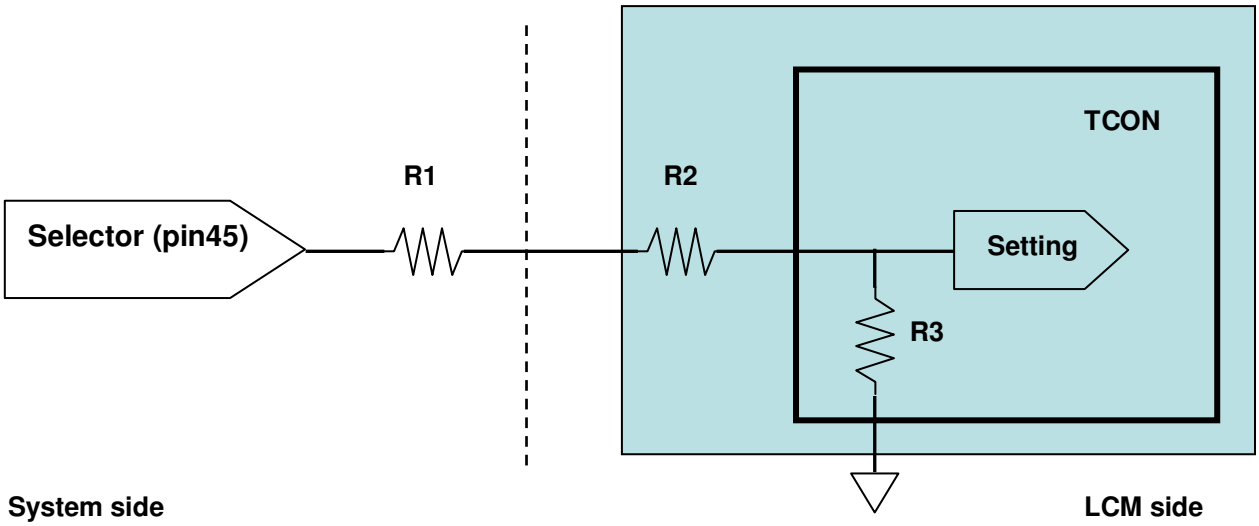
Note (2) Reserved for internal use. Please leave it open.

Note (3) Connect to +3.3V: VESA Format, Open or connect to GND: JEIDA Format.

SELLVDS	Mode
L(default)	JEIDA
H	VESA

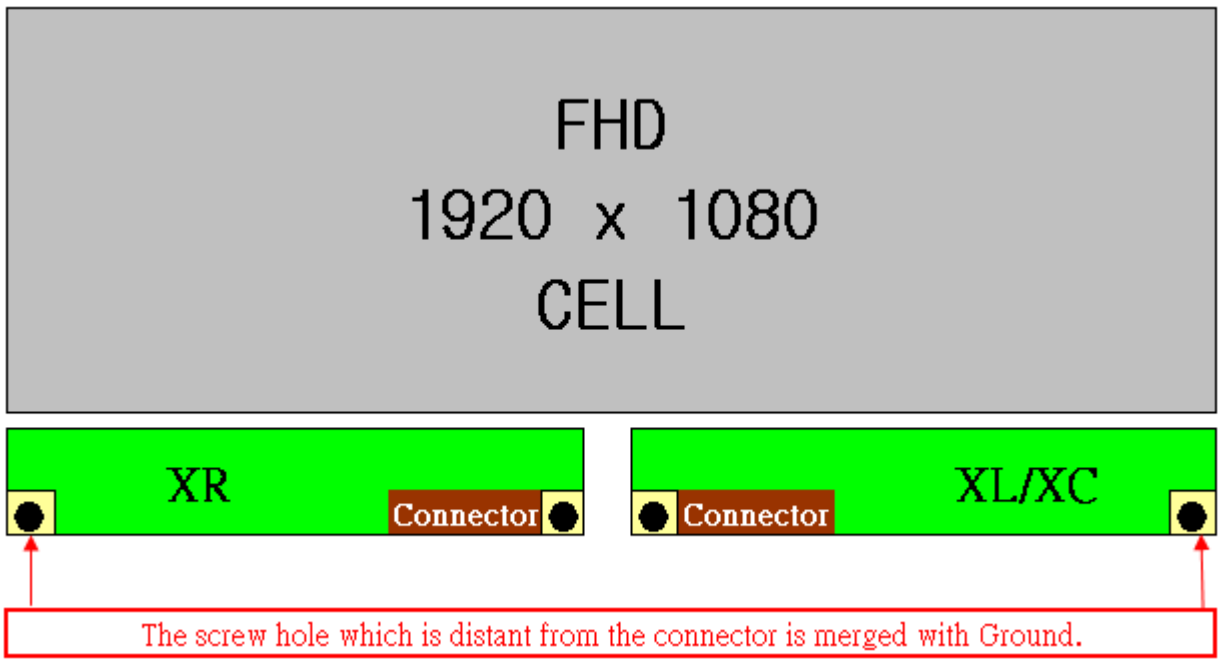
L: Connect to GND, H: Connect to +3.3V

Note (4) LVDS signal pin connected to the LCM side has the following diagram. R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



Note (5) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

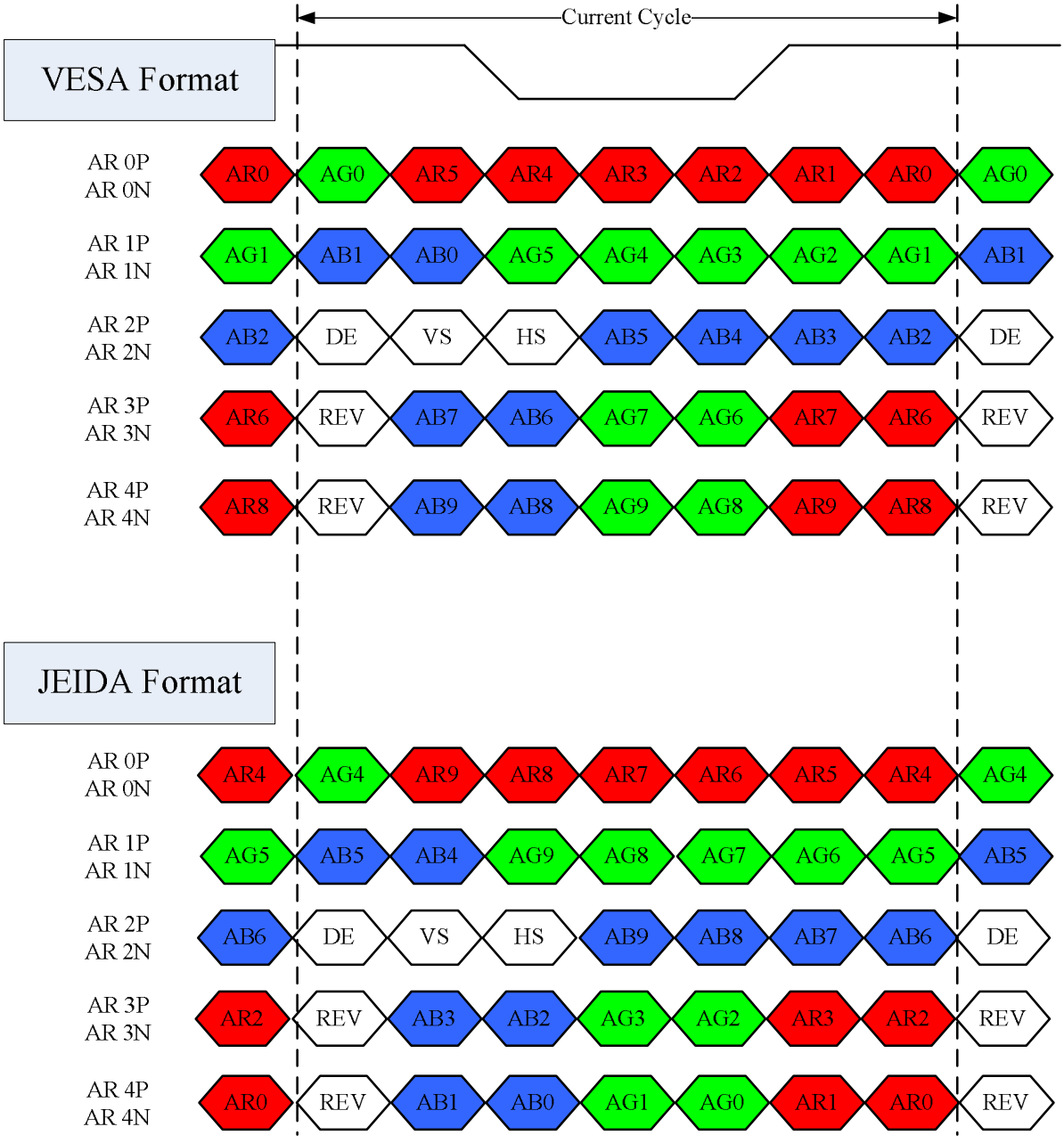
Note (6) The screw hole which is distant from the connector is merged with Ground



5.2 LVDS INTERFACE

VESA Format : SELLVDS = H

JEIDA Format : SELLVDS = L or Open



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSV: Reserved

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red (253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green (254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green (255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue (254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0

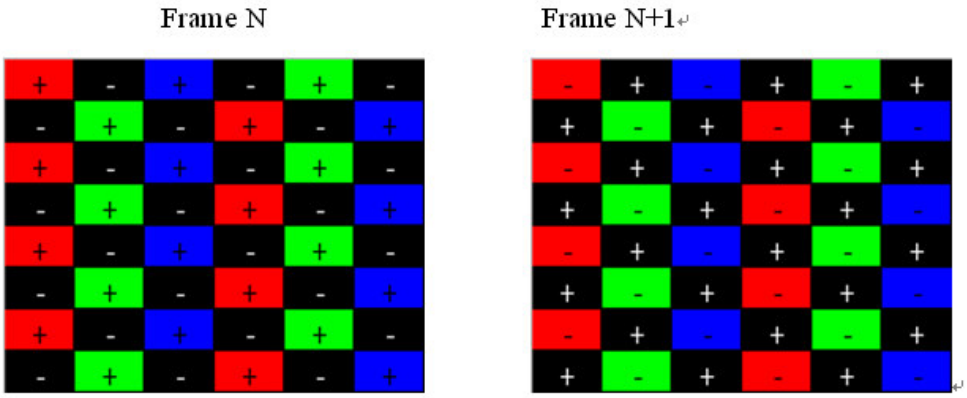
	Blue (255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

Dot-inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE. (bright sub-pixel：G128 ; dark sub-pixel：G0)



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(5)
Vertical Active Display Term	Frame Rate	F_{r5}	—	50	—	Hz	
		F_{r6}	—	60	—	Hz	
	Total	Tv	1115	1125	1135	Th	Tv=Tvd+Tvb
	Display	Tvd	1080	1080	1080	Th	—
	Blank	Tvb	35	45	55	Th	—
Horizontal Active Display Term	Total	Th	1030	1100	1325	Tc	Th=Thd+Thb
	Display	Thd	960	960	960	Tc	—
	Blank	Thb	70	140	365	Tc	—

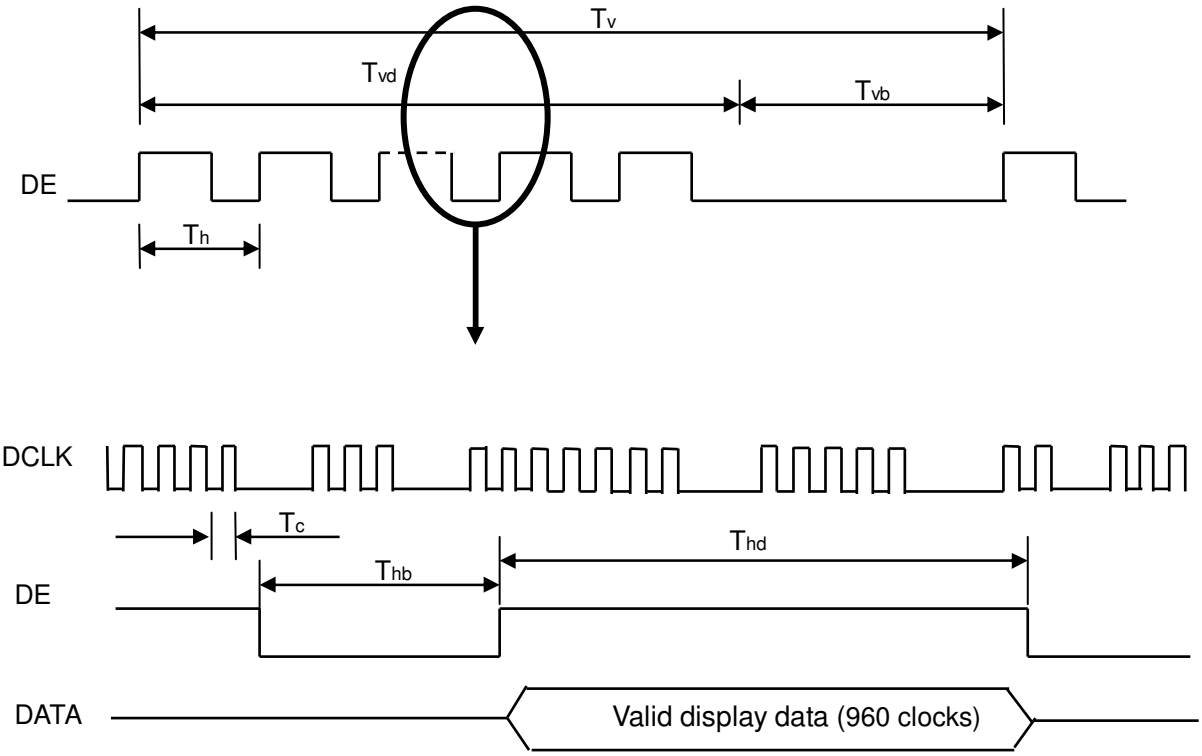
Note (1) Please make sure the range of pixel clock has follow the below equation：

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

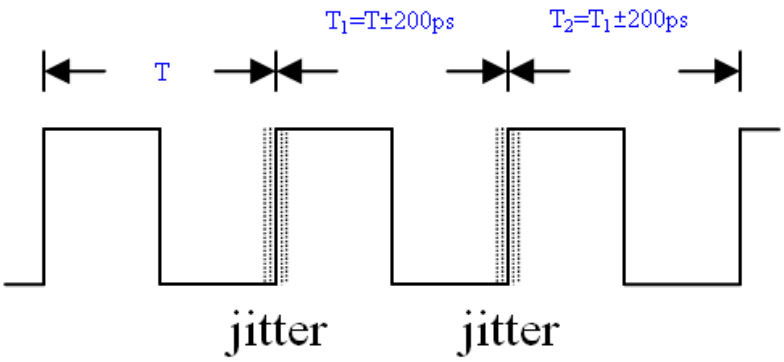
$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below：

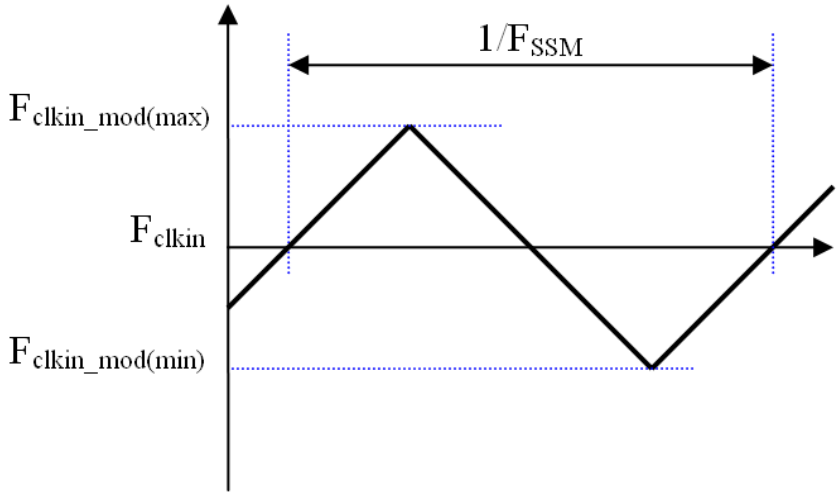
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

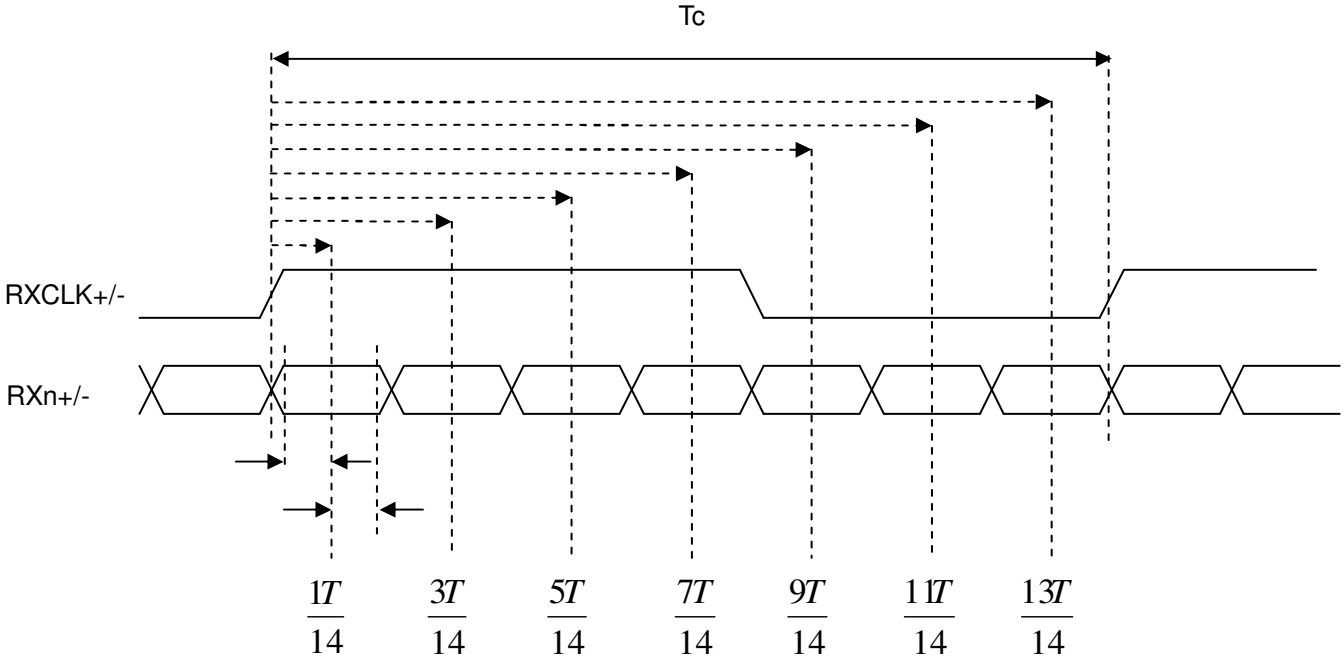


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

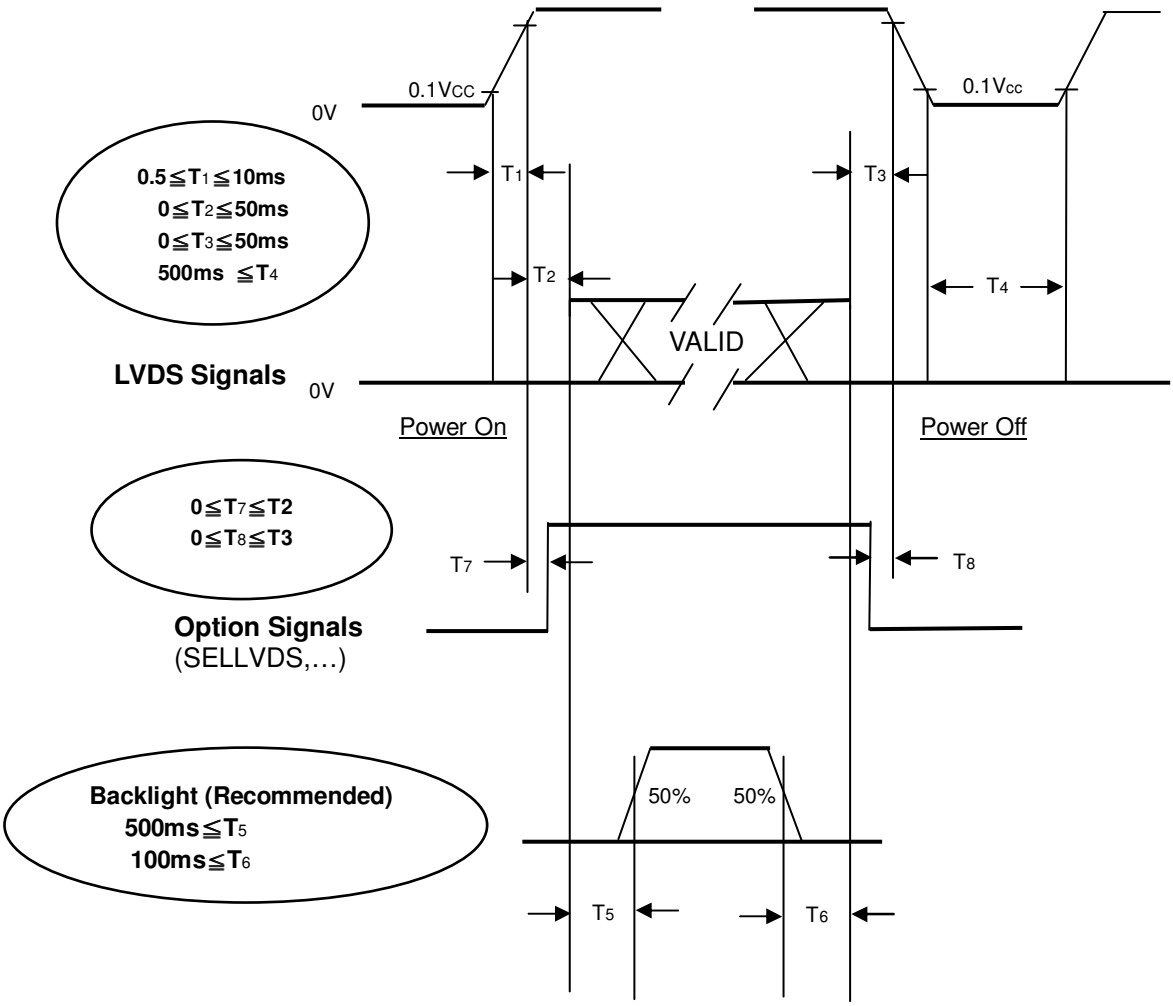
LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Pow

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

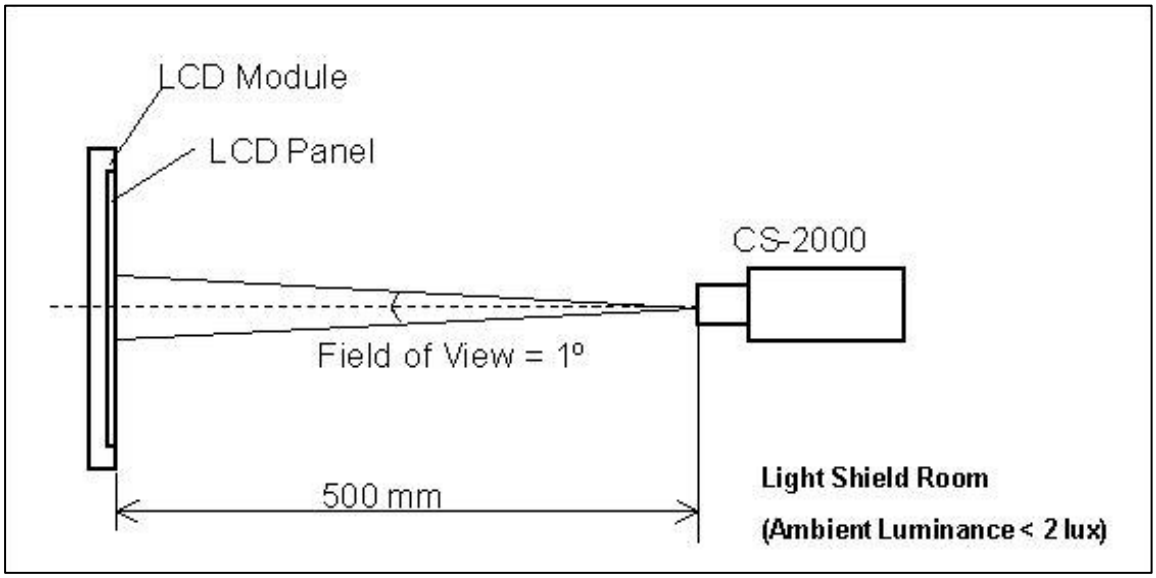
Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I_L	115	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	Typ. -0.03	0.662	Typ. +0.03	-	(0)
		Rcy			0321		-	
	Green	Gcx			0.264		-	
		Gcy			0.563		-	
	Blue	Bcx			0.135		-	
		Bcy			0.100		-	
	White	Wcx			0.302		-	
		Wcy			0.346		-	
Center Transmittance		T%	θ_x=0°, θ_Y =0° with CMI module	-	5.1		%	(1),(6)
Contrast Ratio		CR			6000		-	(1),(3)
Response Time		Gray to gray	θ_x=0°, θ_Y =0° with CMI Module	-	8		ms	(1),(4)
White Variation		δW	θ_x=0°, θ_Y =0° with CMI module	-	-	1.3	-	(1),(5)
Viewing Angle	Horizontal	θ_x+	CR≥20 With CMI module	-	88	-	Deg.	(1),(2)
		θ_x-		-	88	-		
	Vertical	θ_Y+		-	88	-		
		θ_Y-		-	88	-		

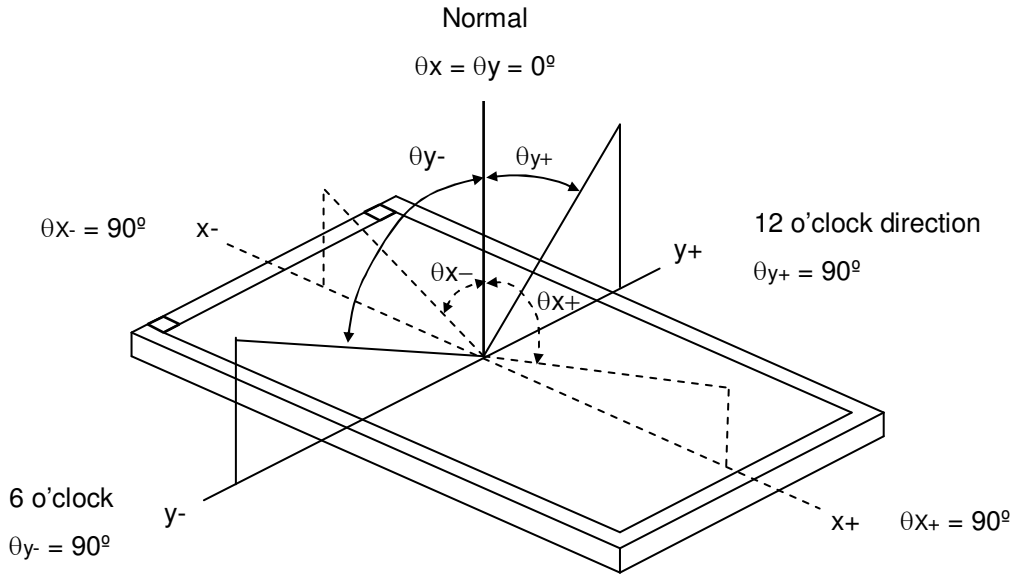
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum at center point. White and R,G,B are with signal input. BLU (for V500HK1-LS5) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

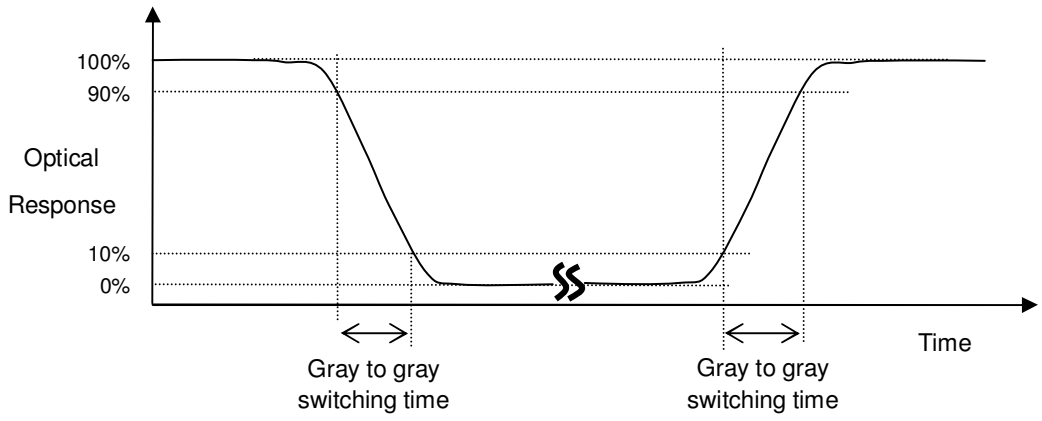
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Gray-to-Gray Switching Time:



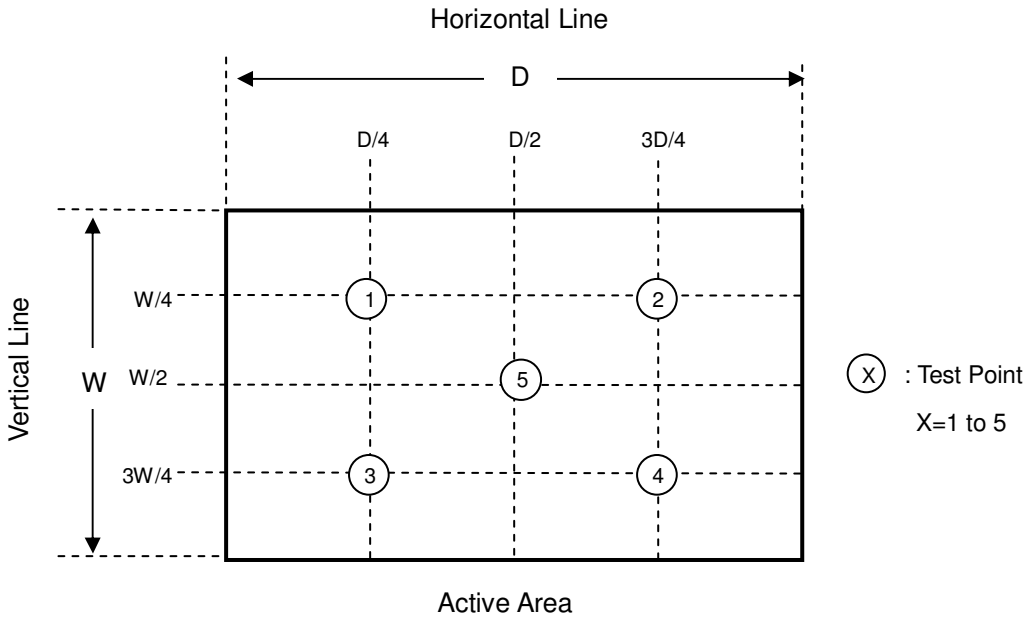
The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



Note (6) Definition of Transmittance (T%) :

Measure the luminance of gray level 1023 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\%$$

8.PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[10] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal contro

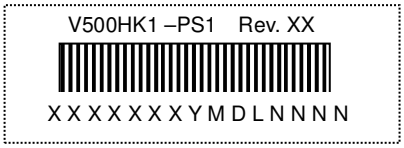
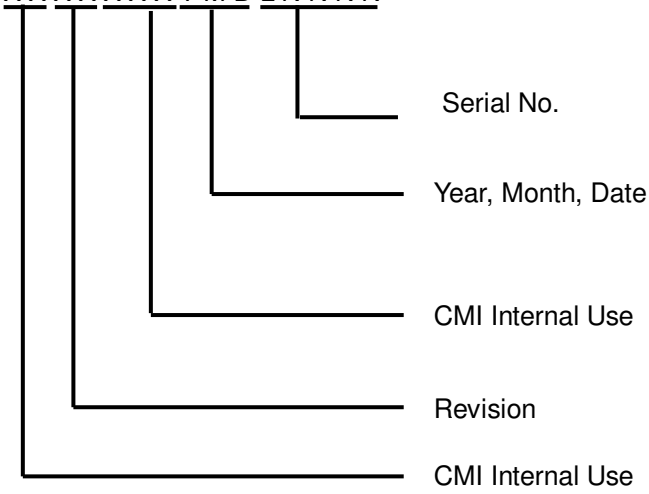


Figure.9-1 Serial No. Label on SPWB

Model Name: V500HK1-PS1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

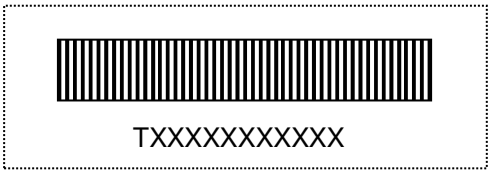
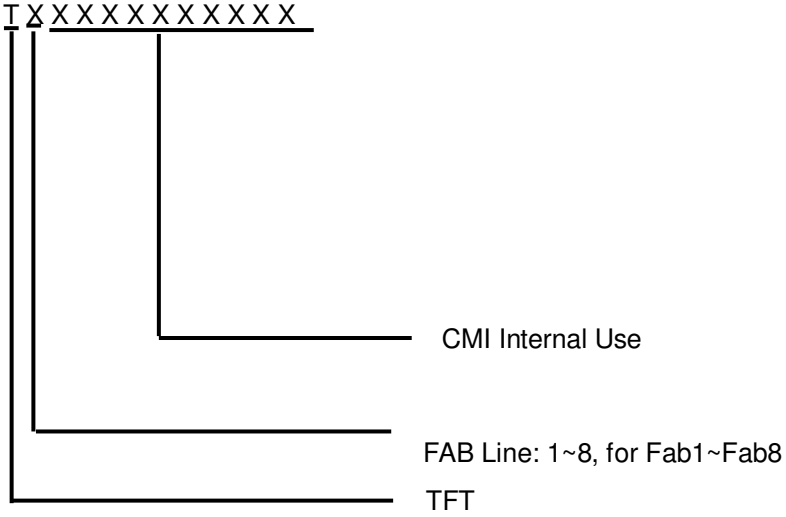


Figure.9-2 Panel ID Label on Cell

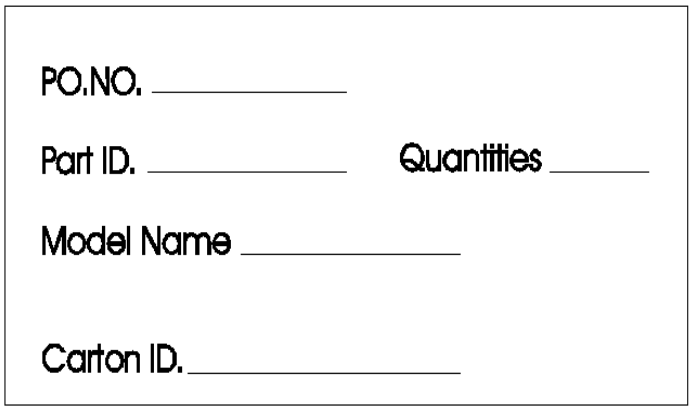
Panel ID Label includes the information as below:

Panel ID: T X X X X X X X X X X X



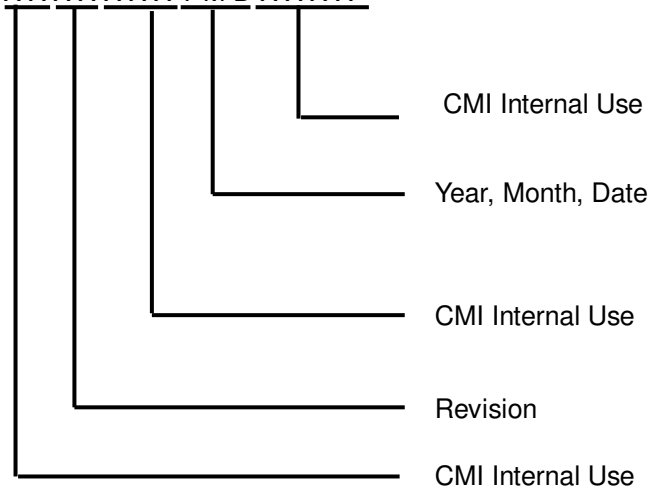
9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



(a) Model Name: V500HK1– PS1

(b) Carton ID: X X X X X X X Y M D X X X X



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

(c) Quantities: 8

10. Packaging

10.1 PACKING SPECIFICATIONS

(1) 8 LCD TV Panels / 1 Box

(2) Box dimensions : 1320 (L) X910 (W) X99 (H)mm

(3) Weight : approximately 38 Kg (8 panels per box)

(4) 80 LCD TV Panels / 1 Group

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

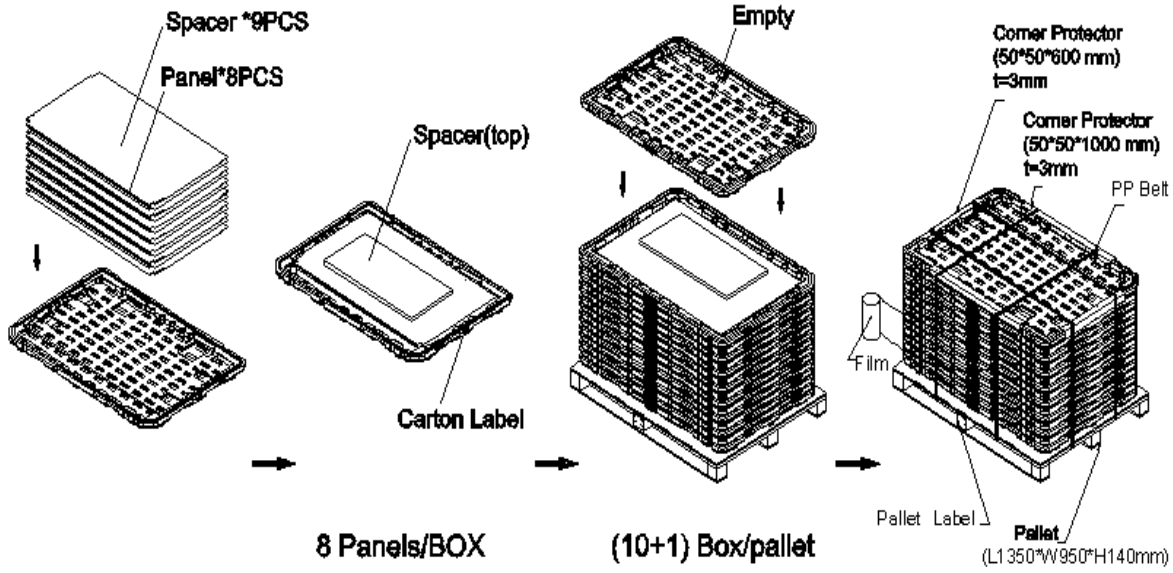
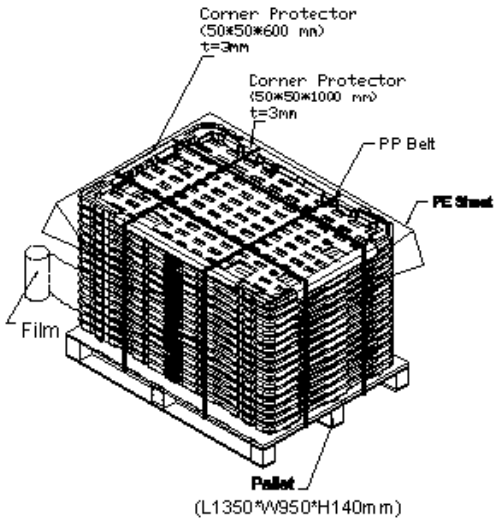


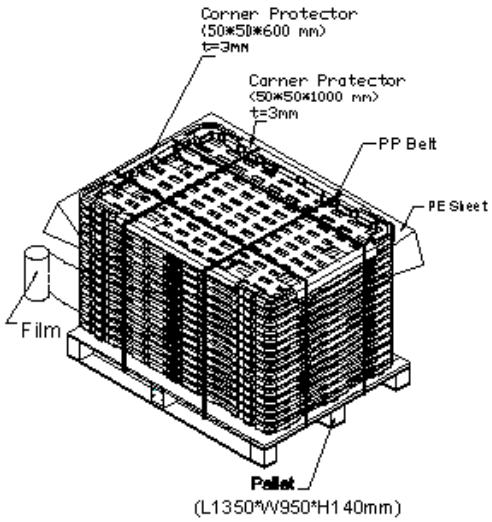
Figure.10-1 packing method

Sea / Land Transportation



(10+1) Box/pallet

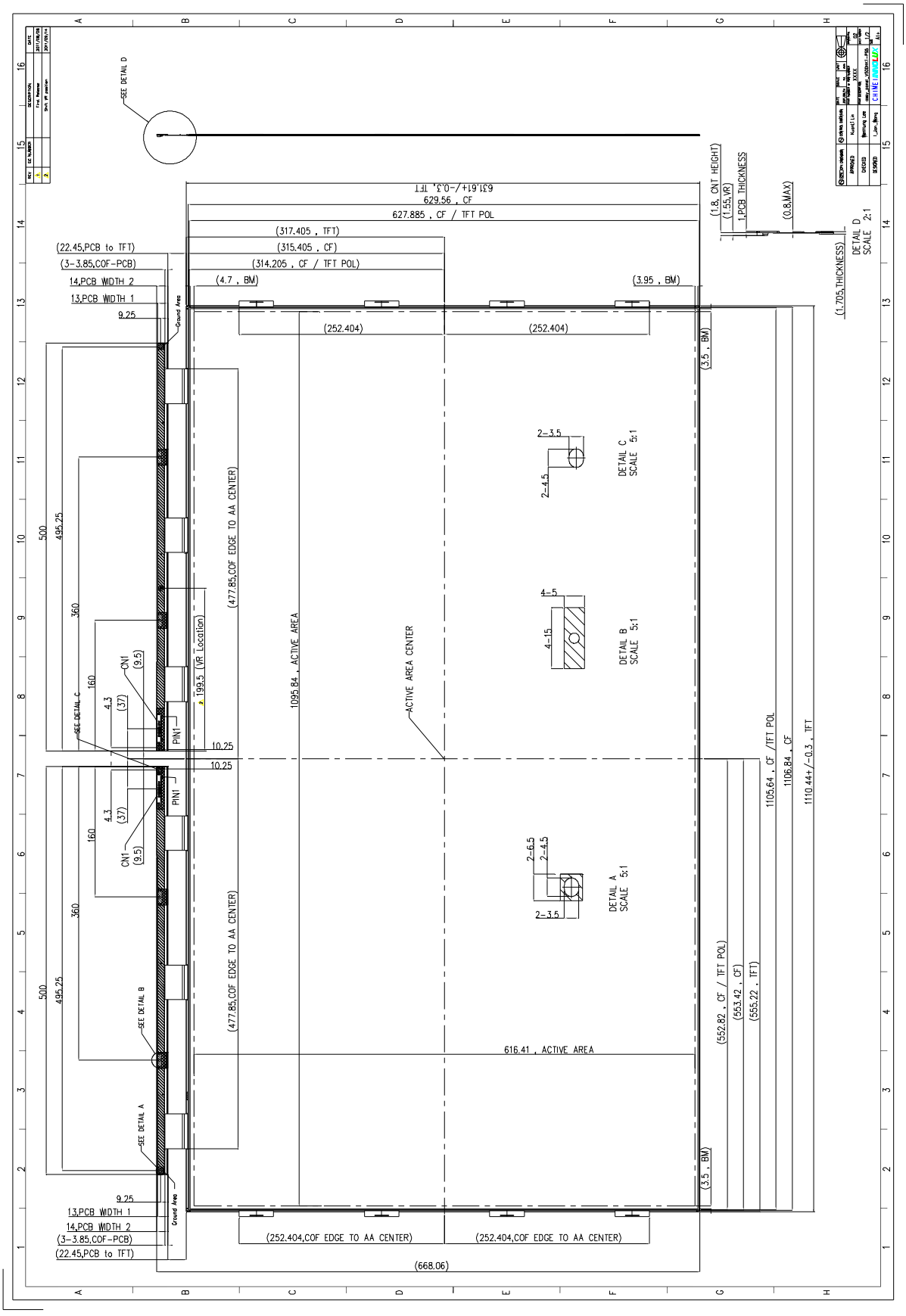
Air Transportation

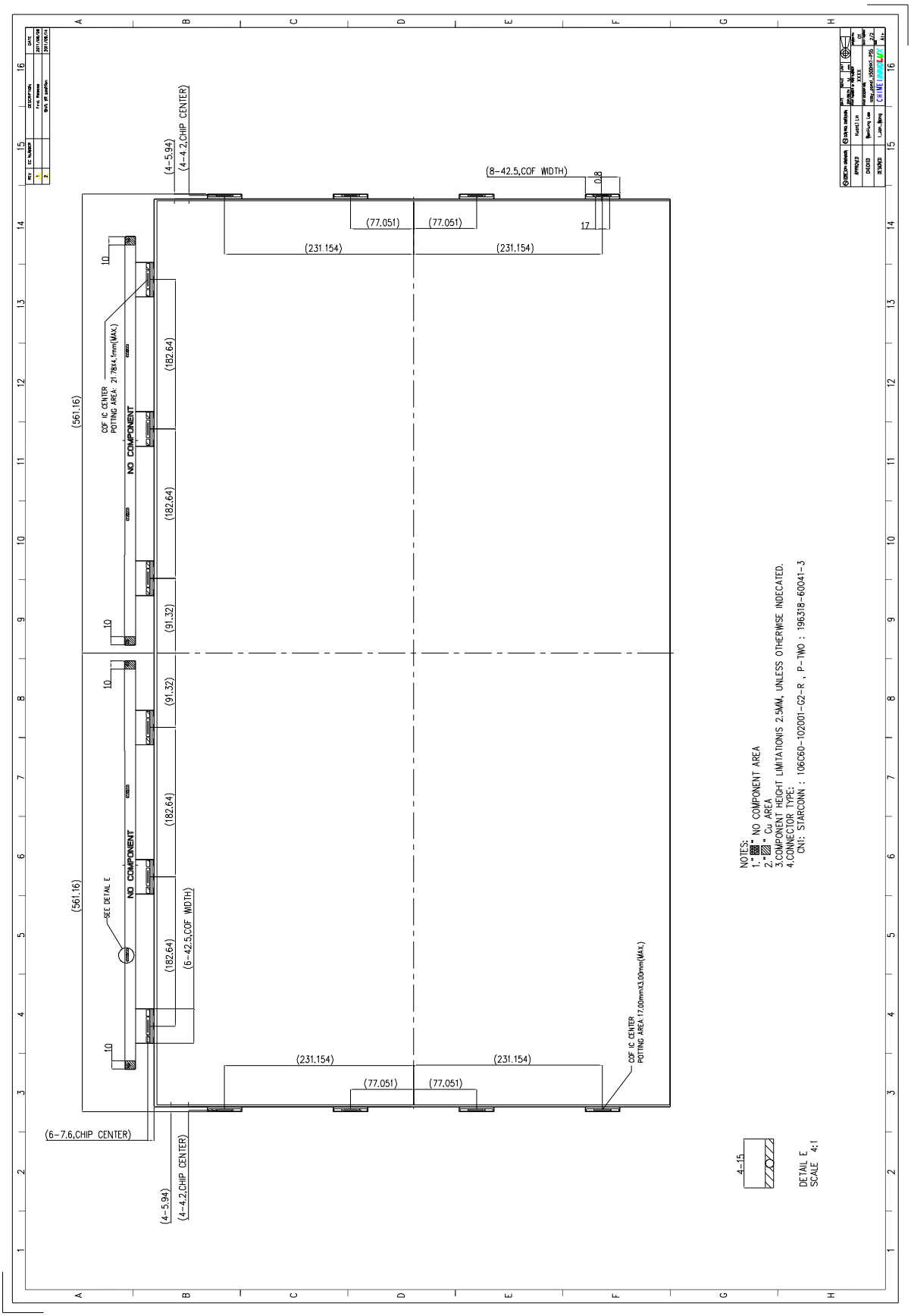


(10+1) Box/pallet

Figure. 10-2 Packing method

11. MECHANICAL CHARACTERISTIC





Appendix A

Local Dimming demo function

A.1 I2C address and write command

Device address: 0xC2

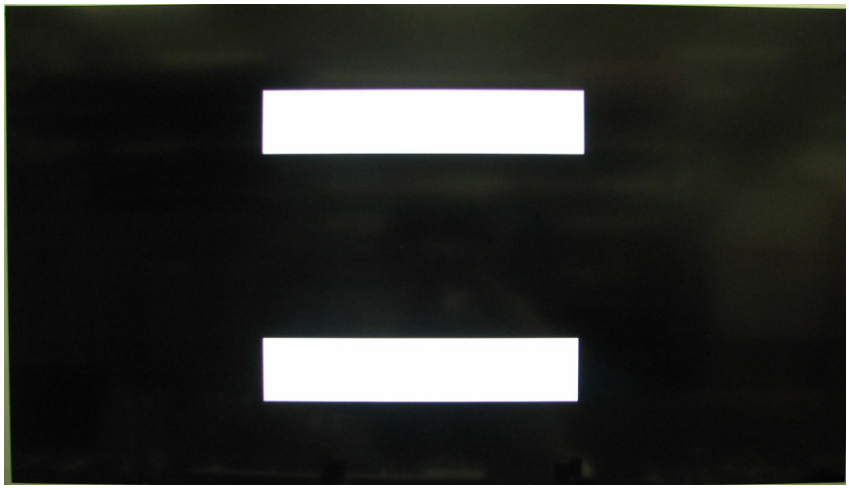
Register address: 0x01

Command data: 0x00: Local Dimming demo mode OFF (Note 1)

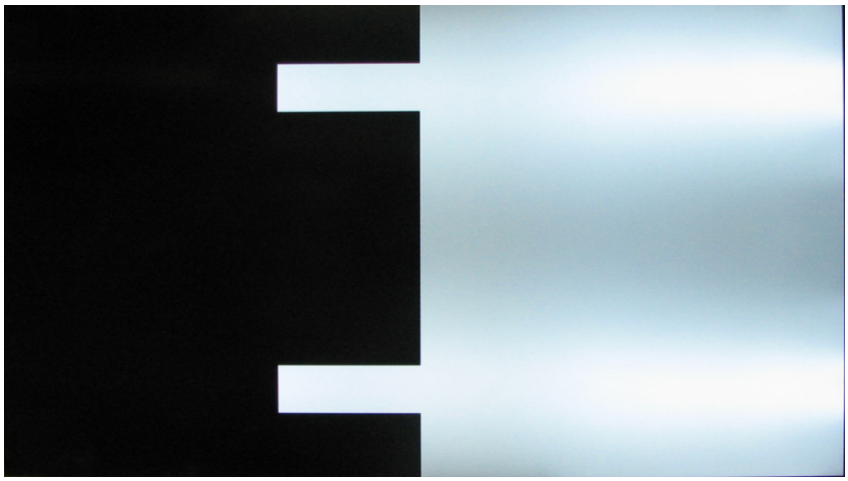
0x01: Local Dimming demo mode ON (Demo in right half screen) (Note 2)

	Device Address		Register Address		Command Data		
START	11000010 (0xC2)	ACK	00000001 (0x01)	ACK	00000001 (0x01)	ACK	STOP

Note 1: Local Dimming demo OFF



Note 2: Local Dimming demo ON



A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns