VITELIC

# V53C404
## HIGH PERFORMANCE, LOW POWER 1M X 4 BIT FAST PAGE MODE CMOS DYNAMIC RAM

PRELIMINARY



| HIGH PERFORMANCE V53C404 | 70/70L | 80/80L | 10/10L |
|---|---|---|---|
| Max. RAS Access Time, ($t_{RAC}$) | 70 ns | 80 ns | 100 ns |
| Max. Column Address Access Time, ($t_{CAA}$) | 35 ns | 40 ns | 50 ns |
| Min. Fast Page Mode Cycle Time, ($t_{PC}$) | 50 ns | 55 ns | 65 ns |
| Min. Read/Write Cycle Time, ($t_{RC}$) | 130 ns | 150 ns | 180 ns |

| LOW POWER V53C404L | 70L | 80L | 10L |
|---|---|---|---|
| Max. CMOS Standby Current, ($I_{DD6}$) | 0.4 mA | 0.4 mA | 0.4 mA |

### Features

- 1M x 4-bit organization
- RAS access time: 70,80,100 ns
- Low power dissipation
  - V53C404-10
    - — Operating Current – 70 mA max.
    - — TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C404 – 1.0 mA max.
  - V53C404L – 0.4 mA max.
- Battery Back-up Mode (V53C404L Only)
- Read-Modify-Write, RAS-Only Refresh, CAS-Before-RAS Refresh capability
- Refresh Interval
  - V53C404 – 1024 cycles/16ms
  - V53C404L – 1024 cycles/64ms
- On-chip substrate bias generator
- Fast Page Mode for a sustained data rate greater than 20 MHz
- Available in 26/20 pin SOJ package (300 mil)

### Description

The Vitelic V53C404 is a high speed 1,048,576x4 bit CMOS dynamic random access memory. Fabricated with Vitelic's VICMOS V technology, the V53C404 offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current and, on request, extended refresh for very low data retention power (V53C404L).

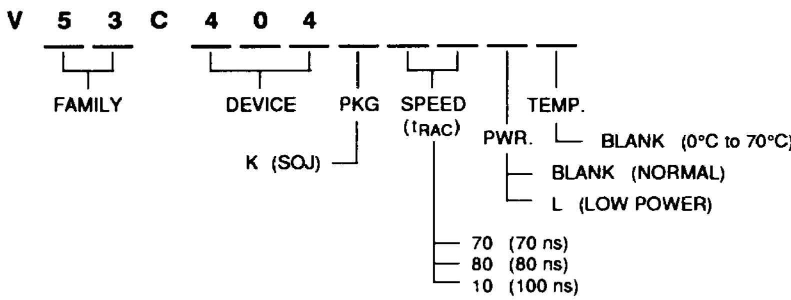
All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 1024 (x4) bits within a row with cycle times as short as 50 ns. Because of static circuitry, the CAS clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C404 ideally suited for graphics, digital signal processing and high performance computing systems.

The V53C404L offers a maximum data retention power of 3.3 mW when operating in CMOS standby mode and performing RAS-only or CAS-before-RAS refresh cycles.

### Device Usage Chart

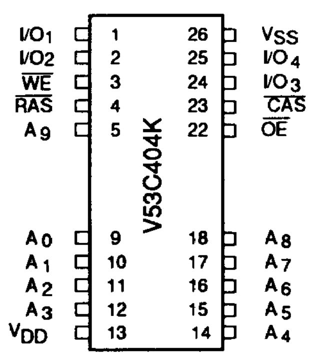
| Operating Temperature Range | Package Outline | Access Time (ns) | | | Power | | Temperature Mark |
|---|---|---|---|---|---|---|---|
| | K | 70 | 80 | 100 | Low | Std. | |
| 0°C to 70 °C | • | • | • | • | • | • | Blank |

V53C404 Rev. 01 September 1991




| *Description* | *Pkg.* | *Pin Count* |
|---|---|---|
| SOJ | K | 26/20 |

## *26/20 Lead SOJ Package PIN CONFIGURATION*
### *Top View*




## *Pin Names*

| | |
|---|---|
| $A_0$–$A_9$ | Address Inputs |
| $\overline{RAS}$ | Row Address Strobe |
| $\overline{CAS}$ | Column Address Strobe |
| $\overline{WE}$ | Write Enable |
| $\overline{OE}$ | Output Enable |
| $I/O_1$–$I/O_4$ | Data Input, Output |
| $V_{DD}$ | +5V Supply |
| $V_{SS}$ | 0V Supply |
| NC | No Connect |

## *Absolute Maximum Ratings**

Ambient Temperature
Under Bias ............................. −10°C to +80°C
Storage Temperature (plastic) .... −55°C to +125°C
Voltage Relative to $V_{SS}$ ...................... −1.0 V to +7.0 V
Data Output Current .................................. 50 mA
Power Dissipation ........................................ 1.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

## *Capacitance**

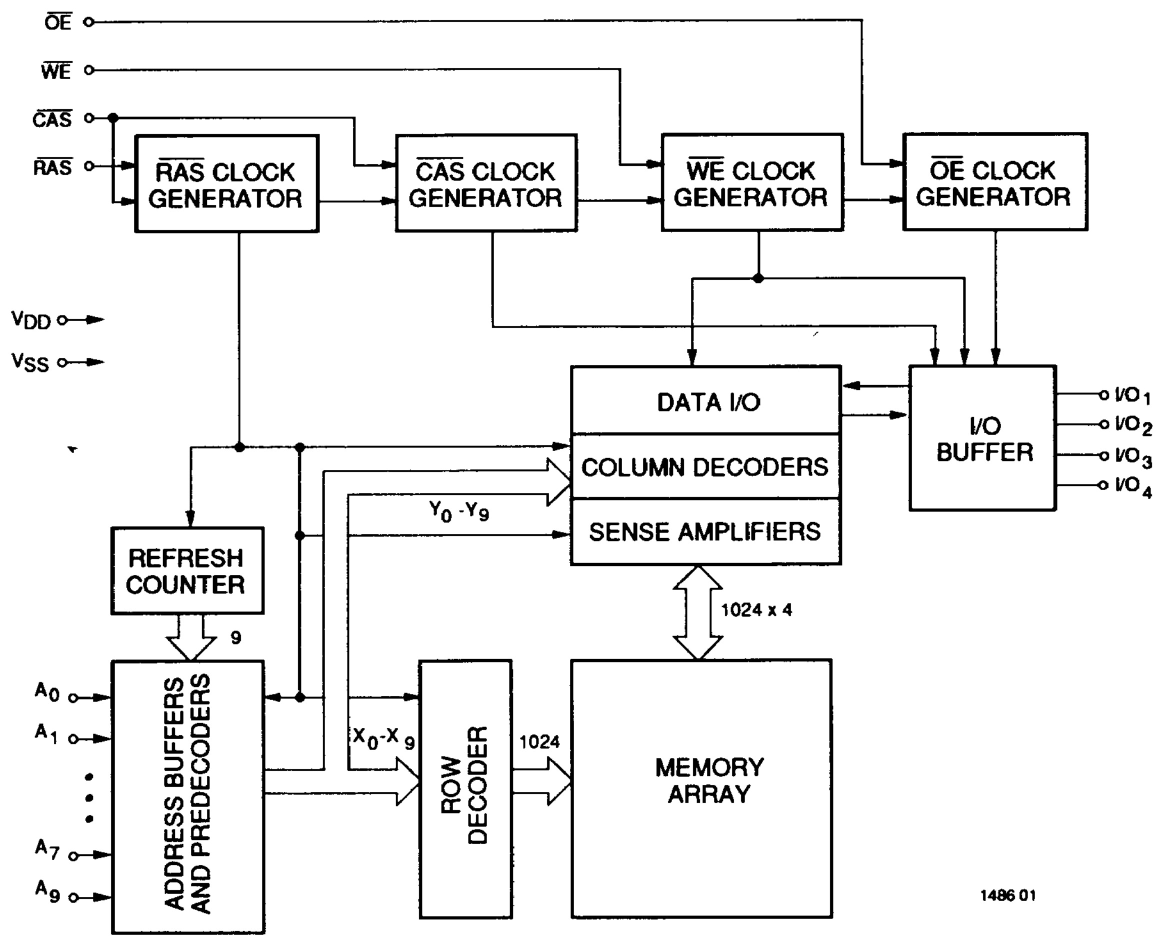
$T_A = 25°C$, $V_{DD} = 5\ V \pm 10\%$, $V_{SS} = 0\ V$

| Symbol | Parameter | Typ. | Max. | Unit |
|---|---|---|---|---|
| $C_{IN1}$ | Address Input | — | 6 | pF |
| $C_{IN2}$ | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$ | — | 7 | pF |
| $C_{OUT}$ | Data Input/Output | — | 7 | pF |

* Note: Capacitance is sampled and not 100% tested

## Block Diagram

**1M x 4**



## *DC and Operating Characteristics* (1-2)

$T_A$ = 0°C to 70°C, $V_{DD}$ = 5 V ± 10%, $V_{SS}$ = 0 V, unless otherwise specified.

| Symbol | Parameter | Access Time | V53C404 Min. | V53C404 Max. | V53C404L Min. | V53C404L Max. | Unit | Test Conditions | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $I_{LI}$ | Input Leakage Current (any input pin) | | −10 | 10 | −10 | 10 | µA | $V_{SS} \le V_{IN} \le V_{DD}$ | |
| $I_{LO}$ | Output Leakage Current (for High-Z State) | | −10 | 10 | −10 | 10 | µA | $V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ | |
| $I_{DD1}$ | $V_{DD}$ Supply Current, Operating | 70 | | 90 | | 90 | mA | $t_{RC} = t_{RC}$ (min.) | 1, 2 |
| | | 80 | | 80 | | 80 | | | |
| | | 100 | | 70 | | 70 | | | |
| $I_{DD2}$ | $V_{DD}$ Supply Current, TTL Standby | | | 2.0 | | 2.0 | mA | $\overline{RAS}$, $\overline{CAS}$ at $V_{IH}$ other inputs ≥ $V_{SS}$ | |
| $I_{DD3}$ | $V_{DD}$ Supply Current, $\overline{RAS}$-Only Refresh | 70 | | 90 | | 90 | mA | $t_{RC} = t_{RC}$ (min.) | 2 |
| | | 80 | | 80 | | 80 | | | |
| | | 100 | | 70 | | 70 | | | |
| $I_{DD4}$ | $V_{DD}$ Supply Current, Fast Page Mode Operation | 70 | | 80 | | 80 | mA | Minimum Cycle | 1, 2 |
| | | 80 | | 70 | | 70 | | | |
| | | 100 | | 60 | | 60 | | | |
| $I_{DD5}$ | $V_{DD}$ Supply Current, Standby, Output Enabled | | | 5 | | 4 | mA | $\overline{RAS}=V_{IH}$, $\overline{CAS}=V_{IL}$ other inputs ≥ $V_{SS}$ | |
| $I_{DD6}$ | $V_{DD}$ Supply Current, CMOS Standby | | | 1 | | 0.4 | mA | $\overline{RAS} \ge V_{DD} - 0.2$ V $\overline{CAS} \ge V_{DD} - 0.2$V other inputs ≥ $V_{SS}$ | |
| $I_{DD7}$ | Battery Back-up Data Retention Current (V53C404L Only) | | | N.A. | | 0.6 | mA | $\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle $t_{RC}$ = 62.5 µs CMOS clock levels | 18 |
| $V_{IL}$ | Input Low Voltage | | −1.0 | 0.8 | −1.0 | 0.8 | V | | 3 |
| $V_{IH}$ | Input High Voltage | | 2.4 | $V_{DD}$+1 | 2.4 | $V_{DD}$+1 | V | | 3 |
| $V_{OL}$ | Output Low Voltage | | | 0.4 | | 0.4 | V | $I_{OL}$ = 4.2 mA | |
| $V_{OH}$ | Output High Voltage | | 2.4 | | 2.4 | | | $I_{OH}$ = −5 mA | |

## AC Characteristics

$T_A$ = 0°C to 70°C, $V_{DD}$ = 5 V ±10%, $V_{SS}$ = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

| # | JEDEC Symbol | Symbol | Parameter | 70/L | | 80/L | | 10/L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 1 | $t_{RL1RH1}$ | $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 70 | 75K | 80 | 75K | 100 | 75K | ns | |
| 2 | $t_{RL2RL2}$ | $t_{RC}$ | Read or Write Cycle Time | 130 | | 150 | | 180 | | ns | |
| 3 | $t_{RH2RL2}$ | $t_{RP}$ | $\overline{RAS}$ Precharge Time | 50 | | 60 | | 70 | | ns | |
| 4 | $t_{RL1CH1}$ | $t_{CSH}$ | $\overline{CAS}$ Hold Time | 70 | | 80 | | 100 | | ns | |
| 5 | $t_{CL1CH1}$ | $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 20 | | 20 | | 25 | | ns | |
| 6 | $t_{RL1CL1}$ | $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay | 20 | 50 | 20 | 60 | 25 | 75 | ns | 4 |
| 7 | $t_{WH2CL2}$ | $t_{RCS}$ | Read Command Setup Time | 0 | | 0 | | 0 | | ns | |
| 8 | $t_{AVRL2}$ | $t_{ASR}$ | Row Address Setup Time | 0 | | 0 | | 0 | | ns | |
| 9 | $t_{RL1AX}$ | $t_{RAH}$ | Row Address Hold Time | 10 | | 10 | | 15 | | ns | |
| 10 | $t_{AVCL2}$ | $t_{ASC}$ | Column Address Setup Time | 0 | | 0 | | 0 | | ns | |
| 11 | $t_{CL1AX}$ | $t_{CAH}$ | Column Address Hold Time | 15 | | 15 | | 20 | | ns | |
| 12 | $t_{CL1RH1(R)}$ | $t_{RSH (R)}$ | $\overline{RAS}$ Hold Time (Read Cycle) | 20 | | 20 | | 25 | | ns | |
| 13 | $t_{CH2RL2}$ | $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | | 5 | | 10 | | ns | |
| 14 | $t_{CH2WX}$ | $t_{RCH}$ | Read Command Hold Time Referenced to $\overline{CAS}$ | 0 | | 0 | | 0 | | ns | 5 |
| 15 | $t_{RH2WX}$ | $t_{RRH}$ | Read Command Hold Time Referenced to $\overline{RAS}$ | 0 | | 0 | | 0 | | ns | 5 |
| 16 | $t_{OEL1RH2}$ | $t_{ROH}$ | $\overline{RAS}$ Hold Time Referenced to $\overline{OE}$ | 20 | | 20 | | 25 | | ns | |
| 17 | $t_{GL1QV}$ | $t_{OAC}$ | Access Time from $\overline{OE}$ | | 20 | | 20 | | 25 | ns | |
| 18 | $t_{CL1QV}$ | $t_{CAC}$ | Access Time from $\overline{CAS}$ | | 20 | | 20 | | 25 | ns | 6,7 |
| 19 | $t_{RL1QV}$ | $t_{RAC}$ | Access Time from $\overline{RAS}$ | | 70 | | 80 | | 100 | ns | 6,8,9 |
| 20 | $t_{AVQV}$ | $t_{CAA}$ | Access Time from Column Address | | 35 | | 40 | | 50 | ns | 6,7, 10 |

## AC Characteristics (Cont'd.)

| # | JEDEC Symbol | Symbol | Parameter | 70/L | | 80/L | | 10/L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 21 | $t_{CL1QX}$ | $t_{LZ}$ | $\overline{OE}$ or $\overline{CAS}$ to Low-Z Output | 0 | | 0 | | 0 | | ns | 16 |
| 22 | $t_{CH2QZ}$ | $t_{HZ}$ | $\overline{OE}$ or $\overline{CAS}$ to High-Z Output | 0 | 20 | 0 | 25 | 0 | 25 | ns | 16 |
| 23 | $t_{RL1AX}$ | $t_{AR}$ | Column Address Hold Time from $\overline{RAS}$ | 55 | | 60 | | 75 | | ns | |
| 24 | $t_{RL1AV}$ | $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 15 | 35 | 15 | 40 | 20 | 50 | ns | 11 |
| 25 | $t_{CL1RH1(W)}$ | $t_{RSH (W)}$ | $\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle | 20 | | 20 | | 25 | | ns | |
| 26 | $t_{WL1CH1}$ | $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 20 | | 20 | | 25 | | ns | |
| 27 | $t_{WL1CL2}$ | $t_{WCS}$ | Write Command Setup Time | 0 | | 0 | | 0 | | ns | 12,13 |
| 28 | $t_{CL1WH1}$ | $t_{WCH}$ | Write Command Hold Time | 10 | | 15 | | 20 | | ns | |
| 29 | $t_{WL1WH1}$ | $t_{WP}$ | Write Pulse Width | 10 | | 15 | | 20 | | ns | |
| 30 | $t_{RL1WH1}$ | $t_{WCR}$ | Write Command Hold Time from $\overline{RAS}$ | 55 | | 60 | | 75 | | ns | |
| 31 | $t_{WL1RH1}$ | $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 20 | | 20 | | 25 | | ns | |
| 32 | $t_{DVWL2}$ | $t_{DS}$ | Data in Setup Time | 0 | | 0 | | 0 | | ns | 14 |
| 33 | $t_{WL1DX}$ | $t_{DH}$ | Data in Hold Time | 15 | | 15 | | 20 | | ns | 14 |
| 34 | $t_{WL1GL2}$ | $t_{WOH}$ | Write to $\overline{OE}$ Hold Time | 20 | | 20 | | 25 | | ns | 14 |
| 35 | $t_{GH2DX}$ | $t_{OED}$ | $\overline{OE}$ to Data Delay Time | 20 | | 20 | | 25 | | ns | 14 |
| 36 | $t_{RL2RL2}$ (RMW) | $t_{RWC}$ | Read-Modify-Write Cycle Time | 185 | | 205 | | 245 | | ns | |
| 37 | $t_{RL1RH1}$ (RMW) | $t_{RRW}$ | Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width | 125 | | 135 | | 165 | | ns | |
| 38 | $t_{CL1WL2}$ | $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay | 50 | | 50 | | 60 | | ns | 12 |
| 39 | $t_{RL1WL2}$ | $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle | 100 | | 110 | | 135 | | ns | 12 |
| 40 | $t_{CL1CH1}$ | $t_{CRW}$ | $\overline{CAS}$ Pulse Width (RMW) | 75 | | 75 | | 90 | | ns | |

## AC Characteristics (Cont'd.)

| # | JEDEC Symbol | Symbol | Parameter | 70/L | | 80/L | | 10/L | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| 41 | $t_{AVWL2}$ | $t_{AWD}$ | Col. Address to $\overline{WE}$ Delay | 65 | | 70 | | 80 | | ns | 12 |
| 42 | $t_{CL2CL2}$ | $t_{PC}$ | Fast Page Mode Read or Write Cycle Time | 50 | | 55 | | 65 | | ns | |
| 43 | $t_{CH2CL2}$ | $t_{CP}$ | $\overline{CAS}$ Precharge Time | 10 | | 10 | | 10 | | ns | |
| 44 | $t_{AVRH1}$ | $t_{CAR}$ | Column Address to $\overline{RAS}$ Setup Time | 35 | | 40 | | 50 | | ns | |
| 45 | $t_{CH2QV}$ | $t_{CAP}$ | Access Time from Column Precharge | | 40 | | 45 | | 55 | ns | 7 |
| 46 | $t_{RL1DX}$ | $t_{DHR}$ | Data in Hold Time Referenced to $\overline{RAS}$ | 55 | | 60 | | 75 | | ns | |
| 47 | $t_{CL1RL2}$ | $t_{CSR}$ | $\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh | 5 | | 5 | | 5 | | ns | |
| 48 | $t_{RH2CL2}$ | $t_{RPC}$ | $\overline{RAS}$ to $\overline{CAS}$ Precharge Time | 5 | | 5 | | 5 | | ns | |
| 49 | $t_{RL1CH1}$ | $t_{CHR}$ | $\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh | 15 | | 15 | | 15 | | ns | |
| 50 | $t_{CL2CL2}$ (RMW) | $t_{PCM}$ | Fast Page Mode Read-Modify-Write Cycle Time | 105 | | 110 | | 130 | | ns | |
| 51 | $t_{WH2RL2}$ | $t_{WRP}$ | $\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh cycle) | 10 | | 10 | | 10 | | ns | |
| 52 | $t_{RL1WL2}$ | $t_{WRH}$ | $\overline{WE}$ Hold Time from $\overline{RAS}$ ($\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle) | 10 | | 10 | | 10 | | ns | |
| 53 | $t_{WL1RL2}$ | $t_{WSR}$ | $\overline{RAS}$ to $\overline{WE}$ set-up Time (Test Mode) | 10 | | 10 | | 10 | | ns | 19 20 |
| 54 | $t_{RL1WH1}$ | $t_{WHR}$ | $\overline{RAS}$ to $\overline{WE}$ hold Time (Test Mode) | 10 | | 10 | | 10 | | ns | |
| 55 | $t_T$ | $t_T$ | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns | 15 |
| 56 | | $t_{REF}$ | Refresh Interval (1024 Refresh Cycles) | | 16 | | 16 | | 16 | ms | 17 |
| 57 | | $t_{REF}$ | Refresh Interval V53C404L Only (1024 Refresh Cycles, $t_{RC}$= 62.5 µs) | | 64 | | 64 | | 64 | ms | 17,18 |

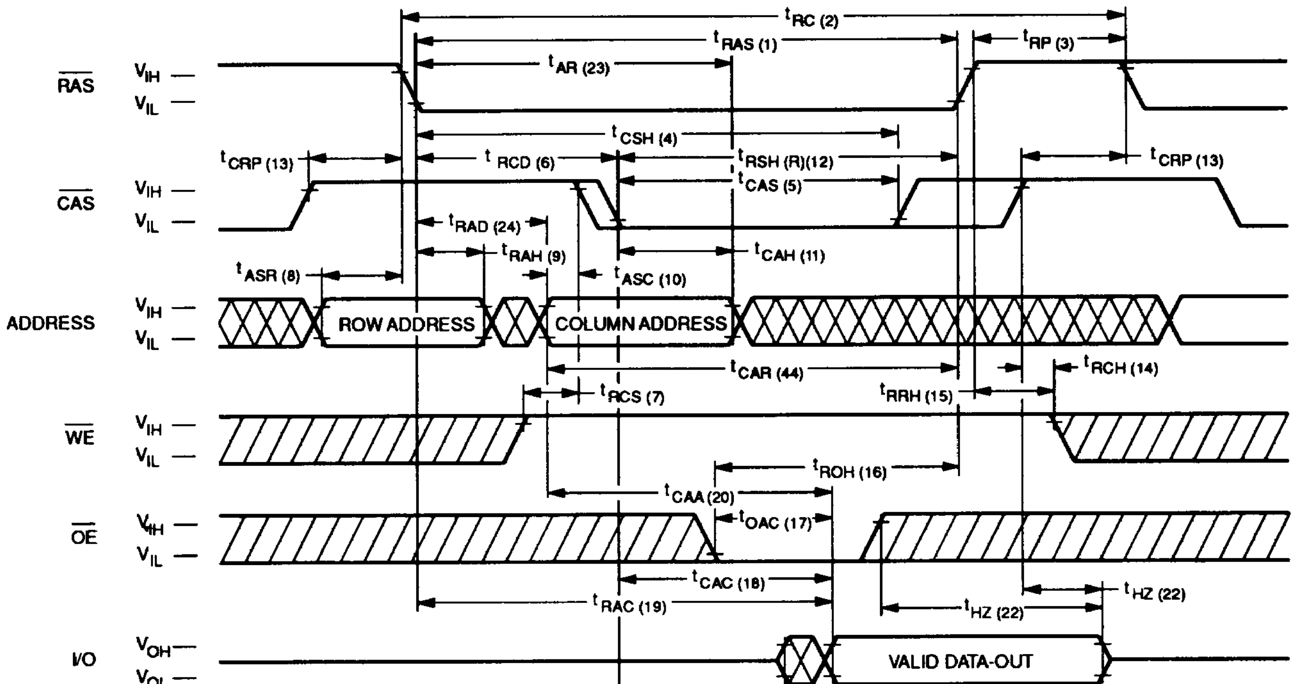
**Notes:**

1. $I_{DD}$ is dependent on output loading when the device output is selected. Specified $I_{DD}$ (max.) is measured with the output open.
2. $I_{DD}$ is dependent upon the number of address transitions. Specified $I_{DD}$ (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified $V_{IL}$ (min.) is steady state operating. During transitions, $V_{IL}$ (min.) may undershoot to −1.0 V for a period not to exceed 20 ns. All AC parameters are measured with $V_{IL}$ (min.) ≥ $V_{SS}$ and $V_{IH}$ (max.) ≤ $V_{DD}$.
4. $t_{RCD}$ (max.) is specified for reference only. Operation within $t_{RCD}$ (max.) limits insures that $t_{RAC}$ (max.) and $t_{CAA}$ (max.) can be met. If $t_{RCD}$ is greater than the specified $t_{RCD}$ (max.), the access time is controlled by $t_{CAA}$ and $t_{CAC}$.
5. Either $t_{RRH}$ or $t_{RCH}$ must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of $t_{CAA}$, $t_{CAC}$ and $t_{CAP}$.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If $t_{RAD}$ is greater than $t_{RAD}$ (max.), $t_{RAC}$ will increase by the amount that $t_{RAD}$ exceeds $t_{RAD}$ (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If $t_{RCD}$ is greater than $t_{RCD}$ (max.), $t_{RAC}$ will increase by the amount that $t_{RCD}$ exceeds $t_{RCD}$ (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the $t_{RAD}$ (max.) limit ensures that $t_{RAC}$ (max.) can be met. $t_{RAD}$ (max.) is specified as a reference point only. If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max.) limit, the access time is controlled by $t_{CAA}$ and $t_{CAC}$.
12. $t_{WCS}$, $t_{RWD}$, $t_{AWD}$ and $t_{CWD}$ are not restrictive operating parameters.
13. $t_{WCS}$ (min.) must be satisfied in an Early Write Cycle.
14. $t_{DS}$ and $t_{DH}$ are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. $t_T$ is measured between $V_{IH}$ (min.) and $V_{IL}$ (max.). AC-measurements assume $t_T$ = 5 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.
18. This is battery backup data retention mode under $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles.
    $t_{RC}$ = 62.5 µs (62.5 µs x 1024 = 64 ms)
    $t_{RAS}$ = $t_{RAS}$ (min) to 1 µs
    Input voltages : $\overline{RAS}$ and $\overline{CAS}$ — $V_{IH} > V_{DD} - 0.2$ V; $V_{IL} < 0.2$ V
    $\overline{WE}$ and $\overline{OE}$ — $V_{IN} > V_{DD} - 0.2$ V
    All other inputs at stable $V_{IH}$ or $V_{IL}$
19. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CAS}$-before-$\overline{RAS}$ cycle. This mode is latched and remains in effect until the exit cycle is generated. The test mode specified in this data sheet is 8-bits parallel testing function.

    CA0 is not used. In the read cycle, if two internal bits on one I/O pin are equal, the I/O pin will indicate a high level. If internal bits on one I/O are not equal, then the I/O pin will indicate a low level.

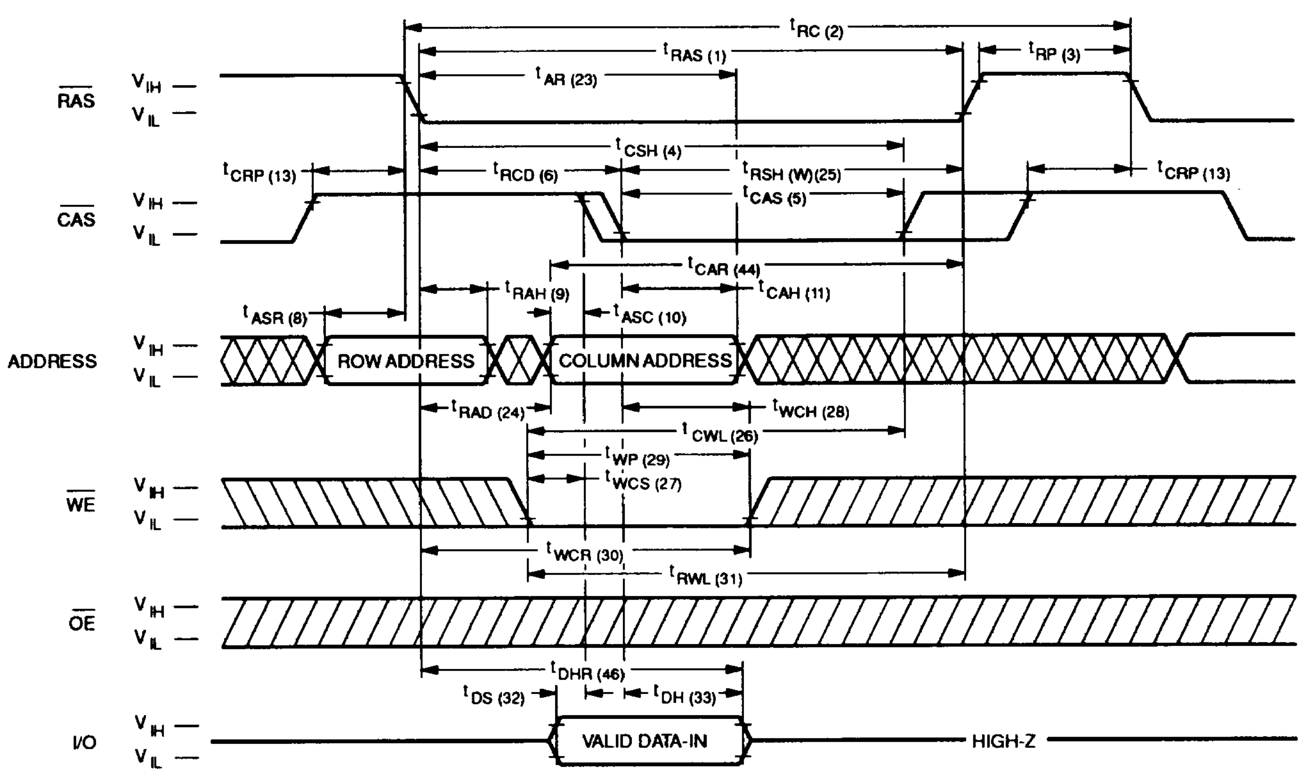
    The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$-only refresh cycle or a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.
20. In a test mode read cycle, the value of access time parameters is delayed by 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value (5 ns) to the specified value in this data sheet.

## Waveforms of Read Cycle



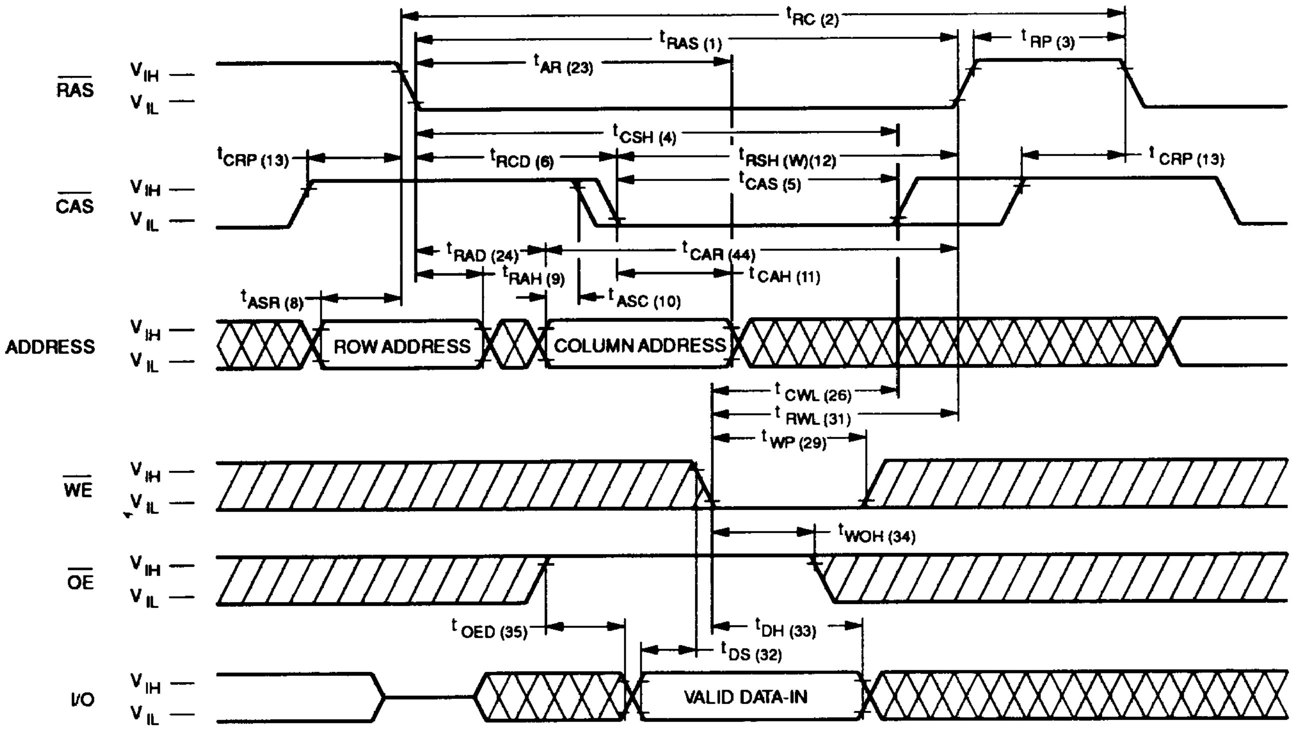
676 01

## Waveforms of Early Write Cycle



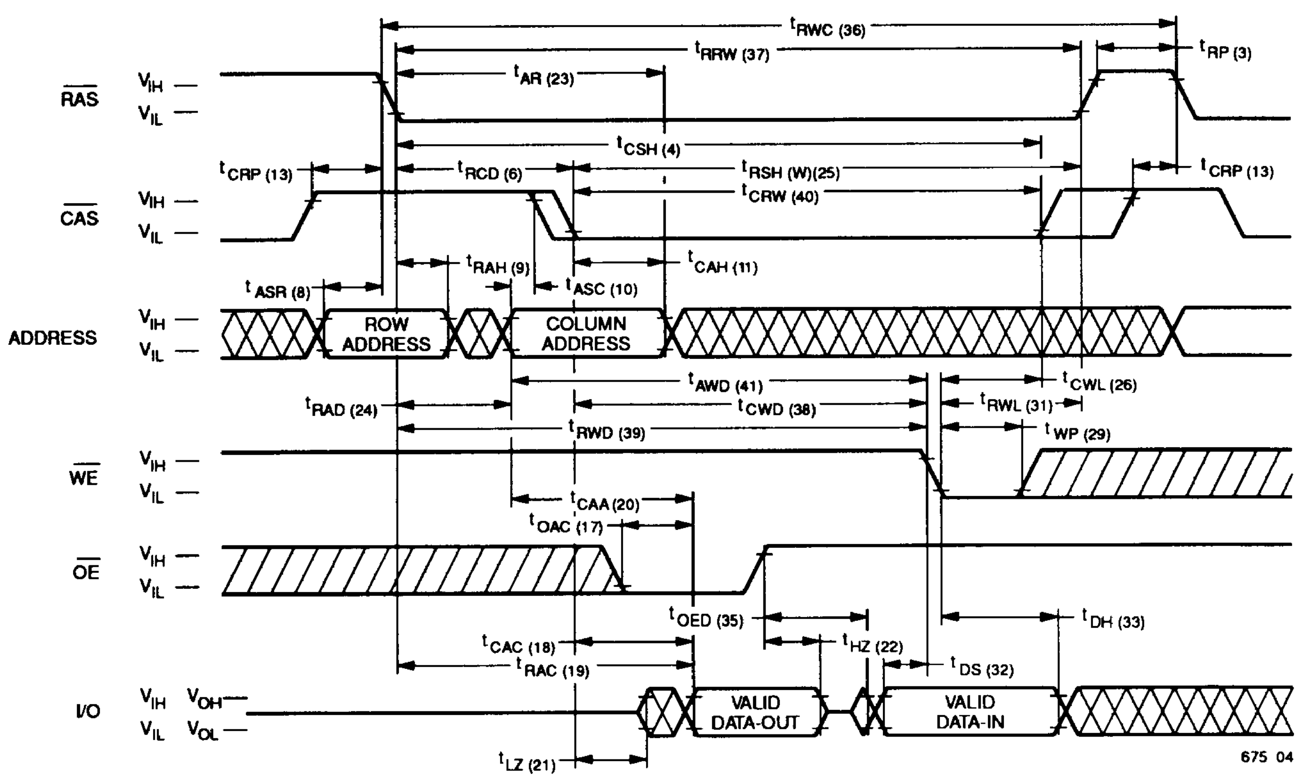
676 02

## Waveforms of $\overline{OE}$-Controlled Write Cycle



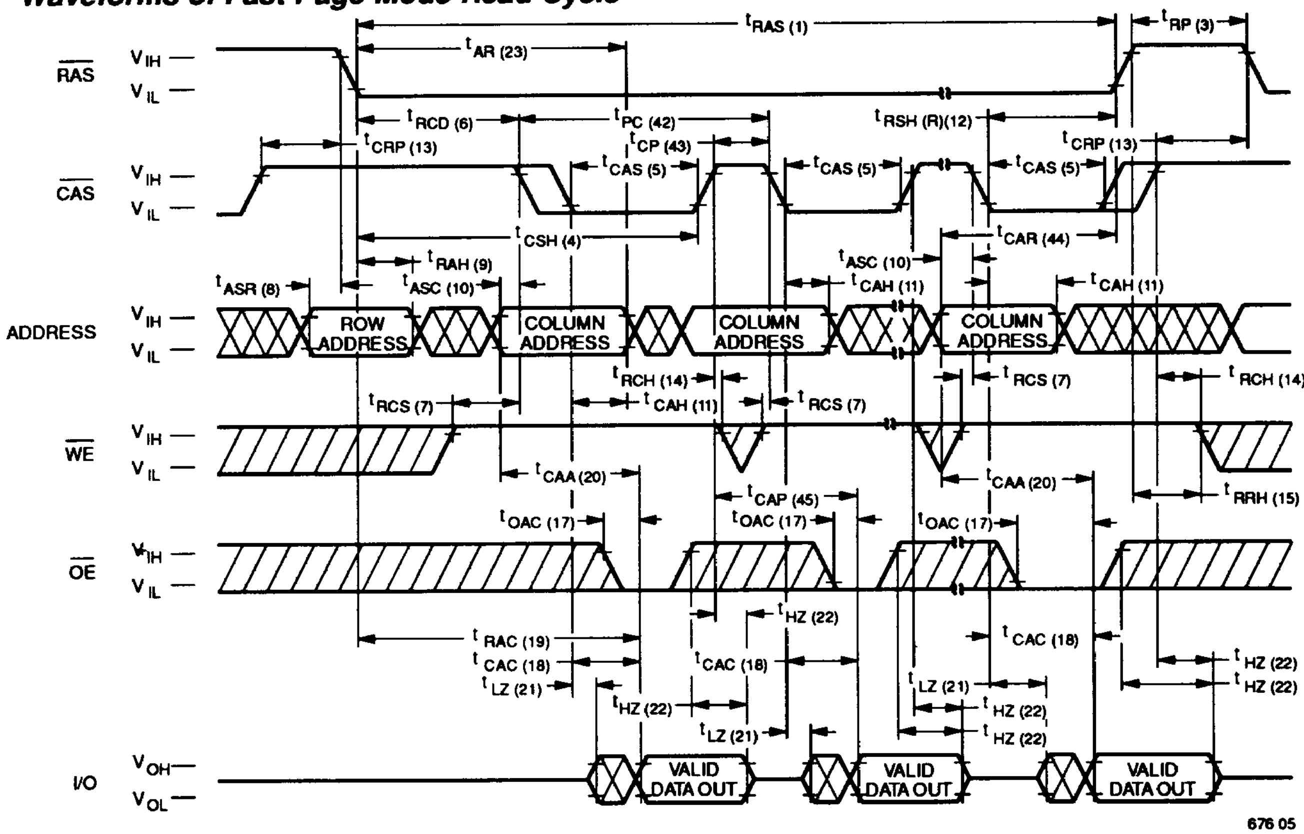

676 03

## Waveforms of Read-Modify-Write Cycle

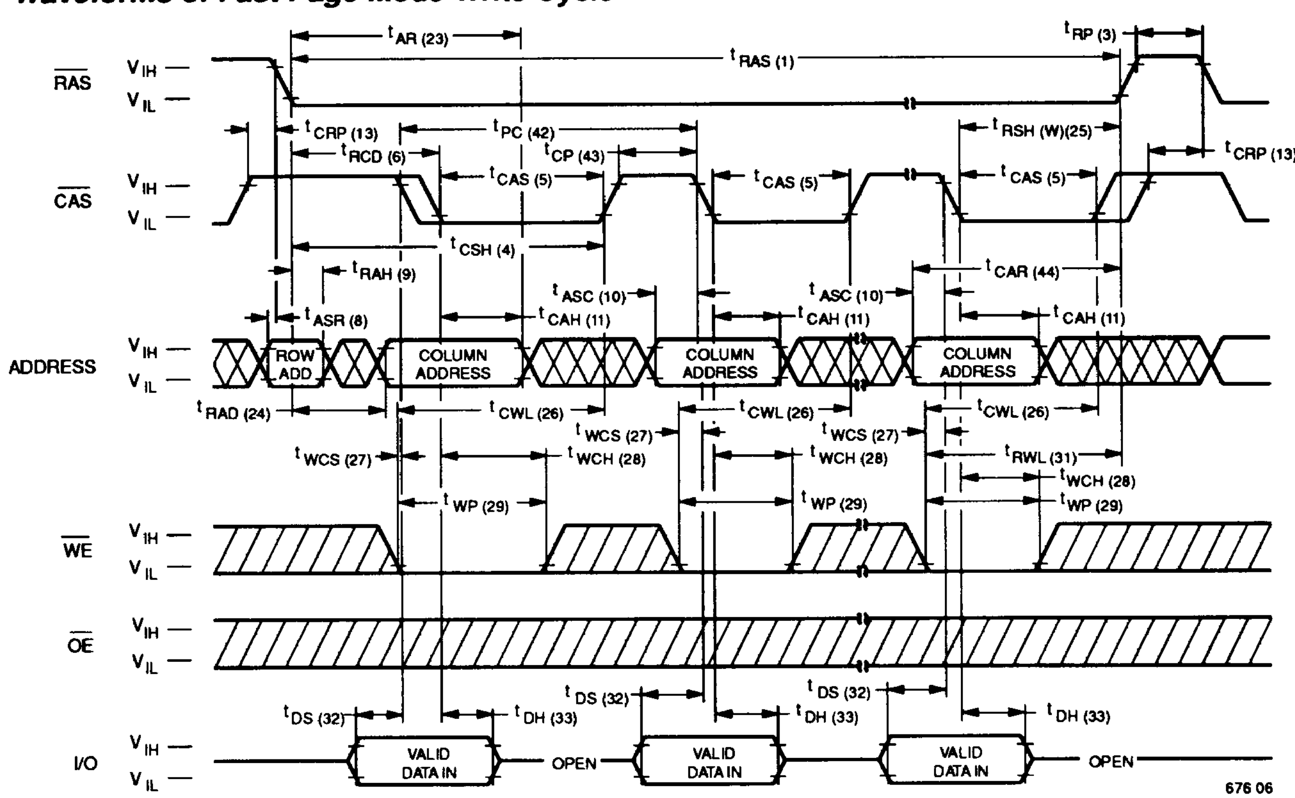



675 04

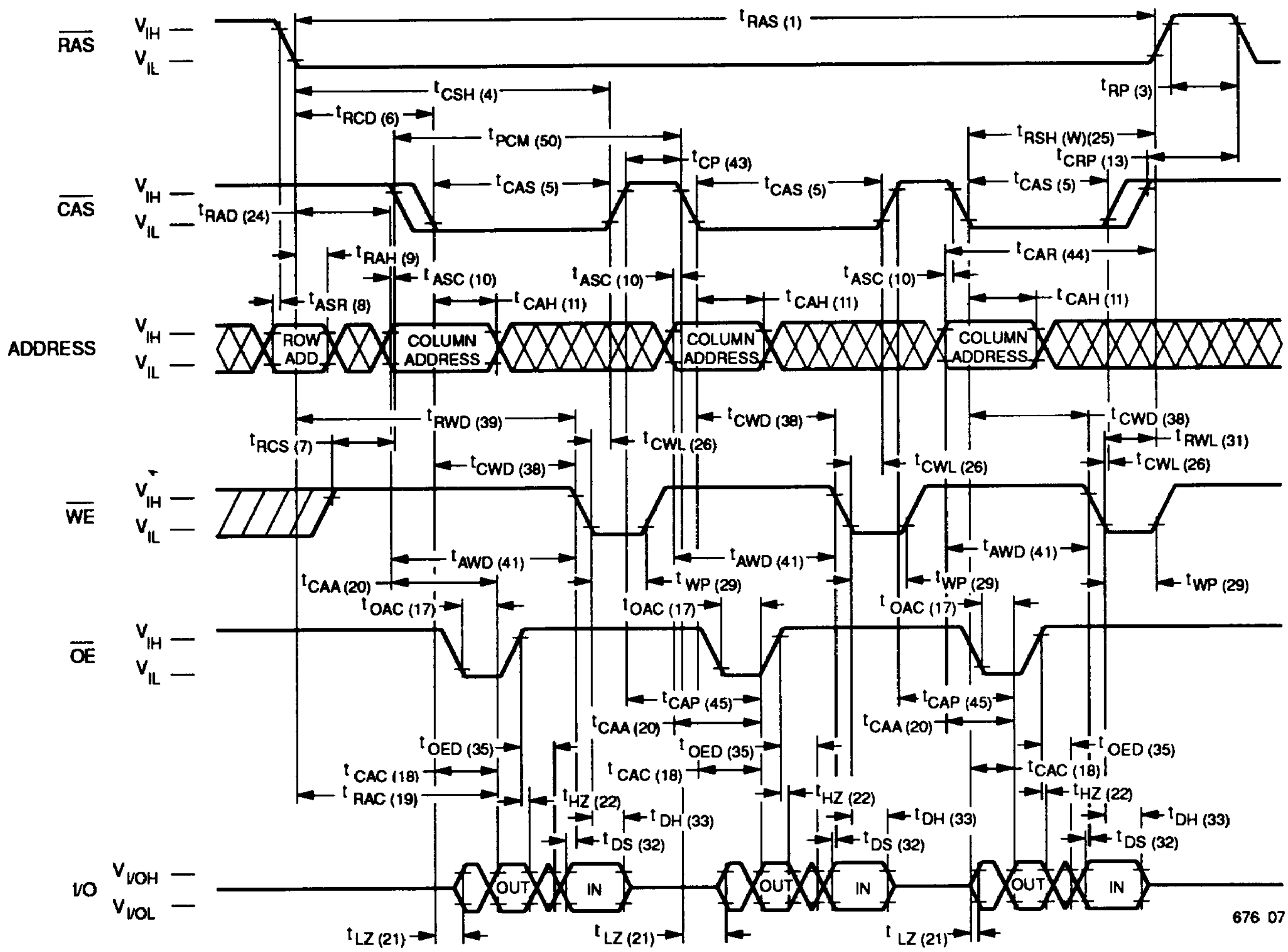
## Waveforms of Fast Page Mode Read Cycle



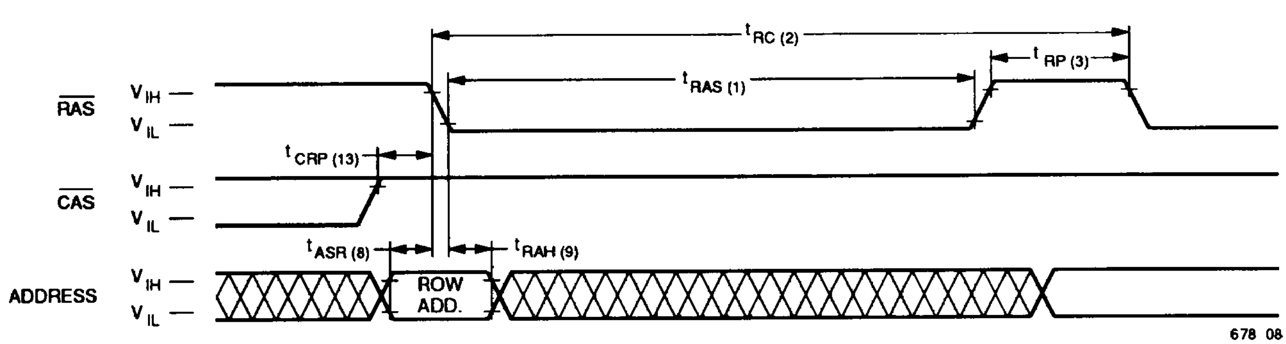

## Waveforms of Fast Page Mode Write Cycle



### Waveforms of Fast Page Mode Read-Write Cycle

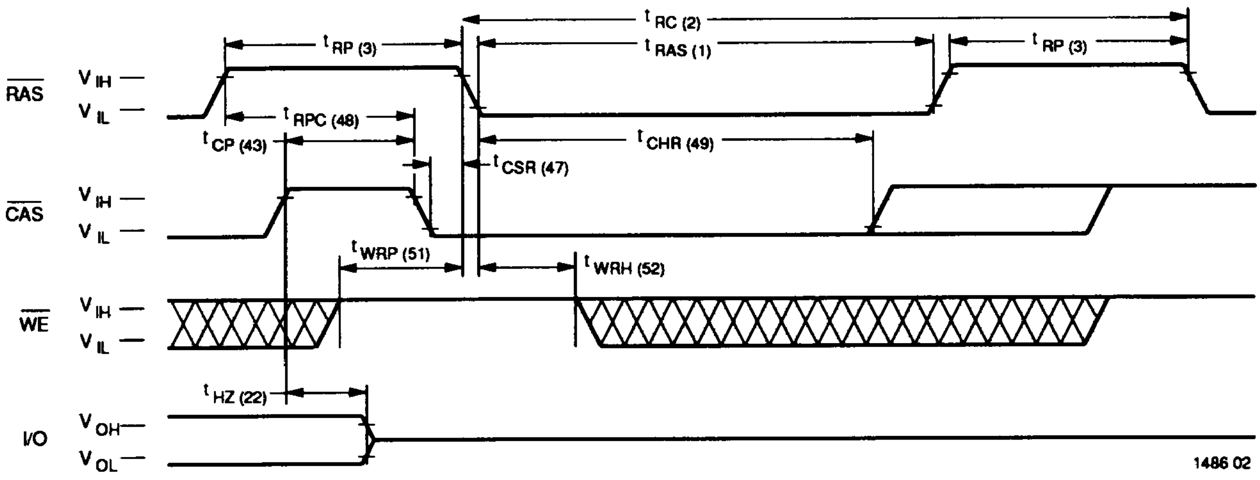



### Waveforms of $\overline{RAS}$-Only Refresh Cycle



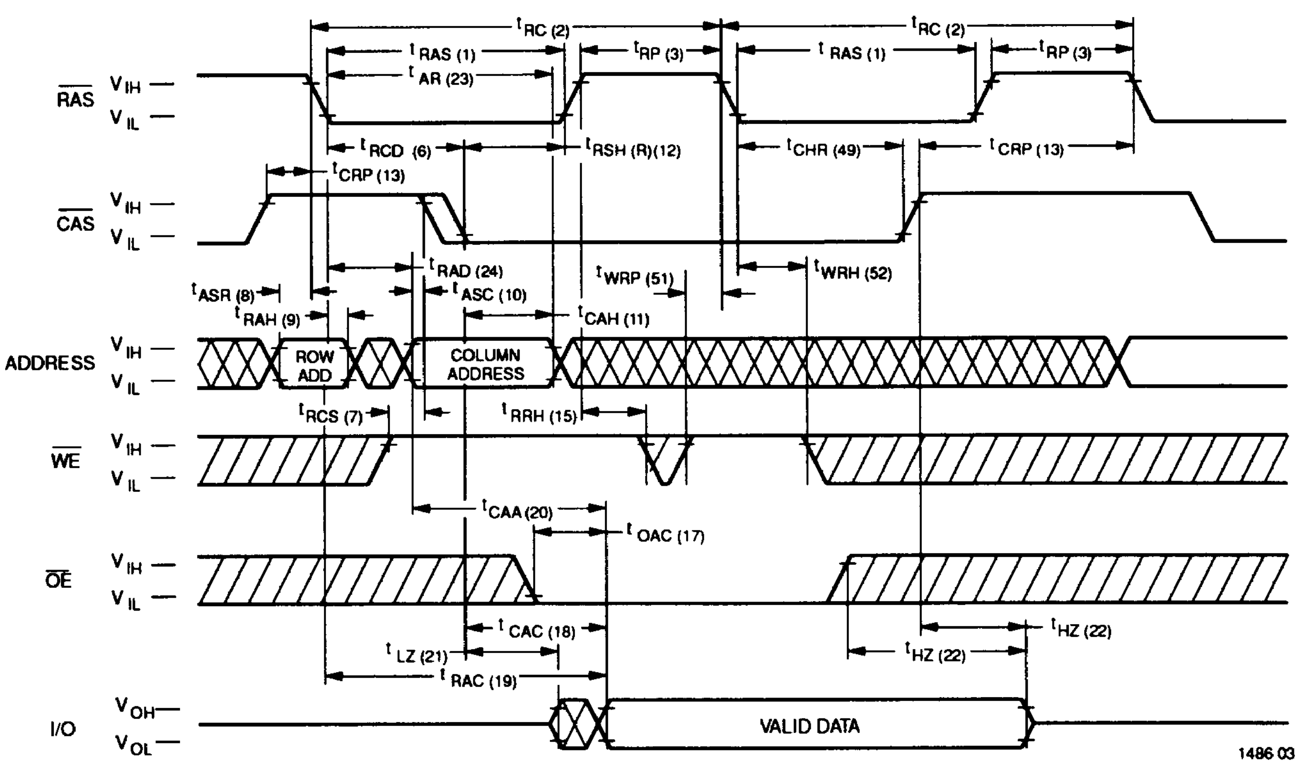

NOTE: $\overline{WE}$, $\overline{OE}$ = Don't care

## Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle

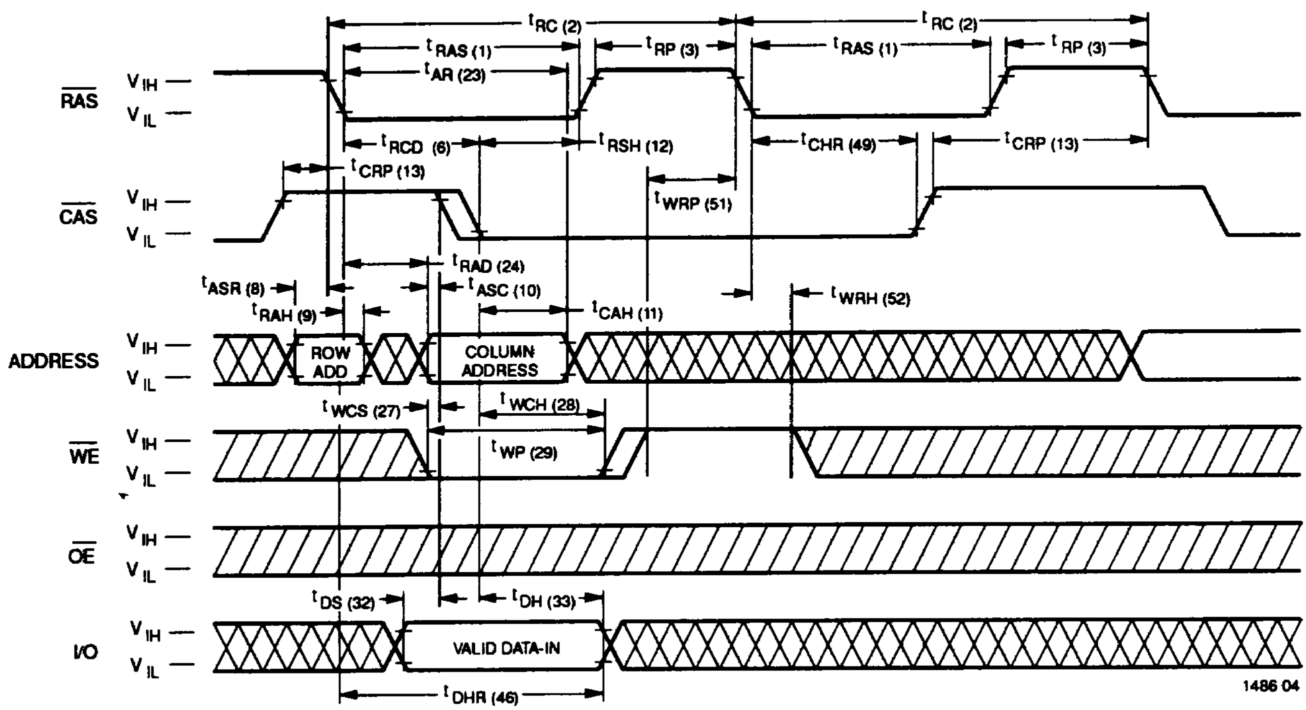



NOTE: $\overline{WE}$, $\overline{OE}$, $A_0$–$A_7$ = Don't care

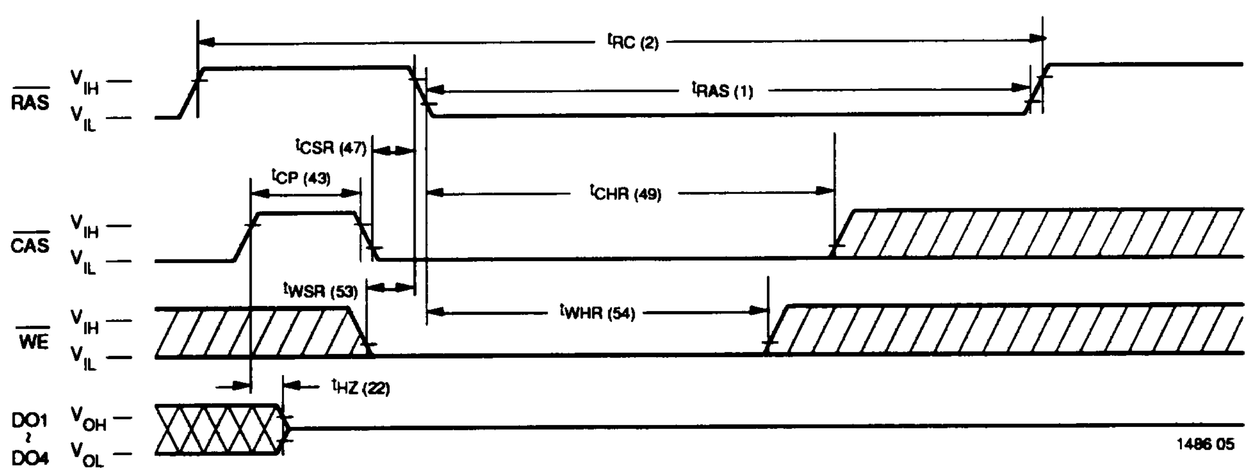
## Waveforms of Hidden Refresh Cycle (Read)



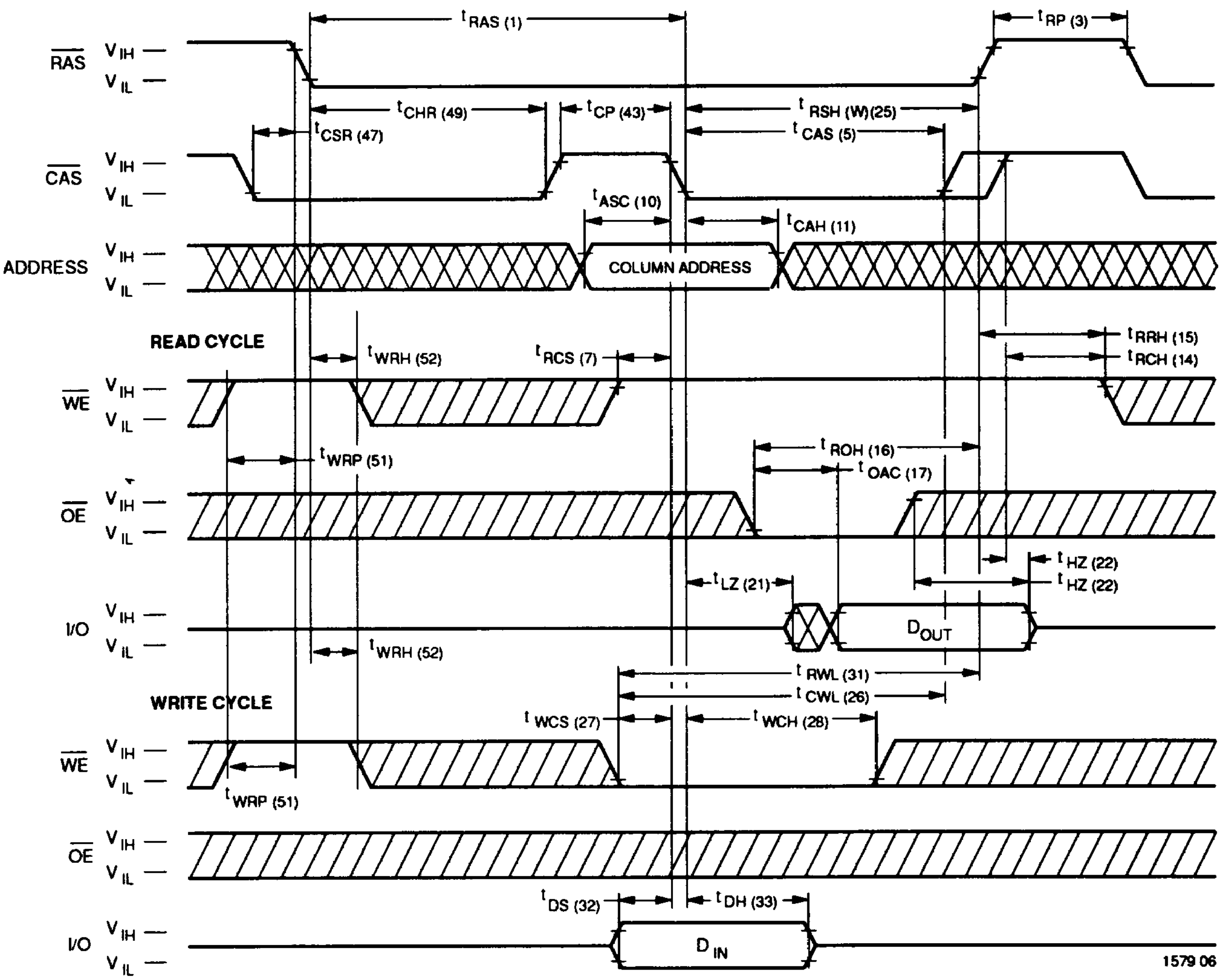
## Waveforms of Hidden Refresh Cycle (Write)




## Test Mode Initiation Cycle



## Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle



## Functional Description

The V53C404 is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C404 reads and writes data by multiplexing an 20-bit address into a 10-bit row and a 10-bit column address. The row address is latched by the Row Address Strobe ($\overline{\text{RAS}}$). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ($\overline{\text{CAS}}$). Because access time is primarily dependent on a valid column address rather than the precise time that the $\overline{\text{CAS}}$ edge occurs, the delay time from $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ has little effect on the access time.

### Memory Cycle

A memory cycle is initiated by bringing $\overline{\text{RAS}}$ low. Any memory cycle, once initiated, must not be ended or aborted before the minimum $t_{RAS}$ time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time $t_{RP}/t_{CP}$ has elapsed.

### Read Cycle

A Read cycle is performed by holding the Write Enable ($\overline{\text{WE}}$) signal High during a $\overline{\text{RAS}}/\overline{\text{CAS}}$ operation. The column address must be held for a minimum specified by $t_{AR}$. Data Out becomes valid only when $t_{OAC}$, $t_{RAC}$, $t_{CAA}$ and $t_{CAC}$ are all satisifed. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by $t_{CAA}$ when $t_{RAC}$, $t_{CAC}$ and $t_{OAC}$ are all satisfied.

### Write Cycle

A Write Cycle is performed by taking $\overline{\text{WE}}$ and $\overline{\text{CAS}}$ low during a $\overline{\text{RAS}}$ operation. The column address is latched by $\overline{\text{CAS}}$. The Write Cycle can be $\overline{\text{WE}}$ controlled or $\overline{\text{CAS}}$ controlled depending on whether $\overline{\text{WE}}$ or $\overline{\text{CAS}}$ falls later. Consequently, the input data must be valid at or before the falling edge of $\overline{\text{WE}}$ or $\overline{\text{CAS}}$, whichever occurs last. In the $\overline{\text{CAS}}$-controlled Write Cycle, when the leading edge of $\overline{\text{WE}}$ occurs prior to the $\overline{\text{CAS}}$ low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function. Ending the Write with $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$ will maintain the output in the High-Z state.

In the $\overline{\text{WE}}$ controlled Write Cycle, $\overline{\text{OE}}$ must be in the high state and $t_{OED}$ must be satisfied.

### Refresh Cycle

To retain data, 1024 Refresh Cycles are required in each 16 ms period. There are two ways to refresh the memory:

1. By clocking each of the 1024 row addresses ($A_0$ through $A_9$) with $\overline{\text{RAS}}$ at least once every 16 ms. Any Read, Write, Read-Modify-Write or $\overline{\text{RAS}}$-only cycle refreshes the addressed row.
2. Using a $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ Refresh Cycle. If $\overline{\text{CAS}}$ makes a transition from low to high to low after the previous cycle and before $\overline{\text{RAS}}$ falls, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh is activated. The V53C404 uses the output of an internal 10-bit counter as the source of row addresses and ignore external address inputs.

$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ counter test mode is provided to ensure reliable operation of the internal refresh counter.

### Data Retention Mode

The V53C404 offers a CMOS standby mode that is entered by causing the $\overline{\text{RAS}}$ clock to swing between a valid $V_{IL}$ and an "extra high" $V_{IH}$ within 0.2 V of $V_{DD}$. While the $\overline{\text{RAS}}$ clock is at the "extra high" level, the V53C404 power consumption is reduced to the low $I_{DD6}$ level. Overall $I_{DD}$ consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where: $t_{RC}$ = Refresh Cycle Time
$t_{RX}$ = Refresh Interval / 1024

### Fast Page Mode Operation

Fast Page Mode operation permits all 1024 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining $\overline{RAS}$ low while performing successive $\overline{CAS}$ cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while $\overline{CAS}$ is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of $\overline{CAS}$, eliminating $t_{ASC}$ and $t_T$ from the critical timing path. $\overline{CAS}$ latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is $t_{CAA}$ or $t_{CAP}$ controlled. If the column address is valid prior to the rising edge of $\overline{CAS}$, the access time is referenced to the $\overline{CAS}$ rising edge and is specified by $t_{CAP}$. If the column address is valid after the rising $\overline{CAS}$ edge, access is timed from the occurrence of a valid address and is specified by $t_{CAA}$. In both cases, the falling edge of $\overline{CAS}$ latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 20 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{1024}{t_{RC} + 1023 \times t_{PC}}$$

### Data Output Operation

The V53C404 Input/Output is controlled by $\overline{OE}$, $\overline{CAS}$, $\overline{WE}$ and $\overline{RAS}$. A $\overline{RAS}$ low transition enables the transfer of data to and from the selected row address in the Memory Array. A $\overline{RAS}$ high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a $\overline{RAS}$ low transition, a $\overline{CAS}$ low transition or $\overline{CAS}$ low level enables the internal I/O path. A $\overline{CAS}$ high transition or a $\overline{CAS}$ high level disables the I/O path and the output driver if it is enabled. A $\overline{CAS}$ low transition while $\overline{RAS}$ is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding $\overline{OE}$ high. The $\overline{OE}$ signal has no effect on any data stored in the output latches. A $\overline{WE}$ low level can also disable the output drivers when $\overline{CAS}$ is low. During a Write cycle, if $\overline{WE}$ goes low at a time in relationship to $\overline{CAS}$ that would normally cause the outputs to be active, it is necessary to use $\overline{OE}$ to disable the output drivers prior to the $\overline{WE}$ low transition to allow Data In Setup Time ($t_{DS}$) to be satisfied.

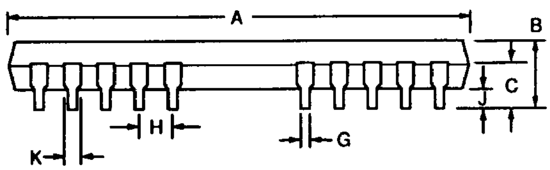
### Power-On

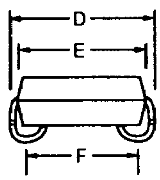
After application of the $V_{DD}$ supply, an initial pause of 200 µs is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the $V_{DD}$ current requirement of the V53C404 is dependent on the input levels of $\overline{RAS}$ and $\overline{CAS}$. If $\overline{RAS}$ is low during Power-On, the device will go into an active cycle and $I_{DD}$ will exhibit current transients. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with $V_{DD}$ or be held at a valid $V_{IH}$ during Power-On to avoid current surges.

**Table 1. Vitelic V53C404 Data Output**
*Operation for Various Cycle Types*

| Cycle Type | I/O State |
|---|---|
| Read Cycles | Data from Addressed Memory Cell |
| $\overline{CAS}$-Controlled Write Cycle (Early Write) | High-Z |
| $\overline{WE}$-Controlled Write Cycle (Late Write) | $\overline{OE}$ Controlled. High $\overline{OE}$ = High-Z I/Os |
| Read-Modify-Write Cycles | Data from Addressed Memory Cell |
| Fast Page Mode Read | Data from Addressed Memory Cell |
| Fast Page Mode Write Cycle (Early Write) | High-Z |
| Fast Page Mode Read-Modify-Write Cycle | Data from Addressed Memory Cell |
| $\overline{RAS}$-only Refresh | High-Z |
| $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle | Data remains as in previous cycle |
| $\overline{CAS}$-only Cycles | High-Z |




## 26/20-pin SOJ

| Dimension | Inches | Millimeters |
|---|---|---|
| A | 0.672/0.684 | 17.069/17.374 |
| B | 0.125/0.135 | 3.175/3.429 |
| C | 0.082/0.093 | 2.083/2.362 |
| D | 0.332/0.342 | 8.433/8.687 |
| E | 0.296/0.304 | 7.518/7.722 |
| F | 0.255/0.275 | 6.477/6.985 |
| G | 0.018 Typ. | 0.457 Typ. |
| H | 0.05 Typ. | 1.270 Typ. |
| J | 0.026 Min. | 0.660 Min. |
| K | 0.028 Typ. | 0.711 Typ. |

## WORLDWIDE VITELIC OFFICES

**U.S.A.**
VITELIC SEMICONDUCTOR
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

**TAIWAN**
VITELIC CORP.
133, MINSHENG E. RD.,
SECTION III, 7B
TAIPEI, TAIWAN, R.O.C.
PHONE: 011-886-2-718-1369
FAX: 011-886-2-718-1362

VITELIC TAIWAN CORP.
1 R&D ROAD I
SCIENCE BASED IND. PARK
HSIN CHU, TAIWAN, R.O.C.
PHONE: 011-886-35-770055
FAX: 011-886-35-776520

**JAPAN**
VITELIC JAPAN CORP.
NIHON SEIMEI KAWASAKI
BLDG., 8TH FL.
1-1 MINAMI-CHO KAWASAKI-KU
KAWASAKI-SHI KANAGAWA 210
JAPAN
PHONE: 011-04-4-246-3021
FAX: 011-04-4-246-3029

**HONG KONG**
VITELIC (HONG KONG) LIMITED
19 DAI FU STREET
TAIPO INDUSTRIAL ESTATE
TAIPO, NT, HONG KONG
PHONE: 011-852-665-4883
FAX: 011-852-664-7535

**KOREA**
VITELIC CORP.
RM. 309, BEUK-EUN BLDG.
1339-1 SEOCHO-DONG,
SEOCHO-KU
SEOUL, KOREA
PHONE: 011-82-2-553-3385
FAX: 011-82-2-553-3675

## VITELIC U.S. SALES OFFICES

**NORTHWESTERN**
VITELIC SEMICONDUCTOR
3910 NORTH FIRST STREET
SAN JOSE, CA 95134
PHONE: 408-433-6000
FAX: 408-433-0185

**SOUTHWESTERN**
VITELIC SEMICONDUCTOR
SUITE 200
5150 E. PACIFIC COAST HWY.
LONG BEACH, CA 90804
PHONE: 213-498-3314
FAX: 213-597-2174

**EASTERN/MIDWESTERN**
VITELIC SEMICONDUCTOR
SUITE 203
619 SEVERN AVENUE
ANNAPOLIS, MD 21403
PHONE: 301-267-9616
FAX: 301-267-7411
or: 301-268-9081



9/91
Printed in U.S.A.



VITELIC subjects its products to normal quality control sampling techniques which are intended to provide an assurance of high quality products suitable for usual commercial applications. VITELIC does not do testing appropriate to provide 100% product quality assurance and does not assume any liability for consequential or incidental arising from any use of its products. If such products are to be used in applications in which personal injury might occur from failure, purchaser must do its own quality assurance testing appropriate to such applications.