

- Tentative Specification
 Preliminary Specification
 Approval Specification

MODEL NO.: V546H1

SUFFIX: LE1

Customer:	
APPROVED BY	SIGNATURE
Name / Title _____	
Note _____	
Please return 1 copy for your confirmation with your signature and comments.	

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Oct. 21, 09'	All	All	Approval Specification Ver 2.0 was first issued.
Ver 2.5	Jan. 14, 10'	8	3.1	Update TFT LCD module Electrical Characteristic
		10	3.2	Update Backlight Unit
		13	4.1	Update TFT LCD module Block Diagram of Interface
		14	5.1	Update TFT LCD module input terminal pin assignment
		18	5.2	Add Backlight pin define
		19	5.4	Update Block Diagram of interface
		23	5.6	Update Color Data Input Assignment
		24	6.1	Update input signal timing Specifications
		28	7.1	Update LED current
		36	10.3	Safety standard update
37	11	Update Mechanical Characteristic		
Ver 2.5	Mar. 08, 10'	28	7.2	Update Optical Specifications
Ver 2.6	Mar. 30, 10'	38	11	Update Mechanical Characteristic
Ver2.7	May. 20, 10'	10	3.2	Update Backlight Unit
		28	7.2	Update Optical Specifications
		38	11	Update Mechanical Characteristic

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V546H1-LE1 is a 54.6" TFT Liquid Crystal Display module with LED Backlight unit and 4ch-LVDS interface.

This module supports 1920 x 1080 HDTV format and can display true 1.073G colors (8-bit + Hi-FRC /color).

The driving board module for backlight is built-in.

1.2 FEATURES

- High brightness 450nits
- High contrast ratio 4000:1
- Fast response time Gray to Gray typical 4.5ms
- High color saturation 76% NTSC
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 120/100 Hz frame rate
- Ultra wide viewing angle: Super MVA technology

1.3 APPLICATION

- Standard Living Room TVs.
- Public Display Application.
- Home Theater Application.
- MFM Application.

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1209.6(H) x 680.4(V) (54.6" diagonal)	mm	(1)
Bezel Opening Area	1217.6 (H) x 688.4 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.21(H) x 0.63(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.073G	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (11% Low Haze) Hardness (3H)	-	(2)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. CMO reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1266.1	1267.6	1269.1	mm	Module Size
	Vertical (V)	737	738.4	739.8	mm	
	Depth (D)	11.3	12.3	13.3	mm	To Rear
		26.0	27.0	28.0	mm	To converter cover
	Weight		15275		G	Weight

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note	
		Min.	Max.			
Storage Temperature	T_{ST}	-20	+60	$^{\circ}\text{C}$	(1)	
Operating Ambient Temperature	T_{OP}	0	50	$^{\circ}\text{C}$	(1), (2)	
Shock (Non-Operating)	S_{NOP}	$\pm X, \pm Y$	-	30	G	(3), (5)
		$\pm Z$	-	30		
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)	

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ($T_a \leq 40^{\circ}\text{C}$).
- (b) Wet-bulb temperature should be 39°C Max. ($T_a > 40^{\circ}\text{C}$).
- (c) No condensation.

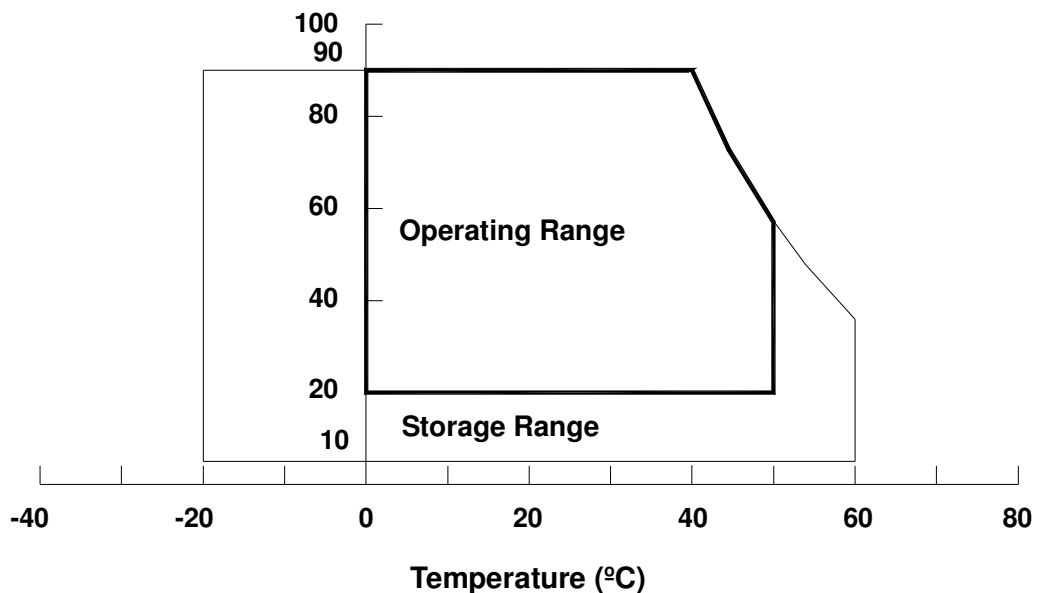
Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65°C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65°C . The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for $\pm X, \pm Y, \pm Z$.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

Relative Humidity (%RH)



2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.2.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	$T_a = 25\text{ }^\circ\text{C}$	-	-	60	V_{RMS}	
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	7	V	

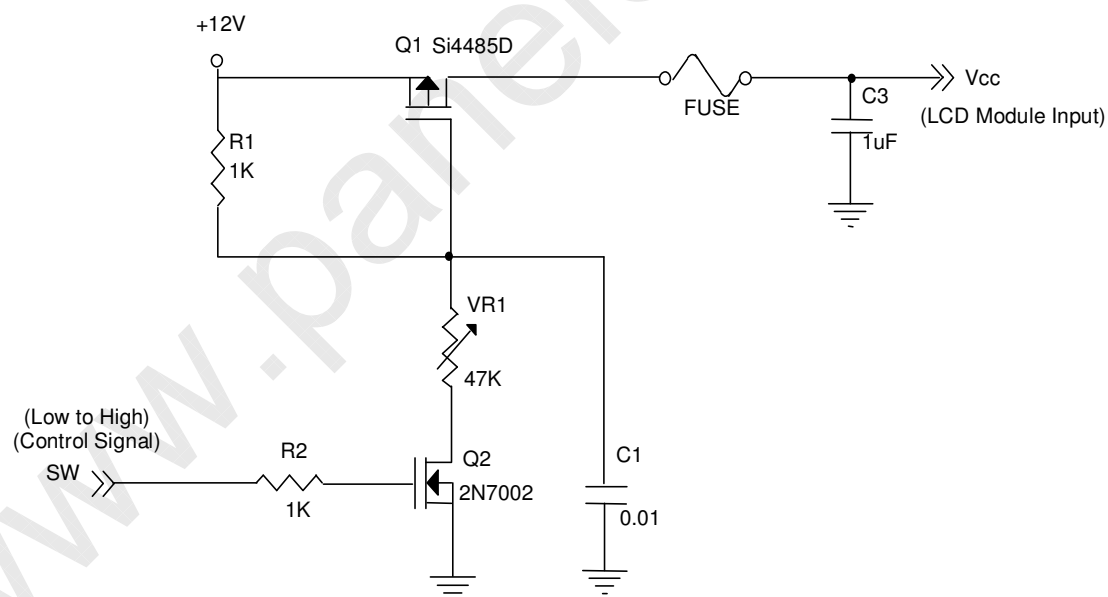
Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS
3.1.1 TFT LCD MODULE (Ta = 25 ± 2 °C)

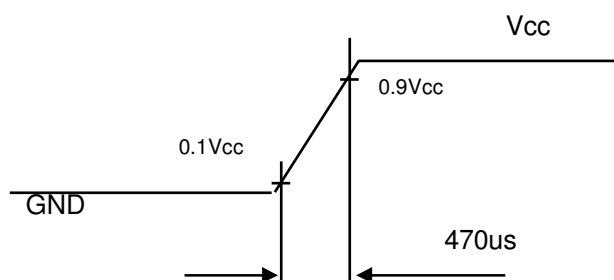
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V _{CC}	10.8	12.0	13.2	V	(1)
Rush Current		I _{RUSH}	-	3.3	5	A	(2)
Power Supply Current	White	I _{CC}	-	0.584	0.8	A	(3)
	Black		-	0.425	0.6	A	
	Horizontal one line stripe		-	1.17	1.55	A	
LVDS Interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V _{LVTL}	-	-	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage (Single-End)	V _{ID}	200	-	600	mV	
	Terminating Resistor	R _T	-	100	-	ohm	
CMOS Interface	Input High Threshold Voltage	V _{IH}	2.7	-	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:



Note (3) The specified power supply current is under the conditions at V_{CC} = 12V, Ta = 25 ± 2 °C, f_v = 120 Hz, whereas a power dissipation check pattern below is displayed.

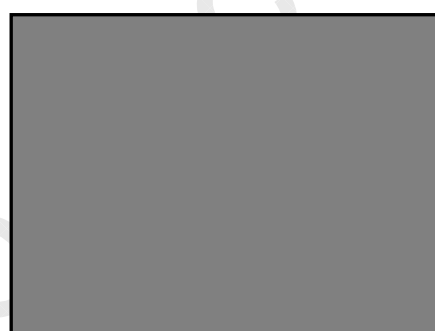
Vcc rising time is 470us

a. White Pattern



Active Area

b. Black Pattern

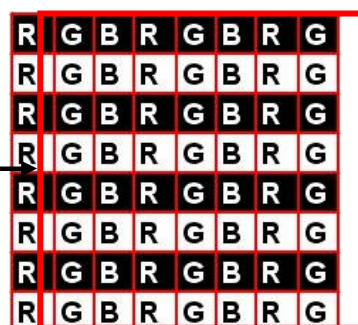


Active Area

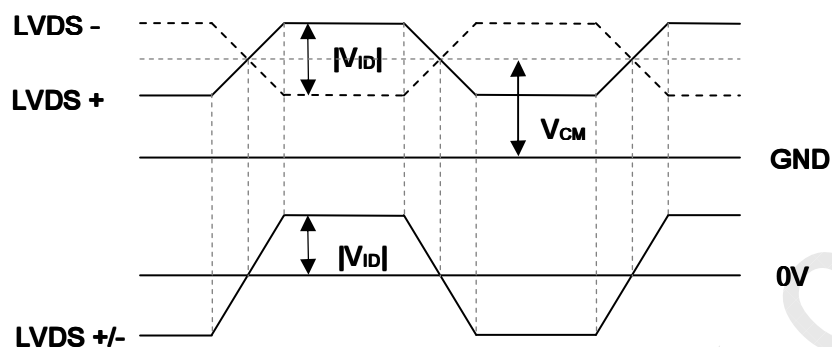
c. Horizontal one line stripe



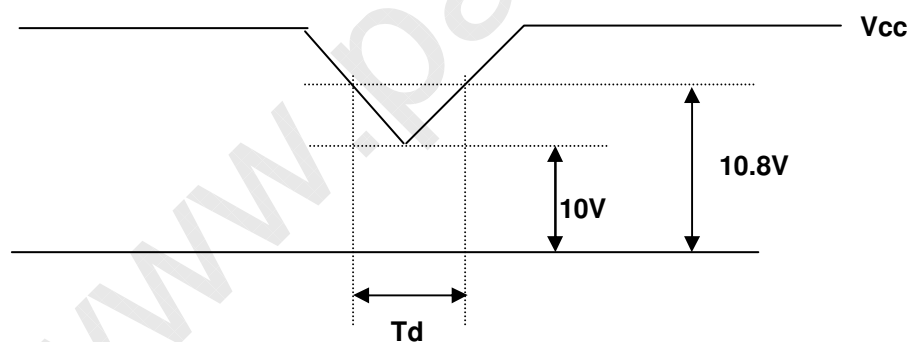
Active Area



Note (4) The LVDS input characteristics are as follows:



3.1.2 Vcc Power Dip Condition:



Dip condition: $10V \leq V_{cc} \leq 10.8V$, $T_d \leq 20ms$

3.2 BACKLIGHT UNIT

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Light Bar Voltage	V _W	-	-	49	V	I _L = 120mA
Forward Voltage	V _f	3.0	-	3.5	V	I _L = 120mA
LED Current	I _L	112.8	120	127.2	mA	

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 °C)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P _{BL}	-	145	160	W	
Converter Input Voltage	V _{BL}	22.8	24	25.2	V _{DC}	
Converter Input Current	I _{BL}	-	6.04	6.67	A	
Dimming Frequency	F _B	150	160	170	Hz	
Minimum Duty Ratio	D _{MIN}	-	5	-	%	

3.2.3 CONVERTER INTERFACE CHARACTERISTICS

External dimming: 150Hz~170Hz, duty ratio: 5%~100%

Parameter		Symbol	Test Condition	Value			Unit	Note
				Min.	Typ.	Max.		
On/Off Control Voltage	ON	VBLON	-	2.0	-	5.0	V	
	OFF		-	0	-	0.8	V	
Internal PWM Control Voltage	MAX	VIPWM	-	3.15	-	3.45	V	maximum duty ratio
	MIN		-	-	0	-	V	minimum duty ratio
External PWM Control Voltage	HI	VEPWM	-	2.0	-	5.0	V	Duty on
	LO		-	0	-	0.8	V	Duty off
Status Signal	HI	Status	-	3.0	3.3	3.6	V	Normal
	LO		-	0	-	0.8	V	Abnormal
VBL Rising Time		Tr1	-	30	-	-	ms	10%-90%V _{BL}
VBL Falling Time		Tf1	-	30	-	-	ms	
Control Signal Rising Time		Tr	-	-	-	100	ms	
Control Signal Falling Time		Tf	-	-	-	100	ms	
PWM Signal Rising Time		TPWMR	-	-	-	50	us	

PWM Signal Falling Time	TPWMF	—	—	—	50	us	
Input Impedance	Rin	—	1	—	—	MΩ	
PWM Delay Time	TPWM	—	100	—	—	ms	
BLON Delay Time	T _{on}	—	300	—	—	ms	
	T _{on1}	—	300	—	—	ms	
BLON Off Time	Toff	—	300	—	—	ms	

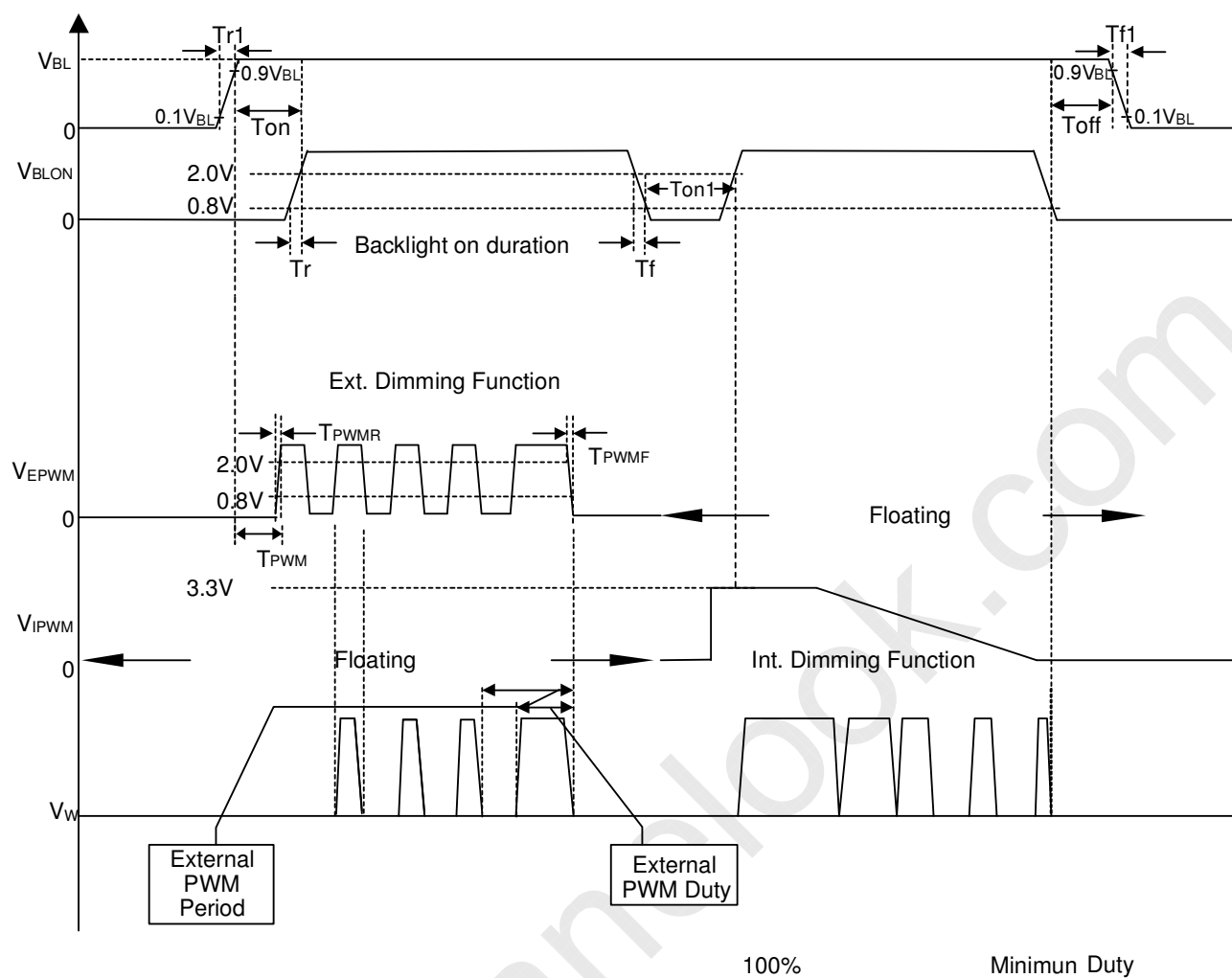
Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

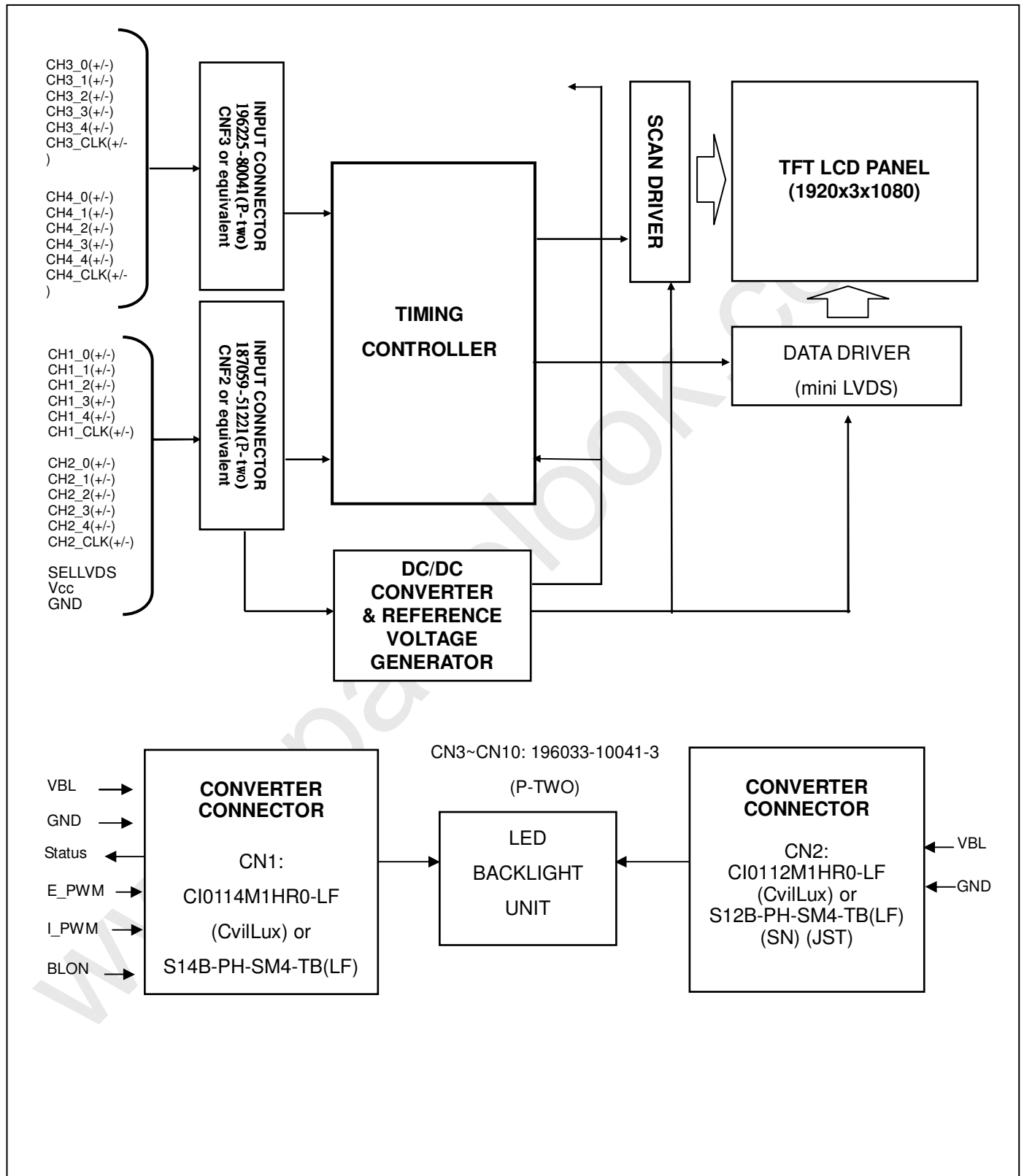
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

CNF2 Connector Pin Assignment (187059-51221(P-two) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	LVDS Data Format Selection	(2)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	(1)
10	N.C.	No Connection	(1)
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 1 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)

28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	
29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	N.C.	No Connection	(1)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF3 Connector Pin Assignment (196225-80041(P-two) or equivalent)

Pin	Name	Description	Note
1	GND	Ground	
2	N.C.	No Connection	(1)
3	N.C.	No Connection	(1)
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)

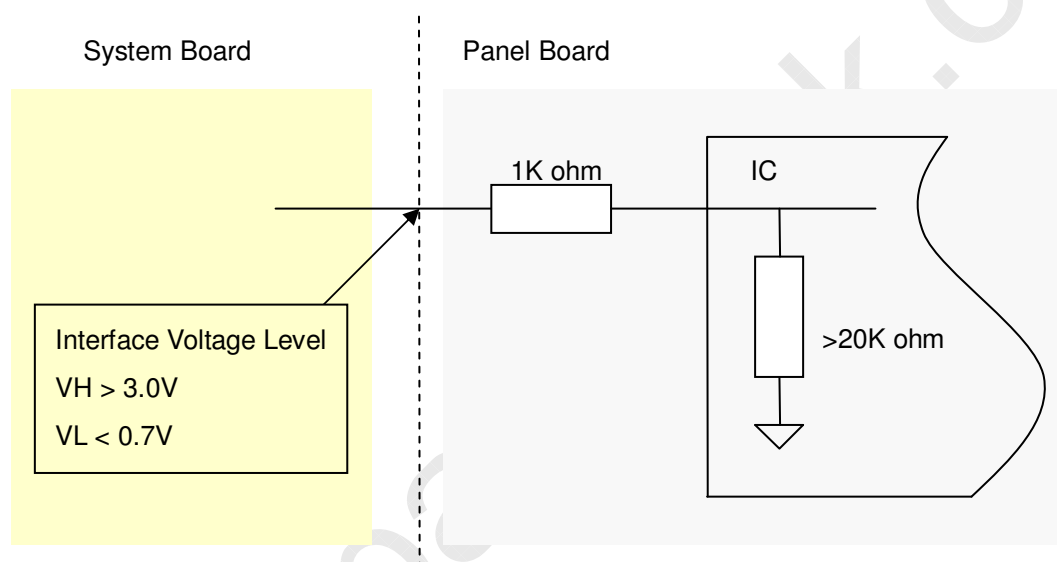
6	N.C.	No Connection	(1)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	(1)
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	N.C.	No Connection	(1)
25	N.C.	No Connection	(1)
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	

37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	N.C.	No Connection	(1)
41	N.C.	No Connection	(1)

Note (1) Reserved for internal use. Please leave it open.

Note (2) High=connect to +3.3V : JEIDA Format ; Low= connect to GND or Open : VESA Format.

Note (3) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement as below.



Note (4) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9,1913, 1917
2nd Port	Second Pixel	2, 6, 10,1914, 1918
3rd Port	Third Pixel	3, 7, 11,1915, 1919
4th Port	Fourth Pixel	4, 8, 12,1916, 1920

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3-CN10 (Housing): 51281-1094 (Molex)

Pin No.	Symbol	Description
1	VLED-	Negative of LED String
2	VLED-	
3	VLED-	
4	NC	No Connection
5	NC	
6	NC	
7	NC	
8	NC	
9	VLED+	Positive of LED String
10	VLED+	

Note (1) The backlight interface housing for high voltage side is a model 51281-1094, manufactured by Molex or equivalent. The mating header on converter part number is 51281-1094

5.3 DRIVING BOARD UNIT

CN1(Header): CI0114M1HR0-LF (CvilLux) or S14B-PH-SM4-TB(LF)(SN) (JST)

Pin No	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	Status	Normal (3.3V) Abnormal (0V)
12	E_PWM	External PWM Control
13	I_PWM	Internal PWM Control
14	BLON	BL ON/OFF

Note (1) Pin 12: External PWM control (use pin 12): Pin 13 must open.

Note (2) Pin 13: Internal PWM control (use pin 13): Pin 12 must open.

Note (3) Pin 12 and Pin 13 can't open in the same period.

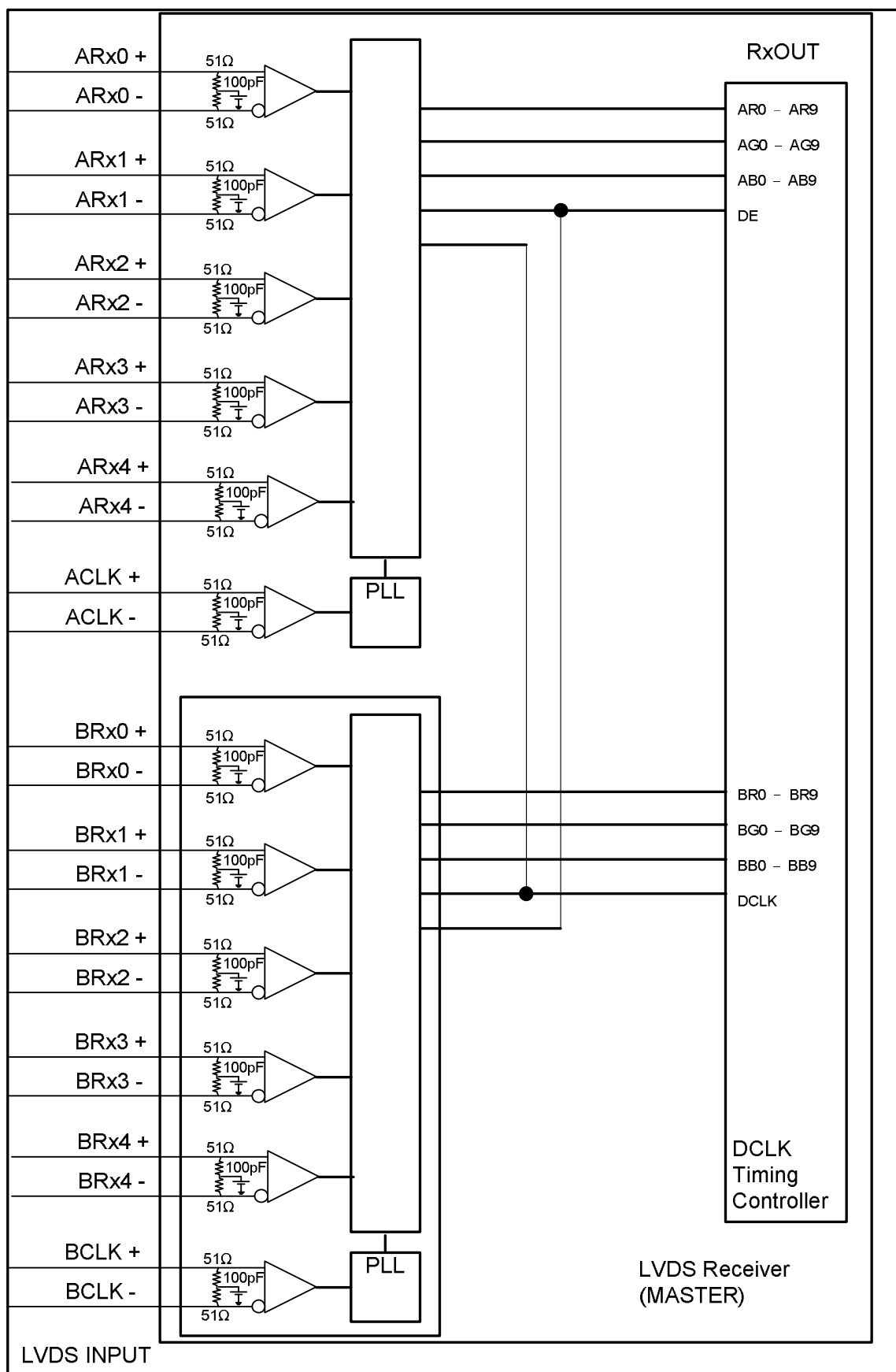
CN2(Header): CI0112M1HR0-LF (Cvillux) or S12B-PH-SM4-TB(LF)(SN) (JST)

Pin №	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

CN3-CN10 (Housing): 196033-10041-3 (P-TWO)

Pin No.	Symbol	Description
1	VLED+	Positive of LED String
2	VLED+	
3	NC	No Connection
4	NC	
5	NC	
6	NC	
7	NC	
8	VLED-	Negative of LED String
9	VLED-	
10	VLED-	

5.4 BLOCK DIAGRAM OF INTERFACE



AR0~AR9: First pixel R data

AG0~AG9: First pixel G data

AB0~AB9: First pixel B data

BR0~BR9: Second pixel R data

BG0~BG9: Second pixel G data

BB0~BB9: Second pixel B data

DE: Data enable signal

DCLK: Data clock signal

The third and fourth pixel are followed the same rules.

CR0~CR9: Third pixel R data

CG0~CG9: Third pixel G data

CB0~CB9: Third pixel B data

DR0~DR9: Fourth pixel R data

DG0~DG9: Fourth pixel G data

DB0~DB9: Fourth pixel B data

Note (1) A ~ D channel are first, second, third and fourth pixel respectively.

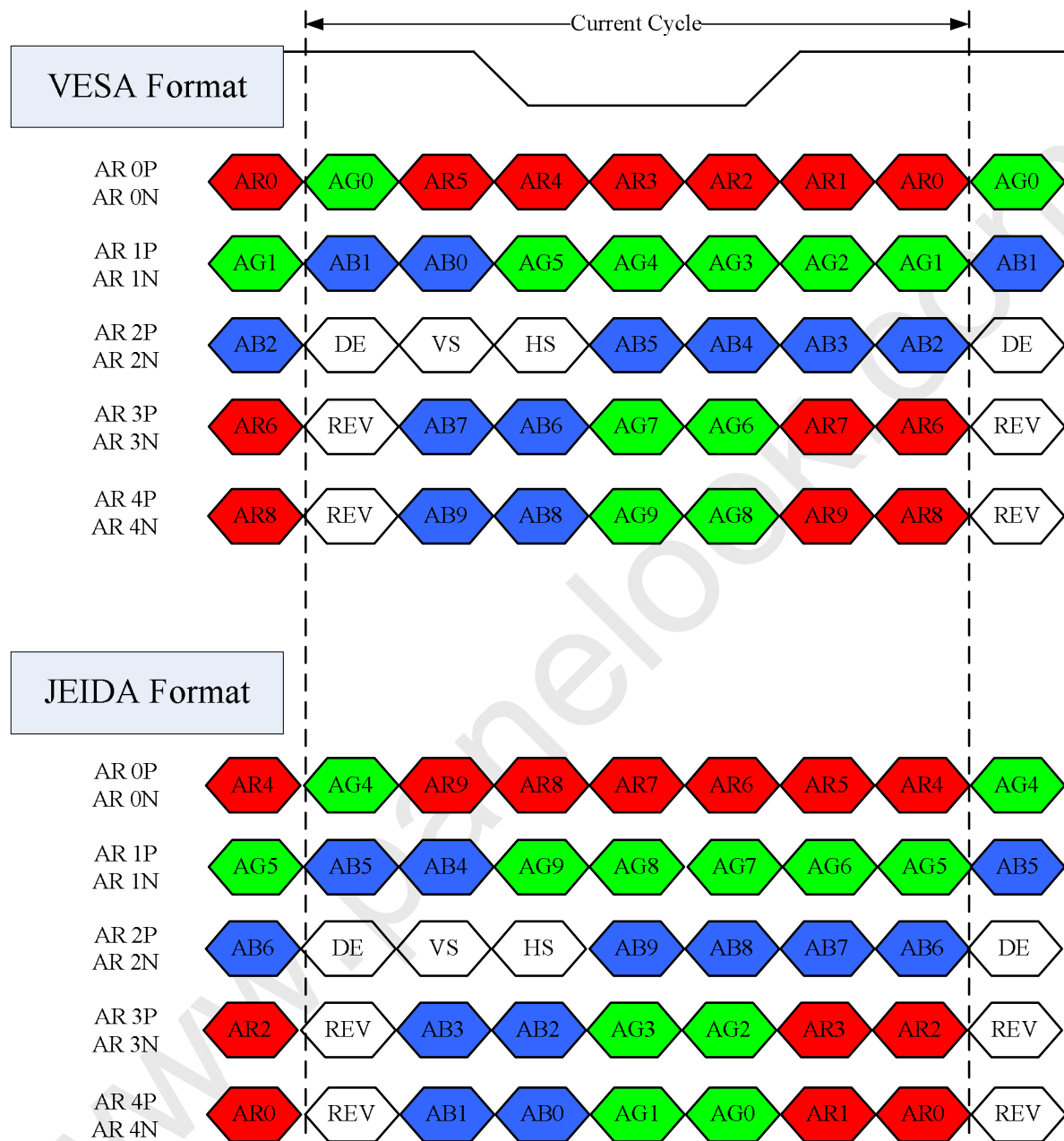
Note (2) The system must have the transmitter to drive the module.

Note (3) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.5 LVDS INTERFACE

VESA Format : SELLVDS = L or Open

JEIDA Format : SELLVDS = H



AR0~AR9: First Pixel R Data (9; MSB, 0; LSB)

AG0~AG9: First Pixel G Data (9; MSB, 0; LSB)

AB0~AB9: First Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

RSVD : Reserved



PRODUCT SPECIFICATION

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																											
		Red										Green										Blue							
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0



Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0
Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage



6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

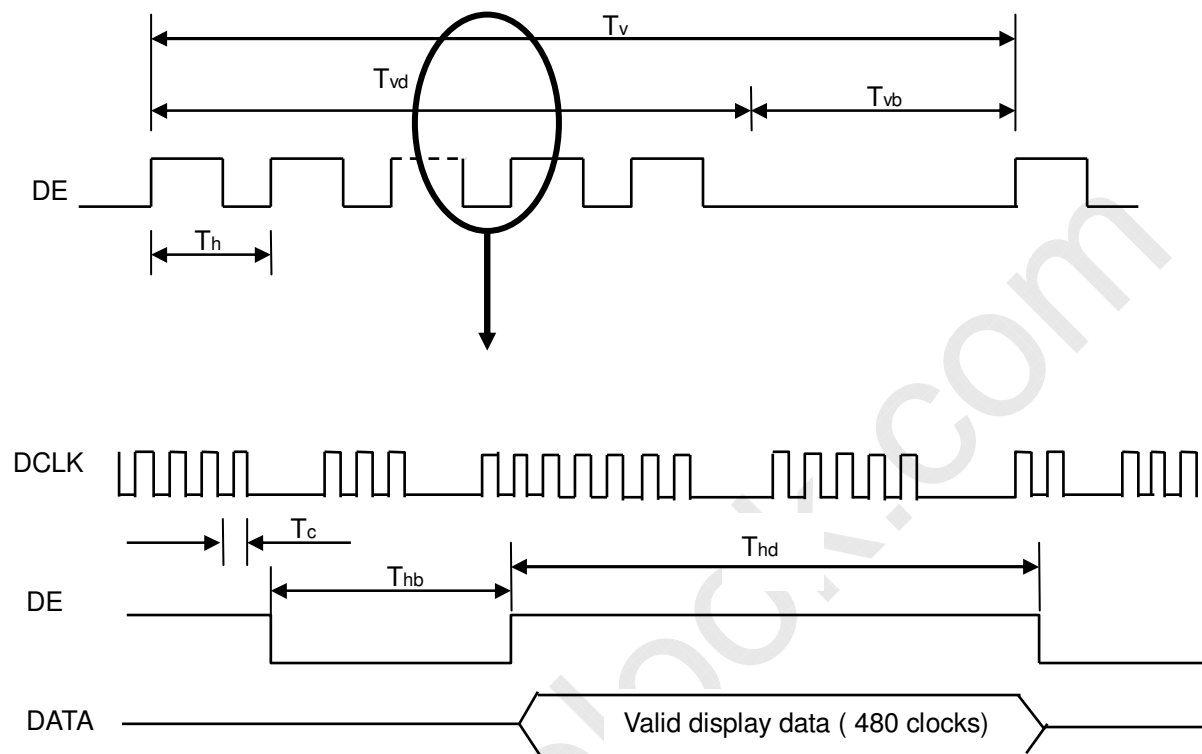
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{clk_{in}}$ ($=1/TC$)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	$F_{clk_{in_mod}}$	$F_{clk_{in}}-2\%$	-	$F_{clk_{in}}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Setup Time	T_{lvsu}	600	-	-	ps	(5)
	Hold Time	T_{lvhd}	600	-	-	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	97	100	103	Hz	(6)
		F_{r6}	117	120	123	Hz	
	Total	T_v	1115	1125	1135	Th	$T_v=T_{vd}+T_{vb}$
	Display	T_{vd}	1080	1080	1080	Th	-
	Blank	T_{vb}	35	45	55	Th	-
Horizontal Active Display Term	Total	T_h	540	550	575	T_c	$T_h=T_{hd}+T_{hb}$
	Display	T_{hd}	480	480	480	T_c	-
	Blank	T_{hb}	60	70	95	T_c	-

Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

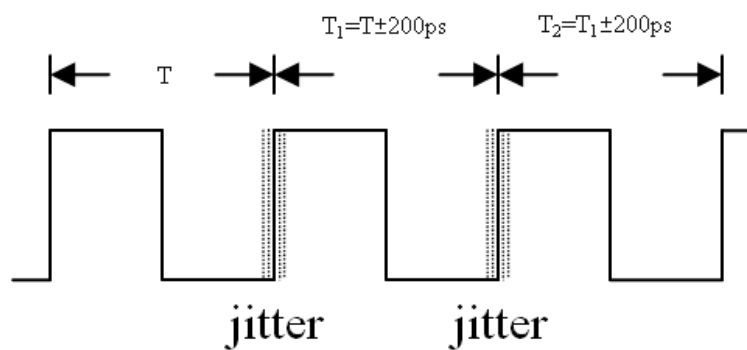
Note (2) Please make sure the range of pixel clock has follow the below equation:

$$F_{clk_{in}}(\max) \geq F_{r6} \times T_v \times T_h$$

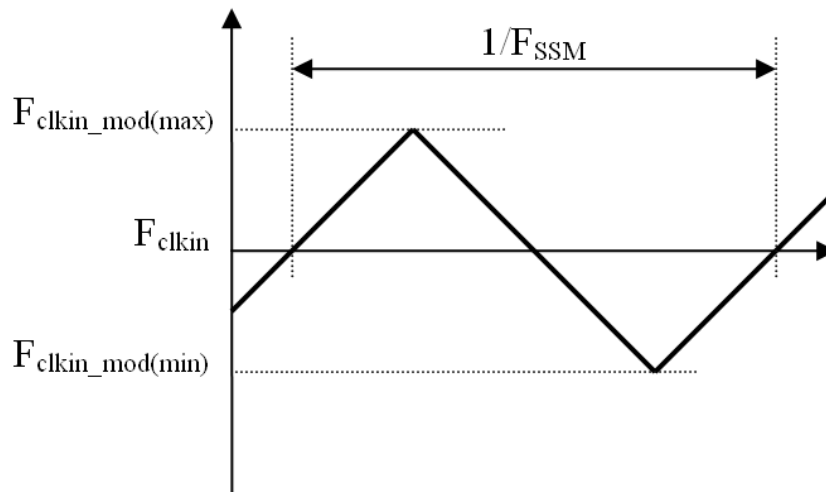
$$F_{r5} \times T_v \times T_h \geq F_{clk_{in}}(\min)$$

INPUT SIGNAL TIMING DIAGRAM


Note (3) The input clock cycle-to-cycle jitter is defined as below figures. $Trcl = |T_1 - T_1|$

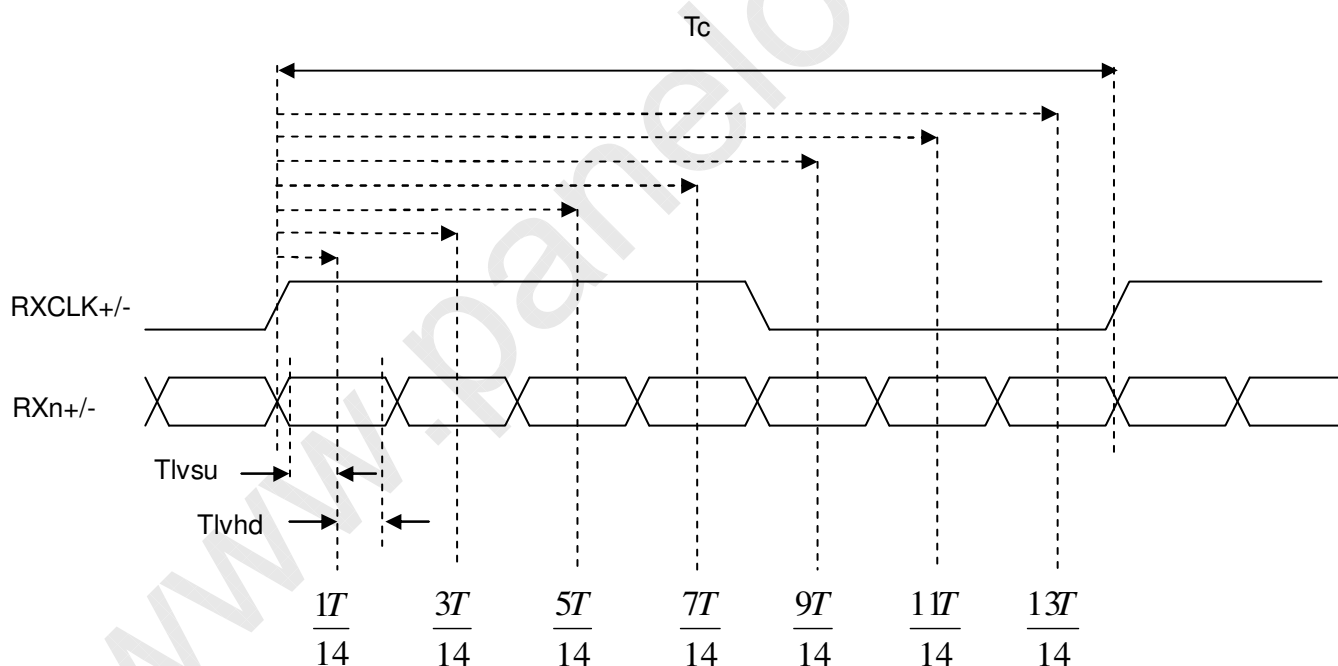


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

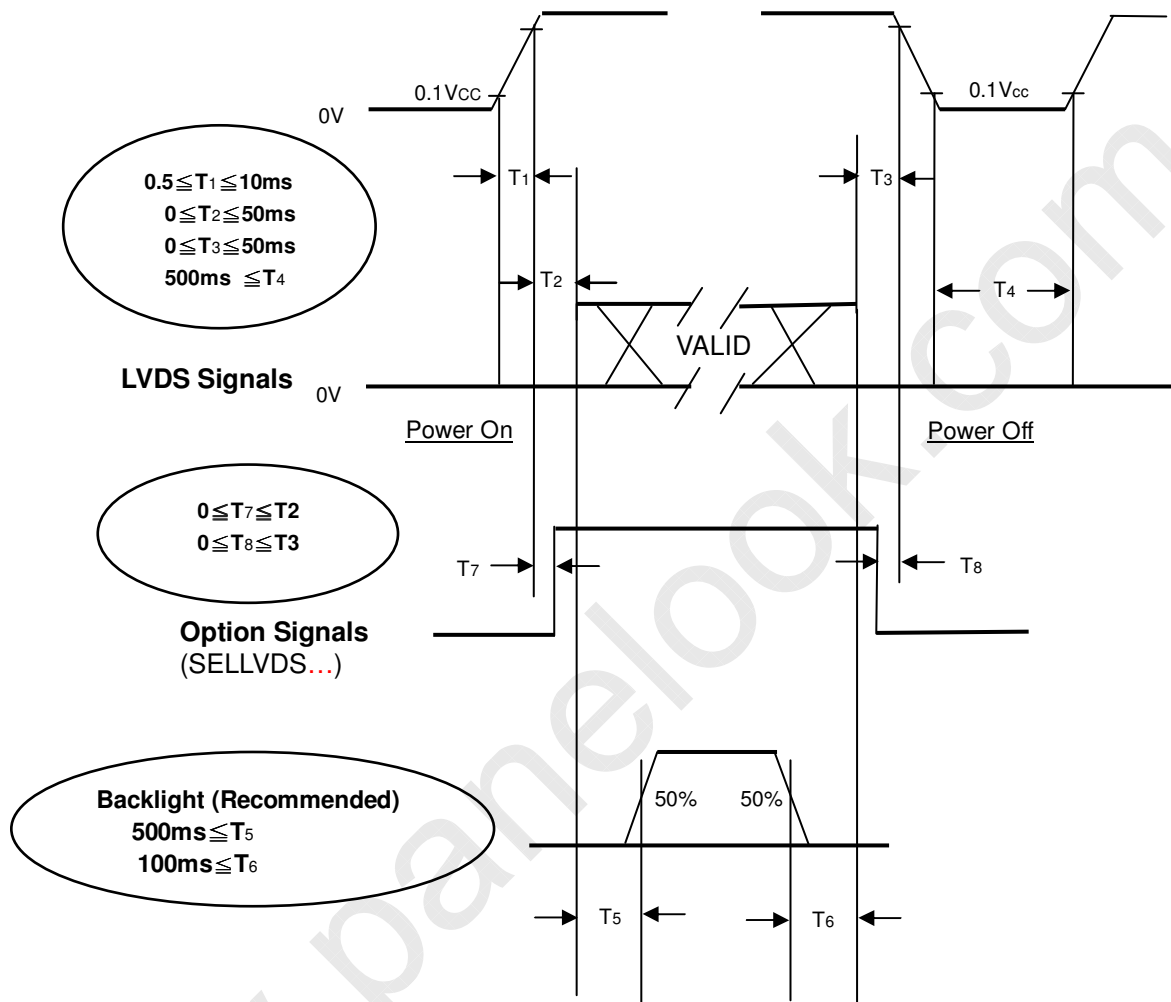
LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) : (ODSEL) = H/L or open for 100/120Hz frame rate. Please refer to 5.1 for detail information

6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should follow the diagram below.



Power ON/OFF Sequence

Note:

- (1) The supply voltage of the external system for the module input should follow the definition of Vcc.
- (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.
- (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.
- (4) T4 should be measured after the module has been fully discharged between power off and on period.
- (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	12V	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I _L	120	mA

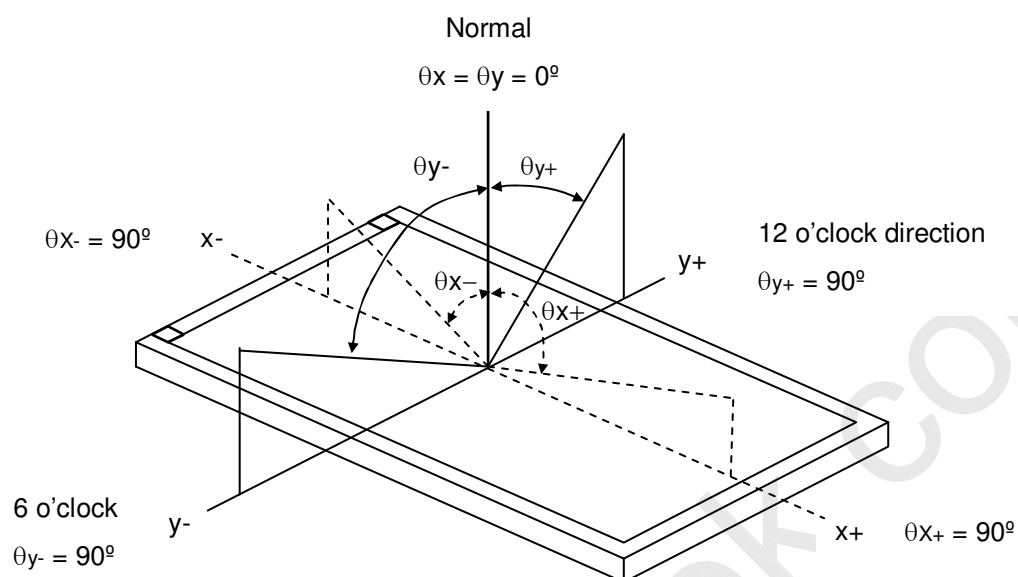
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note		
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	2500	4000	-	-	Note (2)		
Response Time		Gray to gray		-	4.5	9	ms	Note (3)		
Center Luminance of White		L _C		350	450	-	cd/m ²	Note (4)		
White Variation		δW		-	-	1.5	-	Note (7)		
Cross Talk		CT		-	-	4	%	Note (5)		
Color Chromaticity	Red	R _x	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing angle at normal direction	Typ.- 0.03	Typ.+ 0.03	-	-	Note (6)		
		R _y							0.644	-
	Green	G _x							0.325	-
		G _y							0.298	-
	Blue	B _x							0.626	-
		B _y							0.152	-
	White	W _x							0.051	-
		W _y							0.280	-
Color Gamut			-	76	-	%	NTSC			
Viewing Angle	Horizontal	θ_{x+}	CR≥20	80	88	-	Deg.	Note (1)		
		θ_{x-}								
	Vertical	θ_{y+}								
		θ_{y-}								

Note (1) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

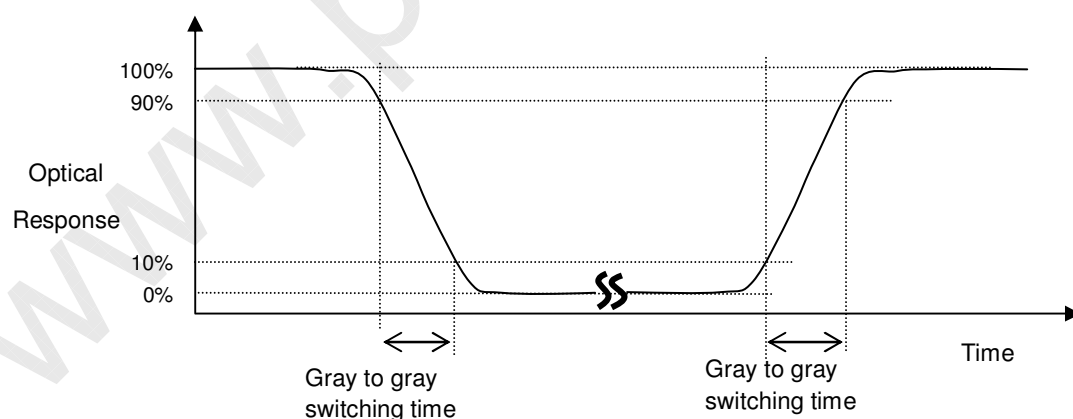
$$\text{Contrast Ratio (CR)} = L_{1023} / L_0$$

L1023: Luminance of gray level 1023

L0: Luminance of gray level 0

CR = CR (X), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7)

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of gray level 0, 127, 255, 383, 511, 639, 767, 895 and 1023.

Gray to gray average time means the average switching time of gray level 0, 127, 255, 383, 511, 639, 767, 895 and 1023 to each other.

Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 1023 at center point.

$L_C = L(5)$, where $L(x)$ is corresponding to the luminance of the point X at the figure in Note (7).

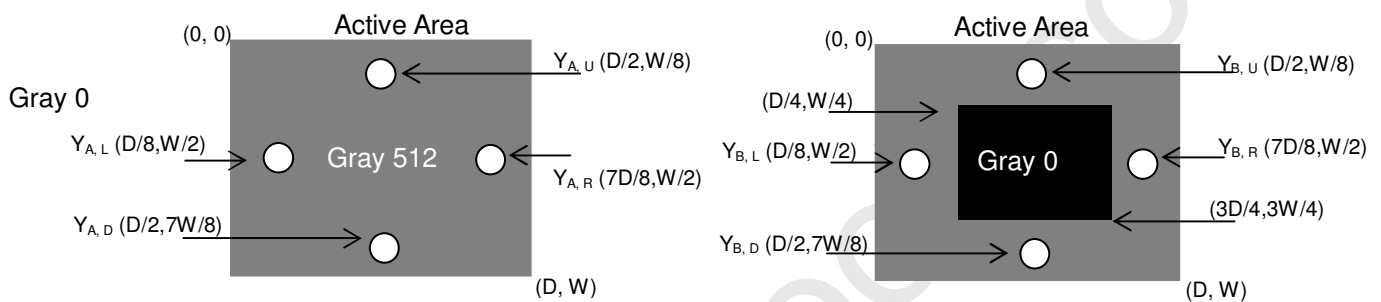
Note (5) Definition of Cross Talk (CT):

$$CT = |Y_B - Y_A| / Y_A \times 100 (\%)$$

Where:

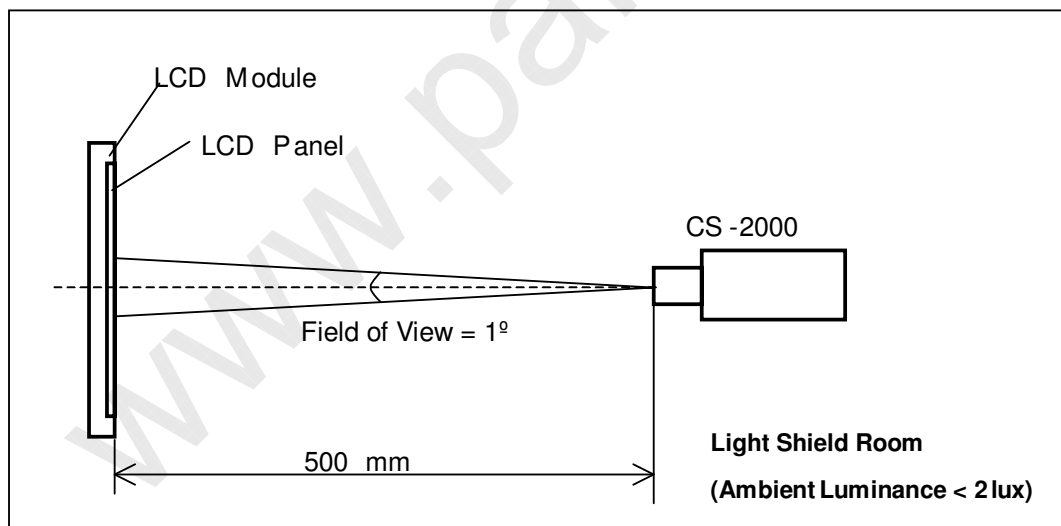
Y_A = Luminance of measured location without gray level 0 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m^2)



Note (6) Measurement Setup:

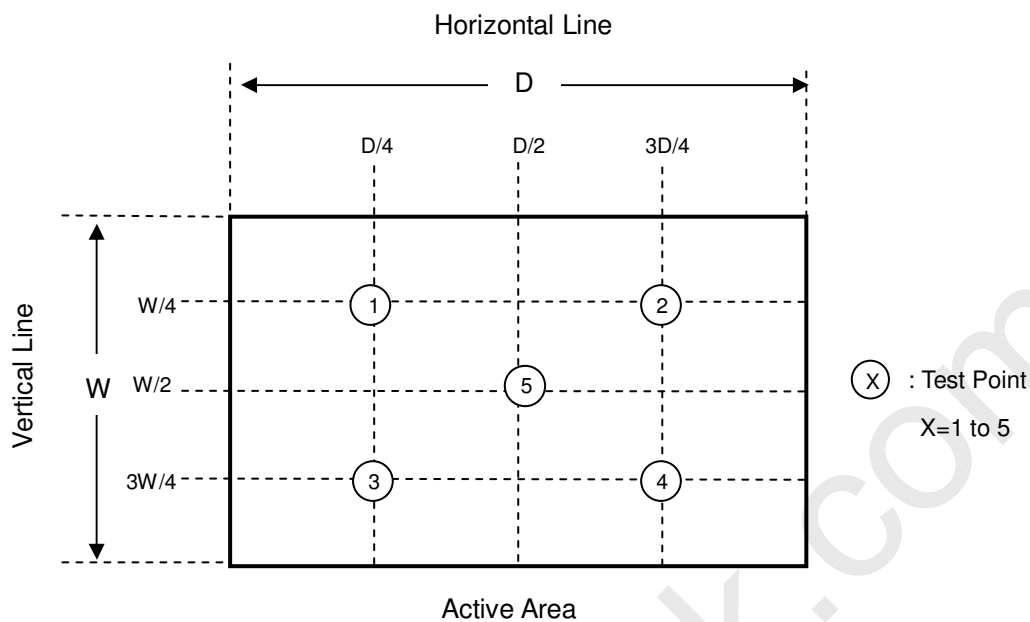
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \text{Maximum} [L(1), L(2), L(3), L(4), L(5)] / \text{Minimum} [L(1), L(2), L(3), L(4), L(5)]$$



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V546H1-LE1
 (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.
 (c) CMO barcode definition:

Serial ID: XX-XX-X-XX-YMD-L-NNNN

Code	Meaning	Description
XX	CMO internal use	-
XX	Revision	Cover all the change
X-XX	CMO internal use	-
YMD	Year, month, day	Year: 2001=1, 2002=2, 2003=3, 2004=4... Month: Jan. ~ Dec.=1, 2, 3, ~, 9, A, B, C Day: 1 st to 31 st =1, 2, 3, ~, 9, A, B, C, ~, W, X, Y, exclude I, O, and U
L	Product line #	Line 1=1, Line 2=2, Line 3=3, ...
NNNN	Serial number	Manufacturing sequence of product

9. Packaging

9.1 PACKING SPECIFICATIONS

- (1) 3 LCD TV modules / 1 Box
- (2) Box dimensions: 1334(L) X 284 (W) X 856 (H)
- (3) Weight: approximately 48 Kg (3 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

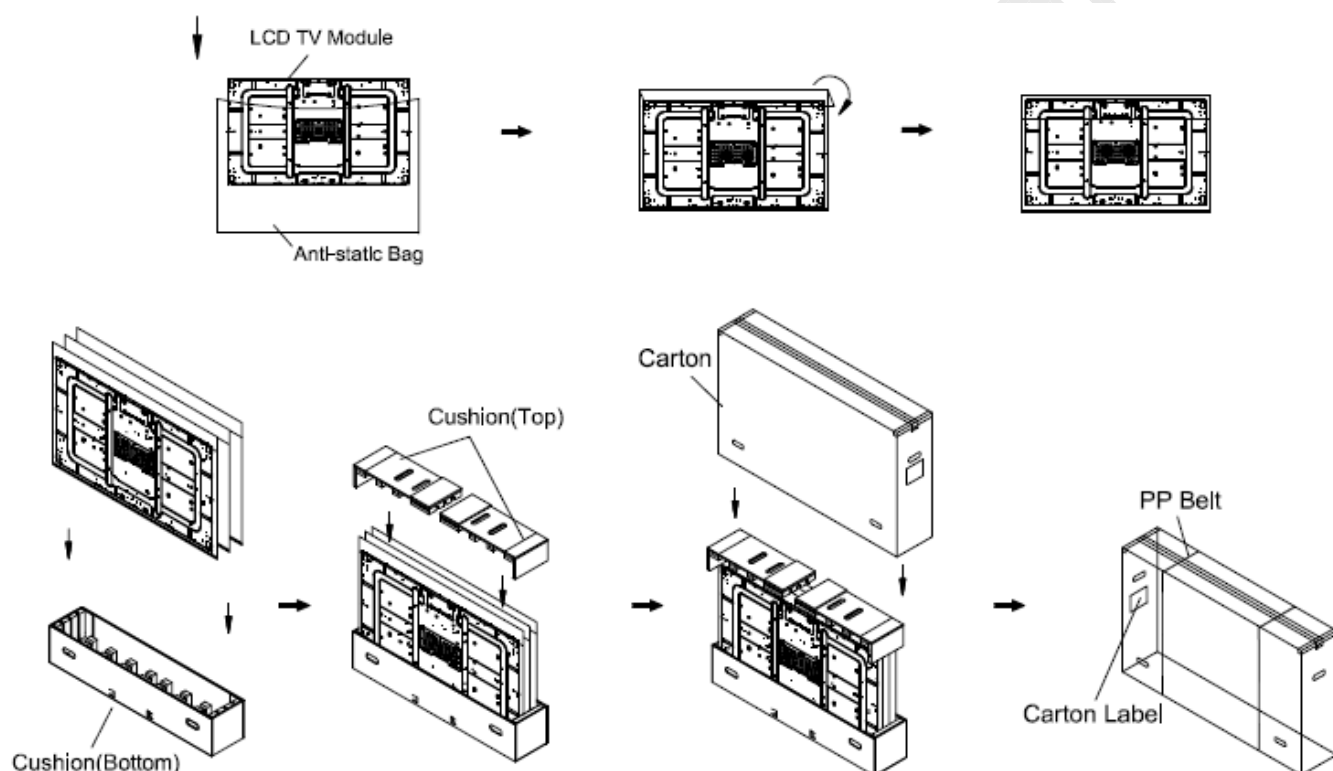


Figure.9-1 packing method

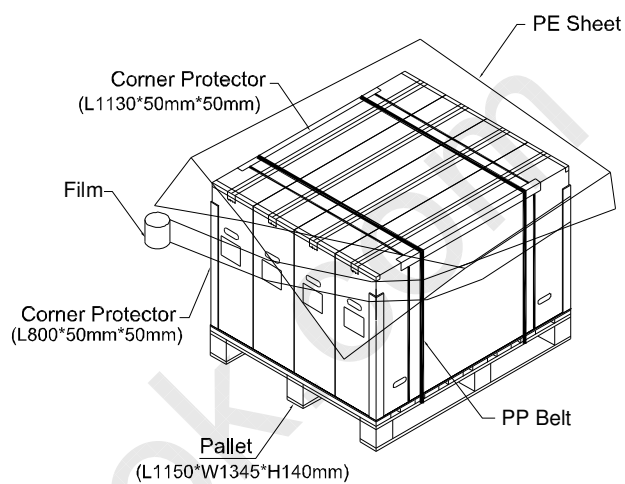
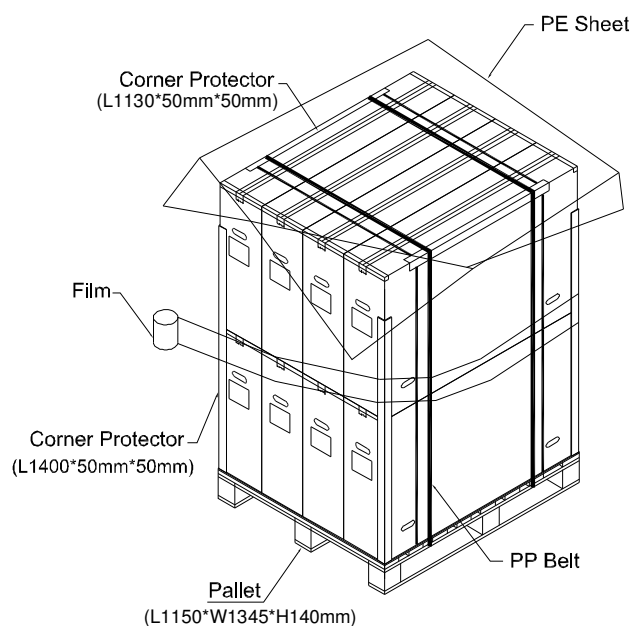
Sea & Land Transportation
Air Transportation


Figure. 9-2 Packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) Do not apply rough force such as bending or twisting to the module during assembly.
- (2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- (3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.
- (4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- (5) Do not plug in or pull out the I/F connector while the module is in operation.
- (6) Do not disassemble the module.
- (7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- (8) Moisture can easily penetrate into LCD module and may cause the damage during operation.
- (9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.
- (10) When ambient temperature is lower than 10°C, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

- (1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.
- (2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- (3) After the module's end of life, it is not harmful in case of normal operation and storage.

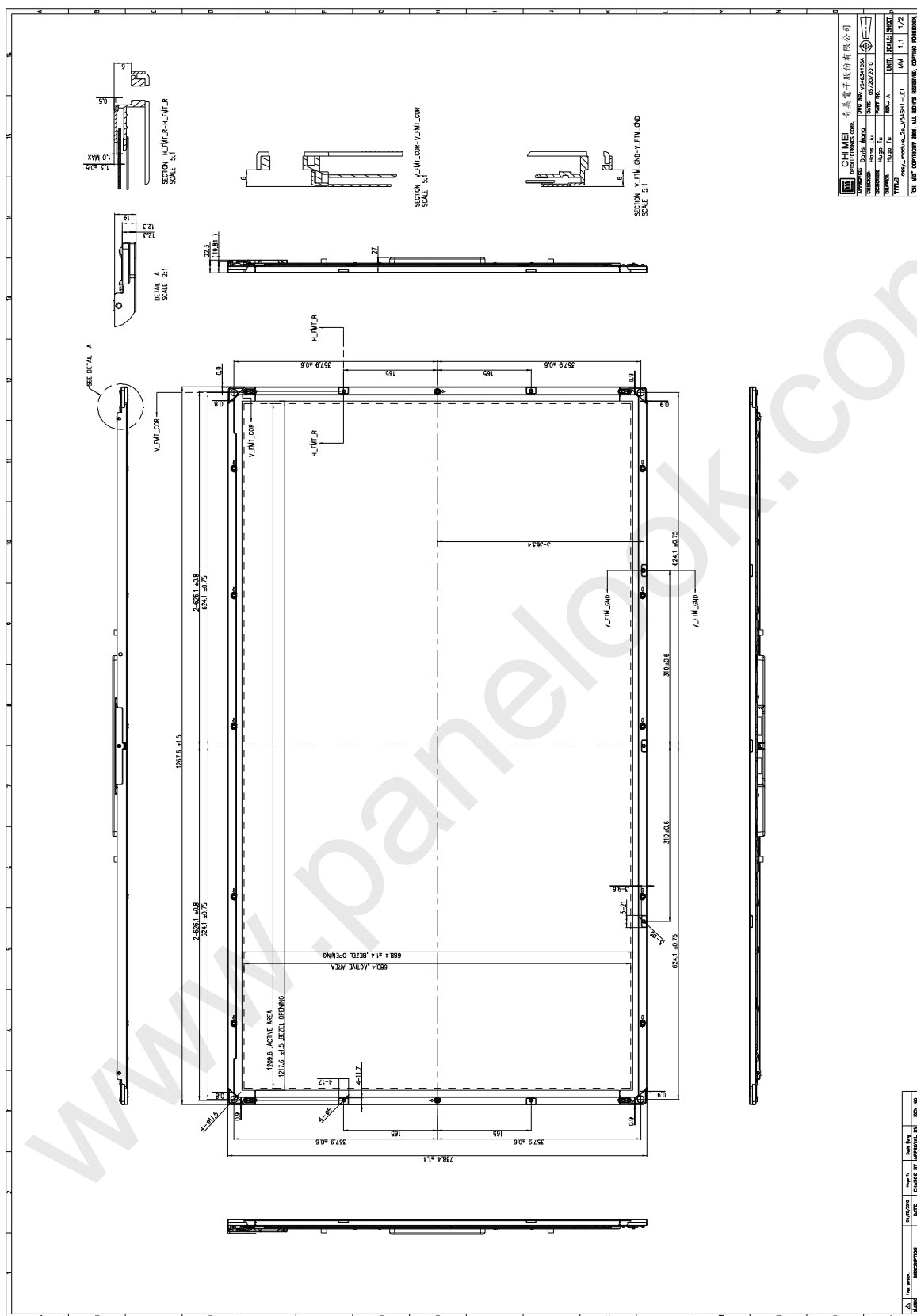
10.3 SAFETY STANDARDS

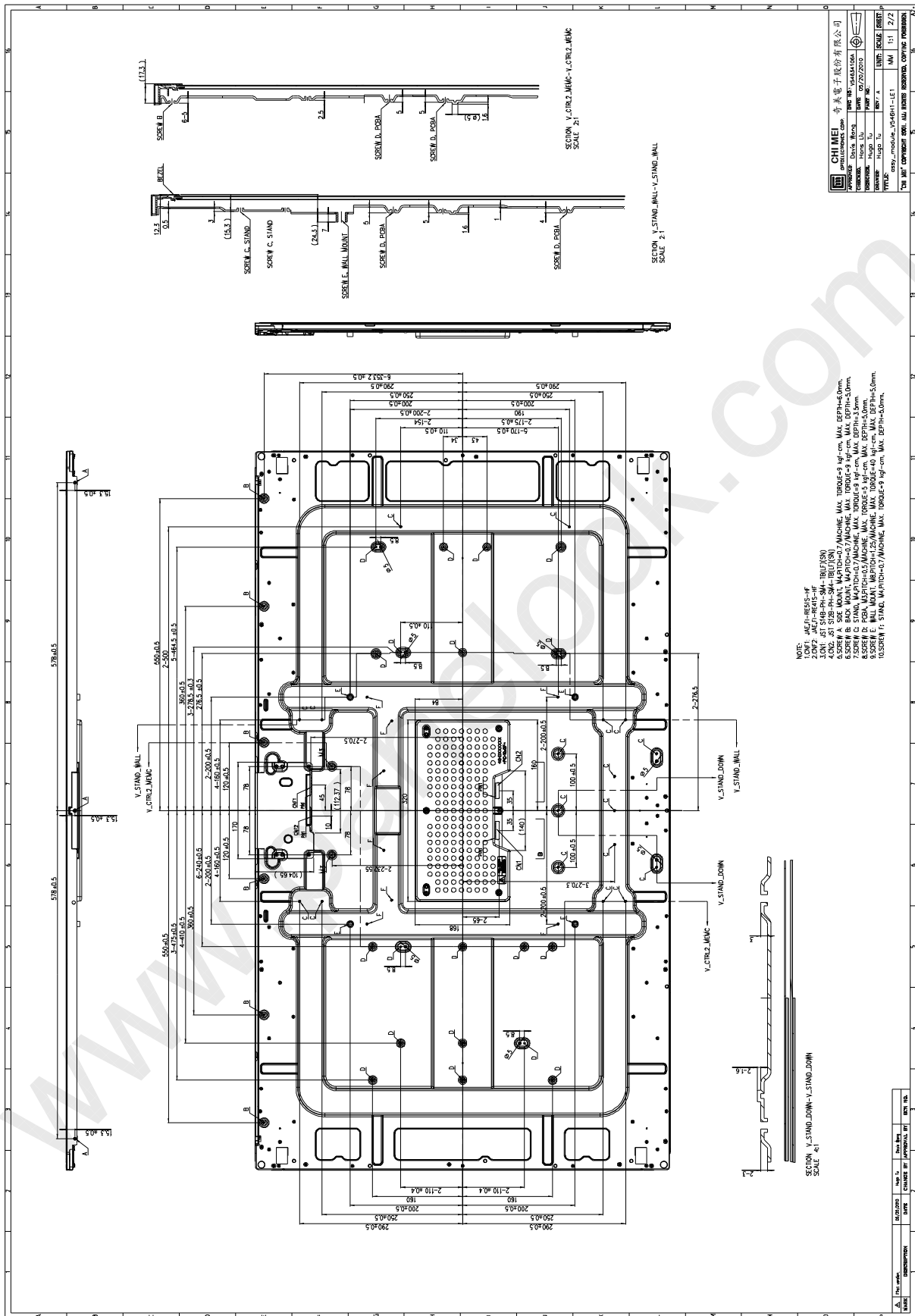
The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

11. MECHANICAL CHARACTERISTIC





CHIMEI	奇美電子股份有限公司
CHIMEI INNO LUX	奇美電子股份有限公司
DATE	2010/05/14
VERSION	1.0
DESIGNER	YANG
CHECKER	YANG
DATE	2010/05/14
SCALE	1:1
UNIT	MM
DATE	2010/05/14
SCALE	1:1
UNIT	MM
DATE	2010/05/14
SCALE	1:1
UNIT	MM

- NOTE:
1. UNIT: ALL DIMENSIONS IN MM.
 2. CON: 1ST STRIP-PIN-SM4-RBUT(SN)
 3. CON: 2ND STRIP-PIN-SM4-RBUT(SN)
 4. CON: 3RD STRIP-PIN-SM4-RBUT(SN)
 5. CON: 4TH STRIP-PIN-SM4-RBUT(SN)
 6. CON: 5TH STRIP-PIN-SM4-RBUT(SN)
 7. CON: 6TH STRIP-PIN-SM4-RBUT(SN)
 8. CON: 7TH STRIP-PIN-SM4-RBUT(SN)
 9. CON: 8TH STRIP-PIN-SM4-RBUT(SN)
 10. CON: 9TH STRIP-PIN-SM4-RBUT(SN)

DATE	2010/05/14	DESIGNER	YANG
DATE	2010/05/14	CHECKER	YANG
DATE	2010/05/14	APPROVAL	YANG