☐ Tentative Specification
☐ Preliminary Specification
■ Approval Specification

MODEL NO.: V580HK1

SUFFIX: LE6

Customer:

APPROVED BY SIGNATURE

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 2.0	Apr. 15, 2013	All	All	Approval Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V580HK1-LE6 is a 58″ TFT Liquid Crystal Display module with LED Backlight unit and 4ch-LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display true 1.07G colors (8-bit+FRC). The driving board module for backlight is built-in.

1.2 FEATURES

- High brightness (300 nits)
- High contrast ratio (5000:1)
- Fast response time (Gray to Gray typical : 7.5 ms)
- High color saturation (NTSC 72%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 100Hz/120Hz frame rate
- Viewing Angle : 178(H)/178(V) (CR>20) VA Technology
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance
- T-con input frame rate: 100Hz/120Hz, output frame rate: 100Hz/120Hz

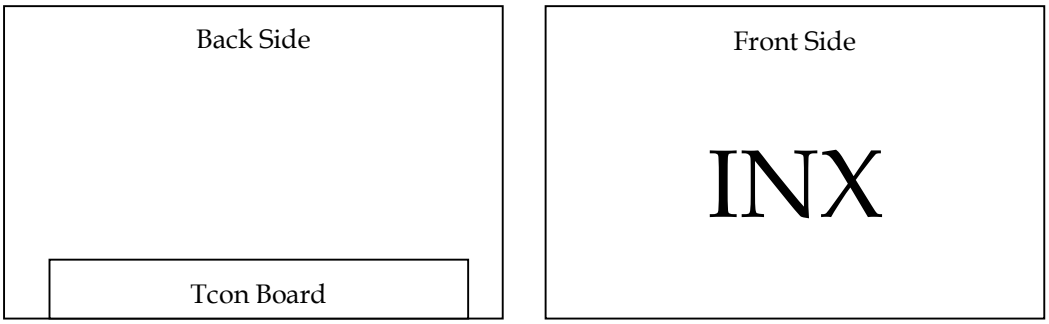
1.3 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	1270.08(H) x 721.44(V) (58″ diagonal)	mm	(1)
Bezel Opening Area	1275.3 (H) x 726.7(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.2205(H) x 0.6680(V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G colors (8-bit+FRC)	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 1%)	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with “INX”		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. INX reserves the rights to change this feature.

Note (3)



1.4 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size Weight	Horizontal (H)	1288.8	1290.3	1291.8	mm	(1), (2)
	Vertical (V)	743.2	744.7	746.2	mm	(1), (2)
	Depth (D)	15.2	16.2	17.2	mm	To Rear
		24.7	26.2	27.7	mm	To converter cover
	Weight	17.25	18.16	19.07	Kg	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T_{OP}	0	50	°C	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

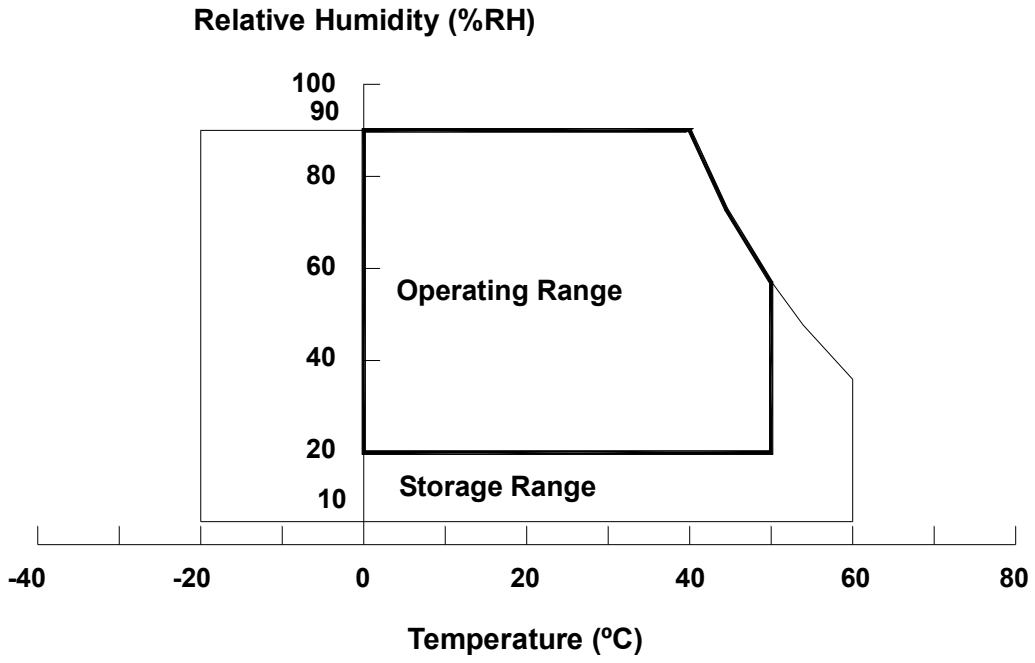
(c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, it is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	Ta = 25 ℃	-	-	60	V_{RMS}	
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

3. ELECTRICAL CHARACTERISTICS

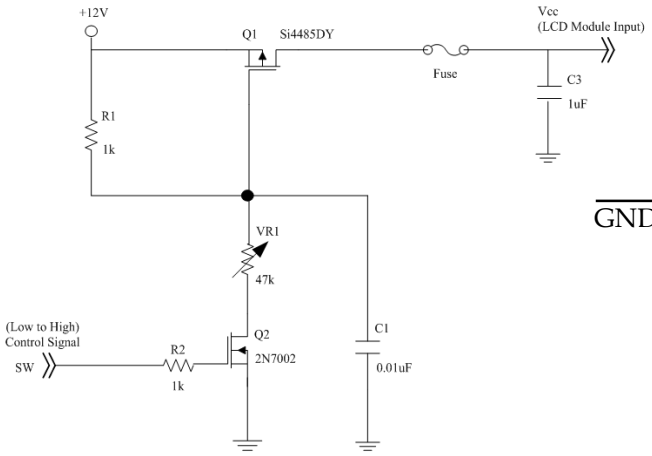
3.1 TFT LCD MODULE

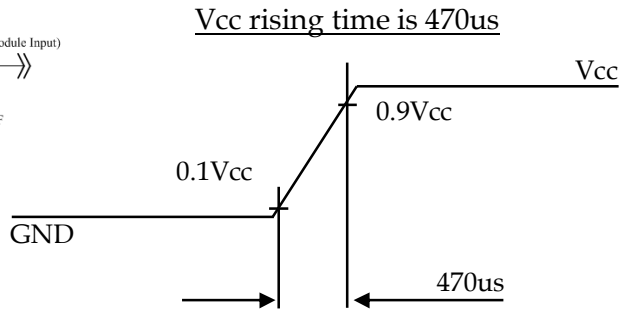
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	3.51	A	(2)
Power Consumption	White Pattern	P_T	—	6.05	7.22	W	(3)
	Black Pattern	P_T	—	5.73	6.86	W	
	Horizontal Stripe	P_T	—	18.32	21.99	W	
Power Supply Current	White Pattern	—	—	0.50	0.60	A	
	Black Pattern	—	—	0.48	0.57	A	
	Horizontal Stripe	—	—	1.53	1.83	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	+300	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-300	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.)

Note (2) Measurement condition :

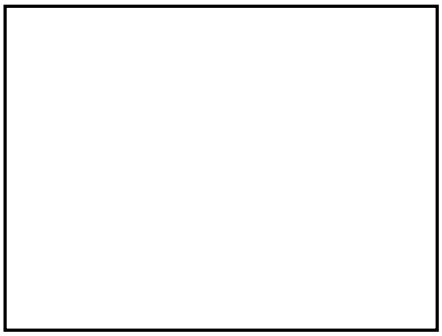




Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 120 Hz, whereas a

power dissipation check pattern below is displayed.

a. White Pattern

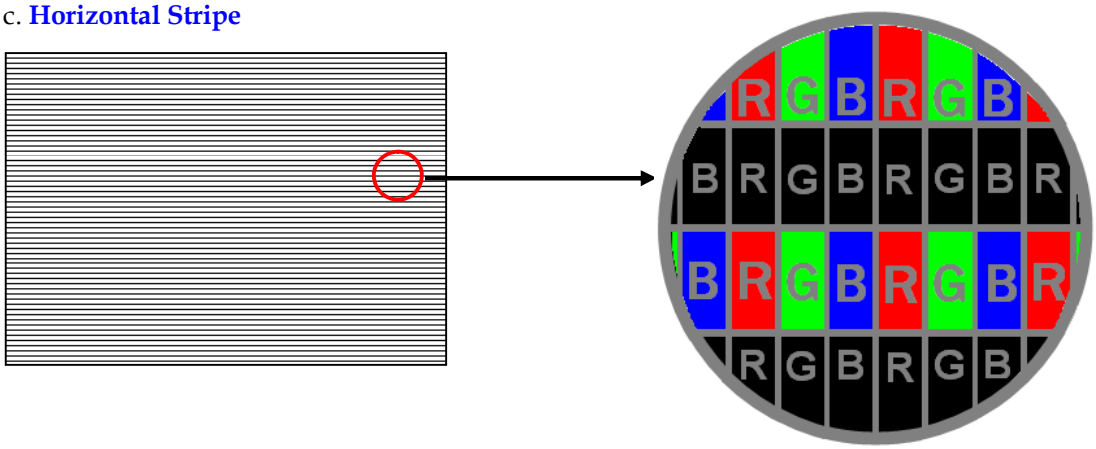


Active Area

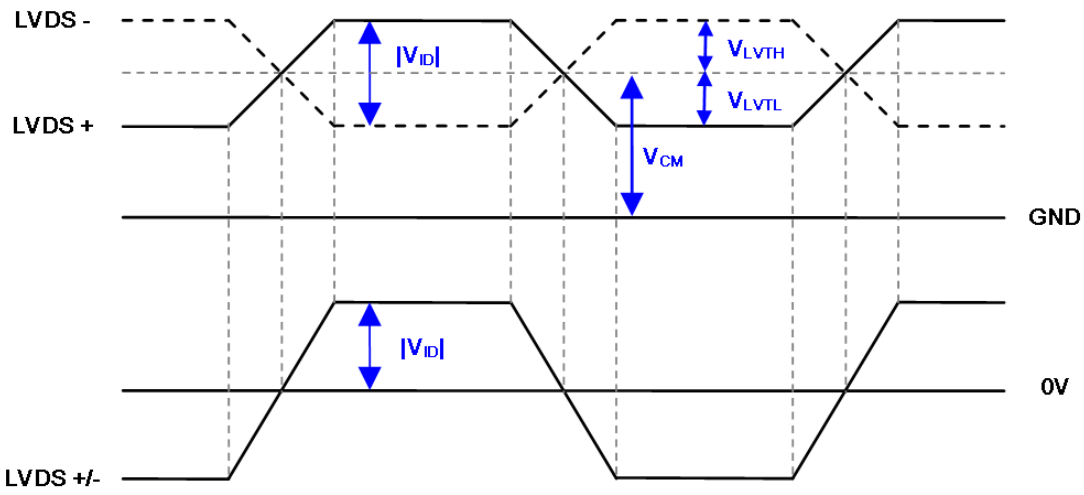
b. Black Pattern

Active Area

c. **Horizontal Stripe**



Note (4) The LVDS input characteristics is shown as below :



3.2 BACKLIGHT UNIT

3.2.1 CONVERTER CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	P_{BL}	-	66	75.6	W	(1), (2)
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	I_{BL}	-	2.75	3.15	A	Non Dimming
Input Inrush Current	I_R	-	-	4.28	Apeak	V_{BL}=22.8V, (3)
Dimming Frequency	FB	170	180	190	Hz	
Dimming Duty Ratio	DDR	5	-	100	%	(4)
Life Time	-	30,000	-	-	Hrs	(5)

Note (1) The power supply capacity should be higher than the total converter power consumption PBL. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

Note (2) The measurement condition of Max. value is based on 58" backlight unit under input voltage 24V.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 20ms.

Note (4) EPWM signal have to input available duty range. 5% minimum duty ratio is only valid for electrical operation.

Note (5) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value, Operating condition: Continuous operating at Ta = 25±2℃

3.2.2 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		F_{EPWM}	—	150	160	170	Hz	Normal mode (7)	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open Collector Normal: GND (4)	
VBL Rising Time		Tr1	—	20	—	—	ms	10%-90%V_{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time		T_{on}	—	300	—	—	ms		
		T_{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. Please refers to Fig.2.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

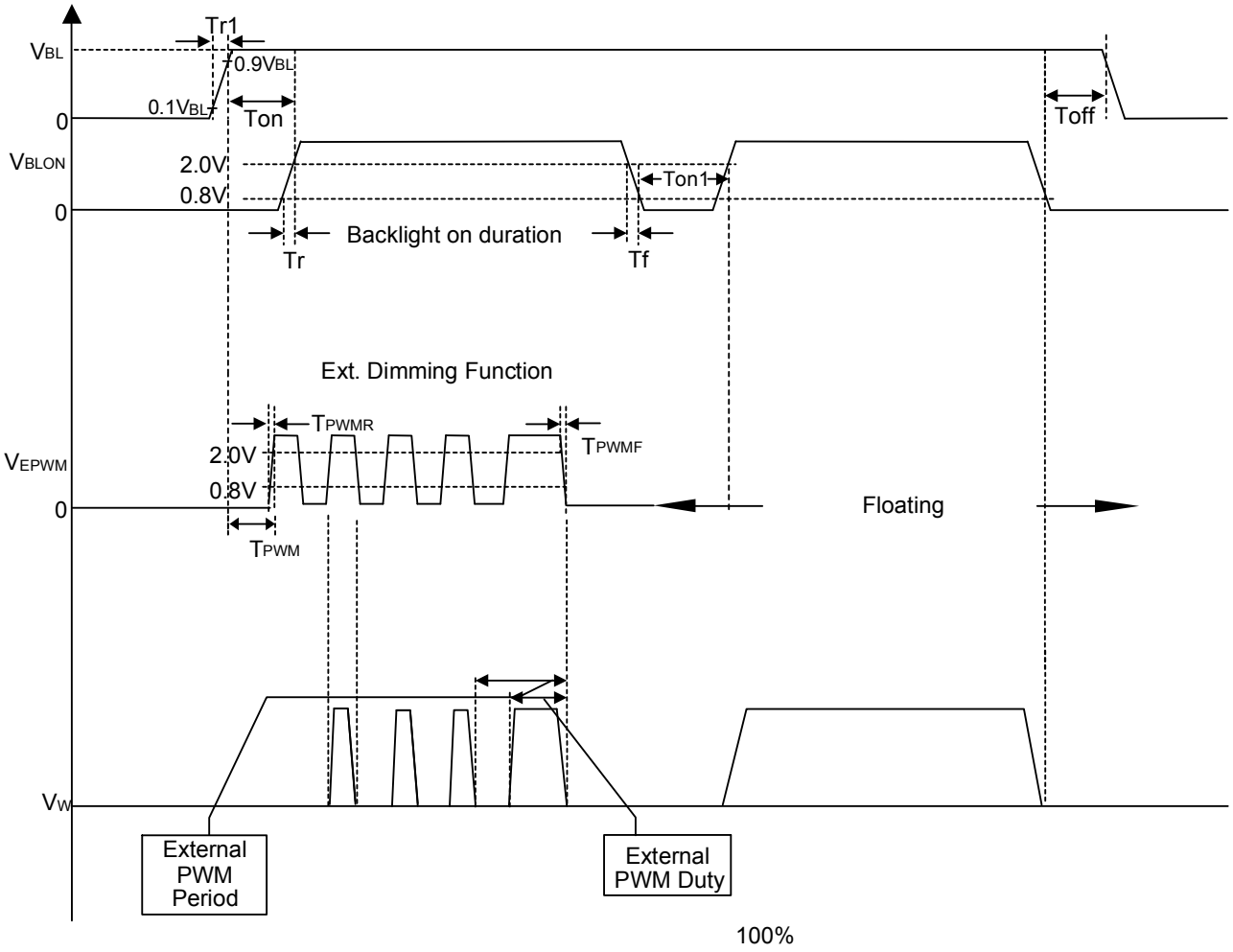


Fig. 1

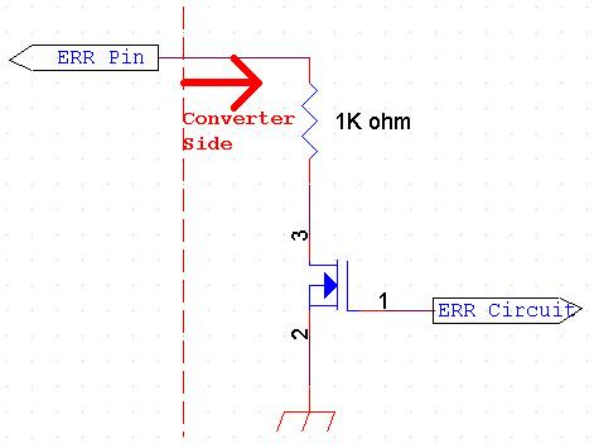


Fig. 2

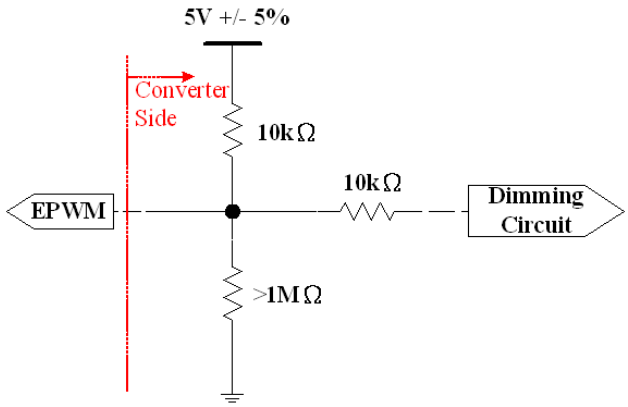
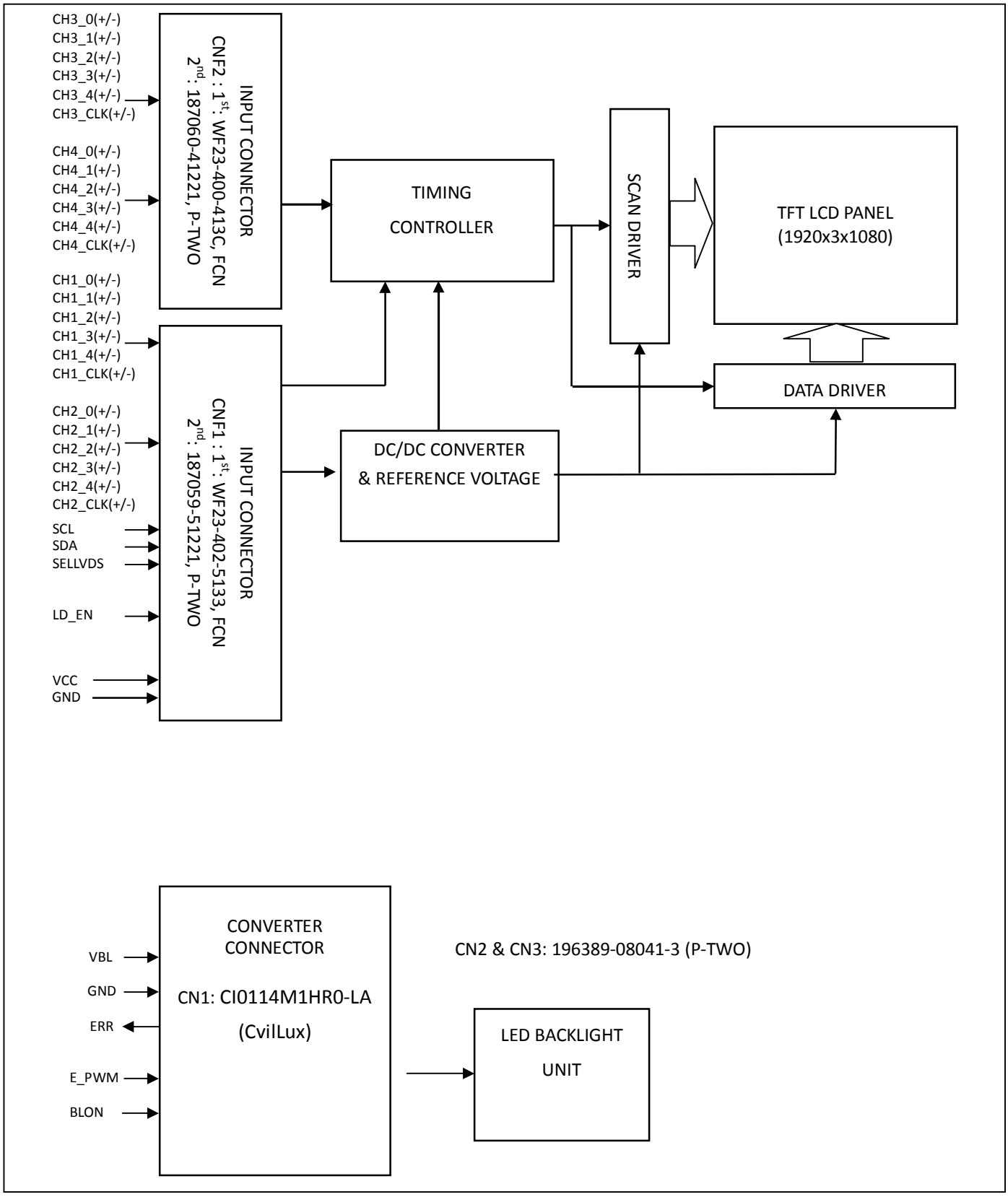


Fig. 3

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment (WF23-402-5133, FCN; 187059-51221, P-TWO)

Matting connector : FI-RE51HL (JAE)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	I2C Serial Clock (for local dimming demo function)	(6)
3	SDA	I2C Serial Data (for local dimming demo function)	
4	N.C.	No Connection	(1)
5	N.C.	No Connection	(1)
6	N.C.	No Connection	(1)
7	SELLVDS	Input signal for LVDS Data Format Selection	(2), (4)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	–
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	(5)
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	–
19	CH1CLK-	First pixel Negative LVDS differential clock input.	(5)
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	–
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	(5)
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	N.C.	No Connection	(1)
27	N.C.	No Connection	(1)

28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	(5)
29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	–
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	(5)
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	–
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	(5)
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	LD_EN	Input signal for Local Dimming Enable	(3), (4)
43	N.C.	No Connection	(1)
44	GND	Ground	–
45	GND	Ground	–
46	GND	Ground	–
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	–
49	VCC	+12V power supply	–
50	VCC	+12V power supply	–
51	VCC	+12V power supply	–

CNF2 Connector pin assignment (WF23-400-413C, FCN; 187060-41221, P-TWO)

Matting connector : FI-RE41HL (JAE)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	

5	N.C.	No Connection	
6	N.C.	No Connection	
7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	–
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	(5)
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	–
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	(5)
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	–
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	(5)
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	–
25	GND	Ground	–
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	(5)
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	–
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	(5)
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	–

36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	(5)
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	
39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	GND	Ground	–
41	GND	Ground	–

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or Open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) Local dimming enable selection.

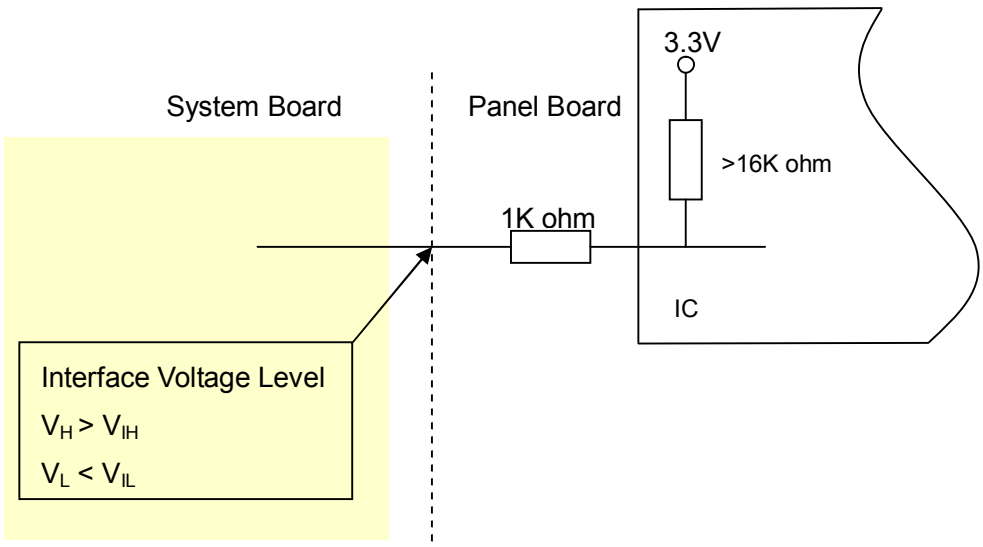
L= Connect to GND，H=Connect to +3.3V or Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

LD_EN enable pin should be set in power on stage.

Backlight should be turned off in the period of changing original setting after power on.

Note (4) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.

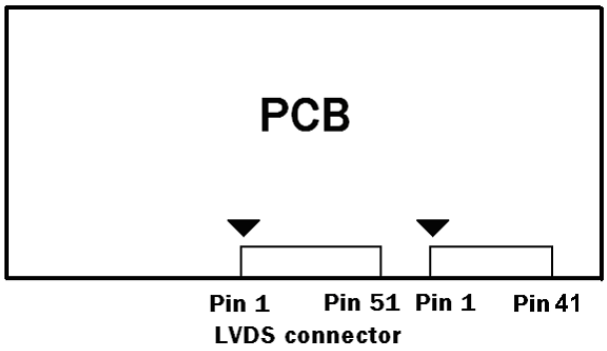


Note (5) LVDS 4-port data mapping

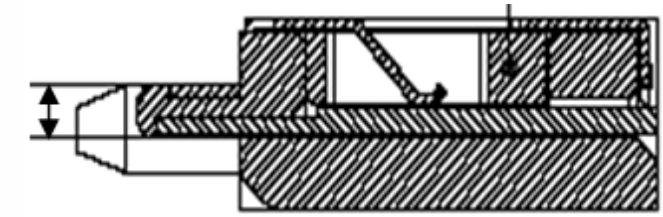
Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

Note (6) Please reference Appendix A

Note (7) LVDS connector pin order defined as follows



Note (8) LVDS connector mating dimension range request is 0.93mm~1.0mm as below



5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2: 196388-12041-3, P-TWO

Pin №	Symbol	Feature
1	N1	Negative of LED String
2	N2	
3	N3	
4	N4	
5	N5	
6	N6	
7	N7	
8	N8	
9	NC	NC
10	VLED	Positive of LED String
11	VLED	
12	VLED	

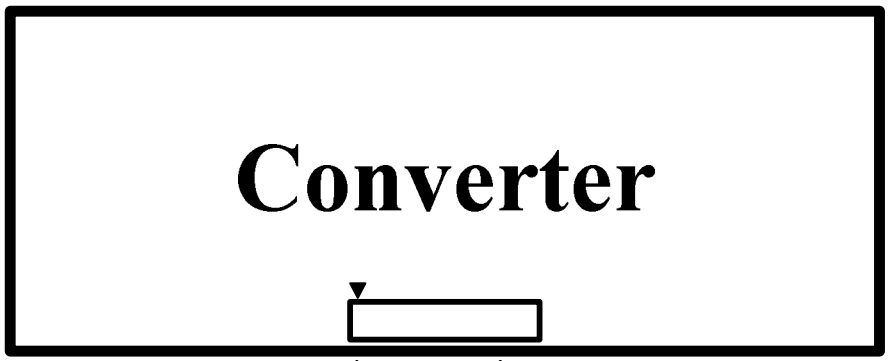
5.3 CONVERTER UNIT

CN1 (Header) : CI0114M1HR0-LA, CvilLux

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) ; Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Note (1) If Pin14 is open, E_PWM is 100% duty.

Note (2) Input connector pin order defined as follows

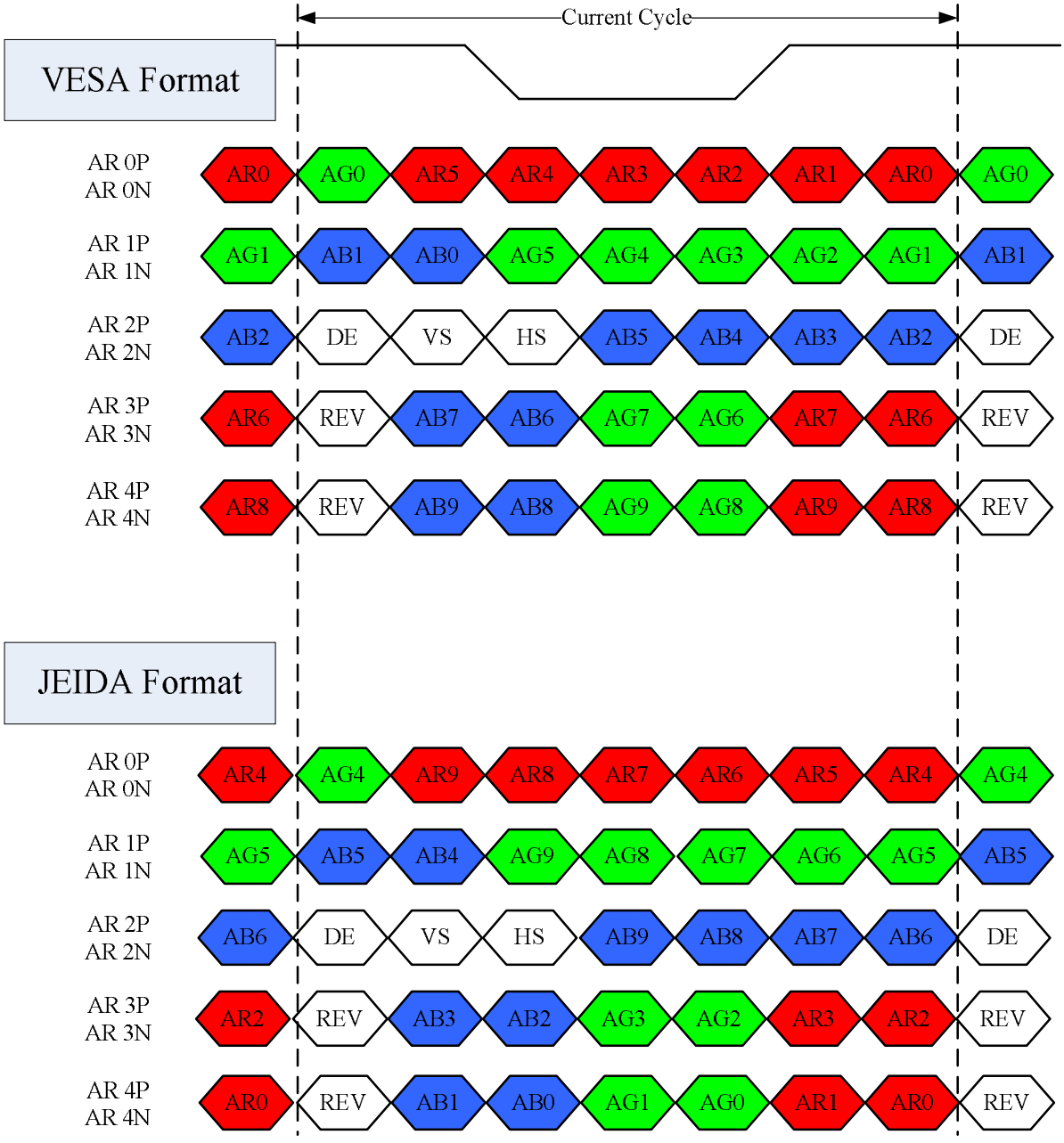


Input Connector

5.4 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open



AR0~AR9	First Pixel R Data (9; MSB, 0; LSB)	DE	Data enable signal
AG0~AG9	First Pixel G Data (9; MSB, 0; LSB)	DCLK	Data clock signal
AB0~AB9	First Pixel B Data (9; MSB, 0; LSB)	RSVD	Reserved

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 °C)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	
	Input cycle to cycle jitter	T_{rcl}	-	-	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	-	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	-	400	ps	(5)

6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	(6), (7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1350	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	270	315	Th	—
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

6.1.2 Timing spec for Frame Rate = 120Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	114	120	126	Hz	(6), (7)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	315	Th	—
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

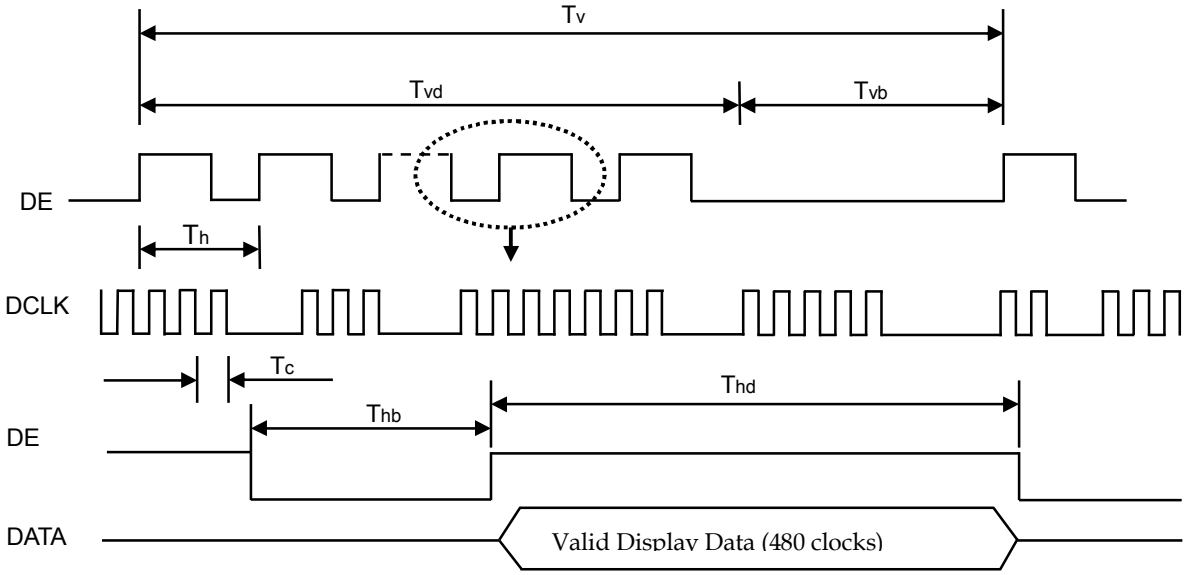
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

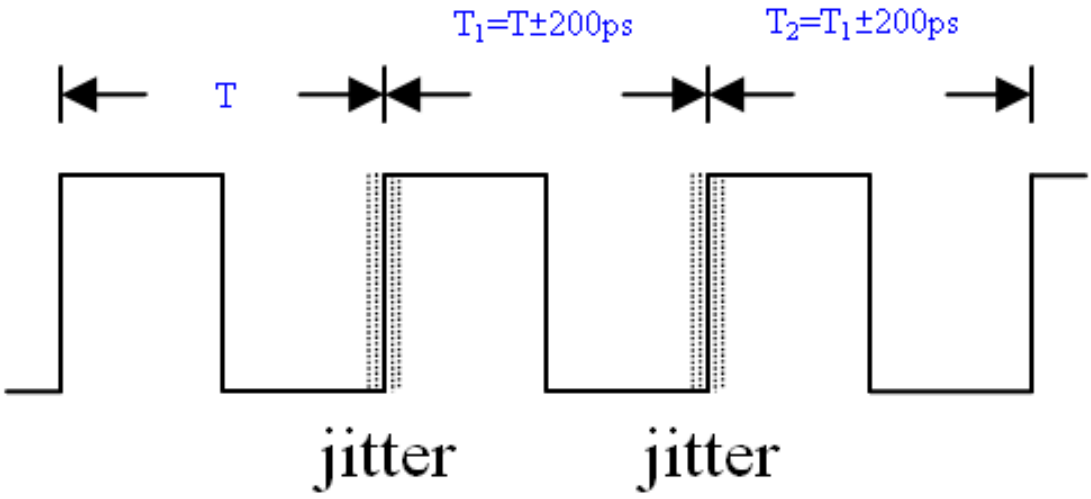
$Fclkin(max) \geqq Fr6 \times Tv \times Th$

$Fr5 \times Tv \times Th \geqq Fclkin(min)$

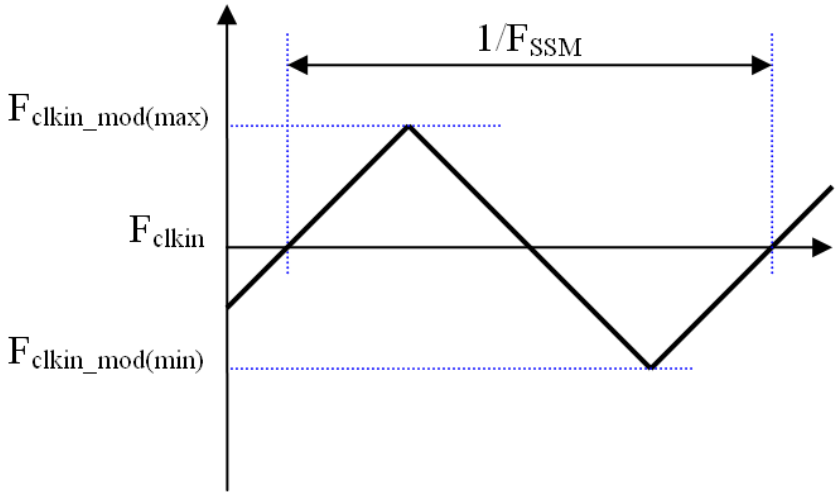
INPUT SIGNAL TIMING DIAGRAM



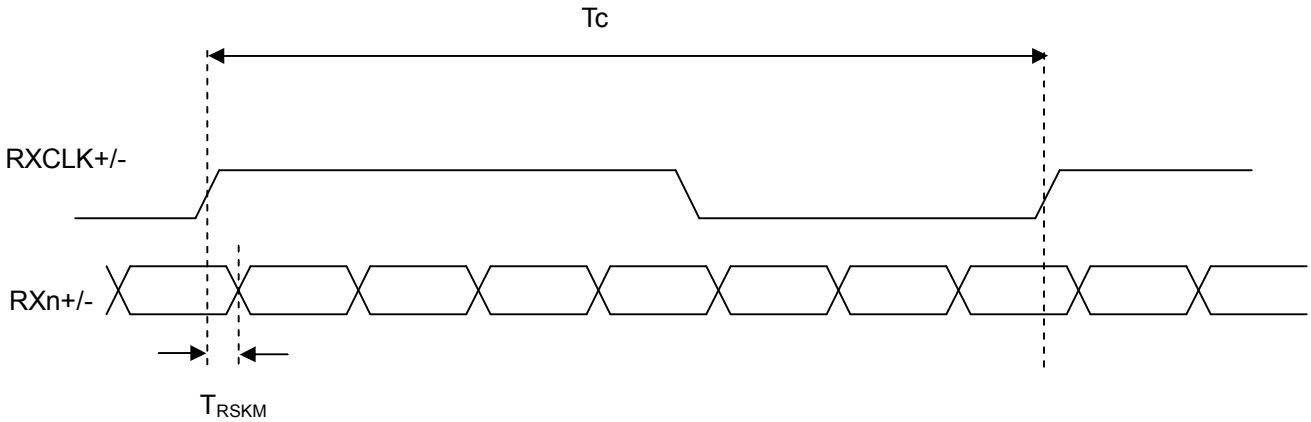
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = | T_1 – T |



Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.

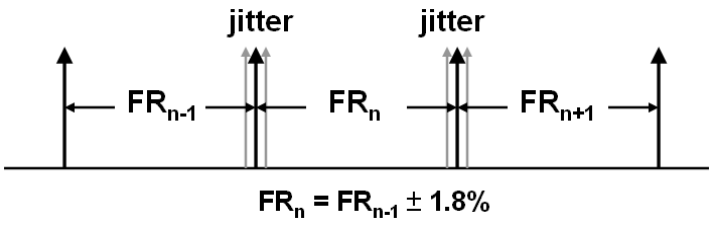


Note (5) The LVDS timing diagram and the receiver skew margin is defined and shown in following figure.



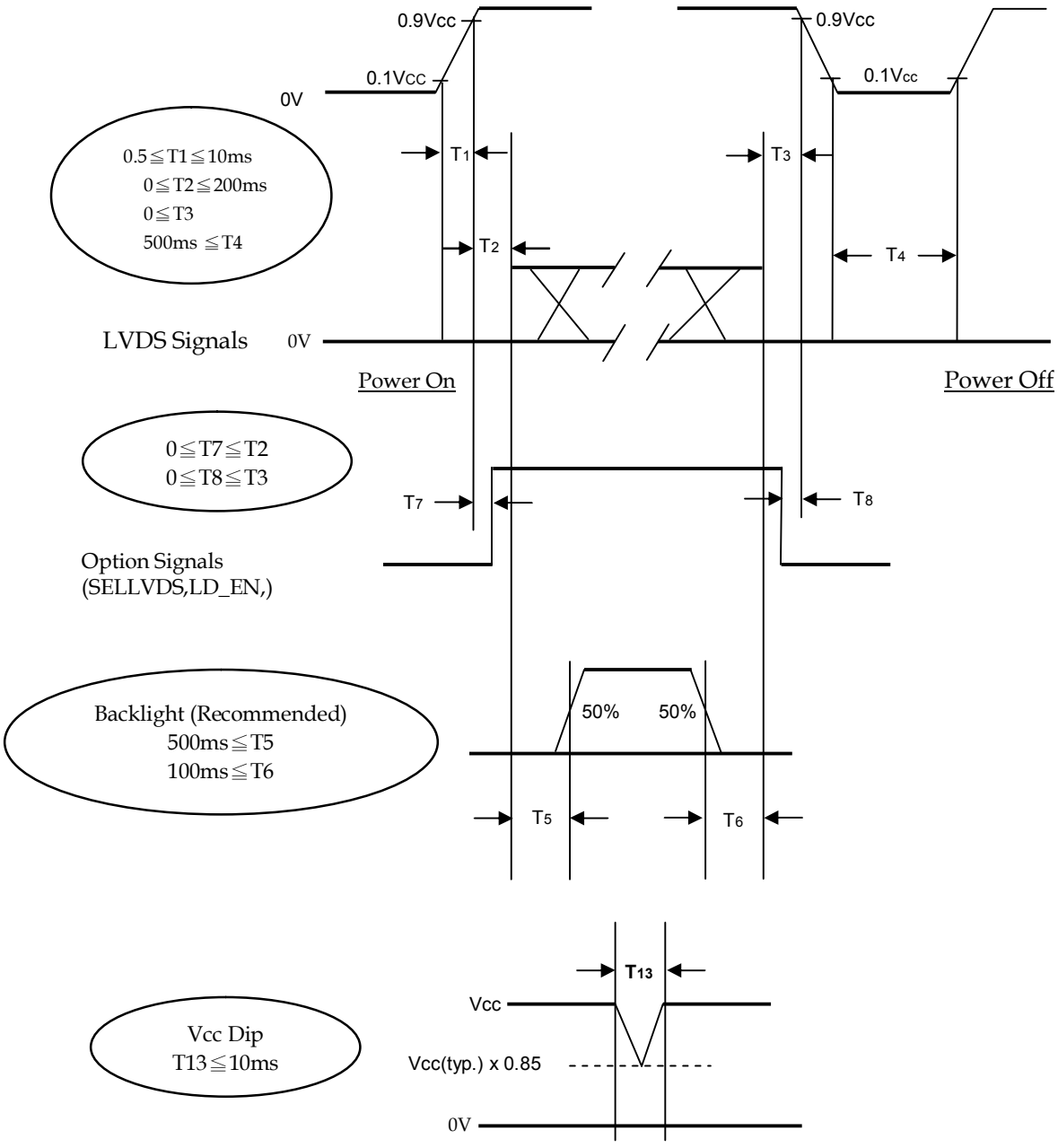
Note (6) The frame-to-frame jitter of the input frame rate is defined as the above figures. FRn = FRn-1 ± 1.8%.

Note (7) The setup of the frame rate jitter > 1.8% may result in the cosmetic LED backlight symptom but the electric function is not affected.



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

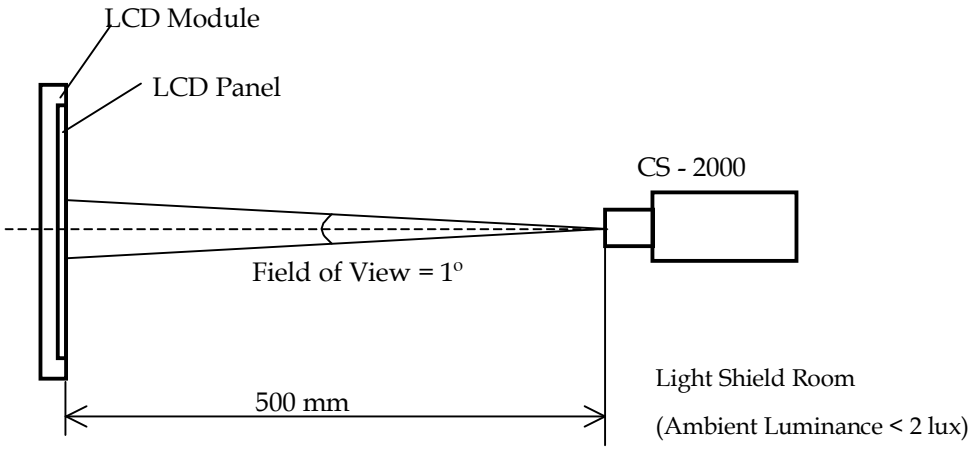
Note (6) Vcc must decay smoothly when power-off.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



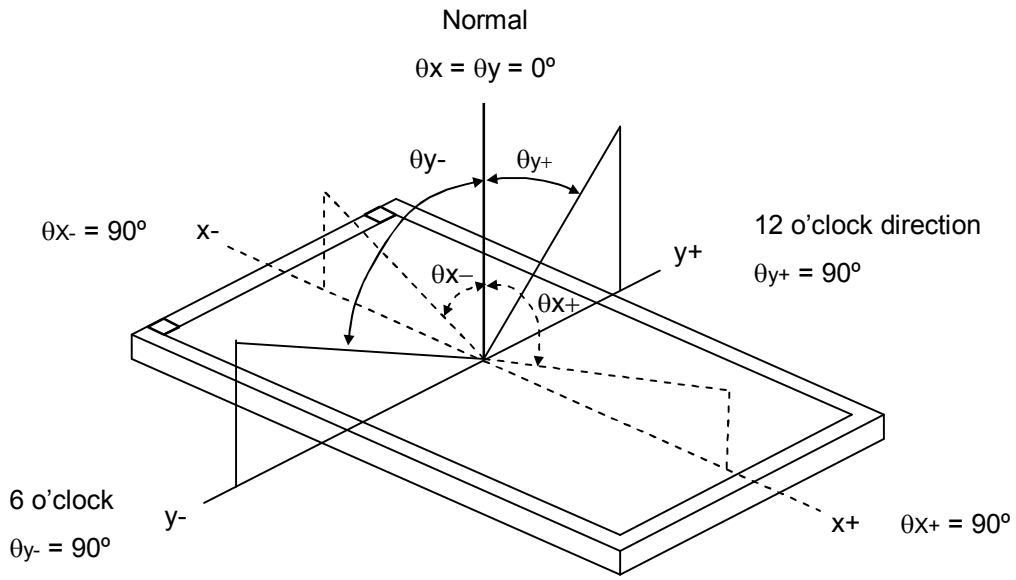
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θx=0°, θy =0° Viewing angle at normal direction	3500	5000		-	(2)
Response Time (VA)		Gray to gray			6.5	13	ms	(3)
Center Luminance of White		L_C		240	300		cd/m²	(4)
White Variation		δW				1.3	-	(6)
Cross Talk		CT				4	%	(5)
Color Chromaticity	Red	Rx		Typ. -0.03	0.638	Typ. +0.03	-	-
		Ry			0.333		-	
	Green	Gx			0.308		-	
		Gy			0.618		-	
	Blue	Bx			0.150		-	
		By			0.060		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Correlated color temperature			-	10000	-	K	-
	Color Gamut	C.G.		-	72	-	%	NTSC
Viewing Angle	Horizontal	θx+	CR≥20	80	88	-	Deg.	(1)
		θx-		80	88	-		
	Vertical	θy+		80	88	-		
		θy-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

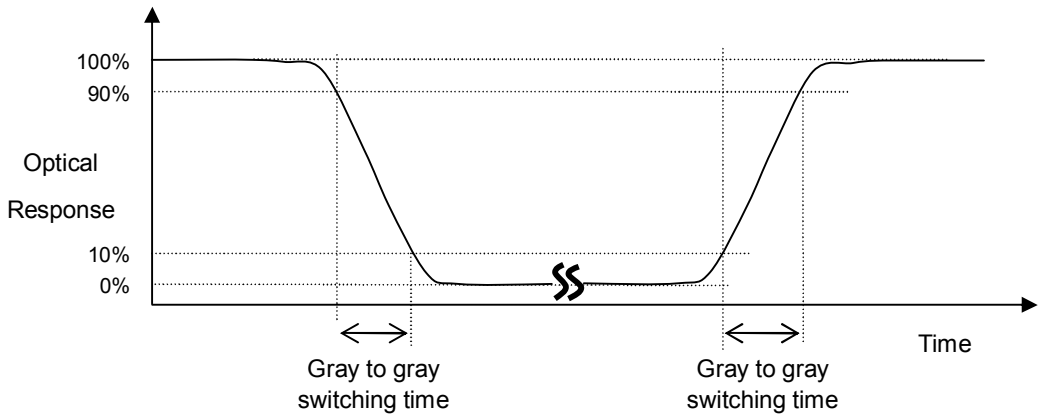
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255.

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}) :

Measure the luminance of gray level 255 at center point and 5 points

LC = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6).

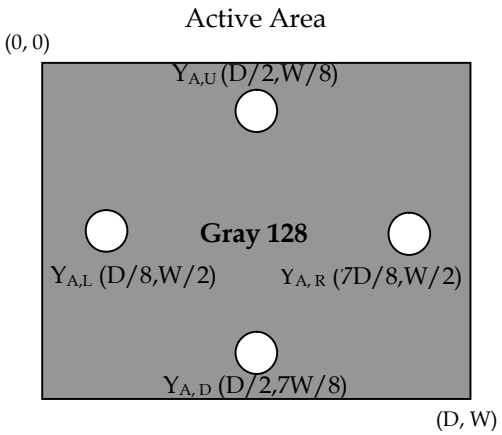
Note (5) Definition of Cross Talk (CT) :

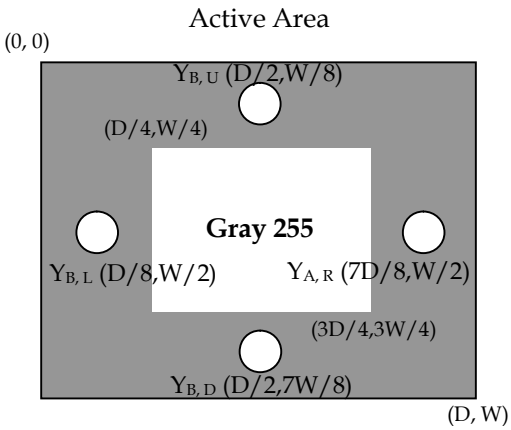
CT = | YB – YA | / YA × 100 (%)

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m2)

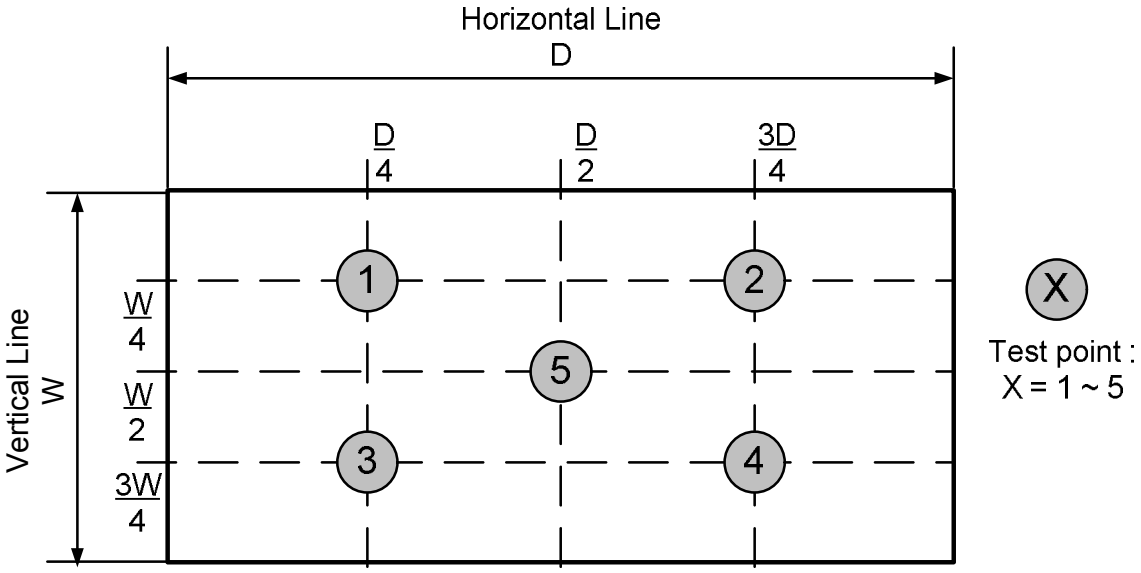




Note (6) Definition of White Variation (δW) :

Measure the luminance of gray level 255 at 5 points

$$\delta W = \frac{\text{Maximum [L (1), L (2), L (3), L (4), L (5)]}}{\text{Minimum [L (1), L (2), L (3), L (4), L (5)]}}$$



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

8.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006+ A11:2008

If the module displays the same pattern for a long period of time, the phenomenon of image sticking may be occurred.

9. DEFINITION OF LABELS

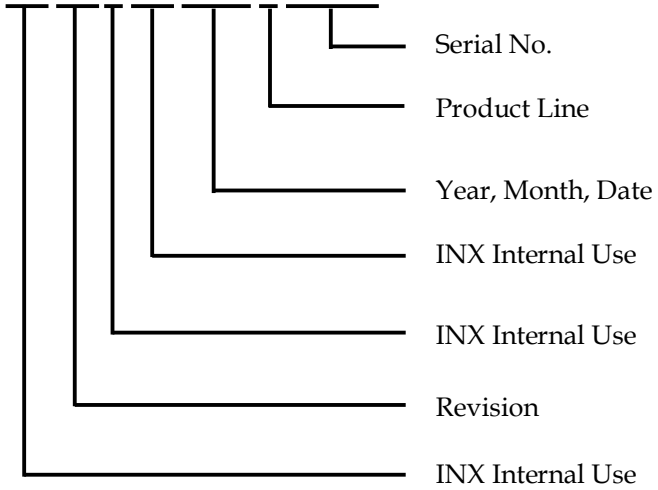
9.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

Model Name : V580HK1-LE6

Revision : Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID : X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

P.O. NO._____

Parts ID._____

Model Name V580HK1-LE6

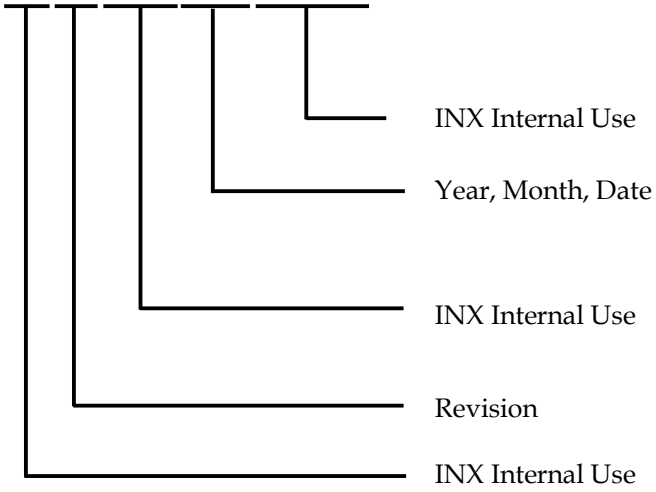
Carton ID._____ Quantities ___

XXXXXXXXXXXXX

Made In Taiwan (Made In China)

Model Name: V580HK1– LE6

Carton ID: X X X X X X X Y M D X X X X



Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS (type-A)

(1) 3 LCD TV modules / 1 Box

(2) Box dimensions: 1448(L) X 283 (W) X 846 (H)

(3) Weight: Approx. 59 Kg (3 modules per box)

10.2 PACKAGING METHOD(type-A)

Packaging method is shown as following figures.

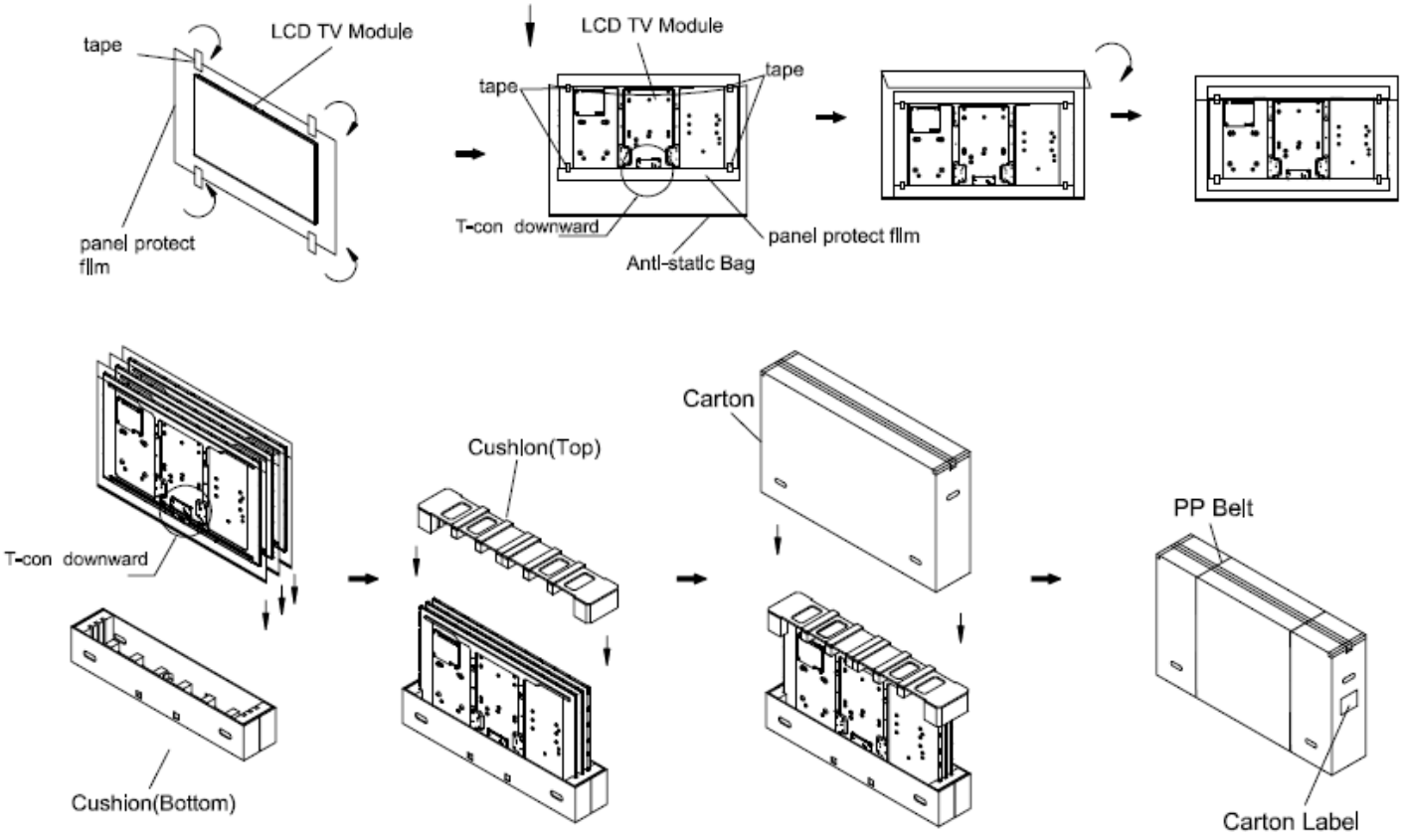


Figure 10-2 packing method (type-A)

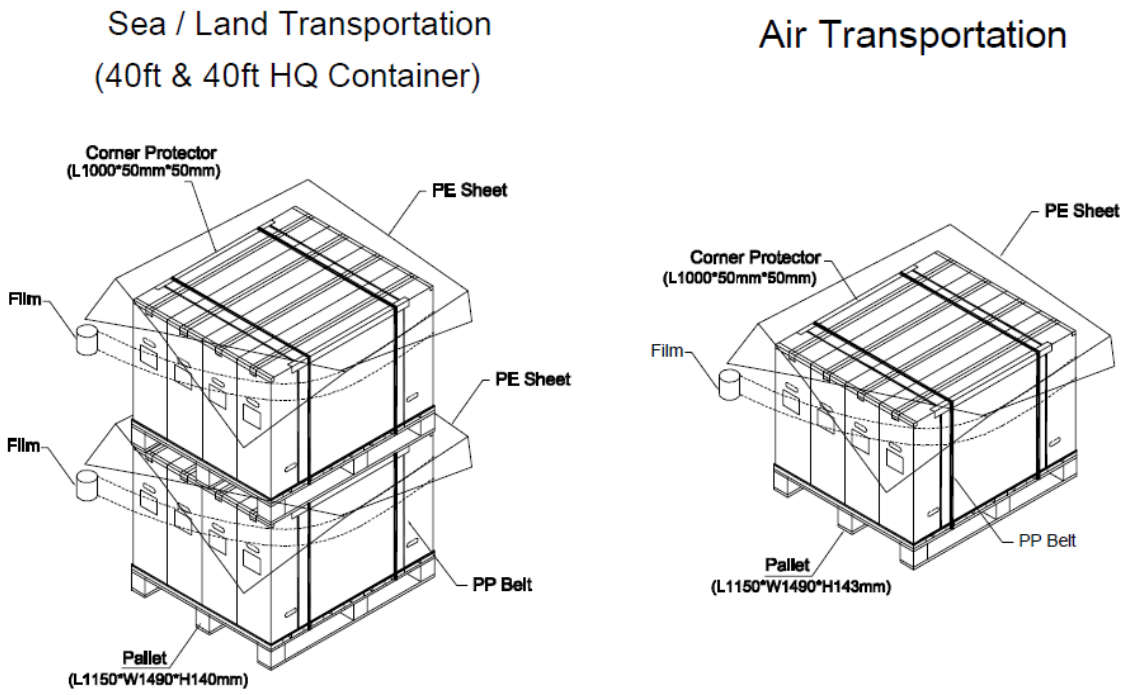


Figure 10-2 packing method (type-A)

10.3 UN-PACKING METHOD (type-A)

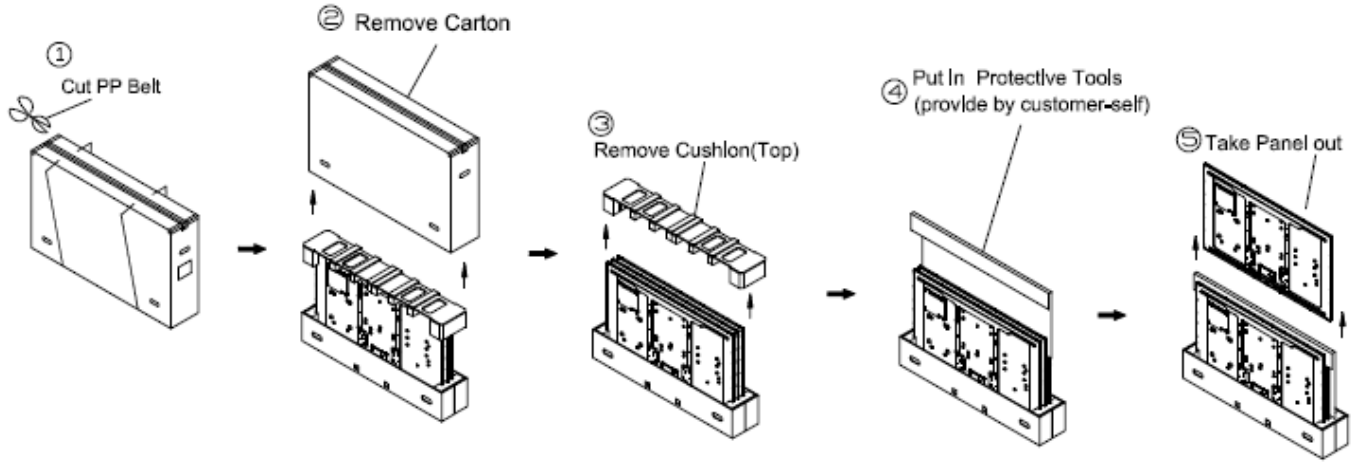


Figure 10-3 un-packing method (type-A)

10.4 PACKAGING SPECIFICATIONS (type-B)

(1) 20 LCD TV modules / 1 Box

(2) Box dimensions: 1448(L) X 1130 (W) X 855 (H)

(3) Weight: Approx. 440 Kg (20 modules per box)

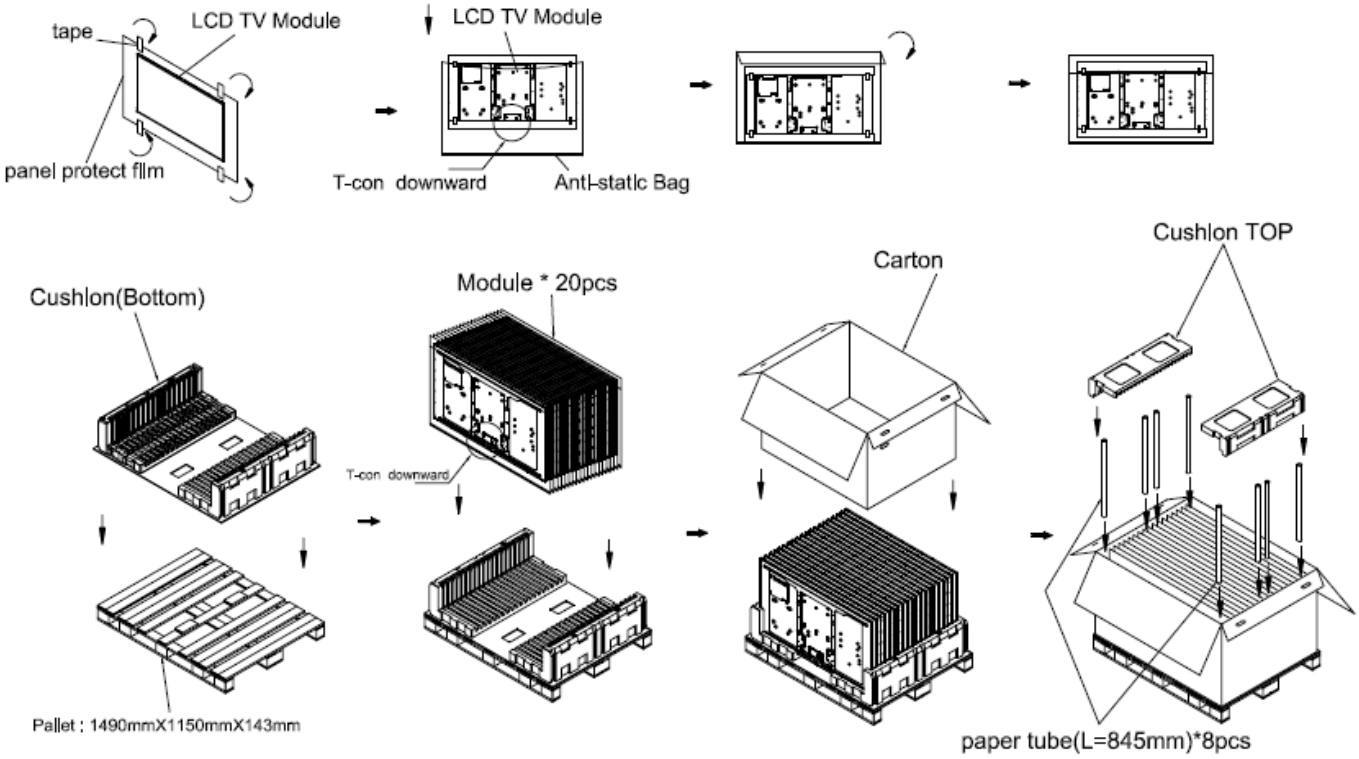


Figure 10-4 packing method (type-B)

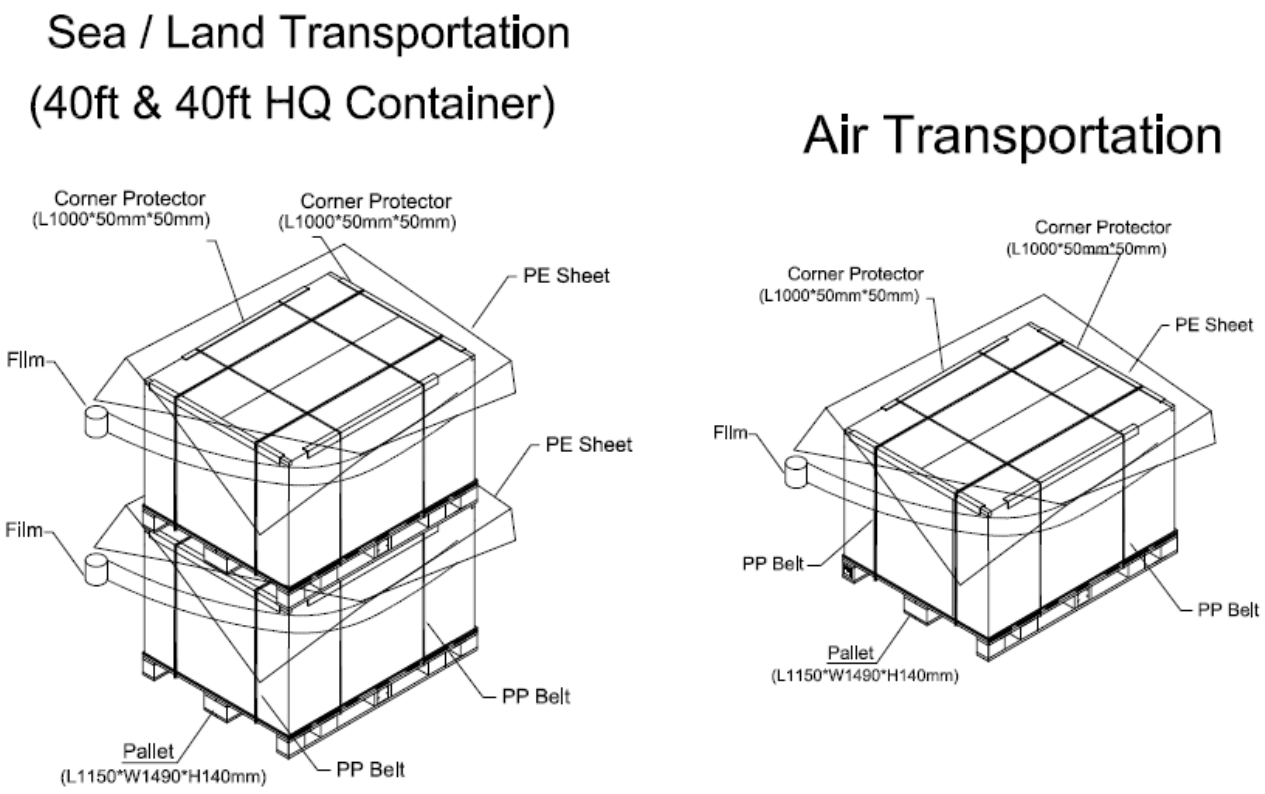


Figure 10-4 packing method (type-B)

10.5 UN-PACKING METHOD (type-B)

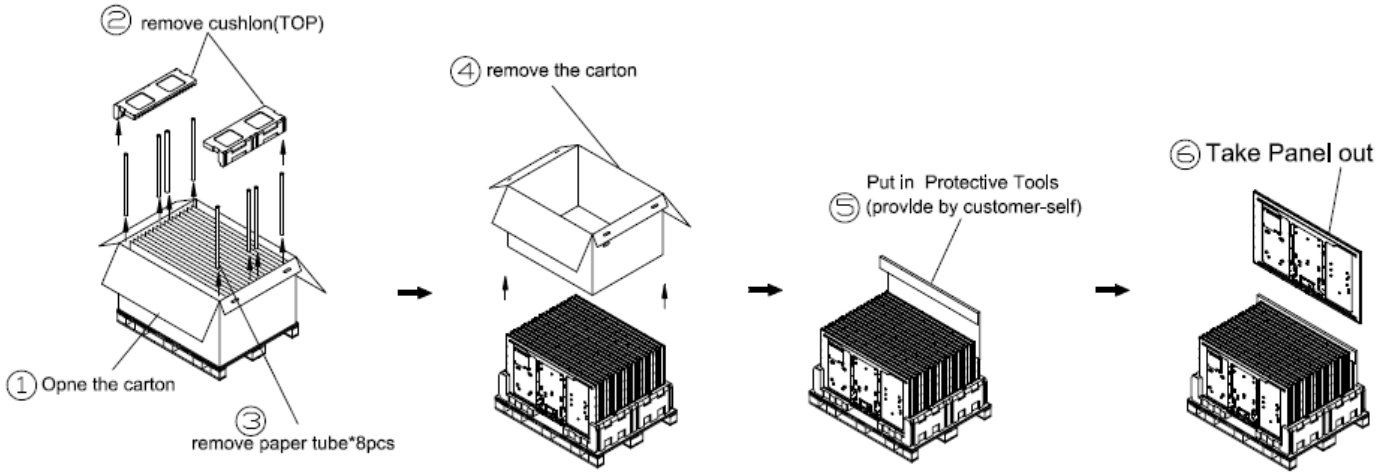
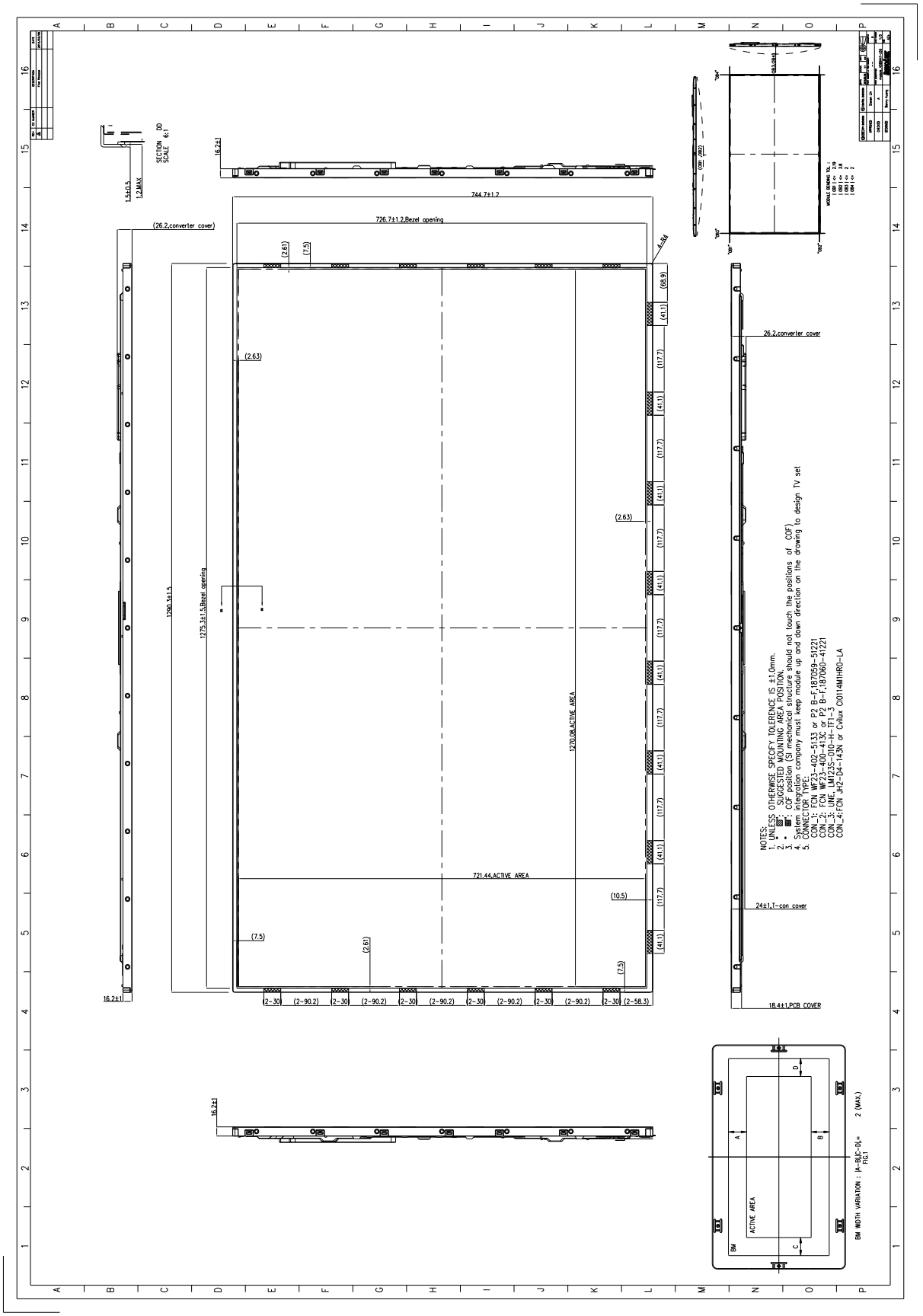
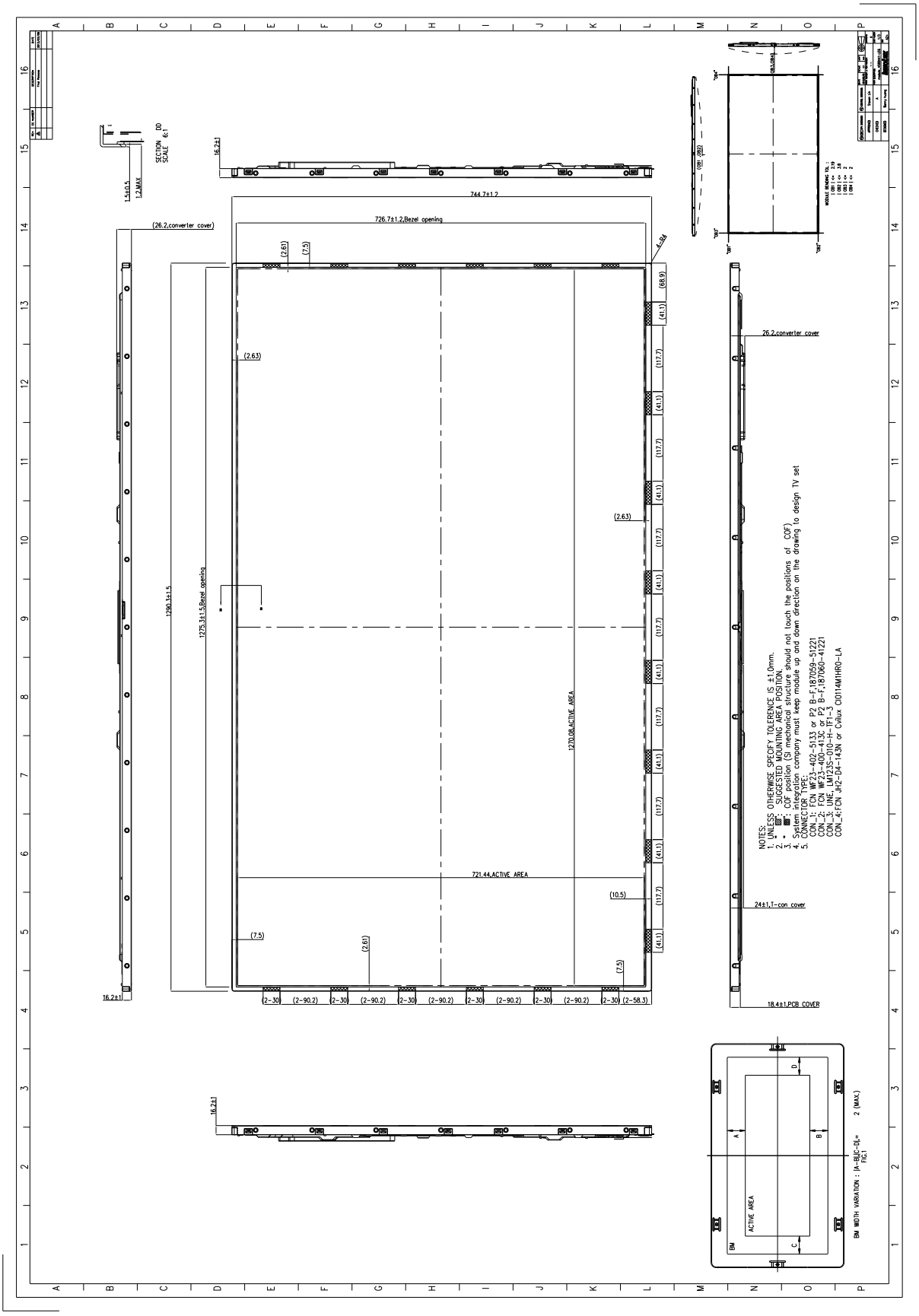
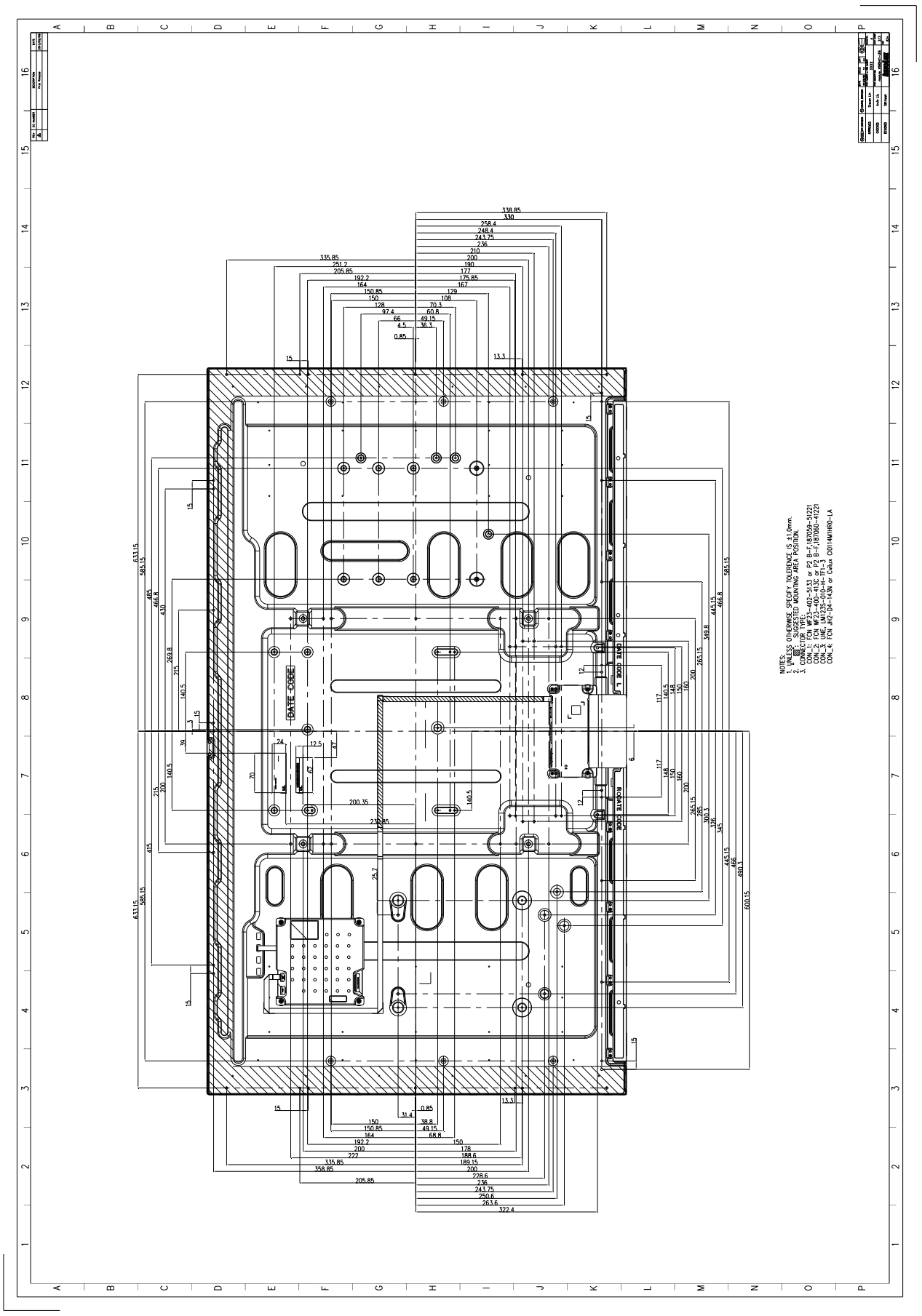


Figure 10-5 un-packing method (type-B)

11. MECHANICAL CHARACTERISTIC







Appendix A

Local Dimming demo function

A.1 I2C address and write command

Device address: 0xC2

Register address: 0x01

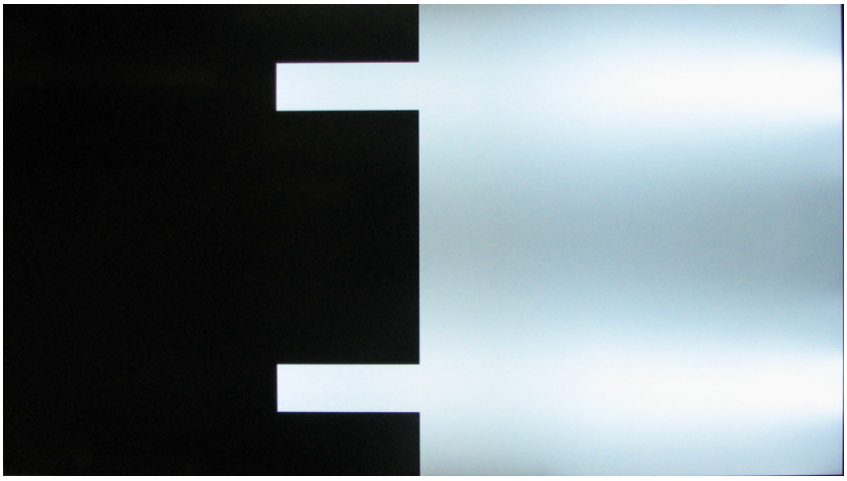
Command data: 0x00: Local Dimming demo mode OFF (Note 1)

0x01: Local Dimming demo mode ON (Demo in right half screen) (Note 2)

	Device Address		Register Address		Command Data		
START	11000010 (0xC2)	ACK	00000001 (0x01)	ACK	00000001 (0x01)	ACK	STOP

Note 1: Local Dimming demo OFF

Note 2: Local Dimming demo ON



A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns