



2, 4 and 8 Muxplex LCD Driver

Description

The V6118 is a universal low multiplex LCD driver. The version V6118 2 drives two ways multiplex (two blackplanes) LCD, the version V6118 4, four way multiplex LCD, and the V6118 8, eight way multiplex LCD. The display refresh is handled on chip via a 40 x 8 bit RAM which holds the LCD content driven by the driver. LCD pixels (or segments) are addressed on a one to one basis with the 40 x 8 bit RAM (a set bit corresponds to an activated LCD pixel). The V6118 has very low dynamic current consumption, 150 μ A max., making it particularly attractive for portable and battery powered applications. The wide operating range on both the logic (V_{DD}) and the LCD (V_{LCD}) supply voltages offers much application flexibility. The LCD bias generation is internal. The voltage bias levels can also be provided externally for applications having large pixels sizes. The V6118 can be used as a column only driver for cascading in large display applications. In the column only mode, 40 column outputs are available to address the display. A BLANK function is provided to blank the LCD, useful at power up to hold the display blank until the microprocessor has updated the display RAM.

Applications

- ☐ Balances and scales
- ☐ Automotive displays
- ☐ Utility meters
- ☐ Large displays (public information panel etc.)
- ☐ Pagers
- ☐ Portable, battery operated products
- ☐ Telephones

Features

- ☐ V6118 2 is 2 way multiplex with 2 rows and 38 columns
- ☐ V6118 4 is 4 way multiplex with 4 rows and 36 columns
- ☐ V6118 8 is 8 way multiplex with 8 rows and 32 columns
- ☐ Low dynamic current, 150 μ A max.
- ☐ Low standby current, 1 μ A max. at +25°C
- ☐ Voltage bias and mux signal generation on chip
- ☐ Display refresh on chip, 40 x 8 RAM for display storage
- ☐ Display RAM addressable as 8, 40 bits words
- ☐ Column driver only mode to have 40 column outputs
- ☐ Crossfree cascadable for large LCD applications
- ☐ Separate logic and LCD supply voltage pins
- ☐ Wide power supply range: V_{DD} : 2 to 6V, V_{LCD} : 2 to 8V
- ☐ BLANK function for LCD blanking on power up etc.
- ☐ Voltage bias inputs for applications with large pixel sizes
- ☐ Bit mapped
- ☐ Serial input / output
- ☐ Very low external component count
- ☐ -40 to + 85 °C temperature range
- ☐ No busy states
- ☐ LCD updating synchronized to the LCD refresh signal
- ☐ QFP52 and TAB packages

Typical Operating Configuration

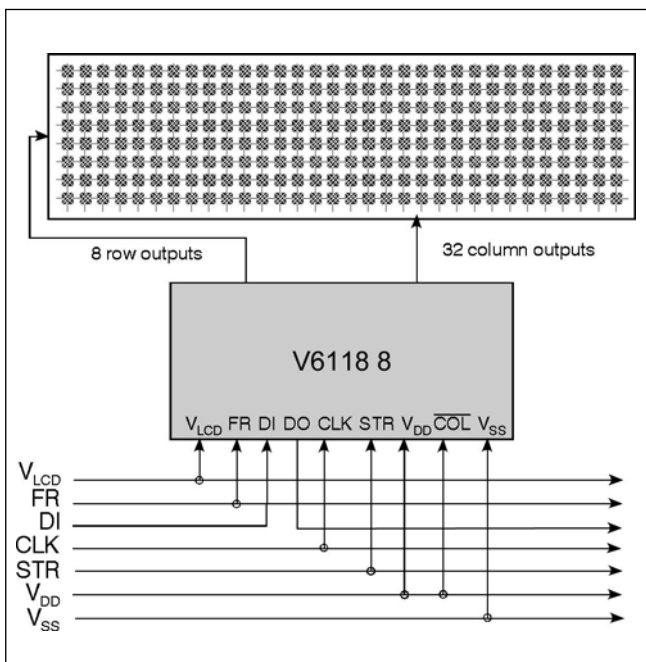


Fig. 1

Pad Assignment

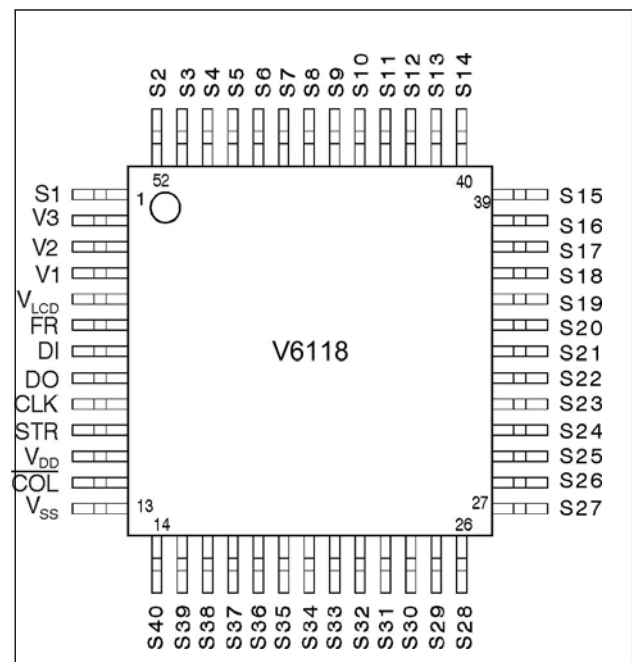


Fig. 2



Absolute Maximum Ratings

Parameter	Symbol	Conditions
Supply voltage range	V _{DD}	-0.3V to +8V
LCD supply voltage range	V _{LCD}	-0.3V to +9V
Voltage at DI, DO, CLK, STR, FR, COL	V _{LOGIC}	-0.3V to V _{DD} +0.3V
Voltage at V1 to V3, S1 to S40	V _{DISP}	-0.3V to V _{LCD} + 0.3V
Storage temperature range	T _{STO}	-65 to +150°C
Power dissipation	P _{MAX}	100mW
Electrostatic discharge max. to MIL-STD-883C method 3015.7 with ref. to V _{SS}	V _{SMAX}	1000V
Maximum soldering conditions	T _S	250°C x 10s

Table 1

Stresses above these listed maximum ratings may cause permanent damages to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component. Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _A	-40		+85	°C
Logic supply voltage	V _{DD}	2	5	6	V
LCD supply voltage	V _{LCD}	2	5	8	V

Table 2

Electrical Characteristics

V_{DD} = 5V ±10%, V_{LCD} = 2 to 7V and T_A = -40 to +85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Dynamic supply current	I _{LCD}	See note 1		100	170	μA
Dynamic supply current	I _{DD}	See note 1 at T _A = 25°C		0.1	1	μA
Dynamic supply current	I _{DD}	See note 1		3	12	μA
Dynamic supply current	I _{DD}	See note 2		200	280	μA
Standby supply current	I _{SS}	See note 3 at T _A = 25°C		0.1	1	μA
Control Signals DI, CLK, STR, FR and COL						
Input leakage	I _{IN}	0 < V _{IN} < V _{DD}		1	100	nA
Input capacitance	C _{IN}	at T _A = 25°C		8		pF
Low level input voltage	V _{IL}		0		0.8	V
High level input voltage for DI, STR, FR and COL	V _{IH}		2.0		V _{DD}	V
High level input voltage for CLK	V _{IH}		3.0		V _{DD}	V
Data Output DO						
High level output voltage	V _{OH}	I _H = 4 mA	2.4			V
Low level output voltage	V _{OL}	I _L = 4 mA			0.4	V
Driver Outputs S1 ... S40						
Driver impedance (note 4)	R _{OUT}	I _{OUT} = 10μA, V _{LCD} = 7V		0.5	1.5	kΩ
Driver impedance (note 4)	R _{OUT}	I _{OUT} = 10μA, V _{LCD} = 3V		1.2	2.5	kΩ
Driver impedance (note 4)	R _{OUT}	I _{OUT} = 10μA, V _{LCD} = 2V		9		kΩ
Bias impedance V1, V2, V3 (note 5)	R _{BIAS}	I _{OUT} = 10μA, V _{LCD} = 7V		16	20	kΩ
Bias impedance V1, V2, V3 (note 5)	R _{BIAS}	I _{OUT} = 10μA, V _{LCD} = 3V		18	25	kΩ
Bias impedance V1, V2, V3 (note 5)	R _{BIAS}	I _{OUT} = 10μA, V _{LCD} = 2V		30		kΩ
DC output component	± V _{DC}	see Tables 4a & 4b, V _{LCD} = 5V		30	50	mV

Table 3

Note 1: All outputs open, STR at V_{SS}, FR = 400 Hz, all other inputs at V_{DD}.

Note 2: All outputs open, STR at V_{SS}, FR = 400 Hz, f_{CLK} = 1 MHz, all other inputs at V_{DD}.

Note 3: All outputs open, all other inputs at V_{DD}.

Note 4: This is the impedance between of the voltage bias level pins (V1, V2 or V3) and the output pins S1 to S40 when a given voltage bias level is driving the outputs (S1 to S40)

Note 5: This is the impedance seen at the segment pin. Outputs measured one at a time.



Column Drivers

Outputs	FR Polarity	COL	Column Data	Measured*	Guaranteed
S1 to S40	logic 1	logic 0	logic 1	$Sx^* - V_{SS}$	$ V_{LCD} - Sx^* = Sx^* - V_{SS} \pm 25 \text{ mV}$
S1 to S40	logic 0	logic 0	logic 1	$V_{LCD} - Sx^*$	
S1 to S40	logic 1	logic 0	logic 0	$V_{LCD} - Sx^*$	$ V_{LCD} - Sx^* = Sx^* - V_{SS} \pm 25 \text{ mV}$
S1 to S40	logic 0	logic 0	logic 0	$Sx^* - V_{SS}$	

Table 4a

*Sx = the output number (ie. S1 to S40)

Row Drivers

Outputs	FR Polarity	COL	Column Data	Measured*	Guaranteed
S1 to Sn*	logic 1	logic 1	logic 1	$V_{LCD} - Sx$	$ V_{LCD} - Sx = Sx - V_{SS} \pm 25 \text{ mV}$
S1 to Sn*	logic 0	logic 1	logic 1	$Sx - V_{SS}$	
S1 to Sn*	logic 1	logic 1	logic 0	$Sx - V_{SS}$	$ V_{LCD} - Sx = Sx - V_{SS} \pm 25 \text{ mV}$
S1 to Sn*	logic 0	logic 1	logic 0	$V_{LCD} - Sx$	

Table 4b

*n = the V6118 version no. (ie. 2, 4 or 8)

Timing Characteristics

$V_{DD} = 5V \pm 10\%$, $V_{LCD} = 2 \text{ to } 8V$ and $T_A = -40 \text{ to } +85^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}	$C_{LOAD} = 50\text{pF}$	120			ns
Clock low pulse width	t_{CL}		120			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and FR fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		20 (note 1)			ns
Data input hold time	t_{DH}		30 (note 1)			ns
Data output propagation	t_{PD}				100	ns
STR pulse width	t_{STR}		100			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		200			ns
FR frequency (vers. 2/4/8)	F_{FR} (note 2)			128/256/512		Hz

Table 5a

Note 1: $t_{DS} + t_{DH}$ minimum must be $\geq 100 \text{ ns}$. If $t_{DS} = 20 \text{ ns}$ then $t_{DH} \geq 80 \text{ ns}$.

Note 2: V6118 n, FR = n times the desired LCD refresh rate where n is the V6118 version number.

$V_{DD} = 2 \text{ to } 6V$, $V_{LCD} = 2 \text{ to } 8V$ and $T_A = -40 \text{ to } +85^\circ\text{C}$

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Clock high pulse width	t_{CH}	$C_{LOAD} = 50\text{pF}$	500			ns
Clock low pulse width	t_{CL}		500			ns
Clock and FR rise time	t_{CR}				200	ns
Clock and RF fall time	t_{CF}				200	ns
Data input setup time	t_{DS}		100 (note 1)			ns
Data input hold time	t_{DH}		150 (note 1)			ns
Data output propagation	t_{PD}				400	ns
STR pulse width	t_{STR}		500			ns
CLK falling to STR rising	t_P		10			ns
STR falling to CLK falling	t_D		1			μs
FR frequency (Vers. 2/4/8)	F_{FR} (note 2)			128/256/512		Hz

Table 5b

Note 1: $t_{DS} + t_{DH}$ minimum must be $\geq 500 \text{ ns}$. If $t_{DS} = 100 \text{ ns}$ then $t_{DH} \geq 400 \text{ ns}$.

Note 2: V6118 n, FR = n times the desired LCD refresh rate where n is the V6118 version number.

Timing Waveforms

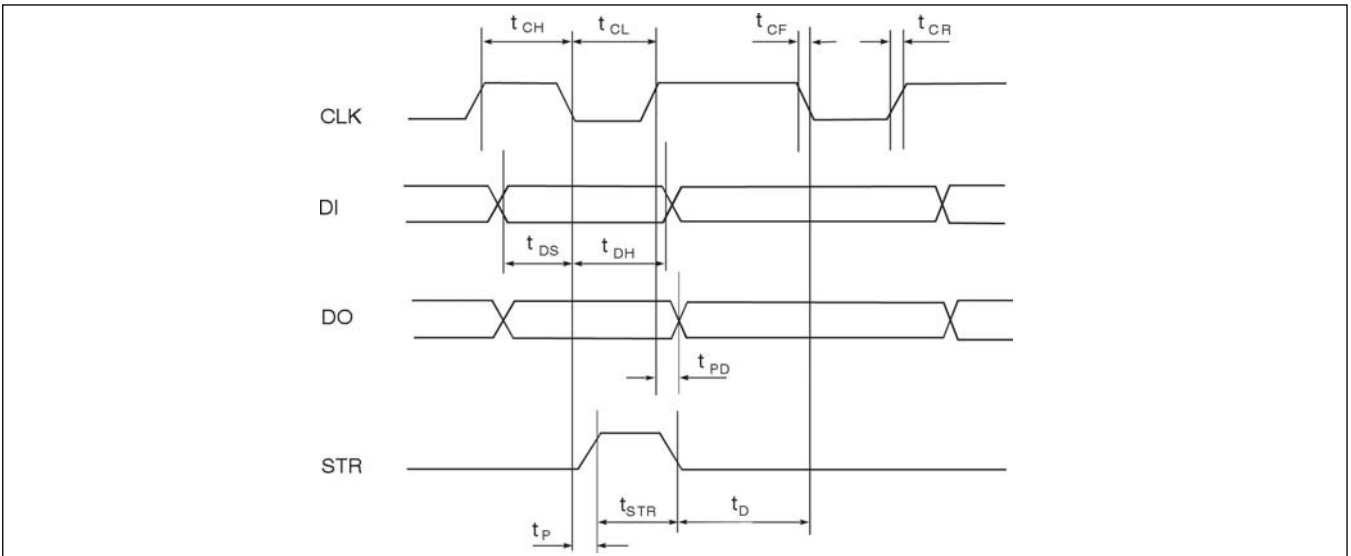


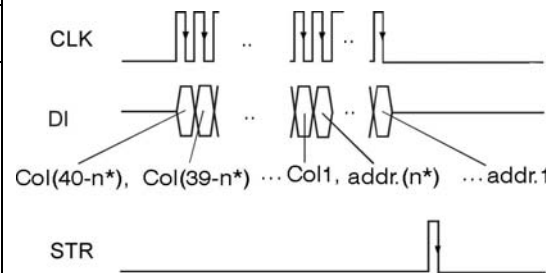
Fig. 3

V6118 Data Transfer Cycle, $\overline{COL}$ Inactive

Address Bits			Display RAM	
Addr. 1 to Addr. n*				
V6118 2	V6118 4	V6118 8	Address	LCD Row (Note1)
10	1000	10000000	10000000	Row 1
01	0100	01000000	01000000	Row 2
	0010	00100000	00100000	Row 3
	0001	00010000	00010000	Row 4
		00001000	00001000	Row 5
		00000100	00000100	Row 6
		00000010	00000010	Row 7
		00000001	00000001	Row 8

Note1: A set address bit corresponds to a write enabled RAM address, the same data can be written to more than one RAM address by setting the required address bits.

V6118 as a row and column driver ($\overline{COL}$ inactive) 40 bit load cycle, RAM address provided by address command bits 1 to (n*).



* n = the V6118 version number (i.e. 2,4, or 8)

Fig. 4

V6118 Data Transfer Cycle, $\overline{COL}$ Active

Address Bits			Display RAM	
Addr. 1 to Addr. 8				
V6118 2	V6118 4	V6118 8	Address	LCD Row (Note1)
10000000	10000000	10000000	10000000	Row 1
01000000	01000000	01000000	01000000	Row 2
	00100000	00100000	00100000	Row 3
	00010000	00010000	00010000	Row 4
		00001000	00001000	Row 5
		00000100	00000100	Row 6
		00000010	00000010	Row 7
		00000001	00000001	Row 8

Note1: A set address bit corresponds to a write enabled RAM address, the same data can be written to more than one RAM address by setting the required address bits.

V6118 as a column driver ($\overline{COL}$ active) 48 bit load cycle, RAM address provided by address command bits 1 to 8.

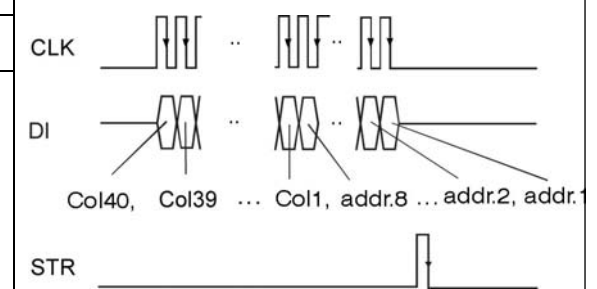


Fig. 5

Block Diagram

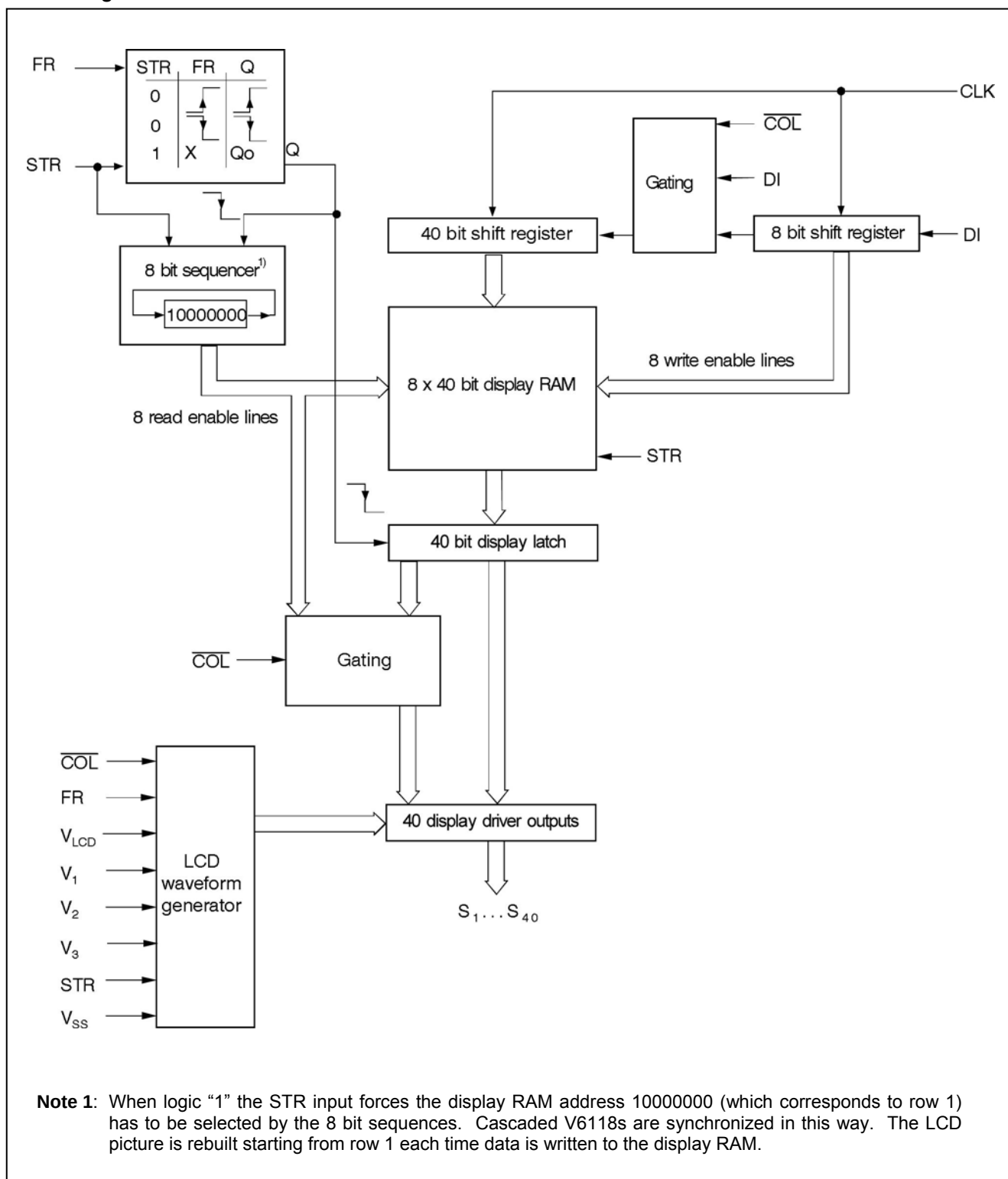


Fig. 6



V6118

Pin Assignment

Name	Function
S1..S40	LCD outputs, see Table 7
V3	LCD voltage bias level 3 (note 1, 2)
V2	LCD voltage bias level 2 (note 1)
V1	LCD voltage bias level 1 (note 1)
V _{LCD}	Power supply for the LCD
FR	AC input signal for LCD driver output
DI	Serial data input
DO	Serial data output
CLK	Data clock input
STR	Data strobe, blank, synchronize input
V _{DD}	Power supply for logic
$\overline{\text{COL}}$	Column only driver mode
V _{SS}	Supply GND

Table 9

Name	$\overline{\text{COL}}$ inactive			$\overline{\text{COL}}$ active
S1	V6118 (2) Row1	V6118 (4) Row1	V6118 (8) Row1	Col1
S2	Row2	Row2	Row2	Col2
S3	Col1	Row3	Row3	Col3
S4	Col2	Row4	Row4	Col4
S5	Col3	Col1	Row5	Col5
S6	Col4	Col2	Row6	Col6
S7	Col5	Col3	Row7	Col7
S8	Col6	Col4	Row8	Col8
S9...S40	Col7...38	Col5...36	Col1...32	Col9...40

Table 7

Note 1: The V6118 has internal voltage bias level generation. When driving large pixels, an external resistor divider chain can be connected to the voltage bias level inputs to obtain enhanced display contrast (see Fig. 12, 13 and 14). The external resistor divider ratio should be in accordance with the internal resistor ratio (see Table 8).

Note 2: V3 is connected internally on the V6118 4.

LCD Voltage Bias Levels

	LCD Drive Type	LCD Bias Configuration	$\frac{V_{OP}}{V_{OFF(rms)}}$ (note 1)	$\frac{V_{ON(rms)}}{V_{OFF(rms)}}$
	V6118 (2) n=2 1:2 MUX	Alt + Pleshko 5 levels	$\sqrt{\frac{2n}{1-\frac{1}{n}}} = 3.69$	$\sqrt{\frac{\sqrt{n}+1}{\sqrt{n}-1}} = 2.41$
	V6118 (4) n=4 1:4 MUX	1/3 Bias 4 Levels	3	$\sqrt{1+\frac{8}{n}} = 1.73$
	V6118 (8) n=8 1:8 MUX	1/4 Bias 5 Levels	$\frac{4}{\sqrt{1+\frac{3}{n}}} = 3.4$	$\sqrt{\frac{n+15}{n+3}} = 1.446$

Table 8

Note 1: $V_{OP} = V_{LCD} - V_{SS}$

Row and Column Multiplexing Waveform V6118 (2)

$$V_{OP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

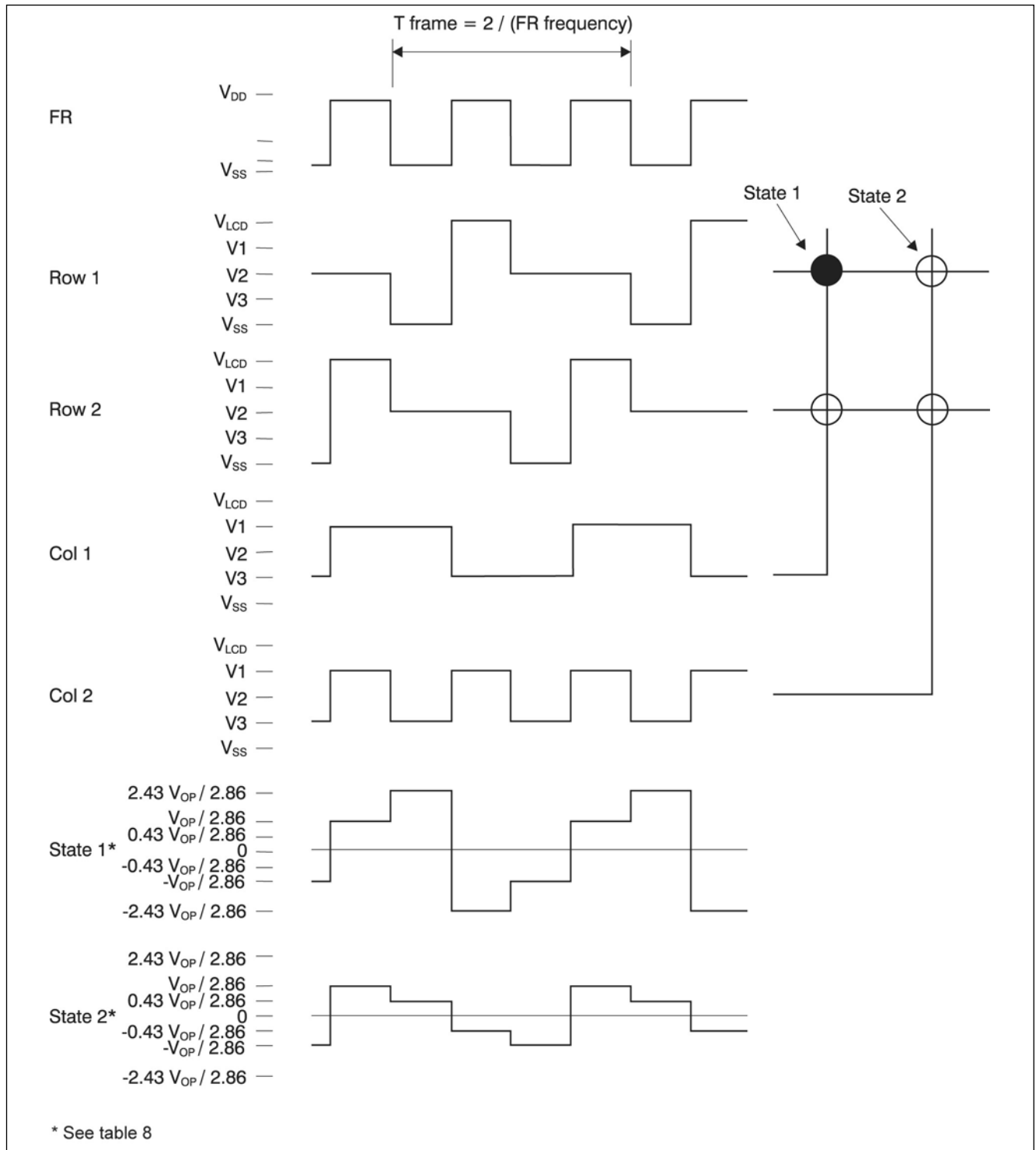


Fig. 7

Row and Column Multiplexing Waveform V6118 (4)

$$V_{OP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

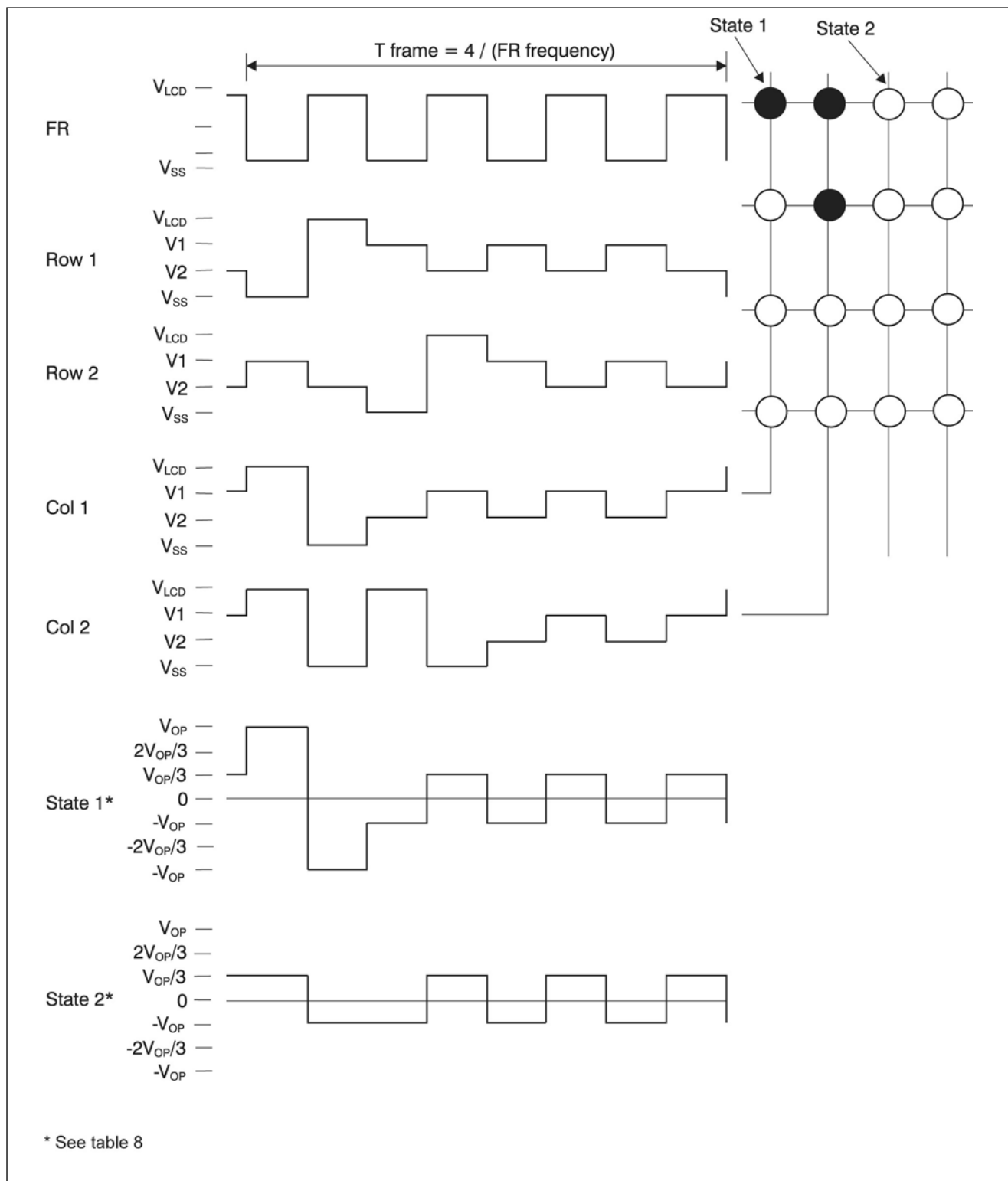


Fig. 8

Row and Column Multiplexing Waveform V6118 (8)

$$V_{OP} = V_{LCD} - V_{SS}, V_{STATE} = V_{COL} - V_{ROW}$$

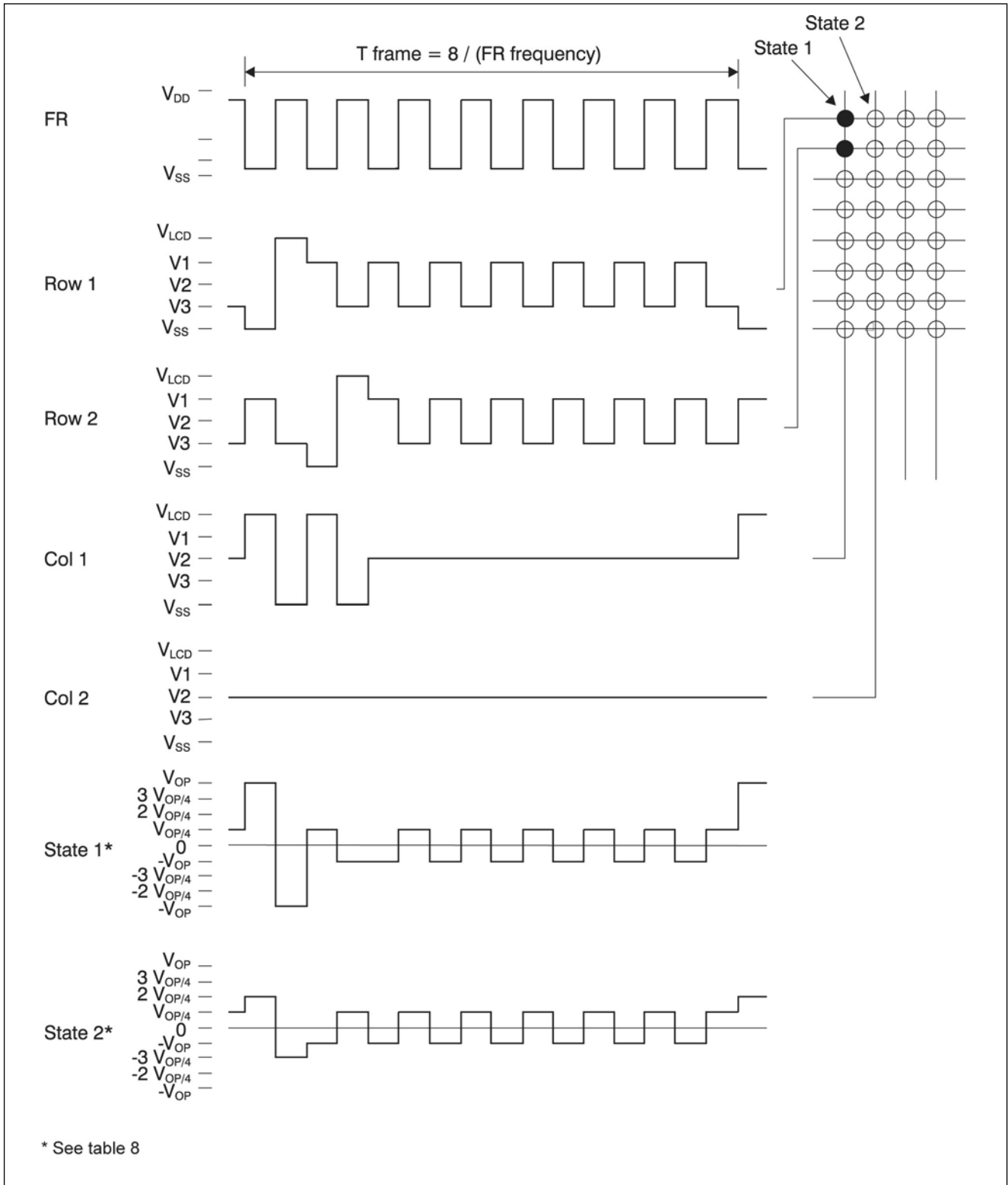


Fig. 9



Functional Description

Supply Voltage V_{LCD} , V_{DD} , V_{SS}

The voltage between V_{DD} and V_{SS} is the supply voltage for the logic and the interface. The voltage between V_{LCD} and V_{SS} is the supply voltage for the LCD and is used for the generation of the internal LCD bias levels. The internal LCD bias levels have a maximum impedance of 25 k Ω for a V_{LCD} voltage from 3 to 8V. Without external connections to the V1, V2, V3 bias level inputs, the V6118 can drive most medium sized LCD (pixel area up to 4'000 mm²).

For displays with a wide variation in pixel sizes, the configuration shown in Fig. 13 can give enhanced contrast by giving faster pixel switching times. On changing the row polarity (see Fig. 7, 8 and 9) the parallel capacitors lower the impedance of the bias level generation to the peak current, giving faster pixel charge times and thus a higher RMS "on" value. A higher RMS "on" value can give better contrast. IF for a given LCD size and operating voltage, the "off" pixels appear "on", or there is poor contrast, then an external bias level generation circuit can be used with the V6118. An external bias generation circuit can lower the bias level impedance and hence improve the LCD contrast (see Fig. 12). The optimum values of R, Rx and C, vary according to the LCD size used and V_{LCD} . They are best determined through actual experimentation with the LCD.

For LCD with very large average pixel area (eg. up to 10'000 mm²), the bias level configuration shown in Fig. 14 should be used.

When V6118s are cascaded, connect the V1, V2 and V3 bias inputs as shown in Fig. 10. The pixel load is averaged across all the cascaded drivers. This will give enhanced display contrast as the effective bias level source impedance is the parallel combination of the total number of drivers. For example, if two V6118 are cascaded as shown in Fig. 10, then the maximum bias level impedance becomes 12.5 k Ω for a V_{LCD} voltage from 3 to 8V.

Table 8 shows the relationship between V1, V2 and V3 for the multiplex rates 2, 4 and 8. Note that $V_{LCD} > V1 > V2 > V3$ for the V6118 2 and V6118 8, and for the V6118 4, $V_{LCD} > V1 > V2$.

Data Input /Output

The data input pin, DI, is used to load serial data into the V6118. The serial data word length is 40 bits when $\overline{COL}$ is inactive, and 48 bits when it is active. Data is loaded in inverse numerical order, the data for bit 40 (bit 48 when $\overline{COL}$ is active) loaded first with the data for bit 1 last. The column data bits are loaded first and then the address bits (see Fig. 4 & 5).

The data output pin, DO, is used in cascaded applications (see Fig. 10). DO transfers the data to the next cascaded chip. The data at DO is equal to the data at DI delayed by 40 clock periods, when $\overline{COL}$ is inactive and 48 clock periods when $\overline{COL}$ is active. In order to cascade V6118s, the DO of one chip must be connected to DI of the following chip (see Fig. 10). In cascaded applications the data for the last V6118 (the one that does not have DO connected) must be loaded first and the data for the first V6118 (its DI is connected to the processor) loaded last (see Fig. 10).

The display RAM word length is 40 bits (see Fig. 6). Each LCD row has a corresponding display RAM address which provides the column data (on or off) when the row is selected (on). When downloading data to the V6118, any display selected RAM address can be chosen, there is no

display RAM addressing sequence (see Fig.4 & 5). The same data can be written to more than one display RAM address. If more than one address bit is set, then more than one display RAM address is write enabled, and so the same data is written to more the one address. This feature can be useful to flash the LCD on and off under software control. If the address bits are all zero then no display RAM address is write enabled and no data is written to the display RAM on the falling edge of STR. Use address 0 to synchronize cascaded V6118s without updating the display RAM.

CLK Input

The CLK input is used to clock the DI serial data into the shift register and to clock the DO serial data out. Loading and shifting of the data occurs at the falling edge of this clock, outputting of the data at the rising edge (see Fig. 3). When cascading devices, all CLK lines should be tied together (see Fig. 10).

STR Input

The STR input is used to write to the display RAM, to blank the LCD, and synchronize cascaded V6118. The STR input writes the data loaded into the shift register, on the DI input, to the display selected RAM on the falling edge of the STR signal. The display RAM address is given by the address bits (see Fig. 4 & 5)

The STR input when high blanks the LCD by disconnecting the internal voltage bias generation from the V_{SS} potential. Segment outputs S1 to S40 (rows and columns) are pulled up to V_{LCD} . The delay to driving the LCD with V_{LCD} on S1 to S40, is dependent on the capacitive load of the LCD and is typically 1 μ s. An LCD pixel responds to RMS voltage and takes approximately 100 ms to turn on or off. The delay from putting STR high to the LCD being blank is dependent on the LCD off time and is typically 100 ms. In applications which have a long STR pulse width (10 μ s) the LCD is driven by V_{LCD} on both the rows and columns during this time. As the time is short (1 μ s), it will have zero measurable effect on the RMS "on" value (over 100 ms) of an LCD pixel and also zero measurable effect on the pixel DC component. Such STR pulses will not be visible to the human eye on an LCD.

Note: if an external voltage bias generation circuit is used as shown in Fig. 12 to 14, the LCD blank function (STR high) will not blank the LCD. When STR is high, the LCD will be driven by the parallel combination of the external voltage bias generation circuit and part of the internal voltage bias generation circuit.

The STR input, when high, synchronizes cascaded V6118s by forcing a new time frame to begin at the next falling edge of the FR input final (see Fig.6). A time frame begins with row 1 and so the LCD picture is rebuilt from row 1 each time cascaded V6118s are synchronized. When cascading devices, all STR lines must be tied together (see Fig. 10).

FR Input

The FR signal controls the segment output frequency generation (see Fig. 7, 8 and 9). To avoid having DC on the display, the FR signal must have a 50% duty cycle. The frequency of the FR signal must be n times the desired display refresh rate, where n is the V6118 version no. (2, 4 or 8). For example, if the desired refresh rate is 40 Hz, the FR signal frequency must be 320 Hz for the V6118 8. A selected row (on) is in phasewith the FR signal (see Fig. 7, 8 and 9).

It is recommended that data transfer to the V6118 should be synchronized to the FR signal to avoid a falling or rising edge on the FR signal while writing data to the V6118. The LCD pixels change polarity with the FR signal. On the edges of the FR signal current spikes will appear on the V_{SS} and V_{LCD} supply lines. If the supply lines have high impedance then voltage spikes will appear. These voltage spikes could interfere with data loading on the DI and CLK pins.

Driver Outputs S1 to S40

There are 40 LCD driver outputs on the V6118. When $\overline{COL}$ is inactive, the outputs S1 to Sn function as row drivers and the outputs S(n+1) to S40 function as column drivers, where n is the V6118 version no. (2, 4 or 8). When $\overline{COL}$ is active, all 40 outputs function as column drivers (see Table 6). There is a one to one relationship between the display selected RAM and the LCD driver outputs. Each pixel (segment) driven by the V6118 on the LCD has a display RAM bit which corresponds to it. Setting the bit turns the segment "on" and clearing it turns it "off".

$\overline{COL}$ Input

The V6118 functions as a row and column driver while the $\overline{COL}$ input is inactive. When active, the $\overline{COL}$ input configures the V6118 to function as a column driver only. The former row outputs function as column outputs. In cascaded applications, one V6118 should be used in the row and column configuration ($\overline{COL}$ inactive) and the rest as pure column drivers ($\overline{COL}$ active) (see Fig. 10).

Note: when cascading V6118s never cascade one version with another. If a V6118 8 is used to drive the rows, then only V6118 8 can be cascaded with it. When $\overline{COL}$ is active the V6118 needs 48 bits of data in a load cycle. 40 bits are used for the column data and 8 bits to address the display RAM regardless of V6118 versions (2, 4 or 8) (see Fig. 4, 5 and 10)

Power Up

On power up the data in the shift registers, the two display RAMs and the 40 bit display latches are undefined. The STR input should be taken high on power up to blank the display, then the display data written to the display selected RAM (see Fig. 11). When finished the initial write to the display selected RAM, take the STR input low to display the display selected RAM contents (see also section "STR Input").

Applications

Two V6118 8s Cascaded

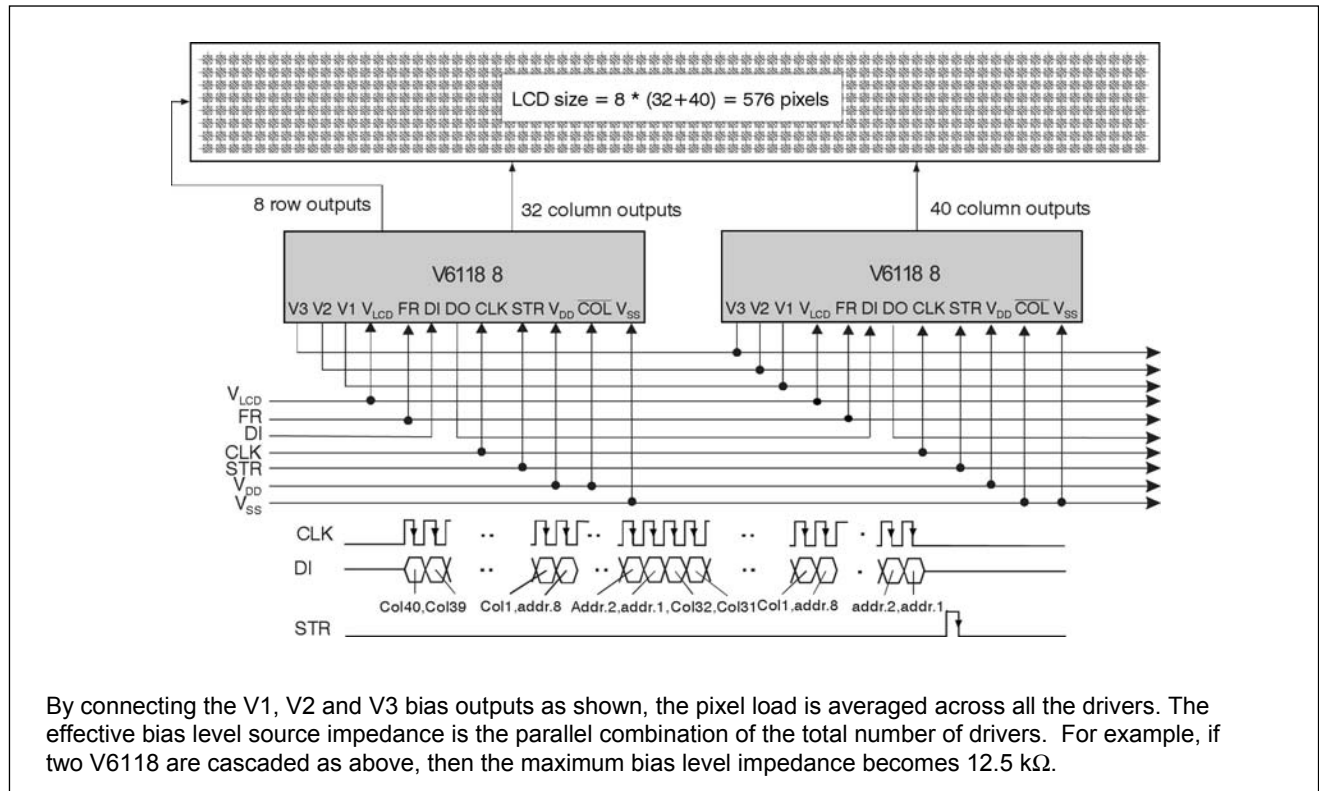


Fig. 10

The diagram illustrates the hardware configuration for the V6118 receiver module. It features three main components:

- 8051 Microcontroller:** Labeled "(Mode 0)", it has pins for RXD, TXD, P2.x, and RESET.
- Oscillator:** A block labeled "Oscillator" providing a "50% duty cycle" signal connected to the FR pin of the V6118.
- V6118 Receiver Module:** A grey-shaded block with pins DI, CLK, STR, and FR.

The connections are as follows:

- The **RESET** pin of the 8051 is connected to the **FR** pin of the V6118.
- The **P2.x** pin of the 8051 is connected to the **STR** pin of the V6118.
- A pull-up resistor, indicated by a box symbol and labeled "1)", connects the **P2.x** pin to the **V_{DD}** supply voltage.
- The **CLK** pin of the V6118 is connected to the **TXD** pin of the 8051.
- The **DI** pin of the V6118 is connected to the **RXD** pin of the 8051.
- An external **Oscillator** provides a "50% duty cycle" signal to the **FR** pin of the V6118.

-
- The timing diagram shows three signals: CLK (clock), DI (data input), and STR (store enable). The CLK signal is a periodic square wave. The DI signal shows data being written to memory, with labels Col32, Col31, Col 1, addr.8, addr.2, and addr.1 indicating the data bus width and address. The STR signal is a pulse that occurs during the store operation. The diagram illustrates the relationship between the clock, data input, and store enable signals during a store operation.

The diagram illustrates the V6118 8 LCD module. The top portion shows a grid of 52 columns and 8 rows of pixels. The bottom portion shows the electrical connections. The module is powered by V_{DD} (V_{SS}) and V_{DD} (V_{LCD}). It has 8 row outputs and 52 column outputs. A temperature compensation / contrast adjustment circuit is shown, consisting of a variable resistor R_x and a capacitor C connected to V_{DD} and V_{SS} .

$$R_x = 4R ((V_{DISP}/V_{LCD})-1) = 10 - 30 \text{ k}\Omega$$

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Enhanced Switching from V6118

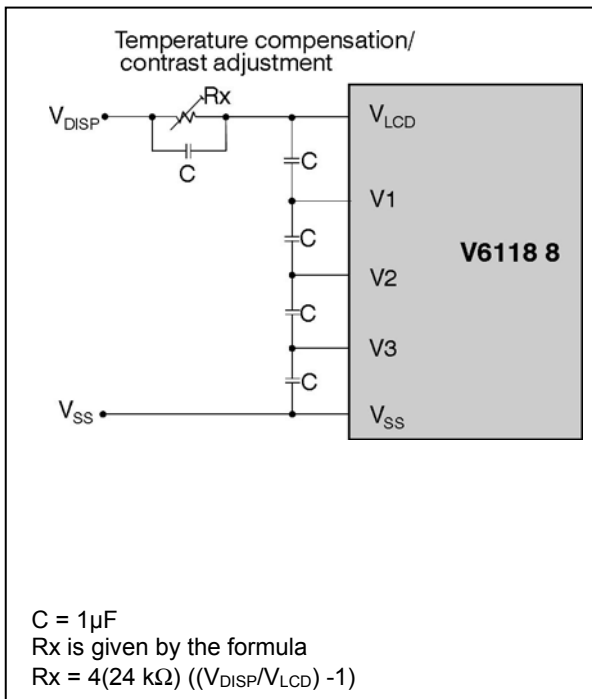


Fig.13

Bias configuration for a large LCD

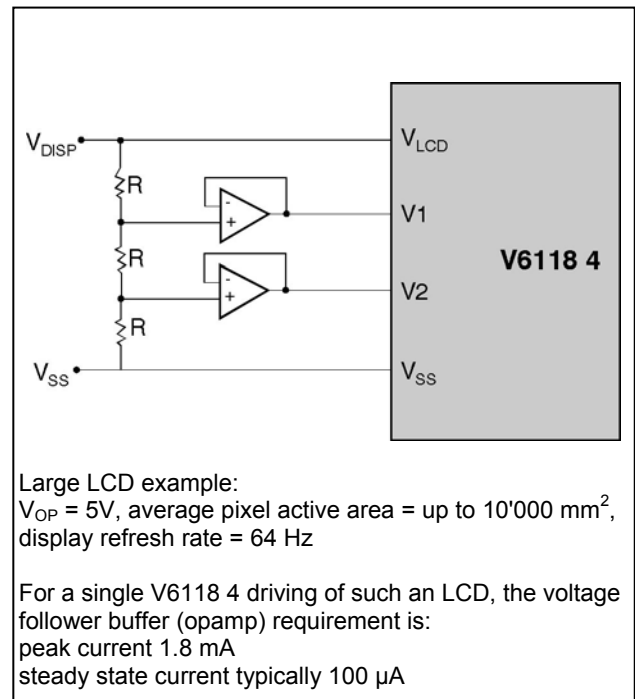


Fig.14

Package and Ordering Information

Dimensions of TAB Package

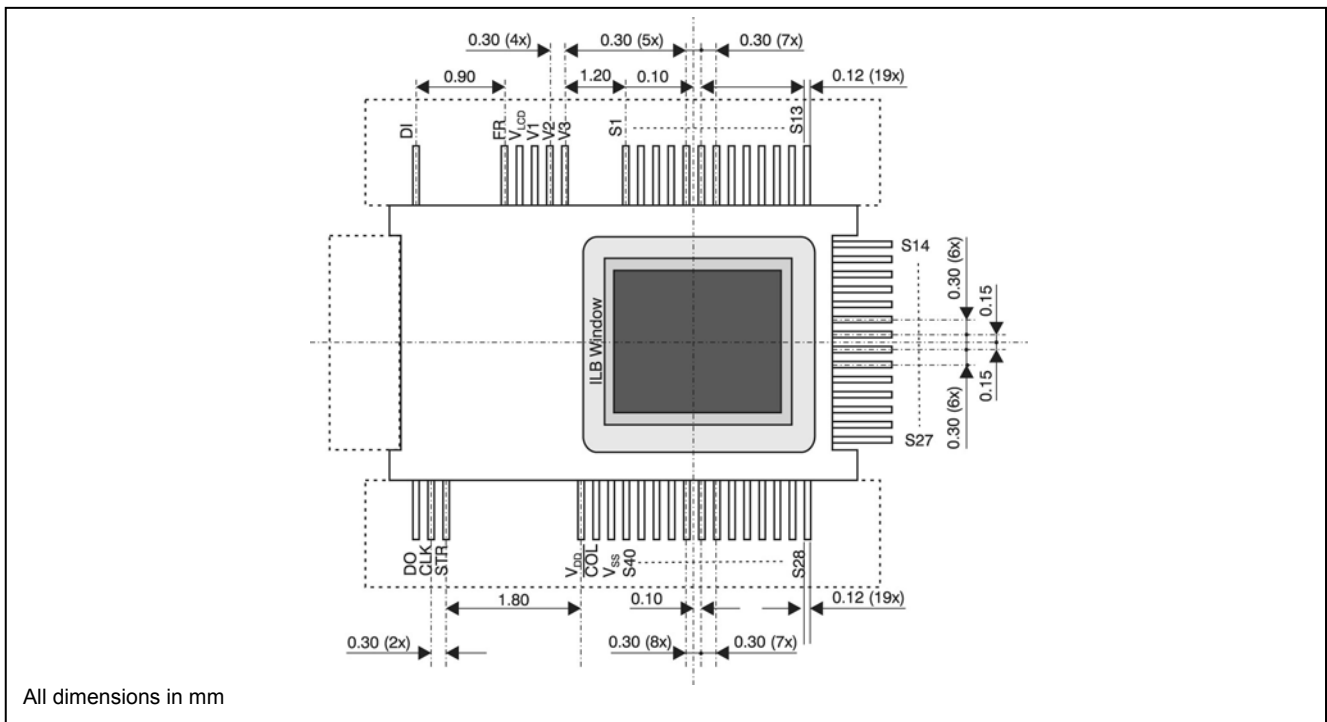


Fig.15

Dimensions of QFP Package

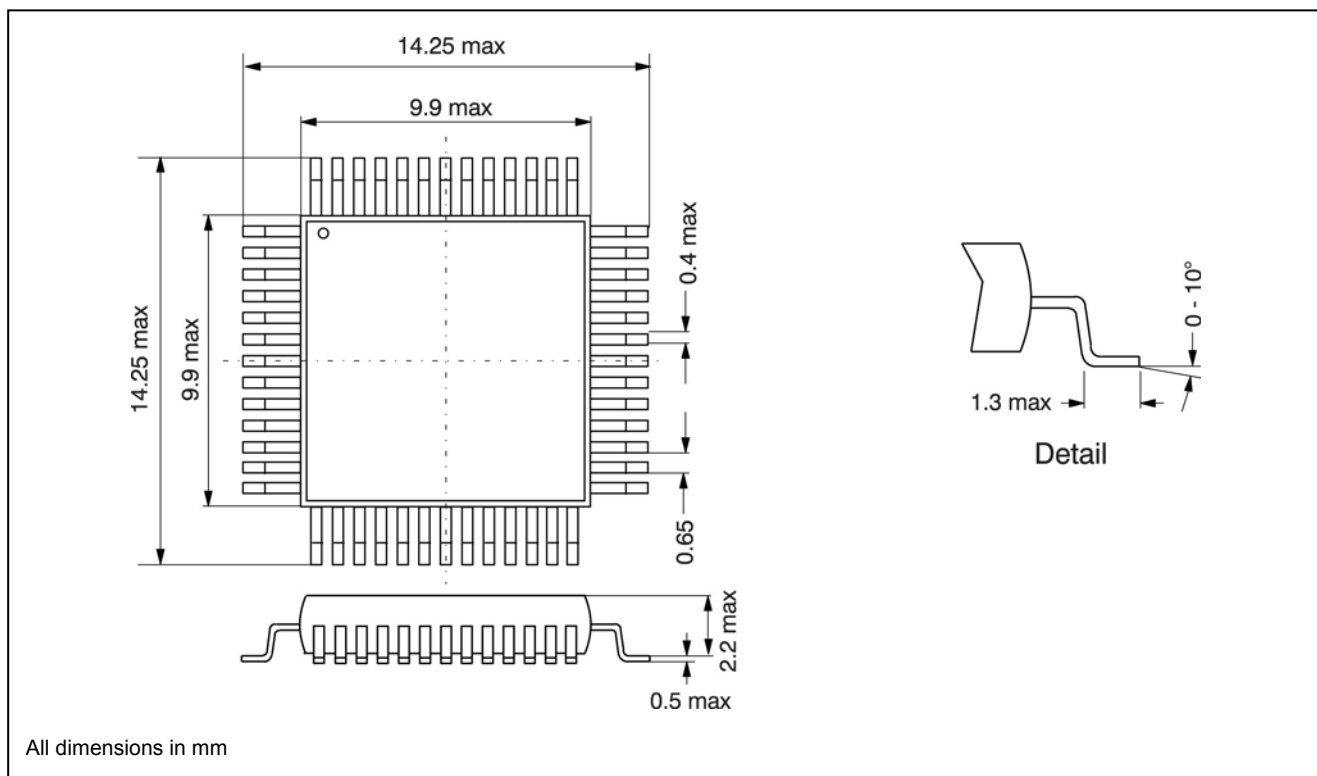


Fig.16



Package and Ordering Information

Dimensions of Chip Form

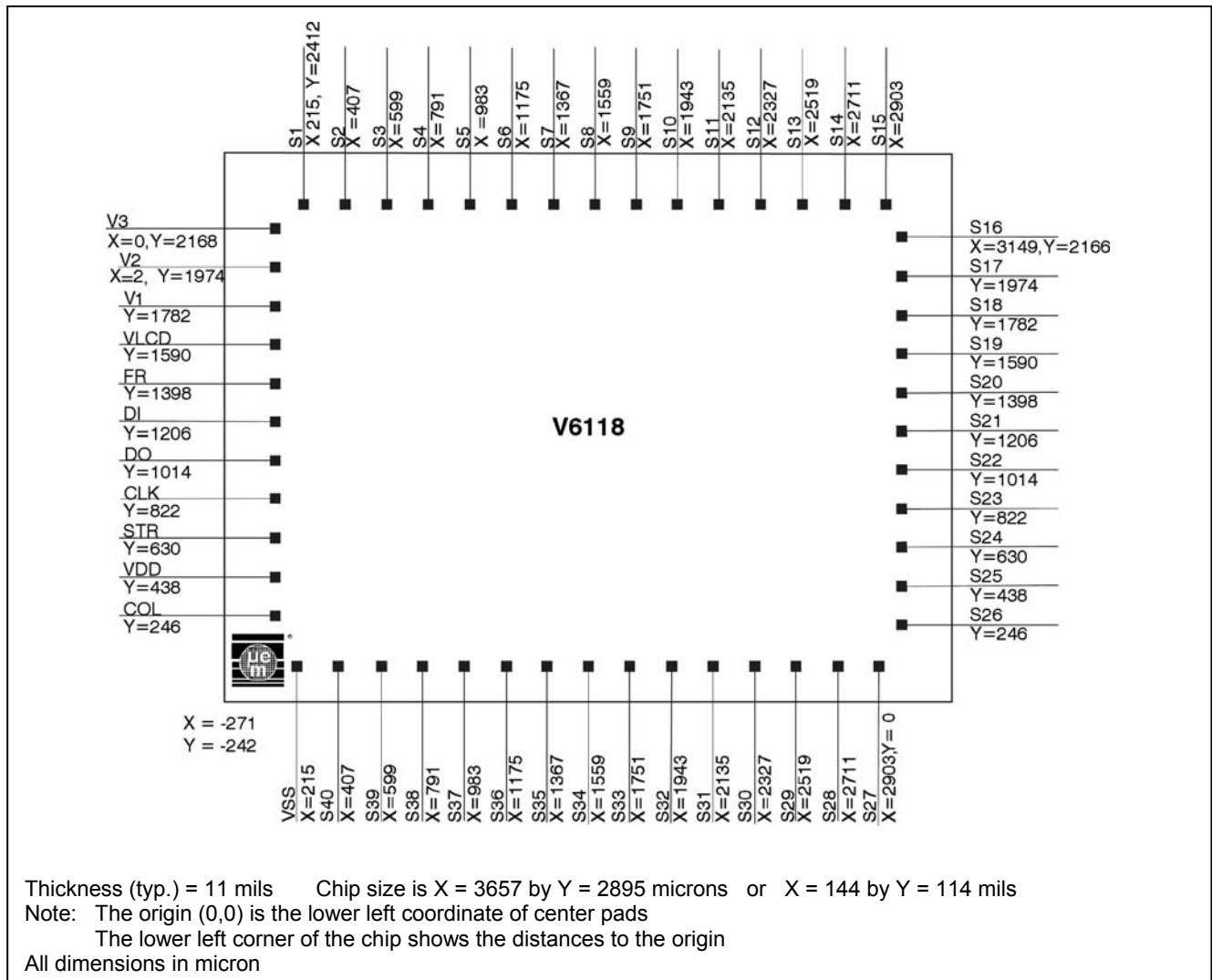


Fig. 17

Ordering Information

The V6118 is available in the following packages:

QFP52, pin plastic package	V6118 2 52F	Chip form	V6118 2 Chip*
	V6118 4 52F		V6118 4 Chip*
	V6118 8 52F		V6118 8 Chip*
TAB, tape automated bonding	V6118 2 TAB	*on request When ordering, please specify the complete part number and package	
	V6118 4 TAB		
	V6118 8 TAB		

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