

- Tentative Specification
- Preliminary Specification
- Approval Specification

MODEL NO.: V645H1
SUFFIX: PE1

Customer: SONY	
CONFIRMED BY	SIGNATURE
Name / Title _____	_____
APPROVED BY	SIGNATURE
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Note	
Please return 1 copy for your confirmation with your signature and comments.	

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REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	08 Apr ,2011	All	All	The approval specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V645H1-PE1 is a 64.5" TFT Liquid Crystal Display product with driver ICs and 6path- 6 pair mini-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 1G colors (10 bit/FRC). The backlight unit is not built in.

1.2 FEATURES

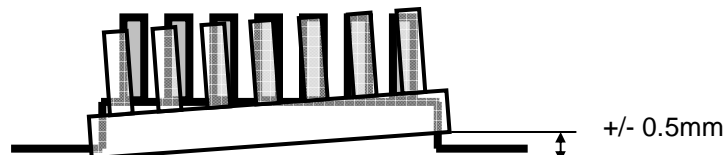
CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	64.5
Pixels [lines]	1920 x 1080
Active Area [mm]	1428.48 (H) x 803.52 (V) (64.5" diagonal)
Sub-Pixel Pitch [mm]	0.248(H) x 0.744(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 4760
Physical Size [mm]	1457.3 (H) x 830.35 (V) x 1.76(D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	5000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR ≥ 20) (Typical value measure at CMI's module)
Color Chromaticity	R = (0.656, 0.326) G = (0.261, 0.581) B = (0.131, 0.114) W = (0.290, 0.345) (Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages.)
Cell Transparency [%]	4.6% (Typical value measured at CMI's module)
Polarizer Surface Treatment Spec	Anti-Glare coating (Haze 11%) Hard coating (Hardness : 3H)
Polarizer Maker	Nitto

1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	-	4760	-	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

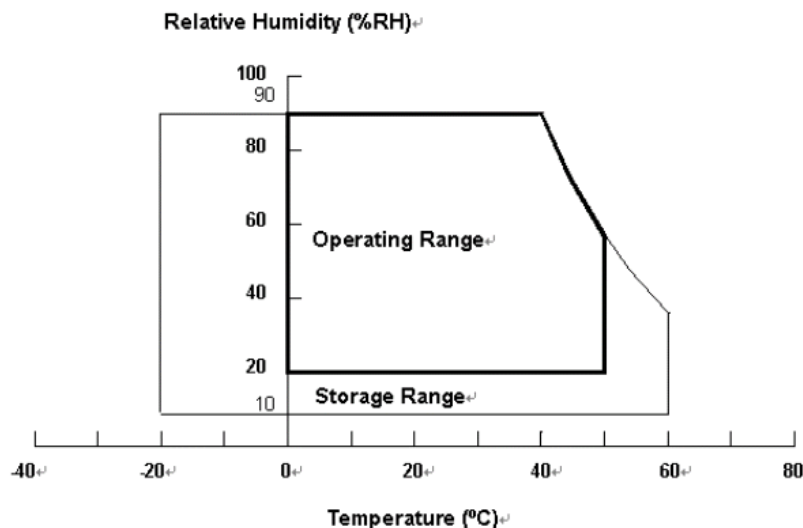
2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	°C	(1) With CMI Module
Operating Ambient Temperature	TOP	0	50	°C	(1), (2) With CMI Module

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ($T_a \leq 40 \text{ }^\circ\text{C}$).
- (b) Wet-bulb temperature should be 39 °C Max. ($T_a > 40 \text{ }^\circ\text{C}$).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Recommended Storage Condition: With shipping package.

Recommended Storage temperature range: 25±5 °C

Recommended Storage humidity range: 50±10%RH

Recommended Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD OPEN CELL

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Voltage for gate driver	VGH	-0.3	40	V	
Voltage for gate driver	VGL	-20	0.3	V	
Voltage range for gate driver	VGH - VGL	-0.3	43	V	
Voltage for data diver	VAA	12	18	V	
Logic Input Voltage	VIN	-0.3	5	V	

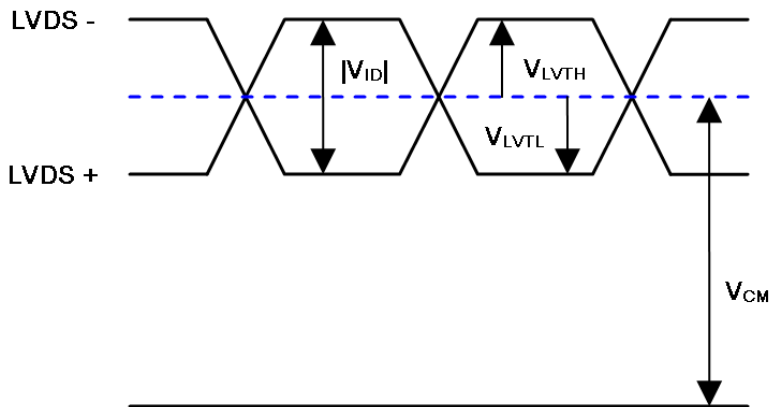
3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD OPEN CELL

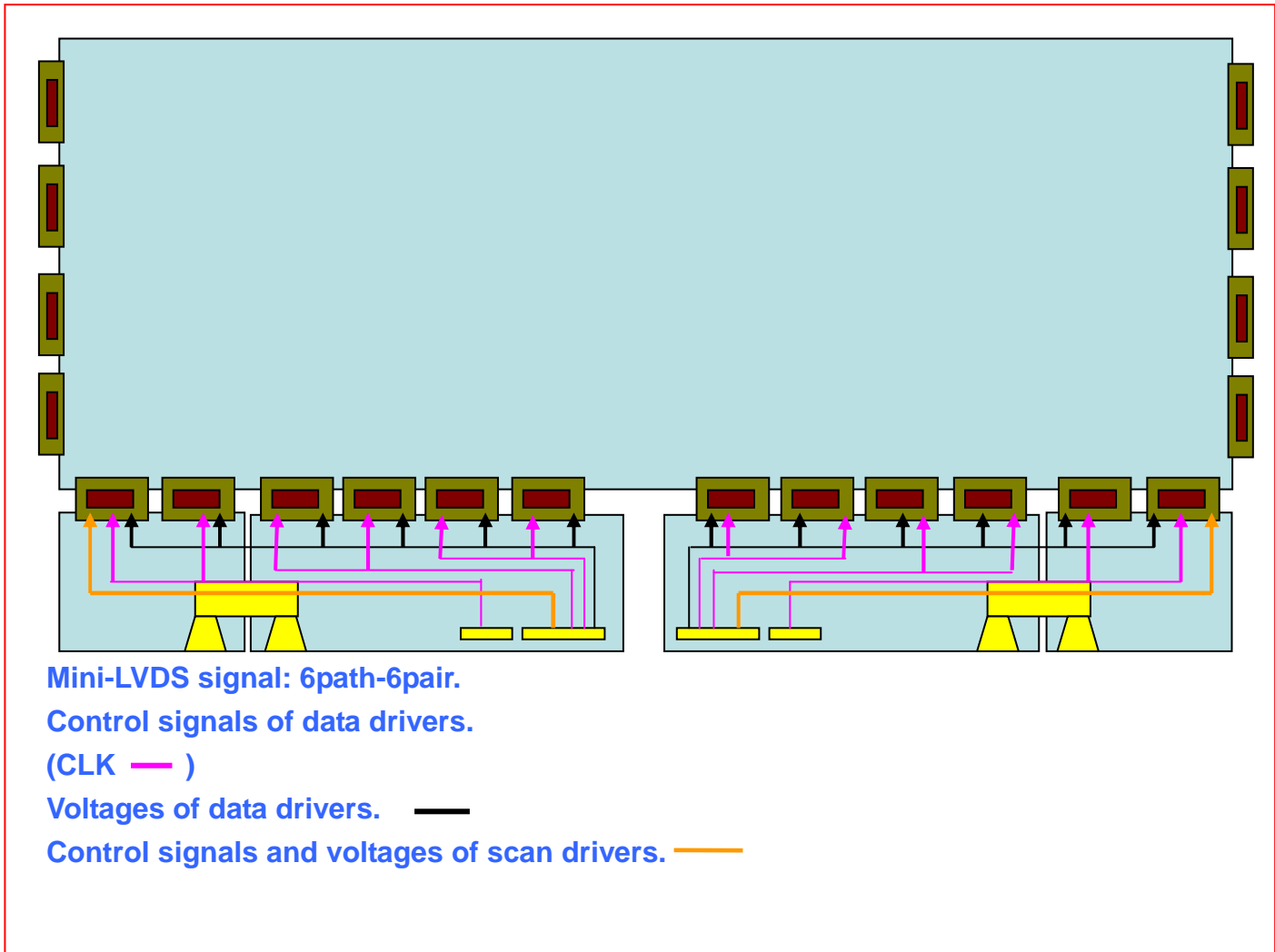
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Voltage for gate driver		VGH	29	30	31	V	
Voltage for gate driver		VGL	-7.7	-8	-8.3	V	
Voltage range for gate driver		VGH - VGL	36.7	38	39.3	V	
Voltage for data driver		VAA	17.4	17.7	18	V	
Voltage for data driver		VAAM	8.4	8.7	9.0	V	
Mini- LVDS interface	Differential Input High Threshold Voltage	V _{LVTH}	+100	—	—	mV	(1)
	Differential Input Low Threshold Voltage	V _{LVTL}	—	—	-100	mV	
	Common Input Voltage	V _{CM}	1.0	1.2	1.4	V	
	Differential input voltage	V _{ID}	200	—	600	mV	
	Terminating Resistor	R _T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V _{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V _{IL}	0	—	0.7	V	

Note (1) The Mini- LVDS input characteristics are as follows:



3.2 CIRCUIT AND WIRING DIAGRAM OF SPWB



3.3 SPWB INFORMATION

	Parts Name	Mt Yender	Manufacturer	Type	Flame Class	UL File
Source Board	Wiring, PCB for Source board (KL)	USI (Universal Scientific Industrial Corp.) TSMT (Alternative) (Taiwan Surface Mounting technology Corp.)	Dynamic	M0-V0 KM-V0	94V-0	E150630(TW) E255400((KunShan)
			Tripod (Alternative)	2-9	94V-0	E222034
			TPT (Alternative)	MV-0 MV-0S	94V-0	E88441
Source Board	Wiring, PCB for Source board (XR)	USI (Universal Scientific Industrial Corp.) TSMT (Alternative) (Taiwan Surface Mounting technology Corp.)	Dynamic	M0-V0 KM-V0	94V-0	E150630(TW) E255400((KunShan)
			Tripod (Alternative)	2-9	94V-0	E222034
			TPT (Alternative)	MV-0 MV-0S	94V-0	E88441
T-con Board	Wiring, PCB for TFT control board	USI (Universal Scientific Industrial Corp.) TSMT (Alternative) (Taiwan Surface Mounting technology Corp.)	Dynamic	M0-V0 KM-V0	94V-0	E150630(TW) E255400((KunShan)
			Tripod (Alternative)	2-9	94V-0	E222034
			TPT (Alternative)	MV-0 MV-0S	94V-0	E88441
	Parts Name	Manufacturer	Type	Flame Class	UL File	
FPC	Source COF(NT39810EH-C5225A)	Toray-Dupont	150EN		94V-0	E73117
	Gate COF(NT39555BH-C5229A)	Toray-Dupont	150EN		94V-0	E73117

4. INPUT TERMINAL PIN ASSIGNMENT

4.1 TFT LCD OPEN CELL

CN1 (XLL) Connector Pin Assignment : P-TWO 196318-80041-3

Pin	Name	Description	Note
1	GND	Ground	
2	MLA0P	Mini-LVDS data signal+	
3	MLA0N	Mini-LVDS data signal-	
4	MLA1P	Mini-LVDS data signal+	
5	MLA1N	Mini-LVDS data signal-	
6	MLA2P	Mini-LVDS data signal+	
7	MLA2N	Mini-LVDS data signal-	
8	GND	Ground	
9	MLCCKP	Mini-LVDS clock signal+	
10	MLCCKN	Mini-LVDS clock signal-	
11	GND	Ground	
12	MLA4P	Mini-LVDS data signal+	
13	MLA4N	Mini-LVDS data signal-	
14	MLA5P	Mini-LVDS data signal+	
15	MLA5N	Mini-LVDS data signal-	
16	MLA6P	Mini-LVDS data signal+	
17	MLA6N	Mini-LVDS data signal-	
18	GND	Ground	
19	GND	Ground	
20	VGH	Scan driver voltage	
21	VGH	Scan driver voltage	
22	GND	Ground	
23	VGL	Scan driver voltage	
24	VGL	Scan driver voltage	
25	GND	Ground	
26	OE1	Scan driver output enable	
27	OE2	Scan driver output enable	
28	CKV	Scan driver clock	
29	STV2	Scan driver start pulse	
30	PAIRMODE	Selects mini-LVDS input mode	
31	POL	Data driver polarity invert	
32	VDASEL	Half VAA selection	(1)
33	TP1	Data driver data latch	
34	CSTV	Scan driver start pulse	
35	GND	Ground	
36	GM18	Gamma voltage	
37	GM17	Gamma voltage	
38	GM16	Gamma voltage	
39	GM13	Gamma voltage	
40	GM12	Gamma voltage	
41	GM10	Gamma voltage	
42	GM9	Gamma voltage	
43	GM7	Gamma voltage	
44	GM6	Gamma voltage	
45	GM3	Gamma voltage	
46	GM2	Gamma voltage	
47	GM1	Gamma voltage	
48	GND	Ground	
49	VDD	Logic power	
50	VDD	Logic power	

51	GND	Ground	
52	VDDAM	Half VAA voltage	
53	VDDAM	Half VAA voltage	
54	GND	Ground	
55	VCM	VCOM voltage	
56	VCM	VCOM voltage	
57	GND	Ground	
58	VDDA	VAA voltage	
59	VDDA	VAA voltage	
60	GND	Ground	

CN1 (XLR) Connector Pin Assignment : P-TWO 196318-80041-3

Pin	Name	Description	Note
1	GND	Ground	
2	VDDA	VAA voltage	
3	VDDA	VAA voltage	
4	GND	Ground	
5	VCM	VCOM voltage	
6	VCM	VCOM voltage	
7	GND	Ground	
8	VDDAM	Half VAA voltage	
9	VDDAM	Half VAA voltage	
10	GND	Ground	
11	VDD	Logic power	
12	VDD	Logic power	
13	GND	Ground	
14	GM1	Gamma voltage	
15	GM2	Gamma voltage	
16	GM3	Gamma voltage	
17	GM6	Gamma voltage	
18	GM7	Gamma voltage	
19	GM9	Gamma voltage	
20	GM10	Gamma voltage	
21	GM12	Gamma voltage	
22	GM13	Gamma voltage	
23	GM16	Gamma voltage	
24	GM17	Gamma voltage	
25	GM18	Gamma voltage	
26	GND	Ground	
27	CSTV	Scan driver start pulse	
28	TP1	Data driver data latch	
29	VDASEL	Half VAA selection	(1)
30	POL	Data driver polarity invert	
31	PAIRMODE	Selects mini-LVDS input mode	
32	STV2	Scan driver start pulse	
33	CKV	Scan driver clock	
34	OE2	Scan driver output enable	
35	OE1	Scan driver output enable	
36	GND	Ground	
37	VGL	Scan driver voltage	
38	VGL	Scand driver voltage	
39	GND	Ground	
40	VGH	Scan driver voltage	
41	VGH	Scan driver voltage	
42	GND	Ground	

43	GND	Ground	
44	MLA6N	Mini-LVDS data signal-	
45	MLA6P	Mini-LVDS data signal+	
46	MLA5N	Mini-LVDS data signal-	
47	MLA5P	Mini-LVDS data signal+	
48	MLA4N	Mini-LVDS data signal-	
49	MLA4P	Mini-LVDS data signal+	
50	GND	Ground	
51	MLACKN	Mini-LVDS clock signal-	
52	MLACKP	Mini-LVDS clock signal+	
53	GND	Ground	
54	MLA2N	Mini-LVDS data signal-	
55	MLA2P	Mini-LVDS data signal+	
56	MLA1N	Mini-LVDS data signal-	
57	MLA1P	Mini-LVDS data signal+	
58	MLA0N	Mini-LVDS data signal-	
59	MLA0P	Mini-LVDS data signal+	
60	GND	Ground	

CN2 (XLR) Connector Pin Assignment : P-TWO 196225-80041

Pin	Name	Description	Note
1	MLC6N	Mini-LVDS data signal-	
2	MLC6P	Mini-LVDS data signal+	
3	MLC5N	Mini-LVDS data signal-	
4	MLC5P	Mini-LVDS data signal+	
5	MLC4N	Mini-LVDS data signal-	
6	MLC4P	Mini-LVDS data signal+	
7	GND	Ground	
8	MLCCKN	Mini-LVDS clock signal-	
9	MLCCKP	Mini-LVDS clock signal+	
10	GND	Ground	
11	MLC2N	Mini-LVDS data signal-	
12	MLC2P	Mini-LVDS data signal+	
13	MLC1N	Mini-LVDS data signal-	
14	MLC1P	Mini-LVDS data signal+	
15	MLC0N	Mini-LVDS data signal-	
16	MLC0P	Mini-LVDS data signal+	
17	GND	Ground	
18	MLB6N	Mini-LVDS data signal-	
19	MLB6P	Mini-LVDS data signal+	
20	MLB5N	Mini-LVDS data signal-	
21	MLB5P	Mini-LVDS data signal+	
22	MLB4N	Mini-LVDS data signal-	
23	MLB4P	Mini-LVDS data signal+	
24	GND	Ground	
25	MLBCKN	Mini-LVDS clock signal-	
26	MLBCKP	Mini-LVDS clock signal+	
27	GND	Ground	
28	MLB2N	Mini-LVDS data signal-	
29	MLB2P	Mini-LVDS data signal+	
30	MLB1N	Mini-LVDS data signal-	
31	MLB1P	Mini-LVDS data signal+	
32	MLB0N	Mini-LVDS data signal-	
33	MLB0P	Mini-LVDS data signal+	
34	GND	Ground	

35	STV2	Scan driver start pulse	
36	CSTV	Scan driver start pulse	
37	POL	Data driver polarity invert	
38	CKV	Scan driver clock	
39	TP1	Data driver data latch	
40	OE2	Scan driver output enable	
41	OE1	Scan driver output enable	
42	GND	Ground	
43	GM18	Gamma voltage	
44	GM17	Gamma voltage	
45	GM16	Gamma voltage	
46	NC	No connection	
47	NC	No connection	
48	GM13	Gamma voltage	
49	GM12	Gamma voltage	
50	NC	No connection	
51	GM10	Gamma voltage	
52	GM9	Gamma voltage	
53	NC	No connection	
54	GM7	Gamma voltage	
55	GM6	Gamma voltage	
56	NC	No connection	
57	NC	No connection	
58	GM3	Gamma voltage	
59	GM2	Gamma voltage	
60	GM1	Gamma voltage	
61	GND	Ground	
62	VDDA	VAA voltage	
63	VDDA	VAA voltage	
64	VDDA	VAA voltage	
65	GND	Ground	
66	VDDAM	Half VAA voltage	
67	VDDAM	Half VAA voltage	
68	GND	Ground	
69	VCM	VCOM voltage	
70	VCM	VCOM voltage	
71	GND	Ground	
72	VDD	Logic power	
73	VDD	Logic power	
74	GND	Ground	
75	VGL	Scan driver voltage	
76	VGL	Scan driver voltage	
77	GND	Ground	
78	VGH	Scan driver voltage	
79	VGH	Scan driver voltage	
80	VGH	Scan driver voltage	

CN3 (XLR) Connector Pin Assignment : Starconn B-F,089H55-000000-G2-R

Pin	Name	Description	Note
1	GND	Ground	
2	MLA6N	Mini-LVDS data signal-	
3	MLA6P	Mini-LVDS data signal+	
4	MLA5N	Mini-LVDS data signal-	
5	MLA5P	Mini-LVDS data signal+	
6	MLA4N	Mini-LVDS data signal-	

7	MLA4P	Mini-LVDS data signal+	
8	GND	Ground	
9	MLACKN	Mini-LVDS clock signal-	
10	MLACKP	Mini-LVDS clock signal+	
11	GND	Ground	
12	MLA2N	Mini-LVDS data signal-	
13	MLA2P	Mini-LVDS data signal+	
14	MLA1N	Mini-LVDS data signal-	
15	MLA1P	Mini-LVDS data signal+	
16	MLA0N	Mini-LVDS data signal-	
17	MLA0P	Mini-LVDS data signal+	
18	GND	Ground	
19	NC	No connection	
20	NC	No connection	
21	NC	No connection	
22	NC	No connection	
23	GND	Ground	
24	NC	No connection	
25	NC	No connection	
26	GND	Ground	
27	GND	Ground	
28	GND	Ground	
29	GND	Ground	
30	GND	Ground	
31	GND	Ground	
32	NC	No connection	
33	NC	No connection	
34	NC	No connection	
35	NC	No connection	
36	NC	No connection	
37	NC	No connection	
38	NC	No connection	
39	NC	No connection	
40	GND	Ground	
41	NC	No connection	
42	NC	No connection	
43	GND	Ground	
44	NC	No connection	
45	NC	No connection	
46	NC	No connection	
47	NC	No connection	
48	NC	No connection	
49	NC	No connection	
50	NC	No connection	
51	NC	No connection	
52	NC	No connection	
53	NC	No connection	
54	NC	No connection	
55	GND	Ground	

CN1 (XRR) Connector Pin Assignment : P-TWO 196318-80041-3

Pin	Name	Description	Note
1	GND	Ground	
2	VDDA	VAA voltage	
3	VDDA	VAA voltage	

4	GND	Ground	
5	VCM	VCOM voltage	
6	VCM	VCOM voltage	
7	GND	Ground	
8	VDDAM	Half VAA voltage	
9	VDDAM	Half VAA voltage	
10	GND	Ground	
11	VDD	Logic power	
12	VDD	Logic power	
13	GND	Ground	
14	GM1	Gamma voltage	
15	GM2	Gamma voltage	
16	GM3	Gamma voltage	
17	GM6	Gamma voltage	
18	GM7	Gamma voltage	
19	GM9	Gamma voltage	
20	GM10	Gamma voltage	
21	GM12	Gamma voltage	
22	GM13	Gamma voltage	
23	GM16	Gamma voltage	
24	GM17	Gamma voltage	
25	GM18	Gamma voltage	
26	GND	Ground	
27	CSTV	Scan driver start pulse	
28	TP1	Data driver data latch	
29	VDASEL	Half VAA selection	(1)
30	POL	Data driver polarity invert	
31	PAIRMODE	Selects mini-LVDS input mode	
32	STV2	Scan driver start pulse	
33	CKV	Scan driver clock	
34	OE2	Scan driver output enable	
35	OE1	Scan driver output enable	
36	GND	Ground	
37	VGL	Scan driver voltage	
38	VGL	Scan driver voltage	
39	GND	Ground	
40	VGH	Scan driver voltage	
41	VGH	Scan driver voltage	
42	GND	Ground	
43	GND	Ground	
44	MLF0P	Mini-LVDS data signal+	
45	MLF0N	Mini-LVDS data signal-	
46	MLF1P	Mini-LVDS data signal+	
47	MLF1N	Mini-LVDS data signal-	
48	MLF2P	Mini-LVDS data signal+	
49	MLF2N	Mini-LVDS data signal-	
50	GND	Ground	
51	MLFCKP	Mini-LVDS clock signal+	
52	MLFCKN	Mini-LVDS clock signal-	
53	GND	Ground	
54	MLF4P	Mini-LVDS data signal+	
55	MLF4N	Mini-LVDS data signal-	
56	MLF5P	Mini-LVDS data signal+	
57	MLF5N	Mini-LVDS data signal-	
58	MLF6P	Mini-LVDS data signal+	
59	MLF6N	Mini-LVDS data signal-	

60	GND	Ground	
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CN1 (XRL) Connector Pin Assignment : P-TWO 196318-80041-3

Pin	Name	Description	Note
1	GND	Ground	
2	MLF6N	Mini-LVDS data signal-	
3	MLF6P	Mini-LVDS data signal+	
4	MLF5N	Mini-LVDS data signal-	
5	MLF5P	Mini-LVDS data signal+	
6	MLF4N	Mini-LVDS data signal-	
7	MLF4P	Mini-LVDS data signal+	
8	GND	Ground	
9	MLFCKN	Mini-LVDS clock signal-	
10	MLFCKP	Mini-LVDS clock signal+	
11	GND	Ground	
12	MLF3N	Mini-LVDS data signal-	
13	MLF3P	Mini-LVDS data signal+	
14	MLF2N	Mini-LVDS data signal-	
15	MLF2P	Mini-LVDS data signal+	
16	MLF1N	Mini-LVDS data signal-	
17	MLF1P	Mini-LVDS data signal+	
18	GND	Ground	
19	GND	Ground	
20	VGH	Scan driver voltage	
21	VGH	Scan driver voltage	
22	GND	Ground	
23	VGL	Scan driver voltage	
24	VGL	Scand driver voltage	
25	GND	Ground	
26	OE1	Scan driver output enable	
27	OE2	Scan driver output enable	
28	CKV	Scan driver clock	
29	STV2	Scan driver start pulse	
30	PAIRMODE	Selects mini-LVDS input mode	
31	POL	Data driver polarity invert	
32	VDASEL	Half VAA selection	(1)
33	TP1	Data driver data latch	
34	CSTV	Scan driver start pulse	
35	GND	Ground	
36	GM18	Gamma voltage	
37	GM17	Gamma voltage	
38	GM16	Gamma voltage	
39	GM13	Gamma voltage	
40	GM12	Gamma voltage	
41	GM10	Gamma voltage	
42	GM9	Gamma voltage	
43	GM7	Gamma voltage	
44	GM6	Gamma voltage	
45	GM3	Gamma voltage	
46	GM2	Gamma voltage	
47	GM1	Gamma voltage	
48	GND	Ground	
49	VDD	Logic power	
50	VDD	Logic power	
51	GND	Ground	

52	VDDAM	Half VAA voltage	
53	VDDAM	Half VAA voltage	
54	GND	Ground	
55	VCM	VCOM voltage	
56	VCM	VCOM voltage	
57	GND	Ground	
58	VDDA	VAA voltage	
59	VDDA	VAA voltage	
60	GND	Ground	

CN2 (XRL) Connector Pin Assignment : P-TWO 196225-80041

Pin	Name	Description	Note
1	VGH	Scan driver voltage	
2	VGH	Scand driver voltage	
3	VGH	Scand driver voltage	
4	GND	Ground	
5	VGL	Scan driver voltage	
6	VGL	Scan driver voltage	
7	GND	Ground	
8	VDD	Logic power	
9	VDD	Logic power	
10	GND	Ground	
11	VCM	VCOM voltage	
12	VCM	VCOM voltage	
13	GND	Ground	
14	VDDAM	Half VAA voltage	
15	VDDAM	Half VAA voltage	
16	GND	Ground	
17	VDDA	VAA voltage	
18	VDDA	VAA voltage	
19	VDDA	VAA voltage	
20	GND	Ground	
21	GM1	Gamma voltage	
22	GM2	Gamma voltage	
23	GM3	Gamma voltage	
24	GND	Ground	
25	GND	Ground	
26	GM6	Gamma voltage	
27	GM7	Gamma voltage	
28	GND	Ground	
29	GM9	Gamma voltage	
30	GM10	Gamma voltage	
31	GND	Ground	
32	GM12	Gamma voltage	
33	GM13	Gamma voltage	
34	GND	Ground	
35	GND	Ground	
36	GM16	Gamma voltage	
37	GM17	Gamma voltage	
38	GM18	Gamma voltage	
39	GND	Ground	
40	STV2	Scan driver start pulse	
41	CSTV	Scan driver start pulse	
42	POL	Data driver polarity invert	
43	CKV	Scan driver clock	

44	TP1	Data driver data latch	
45	OE2	Scan driver output enable	
46	OE1	Scan driver output enable	
47	GND	Ground	
48	MLE6N	Mini-LVDS data signal-	
49	MLE6P	Mini-LVDS data signal+	
50	MLE5N	Mini-LVDS data signal-	
51	MLE5P	Mini-LVDS data signal+	
52	MLE4N	Mini-LVDS data signal-	
53	MLE4P	Mini-LVDS data signal+	
54	GND	Ground	
55	MLECKN	Mini-LVDS clock signal-	
56	MLECKP	Mini-LVDS clock signal+	
57	GND	Ground	
58	MLE2N	Mini-LVDS data signal-	
59	MLE2P	Mini-LVDS data signal+	
60	MLE1N	Mini-LVDS data signal-	
61	MLE1P	Mini-LVDS data signal+	
62	MLE0N	Mini-LVDS data signal-	
63	MLE0P	Mini-LVDS data signal+	
64	GND	Ground	
65	MLD6N	Mini-LVDS data signal-	
66	MLD6P	Mini-LVDS data signal+	
67	MLD5N	Mini-LVDS data signal-	
68	MLD5P	Mini-LVDS data signal+	
69	MLD4N	Mini-LVDS data signal-	
70	MLD4P	Mini-LVDS data signal+	
71	GND	Ground	
72	MLDCKN	Mini-LVDS clock signal-	
73	MLDCKP	Mini-LVDS clock signal+	
74	GND	Ground	
75	MLD2N	Mini-LVDS data signal-	
76	MLD2P	Mini-LVDS data signal+	
77	MLD1N	Mini-LVDS data signal-	
78	MLD1P	Mini-LVDS data signal+	
79	MLD0N	Mini-LVDS data signal-	
80	MLD0P	Mini-LVDS data signal+	

CN3 (XRL) Connector Pin Assignment : Starconn B-F,089H55-000000-G2-R

Pin	Name	Description	Note
1	GND	Ground	
2	NC	No connection	
3	NC	No connection	
4	NC	No connection	
5	NC	No connection	
6	NC	No connection	
7	NC	No connection	
8	NC	No connection	
9	NC	No connection	
10	NC	No connection	
11	NC	No connection	
12	NC	No connection	
13	GND	Ground	
14	NC	No connection	
15	NC	No connection	

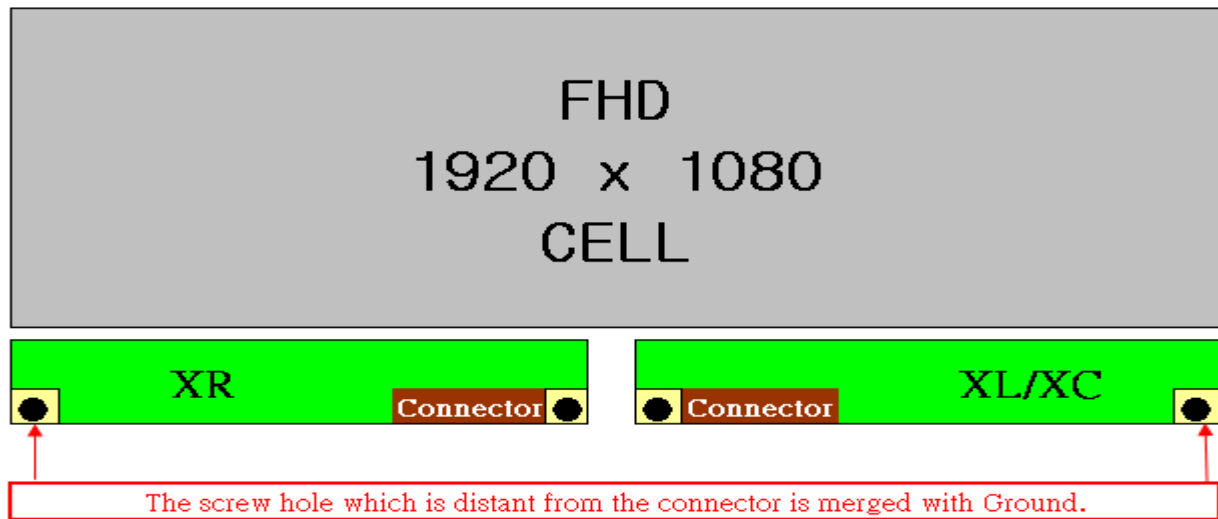
16	GND	Ground	
17	NC	No connection	
18	NC	No connection	
19	NC	No connection	
20	NC	No connection	
21	NC	No connection	
22	NC	No connection	
23	NC	No connection	
24	NC	No connection	
25	GND	Ground	
26	GND	Ground	
27	GND	Ground	
28	GND	Ground	
29	GND	Ground	
30	GND	Ground	
31	NC	No connection	
32	NC	No connection	
33	GND	Ground	
34	NC	No connection	
35	NC	No connection	
36	NC	No connection	
37	NC	No connection	
38	GND	Ground	
39	MLF6N	Mini-LVDS data signal-	
40	MLF6P	Mini-LVDS data signal+	
41	MLF5N	Mini-LVDS data signal-	
42	MLF5P	Mini-LVDS data signal+	
43	MLF4N	Mini-LVDS data signal-	
44	MLF4P	Mini-LVDS data signal+	
45	GND	Ground	
46	MLFCKN	Mini-LVDS clock signal-	
47	MLFCKP	Mini-LVDS clock signal+	
48	GND	Ground	
49	MLF2N	Mini-LVDS data signal-	
50	MLF2P	Mini-LVDS data signal+	
51	MLF1N	Mini-LVDS data signal-	
52	MLF1P	Mini-LVDS data signal+	
53	MLF0N	Mini-LVDS data signal-	
54	MLF0P	Mini-LVDS data signal+	
55	GND	Ground	

Note (1) VDA select: Half/Full VAA operating range selection.

Low = Connect to GND, High = Connect to +3.3V

VDA SEL	Note
L	Full VAA
H	Half VAA (V460H1-PE5 setting)

Note (2) The screw hole which is distant from the connector is merged with Ground

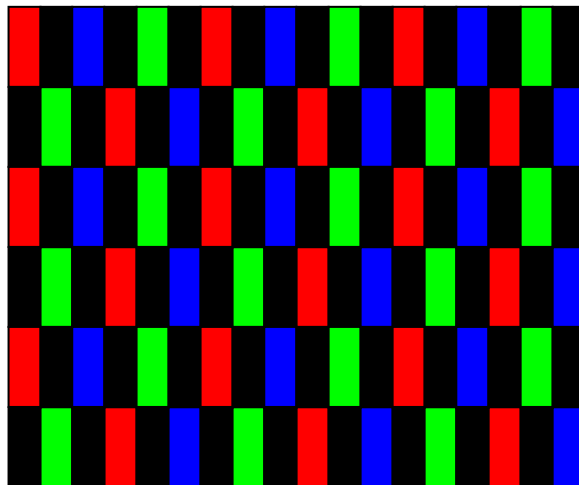


4.2 FLICKER (Vcom) ADJUSTMENT

(1) Adjustment Pattern:

Sub-pixel on-off pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

(bright sub-pixel : G128 ; dark sub-pixel : G0)



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

- a. USB Sensor Board.
- b. Programmable software.

5. INTERFACE TIMING

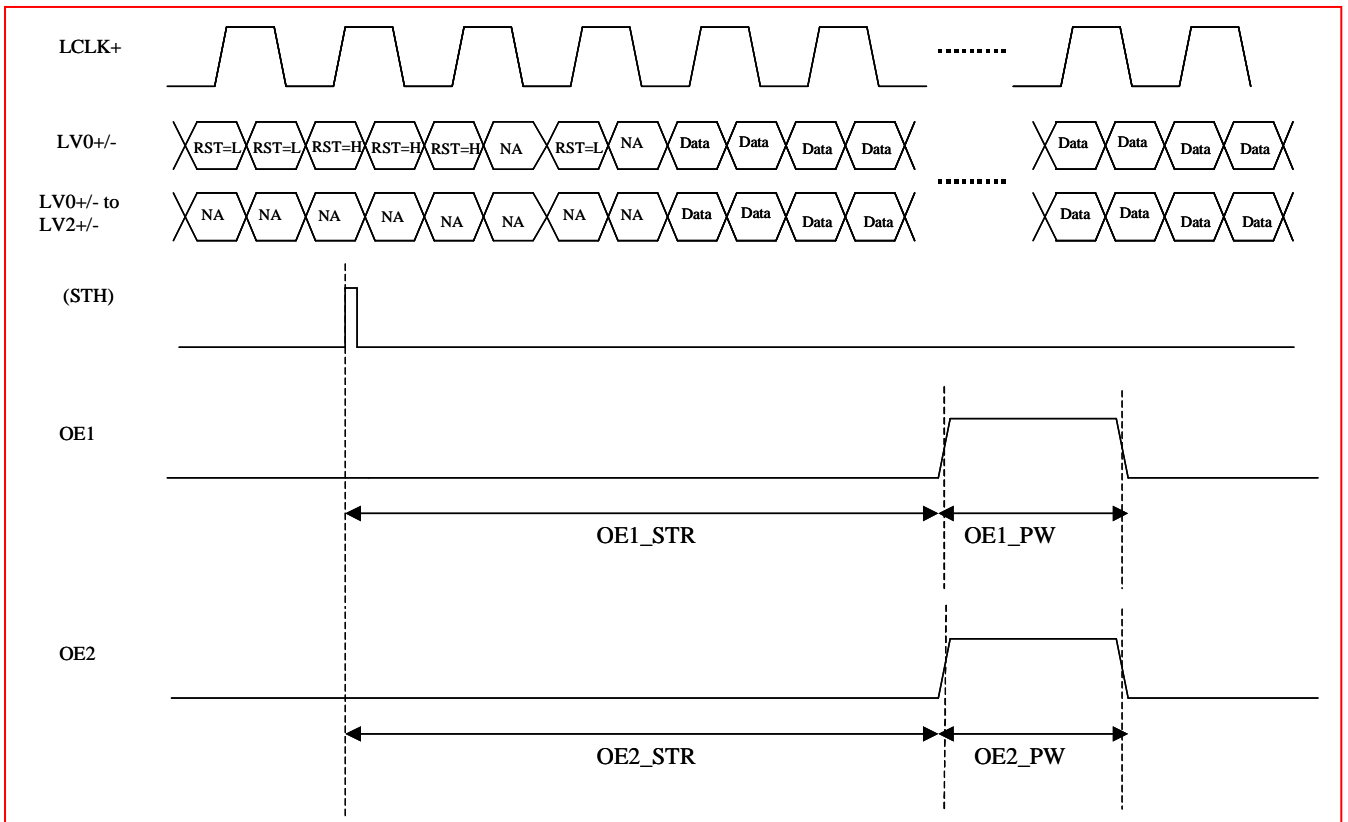
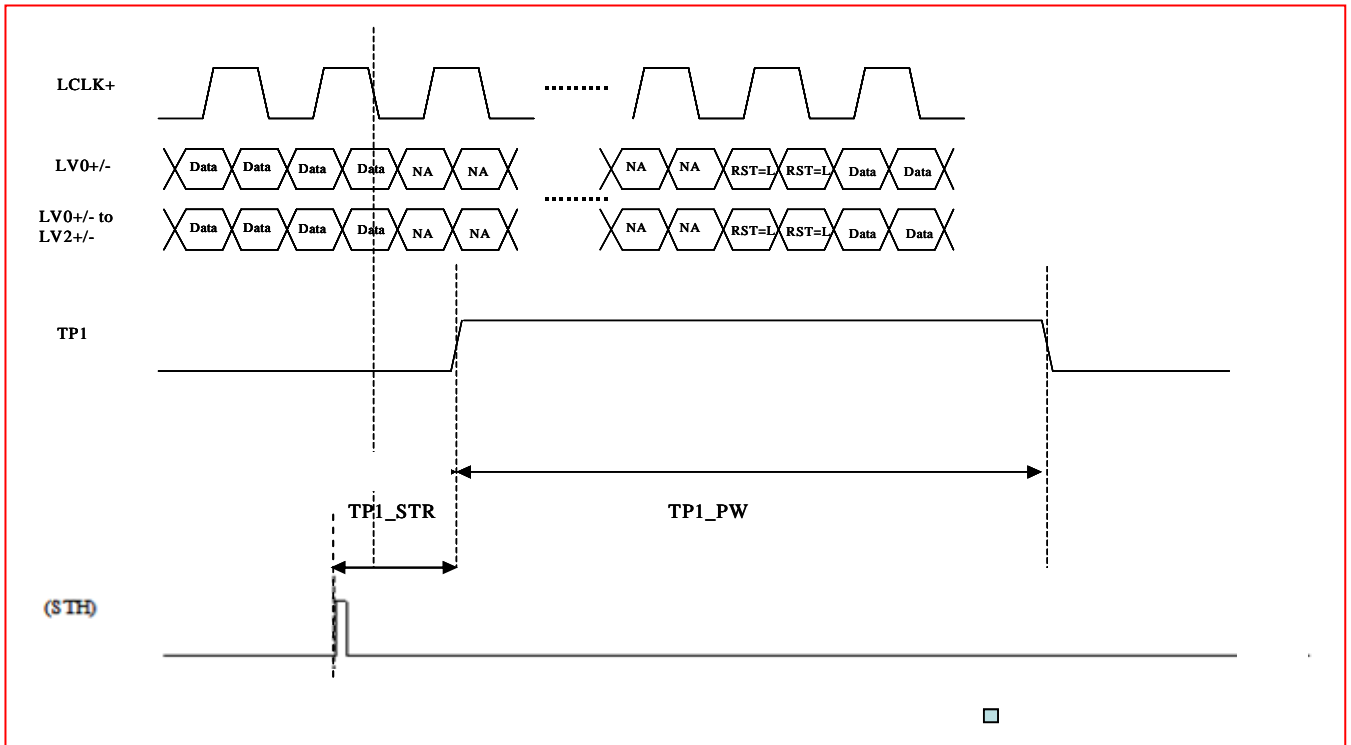
5.1 INPUT SIGNAL TIMING SPECIFICATIONS

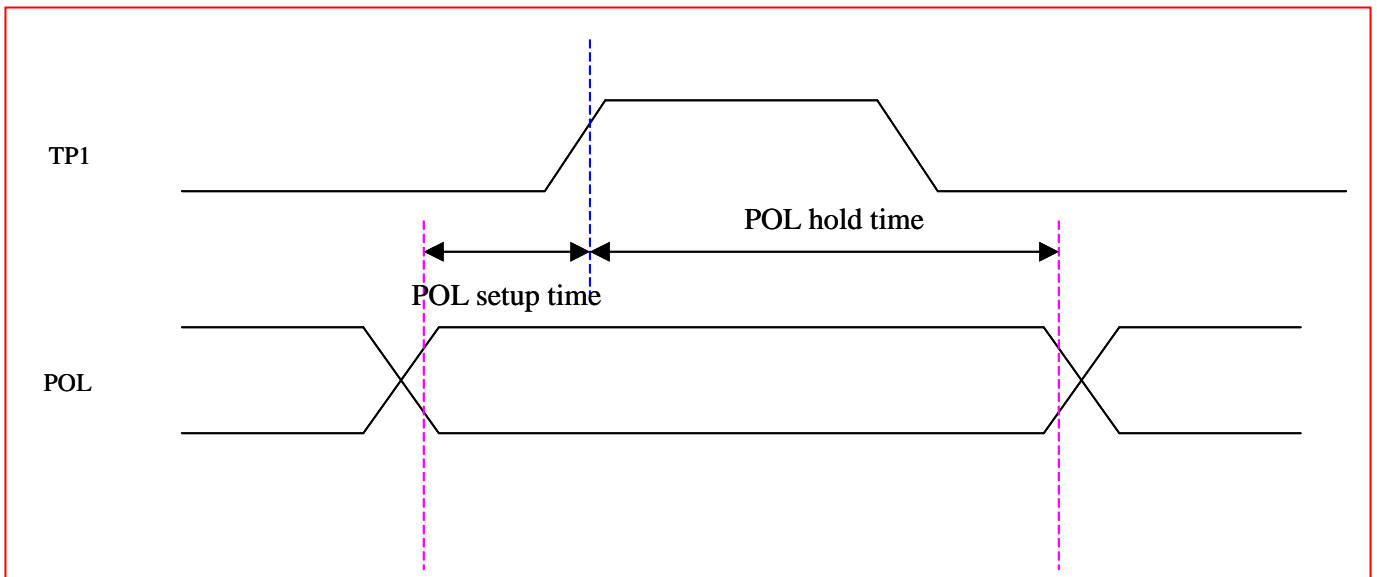
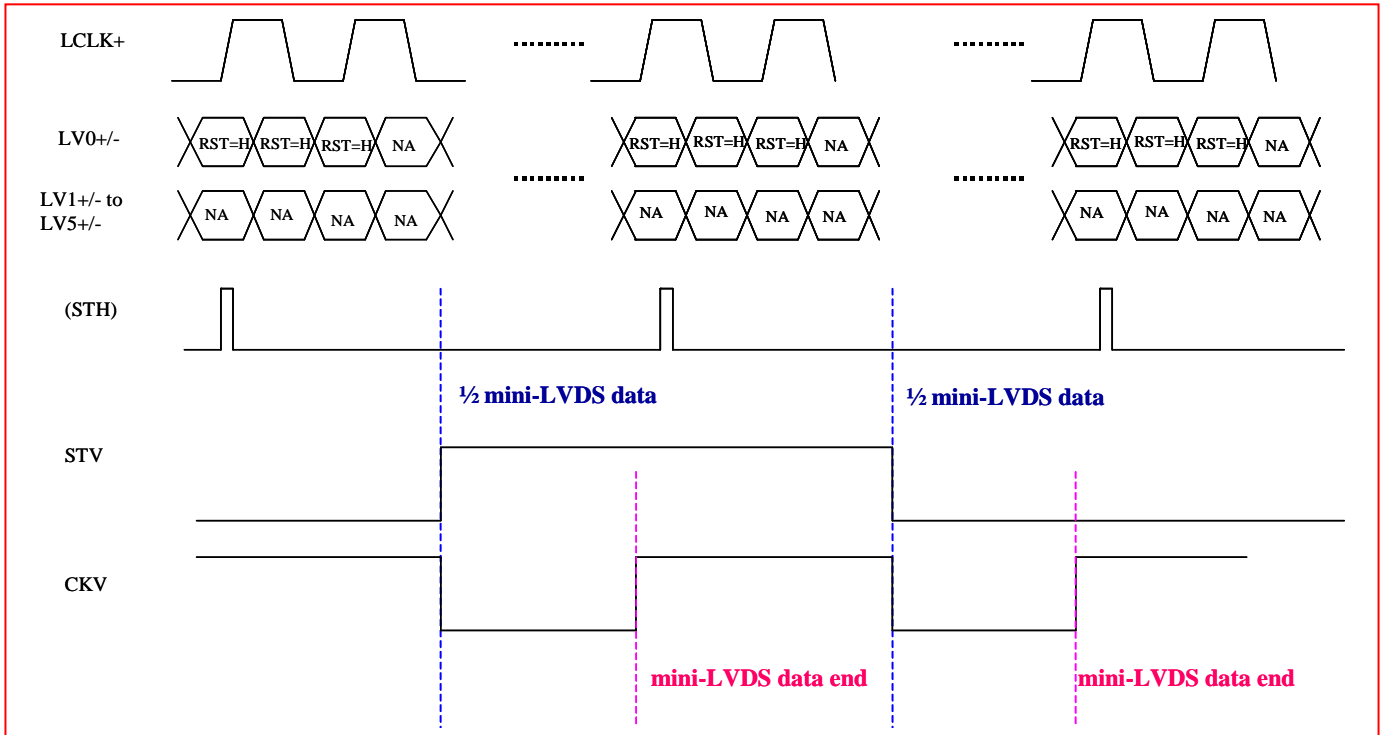
(Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

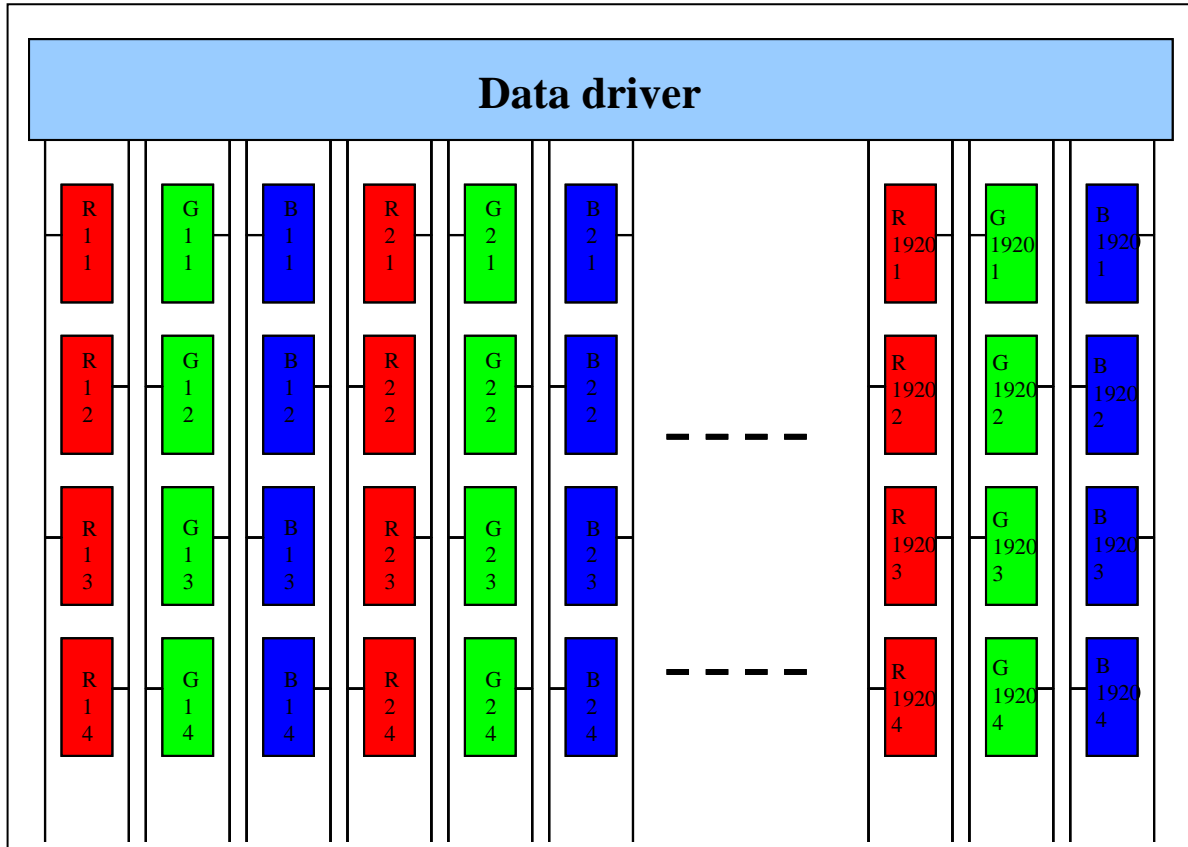
Test condition : LVDS Receiver Clock 74.25MHz

Signal	Item	Symbol	Typ	Unit
TP1	TP1 start	TP1_STR	0.33	us
	TP1 pulse width	TP1_PW	6.9	us
OE	OE1 start	OE1_STR	5.7	us
	OE1 pulse width	OE1_PW	1.63	us
	OE2 start	OE2_STR	3.24	us
	OE2_PW	OE2_PW	4.09	us
STV	Scan driver start pulse	STV	3.77	us
CKV	Scan driver clock	CKV	3.77	us
POL	Data driver polarity invert	POL	4.16	us
Data arrangement			2D2G	





Note: Data arrangement of 2G2D



6. OPTICAL CHARACTERISTICS

6.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Vertical Frame Rate	Fr	240	Hz

6.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 6.1 and stable environment shown in 6.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Angle at Normal Direction Standard light source "C"	Typ.- 0.03	0.656	Typ.+ 0.03	-	(0),(6)
		Rcy			0.326		-	
	Green	Gcx			0.261		-	
		Gcy			0.581		-	
	Blue	Bcx			0.131		-	
		Bcy			0.114		-	
	White	Wcx			0.290		-	
		Wcy			0.345		-	
Center Transmittance		T%	$\theta_x=0^\circ, \theta_y=0^\circ$ with CMI module	-	4.6	-	%	(1),(5)
Contrast Ratio		CR		4000	5000	-	-	(1),(3)
Response Time		T _R	$\theta_x=0^\circ, \theta_y=0^\circ$ with CMI Module@120Hz, Panel temperature is 34±1°C	-	25	-	ms	(1),(4)
		T _F		-	4.0	-	ms	
Viewing Angle	Horizontal	θ_{x+}	CR≥20 With CMI module	80	88	-	Deg.	(1),(2)
		θ_{x-}		80	88	-		
	Vertical	θ_{y+}		80	88	-		
		θ_{y-}		80	88	-		

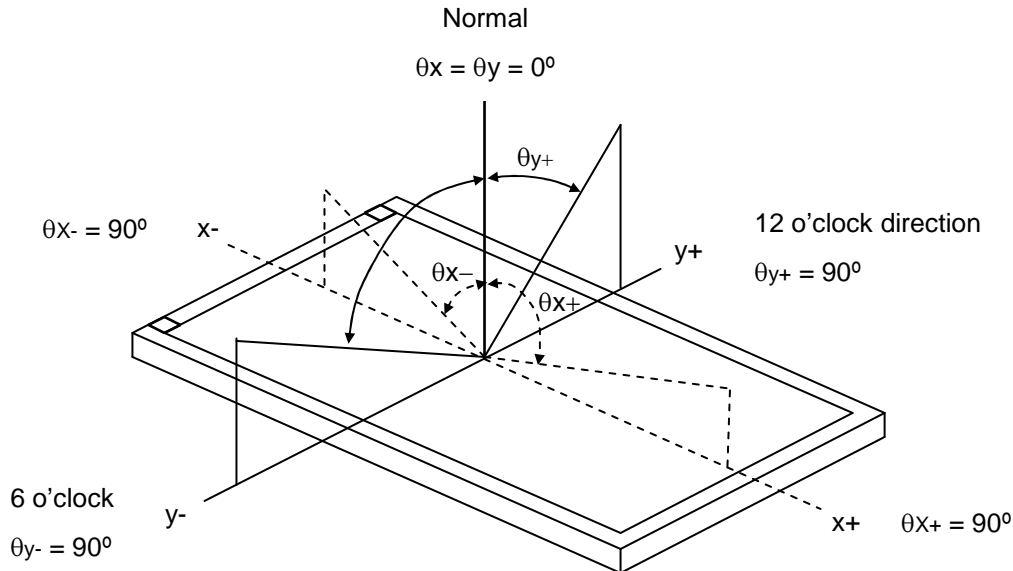
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following :

1. Measure Module's and BLU's spectrums. W, R, G, B are with signal input. BLU (for V645H1-LE1) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θ_x, θ_y):

Viewing angles are measured by Autronic Conoscope Cono-80



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

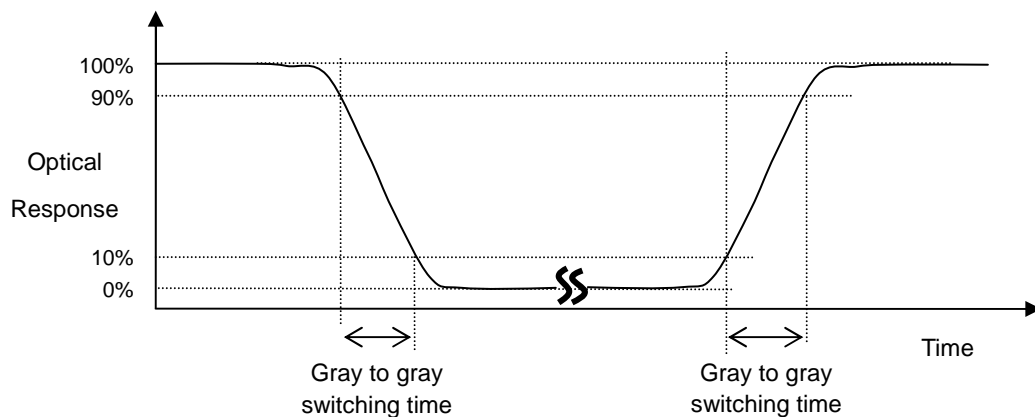
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (X), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (4) Definition of Response Time (T_R, T_F):



T_R means switching time from gray 0 to 255

T_F means switching time from gray 255 to 0

Note (5) Definition of Transmittance (T%) :

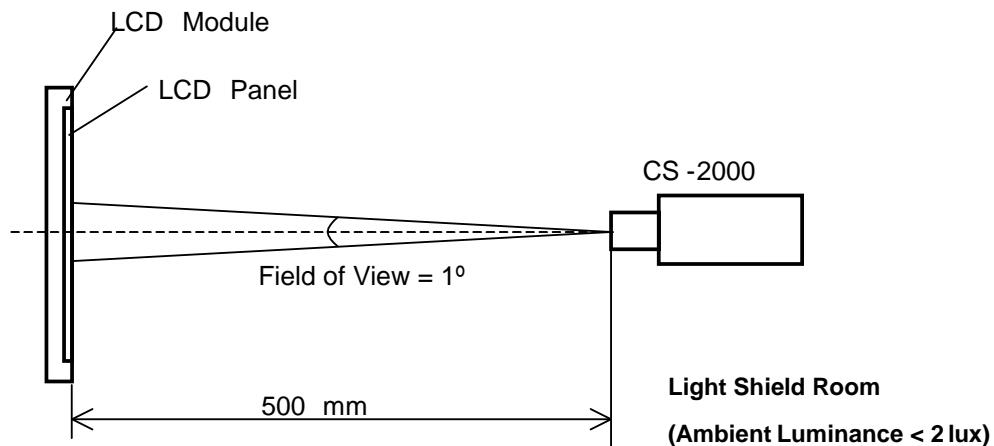
Measure the luminance of gray level 255 at center point of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{Luminance of LCD module}}{\text{Luminance of backligh unit}} \times 100\%$$

Film structure : 3 pieces of Diffusers

Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 1 hour in a windless room.



7. RELIABILITY TEST CONDITION

NO.	Test Item	Test Condition
1	HT Operation	Ta=50°C, 1000hrs
2	HT Storage	Ta=60°C, 500hrs
3	LT Operation	Ta=0°C, 500hrs
4	LT Storage	Ta=-20°C, 500hrs
5	HTHH Operation	Ta=50°C / 80%RH, 500hrs
6	HTHH Storage	Ta=50°C / 90%RH, 500hrs
7	Thermal Shock (Non-operation)	[(-20°C 30min)→(60°C 30min)]/cycle, 200cycles
8	Image Sticking	Ta=50°C, 300hrs
9	ESD-Air mode Discharge	150pf · 330Ω, ±15KV (operation) Class C (With CMI Module)
10	ESD-Contact Mode Discharge	150pf · 330Ω, ±8KV (operation) Class B (With CMI Module)
11	Packing Vibration	1.14Grms Random frequency 1~200Hz 30min/Bottom, 15min/Right-Left, 15min/Front-Back
12	Packing Drop	Bottom 20cm+ 4 edges with 15 angle

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [1] Do not apply rough force such as bending or twisting to the module during assembly.
- [2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel.
- [4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [5] The distance between COF edge and rib of BLU is suggested to be larger than 5mm, in order to prevent from damage on COF during module assembly.
- [6] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.
- [7] If COF would be bended during module assembly, it is suggested not to locate the IC on the bending corner of COF.
- [8] The gap between COF IC and any structure of BLU is suggested to be larger than 2mm, in order to prevent from damage on COF IC.
- [9] Bezel opening must have no burr. Burr will scrape the panel surface.
- [10] It is suggested that bezel of module and bezel of TV set can not press or touch the panel surface. It will make light leakage or scrape.
- [11] When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.
- [12] The gap between Panel and any structure of Bezel is suggested to be larger than 2mm, in order to prevent from damage on Panel.
- [13] Do not plug in or pull out the I/F connector while the module is in operation.
- [14] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [15] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [16] When storing modules as spares for a long time, the following precaution is necessary.
 - [16.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
 - [16.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [17] When ambient temperature is lower than 10°C, the display quality might be reduced.
- [18] The peeling strength of COF is 200gf/cm.
- [19] During module assembly process, the static electricity around the environment should be less than 300V.

8.2 SAFETY PRECAUTIONS

- [1] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [2] After end of life of the open cell product, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

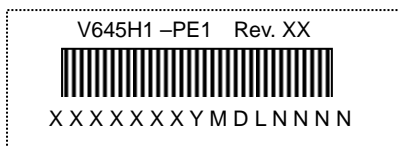
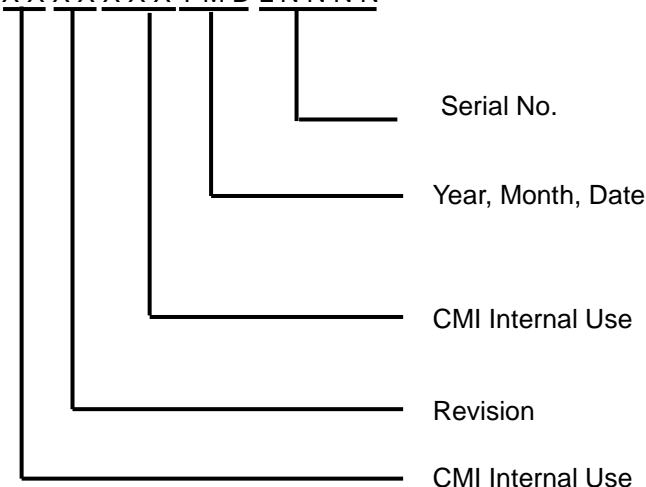


Figure.9-1 Serial No. Label on SPWB and Cell

Model Name: V645H1-PE1

Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2...etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

Serial No.: Manufacturing sequence of product

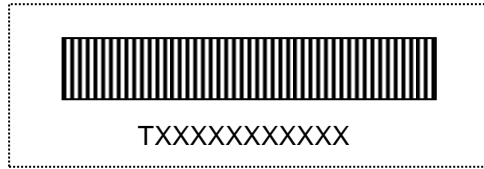
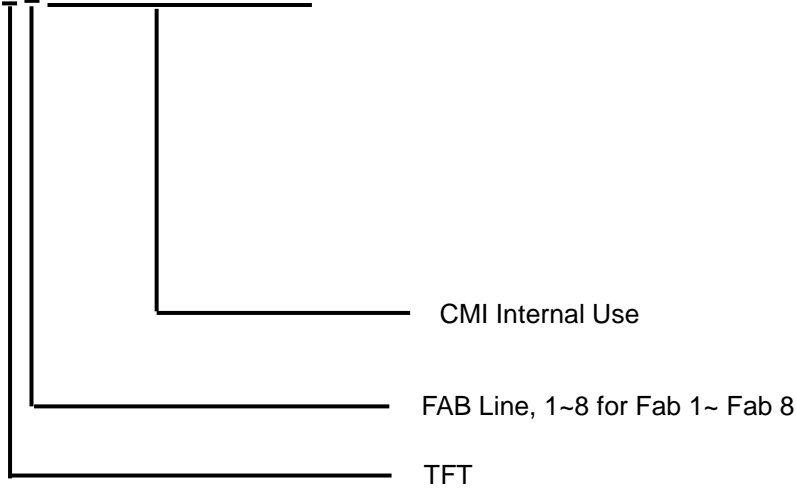


Figure.9-2 Panel ID Label on Cell

Panel ID Label includes the information as below:

Panel ID: T X X X X X X X X X X



9.2 CARTON LABEL

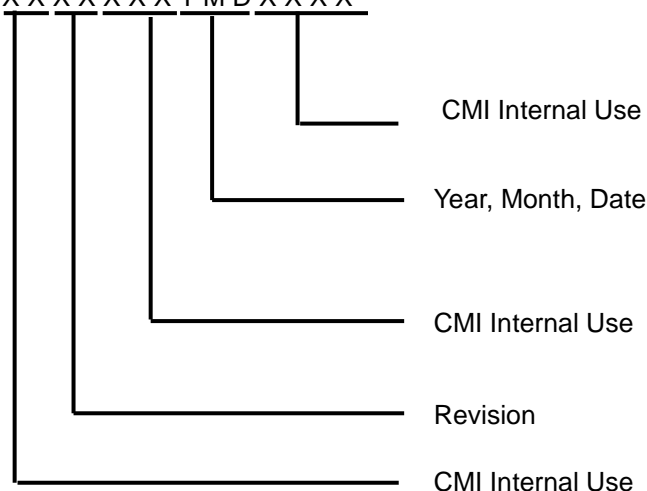
The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.



Carton label includes the information as below:

(a) Model Name: V645H1-PE1

(b) Carton ID: X X X X X X Y M D X X X X



Serial ID includes the information as below:

Manufactured Date:

Year: 2010=0, 2011=1,2012=2...etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

(c) Quantities: 8

10. PACKAGING

10.1 PACKING SPECIFICATIONS

- (1) 4PCS LCD TV Panels / 1 Box
- (2) Box dimensions : 1642(L) X 1120 (W) X 240 (H)
- (3) Weight : approximately 49 Kg (4 panels per box)
- (4) Desiccant (Drier) : Weight 30g / 1 piece, Quantity 6 pcs, Cobalt chloride free.

10.2 PACKING METHOD

Figures 10-1 and 10-2 are the packing method

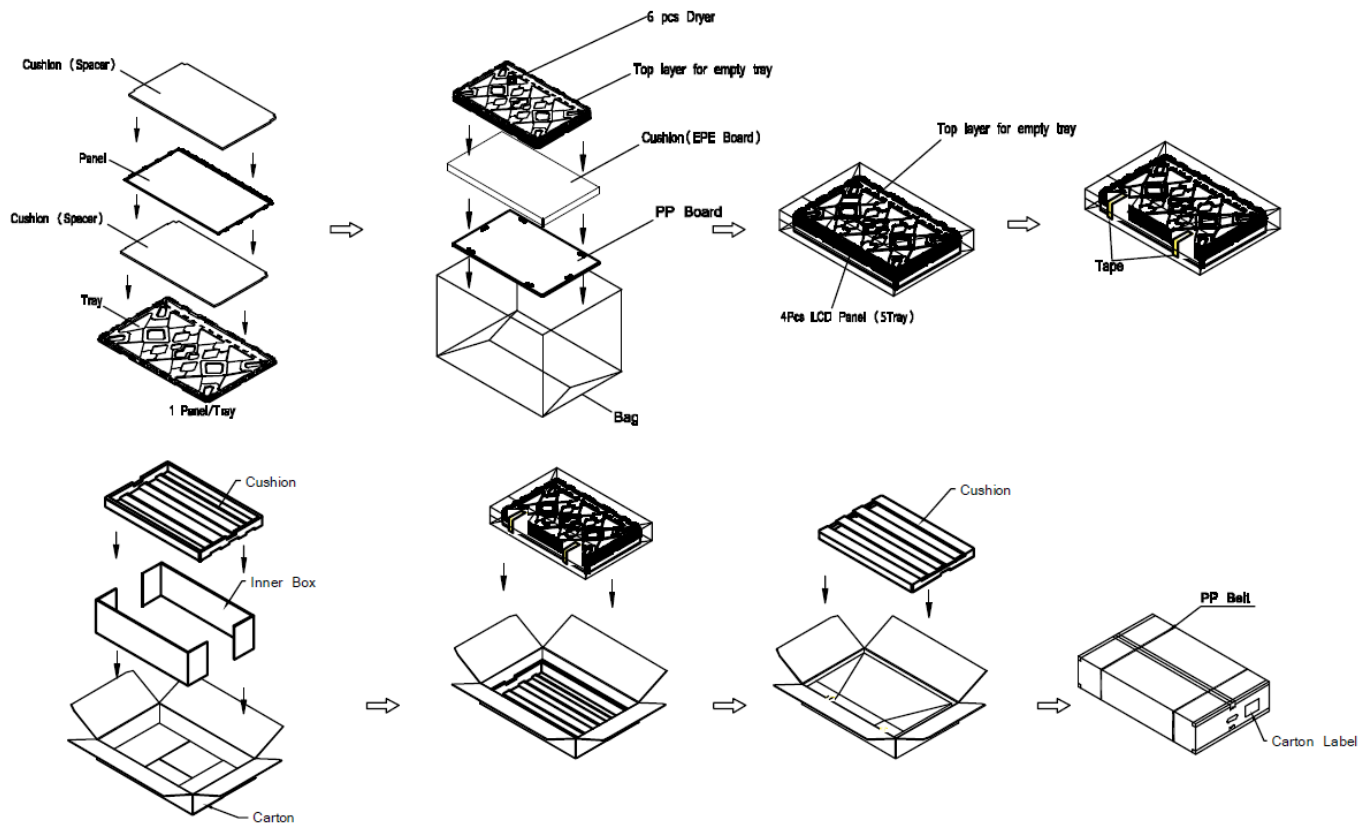
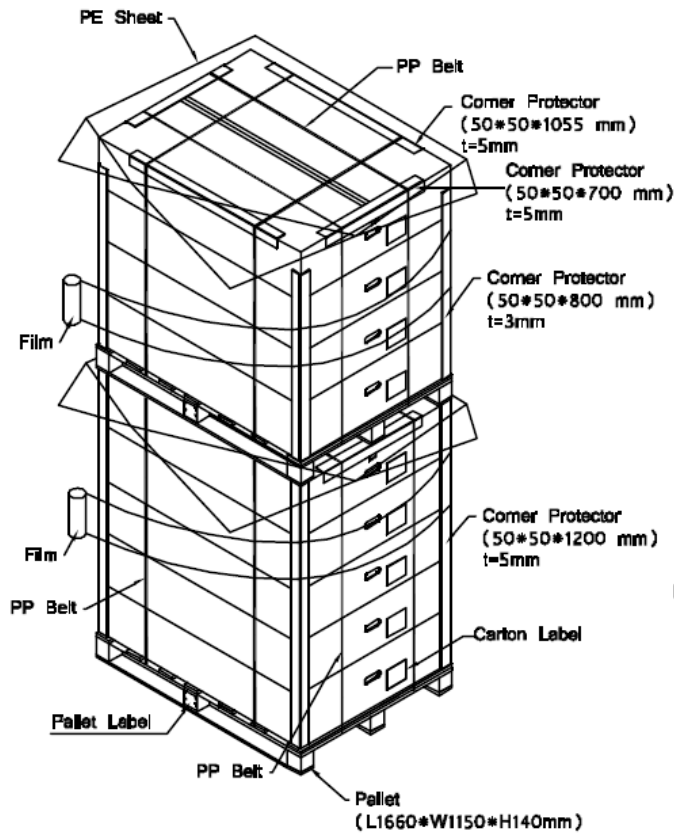
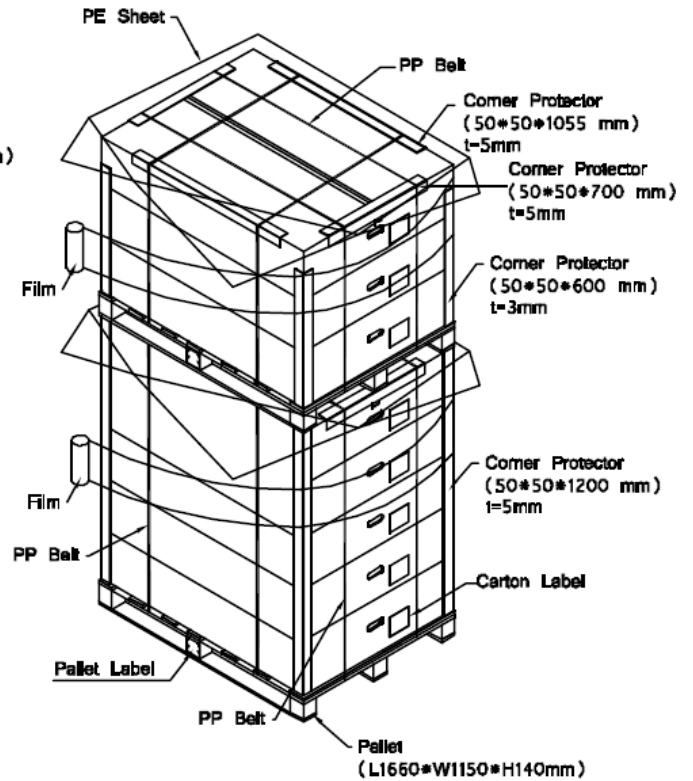


Figure.10-1 packing method

**Sea&Land Transportation
(40ft HQ Container)**



Sea&Land Transportation



Air Transportation

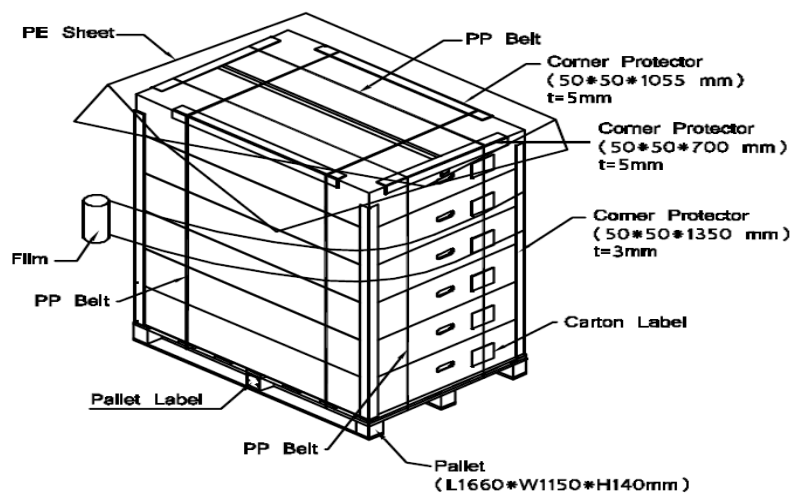
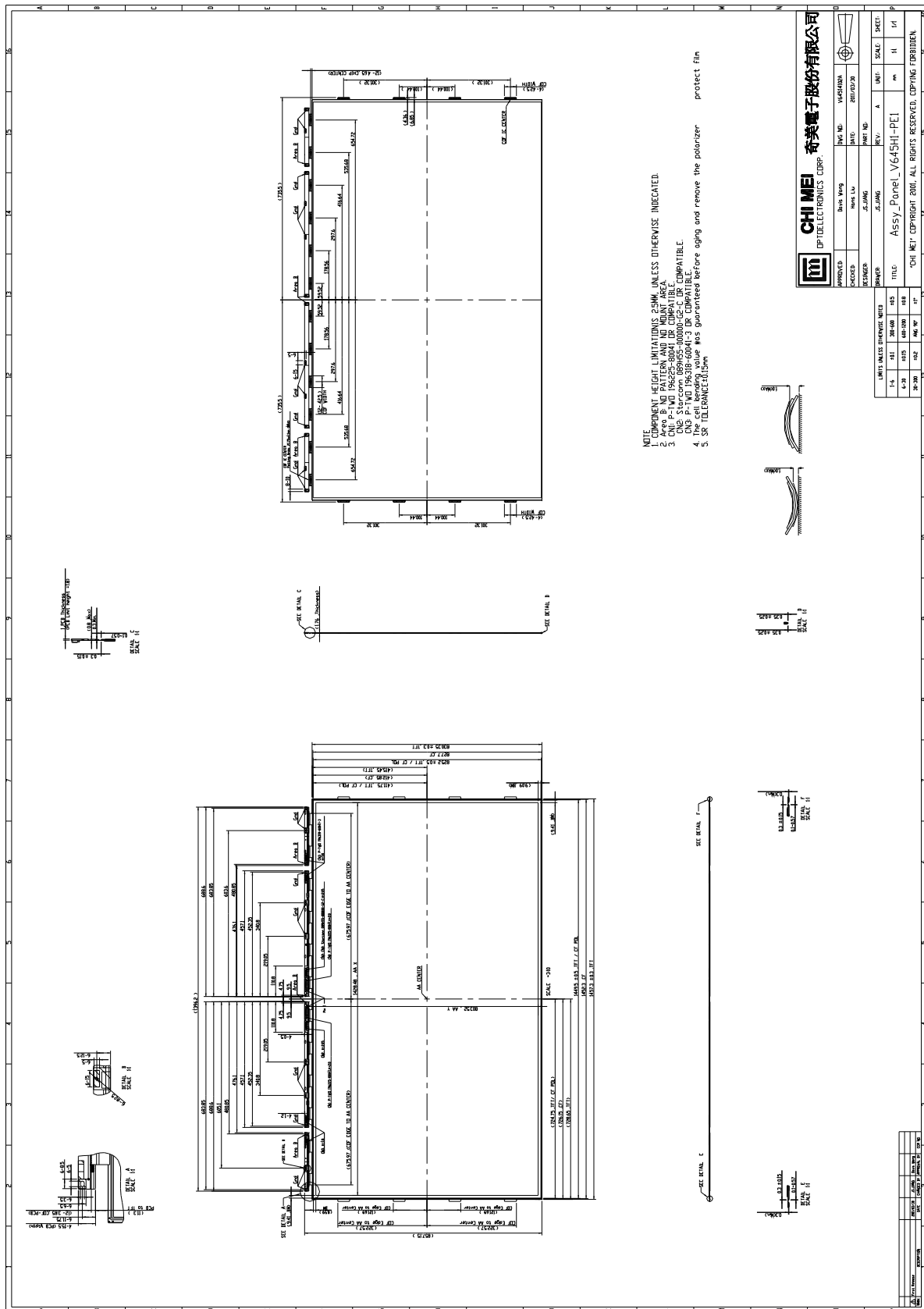
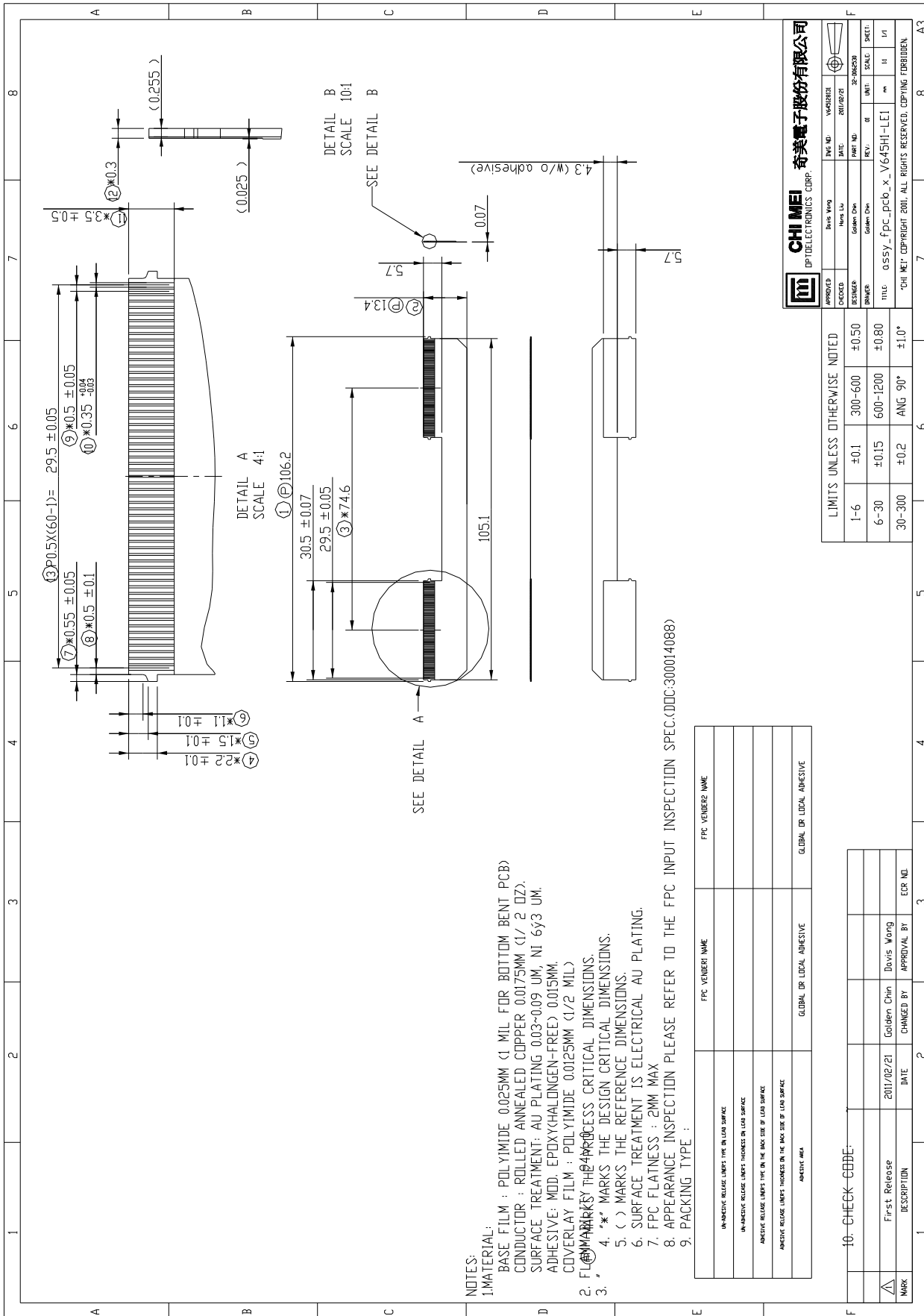


Figure.10-2 packing method

11. MECHANICAL CHARACTERISTIC





- NOTES:
1. MATERIAL:
BASE FILM : POLYIMIDE 0.025MM (1 MIL FOR BOTTOM BENT PCB)
CONDUCTOR : ROLLED ANNEALED COPPER 0.0175MM (1/2 OZ).
SURFACE TREATMENT: AU PLATING 0.03-0.09 UM, NI 6/3 UM.
ADHESIVE : MOD. EPDXY(HALOGEN-FREE) 0.015MM.
COVERLAY FILM : POLYIMIDE 0.0125MM (1/2 MIL)
2. FLOW MARKS THE PROCESS CRITICAL DIMENSIONS.
3. * (*) MARKS THE DESIGN CRITICAL DIMENSIONS.
4. * (*) MARKS THE REFERENCE DIMENSIONS.
5. (<) MARKS THE REFERENCE DIMENSIONS.
6. SURFACE TREATMENT IS ELECTRICAL AU PLATING.
7. FPC FLATNESS : 2MM MAX
8. APPEARANCE INSPECTION PLEASE REFER TO THE FPC INPUT INSPECTION SPEC.(DDC:300014088)
9. PACKING TYPE :

	FPC VENDOR NAME	FPC VENDOR NAME
UNADHESIVE RELEASE LIMITS TYPE ON LEAD SURFACE		
UNADHESIVE RELEASE LIMITS THICKNESS ON LEAD SURFACE		
ADHESIVE RELEASE LIMITS TYPE ON THE BACK SIDE OF LEAD SURFACE		
ADHESIVE RELEASE LIMITS THICKNESS ON THE BACK SIDE OF LEAD SURFACE		
ADHESIVE AREA	GLOBAL OR LOCAL ADHESIVE	GLOBAL OR LOCAL ADHESIVE

10. CHECK CODE:

MARK	DESCRIPTION	DATE	CHANGED BY	APPROVAL BY	ECR NO.
△	First Release	2011/02/21	Golden Chin	Davis Wong	

CHI MEI 奇美電子股份有限公司		CHI MEI ELECTRONICS CORP.	
APPROVER	Davis Wong	DWG NO.	VECH081
CHECKER	Hans Liu	DATE	2011/02/21
DESIGNER	Golden Chin	PART NO.	30-000208
DRAWER	Golden Chin	REV.	01
TITLE	assy_fpc_pcb_x_V645HI-LET	UNIT	SCALE
		mm	1:1
CHI MEI: COPYRIGHT 2001. ALL RIGHTS RESERVED. COPYING FORBIDDEN			

LIMITS	UNLESS OTHERWISE NOTED
1-6	±0.1 300-600 ±0.50
6-30	±0.15 600-1200 ±0.80
30-300	±0.2 ANG 90° ±1.0°