□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V645HQ1
SUFFIX: LS1

Customer:

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	Chloe Chen

CONTENTS

REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver. 2.0	Mar. 05,2012	All	All	The Approval Specification was first issued.
Ver. 2.1	Apr. 19,2012	P32	6.2	Modify 6.2 POWER ON/OFF SEQUENCE

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V645HQ1-LS1 is a 64.5" TFT Liquid Crystal Display module with LED Backlight unit and 2ch LVDS interface. This module supports 1920 x 1080 Full HDTV format and can display 1.07G colors (8-bit+hi-FRC). The converter module for backlight is built-in.

1.2 FEATURES

- High contrast ratio (5000:1)
- Fast response time (4ms)
- High color saturation (NTSC 70%)
- Full HDTV (1920 x 1080 pixels) resolution, true HDTV format
- LVDS (Low Voltage Differential Signaling) interface
- Optimized response time for 240 Hz frame rate
- Ultra wide viewing angle : Super MVA technology
- Viewing Angle : 176(H)/176(V) (CR>20)
- RoHS compliance

1.3 APPLICATION

- Standard Living Room TVs
- Public Display Application
- Home Theater Application
- MFM Application

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1428.48 (H) x 803.52 (V) (64.5" diagonal)	mm	(1)
Bezel Opening Area	1440.6(H) x 814.6(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1920 x R.G.B. x 1080	pixel	-
Pixel Pitch(Sub Pixel)	0.248 (H) x 0.744 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G colors (8-bit+hi-FRC)	color	-
Display Operation Mode	Transmissive mode / Normally Black	-	-
Surface Treatment	Anti-Glare coating Haze<4%，Hardness:3H	-	(2)

Note (1) Please refer to the attached drawings in chapter 11 for more information about the front and back outlines.

Note (2) The spec. of the surface treatment is temporarily for this phase. CMI reserves the rights to change this feature.

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1472.3	1474.1	1475.9	mm	(1)
	Vertical (V)	849.1	850.6	852.1	mm	(1)
	Depth (D)	34	35	36	mm	(2)
	Depth (D)	28.8	29.8	30.8	mm	(3)
Weight		-	29600	-	g	-

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth is between bezel to T-CON cover.

Note (3) Module Depth is between bezel to converter cover.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	TST	-20	+60	ºC	(1)
Operating Ambient Temperature	TOP	0	50	ºC	(1), (2)
Shock (Non-Operating)	SNOP	-	35	G	(3), (5)
Vibration (Non-Operating)	VNOP	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

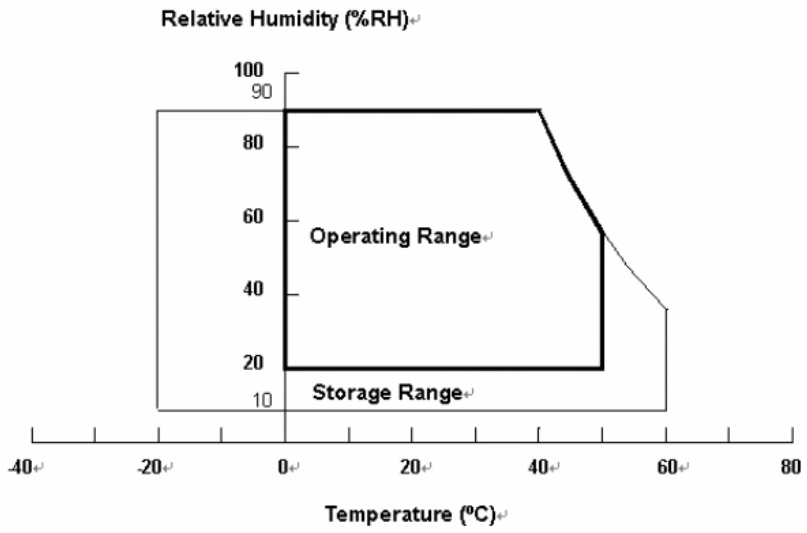
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	Ta = 25 ℃	-	-	60	V_{RMS}	
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control

3. ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

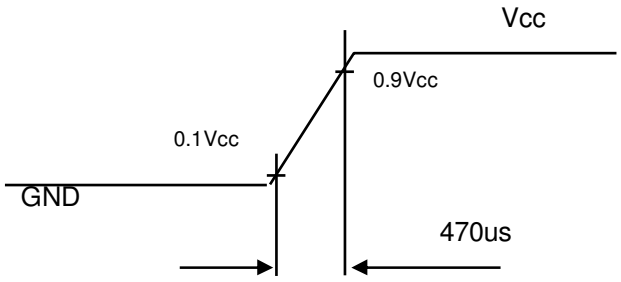
(Ta = 25 ± 2 ºC)

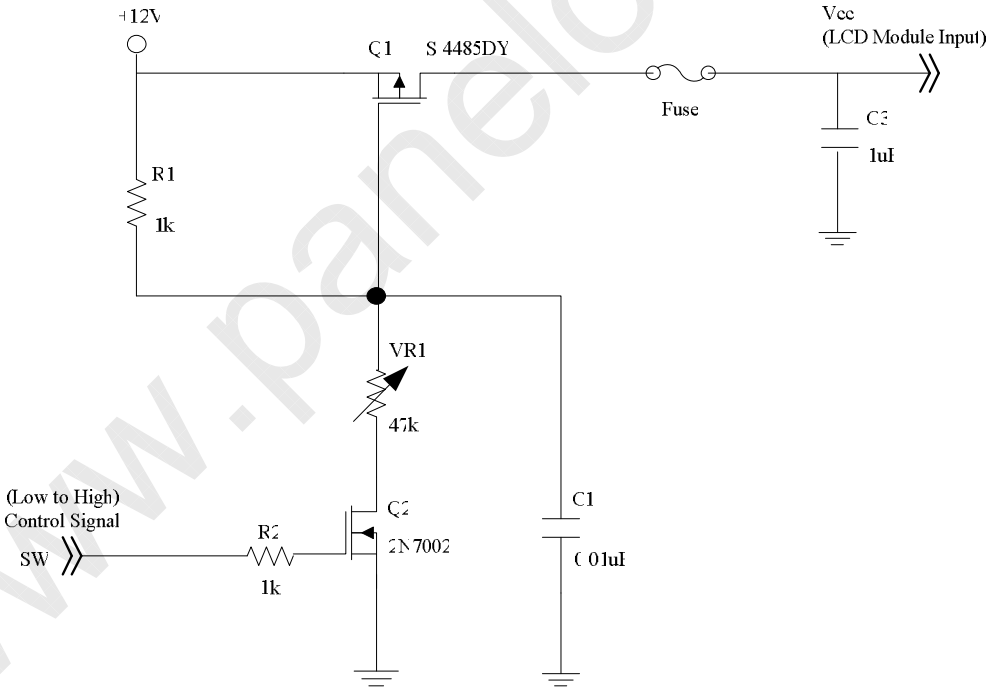
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	4.5	A	(2)
Power consumption	White Pattern	P_T	—	21	25.2	W	(3)
	Horizontal Stripe	P_T	—	41.64	51.24	W	
	Black Pattern	P_T	—	19.8	23.88	W	
Power Supply Current	White Pattern	—	—	1.75	2.1	A	(3)
	Horizontal Stripe	—	—	3.47	4.27	A	
	Black Pattern	—	—	1.65	1.99	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	—	—	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	—	—	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	—	600	mV	
	Terminating Resistor	R_T	—	100	—	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges.

Note (2) Measurement condition:

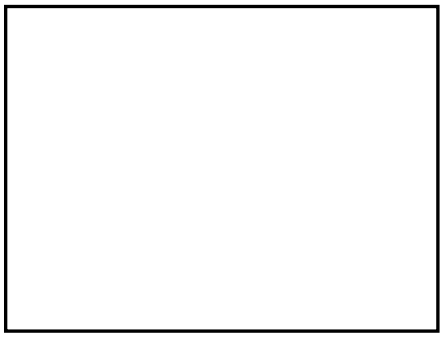
Vcc rising time is 470us





Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, f_v = 240 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

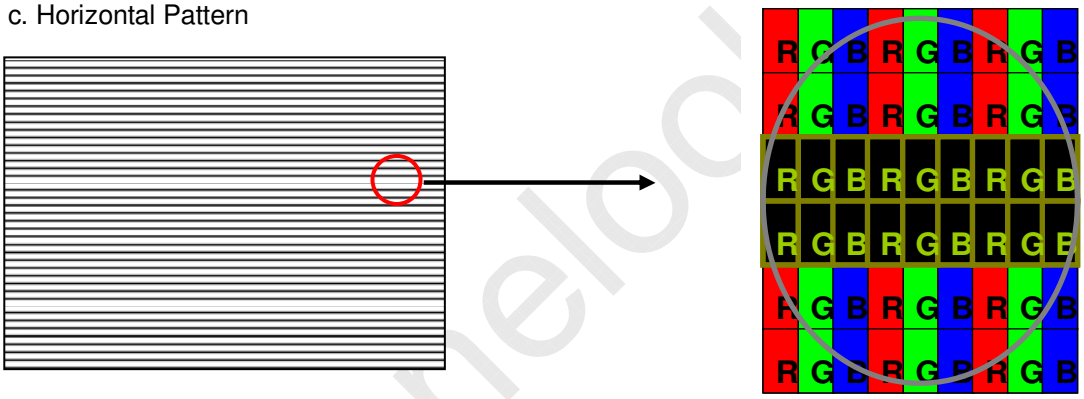


Active Area

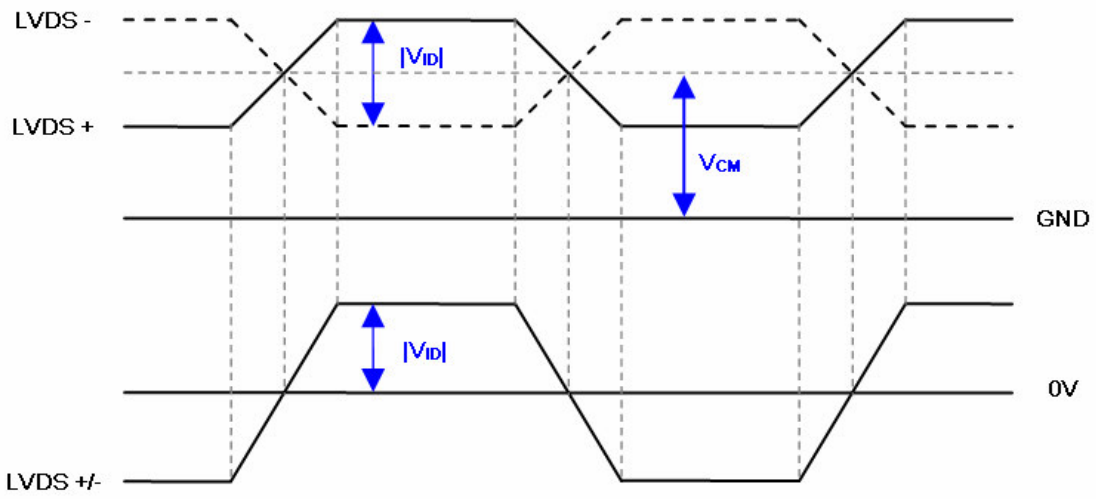
b. Black Pattern

Active Area

c. Horizontal Pattern



Note (4) The LVDS input characteristics are as follows :



3.2 BACKLIGHT CONNECTOR PIN CONFIGURATION

3.2.1 LED LIGHT BAR CHARACTERISTICS (Ta = 25 ± 2 ºC)

The backlight unit contains 8pcs light bar.

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Current	If	4512	4800	5088	mA	32 String
One String Current	$I_{L(2D)}$	141	150	159	mA	
	$I_{L(3D)}$	TBD	450	TBD	mApeak	3D ENA=ON
LED Forward Voltage	Vf	2.8	3.2	3.6	V_{DC}	I_L =150mA
One String Voltage	V_W	30.8	-	39.6	V_{DC}	I_L =150mA
One String Voltage Variation	$\triangle V_W$	-	-	2	V	For 1 BLU
Life time	-	30000	-	-	Hrs	(1)

Note (1) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value. Operating condition: Continuous operating at Ta = 25±2℃, I_L =150mA

3.2.2 CONVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	$P_{BL(2D)}$	-	188	216.5	W	(1), (2) IL = 150 mA
	$P_{BL(3D)}$	-	185.6	222.7	W	(1), (2) IL=450mApeak.
Converter Input Voltage	VBL	22.8	24.0	25.2	V_{DC}	
Converter Input Current	$I_{BL(2D)}$	-	7.83	9	A	Non Dimming
	$I_{BL(3D)}$	-	7.7	9.28	A	
Input Inrush Current	$I_{R(2D)}$	-	-	13	Apeak	V_{BL}=22.8V,(IL=typ.) (3), (6)
	$I_{R(3D)}$	-	-	25	Apeak	V_{BL}=22.8V,(IL=3*typ.) (3), (6)
Dimming Frequency	FB	150	160	170	Hz	(5)
Minimum Duty Ratio	DMIN	5	10	-	%	(4), (5)

Note (1) The power supply capacity should be higher than the total converter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

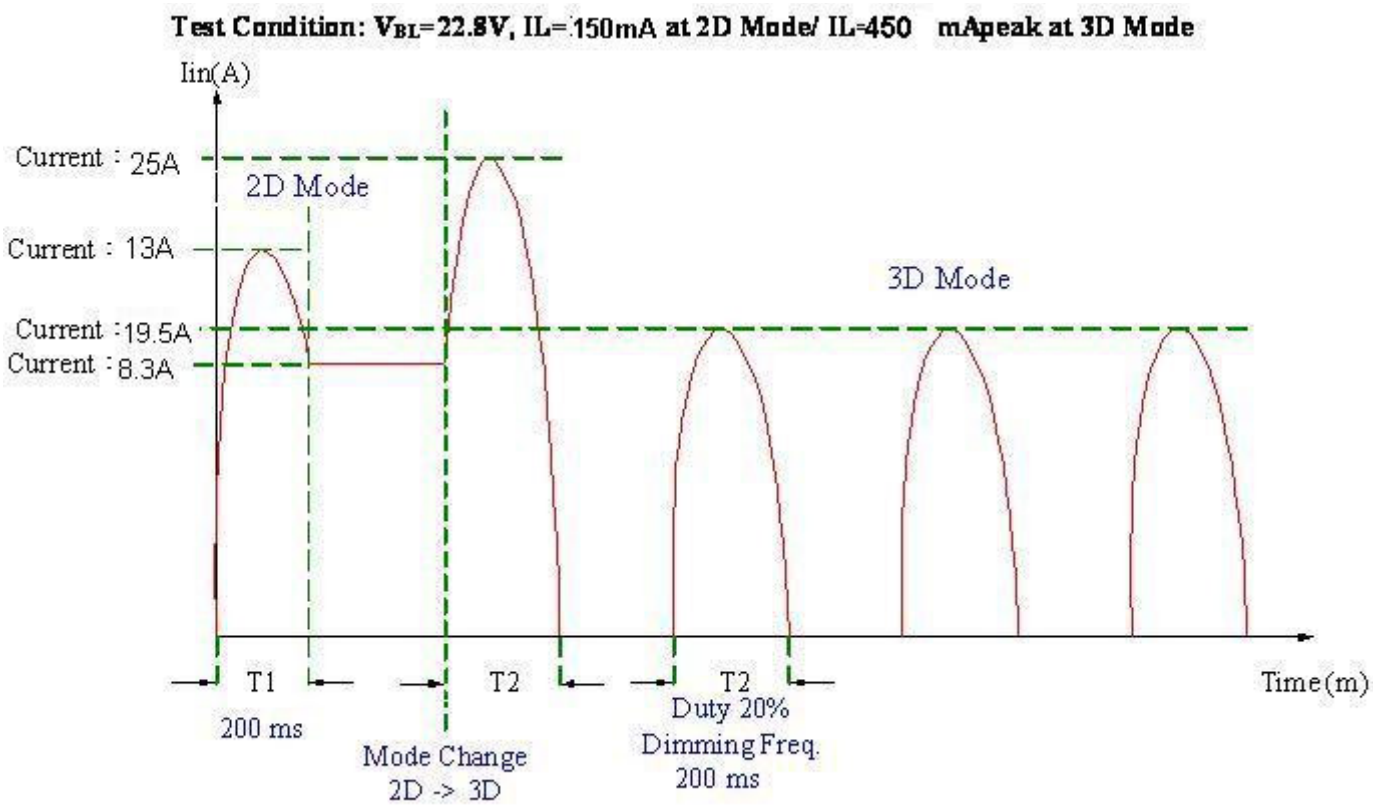
Note (2) The measurement condition of Max. value is based on 64.5" backlight unit under input voltage 24V, average LED current 150mA at 2D Mode (LED current 450mA_{peak} at 3D Mode) and lighting 1 hour later.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 30ms.

Note (4) 5% minimum duty ratio is only valid for electrical operation.

Note (5) FB and DMIN are available only at 2D Mode.

Note (6) Below diagram is only for power supply design reference.



3.2.3 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	V_{BLON}	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	V_{EPWM}	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		F_{EPWM}	—	150	160	170	Hz	Normal mode	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open collector Normal: GND (4)	
VBL Rising Time		T_{r1}	—	30	—	—	ms	10%-90%V_{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		T_{PWMR}	—	—	—	50	us	(6)	
PWM Signal Falling Time		T_{PWMF}	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		T_{PWM}	—	100	—	—	ms	(6)	
BLON Delay Time		T_{on}	—	300	—	—	ms		
		T_{on1}	—	300	—	—	ms		
BLON Off Time		T_{off}	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.2.

Note (6) EPWM is available only at 2D Mode.

Note(7): [Recommend] EPWM duty ratio is set at 100%(Max. Brightness) in 3D Mode.

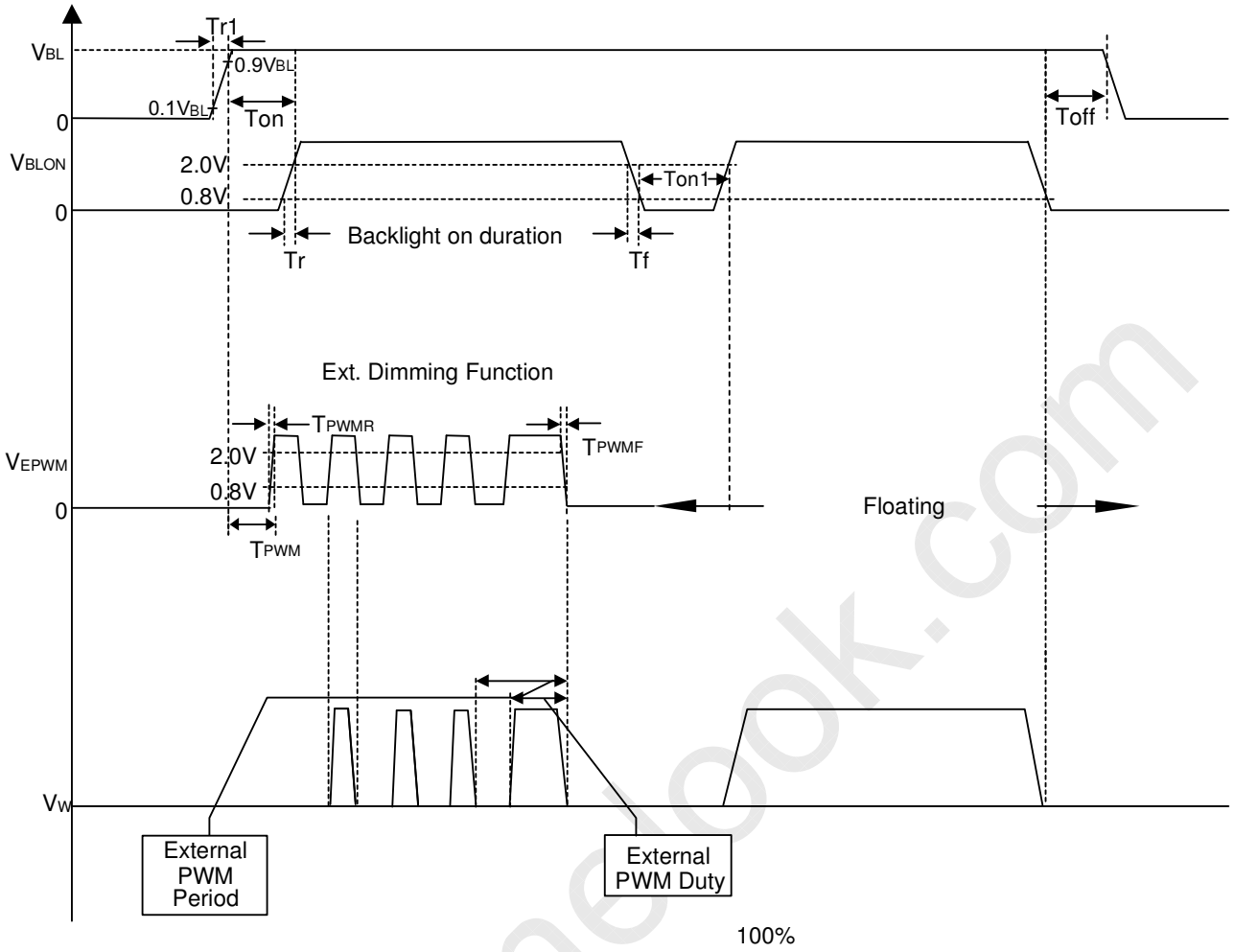


Fig. 1

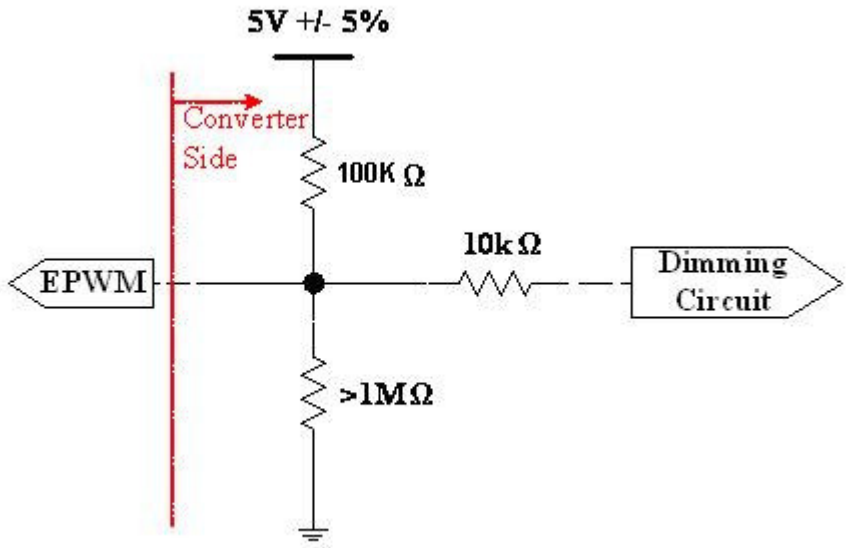
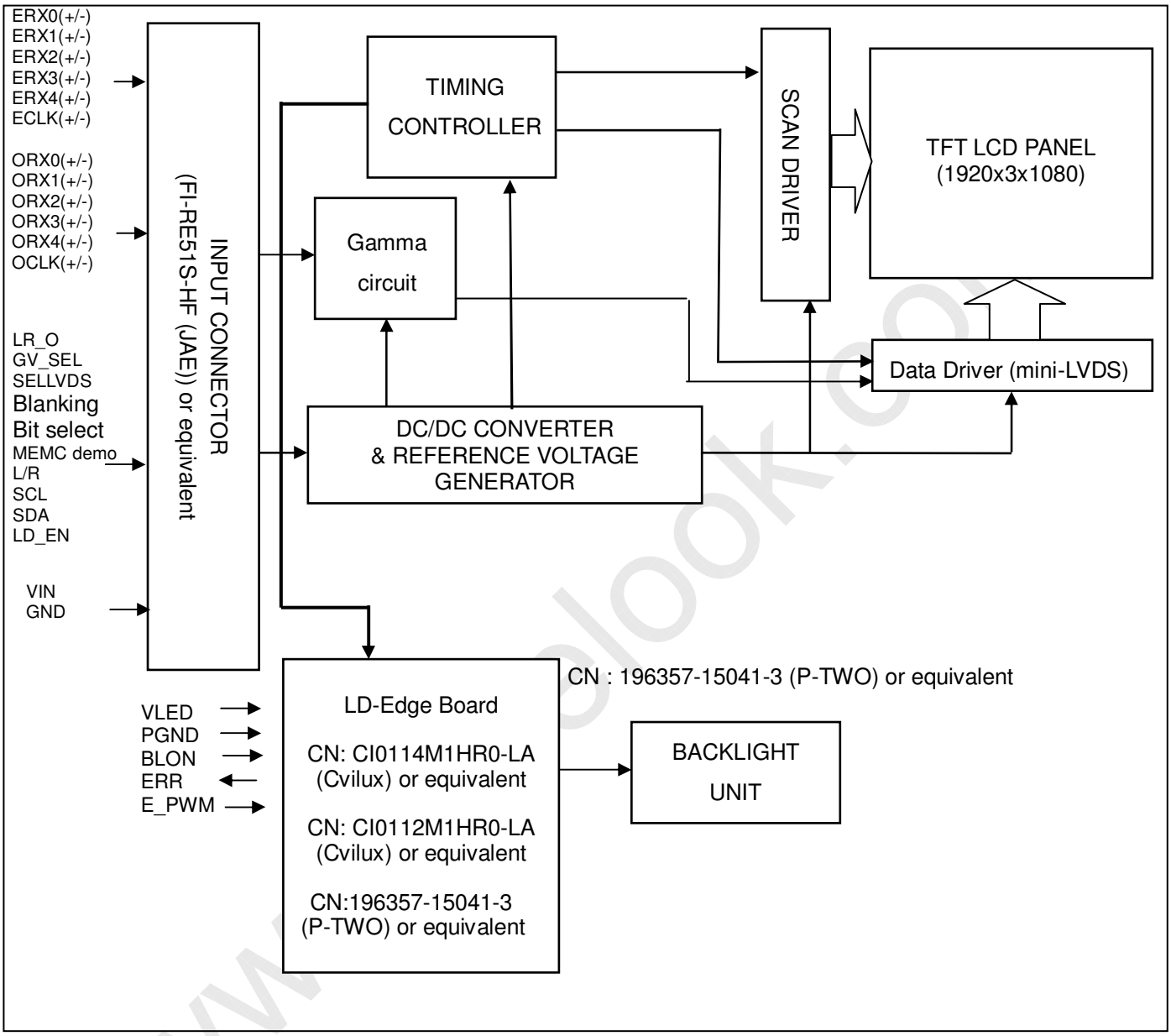


Fig. 2

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD Module Input

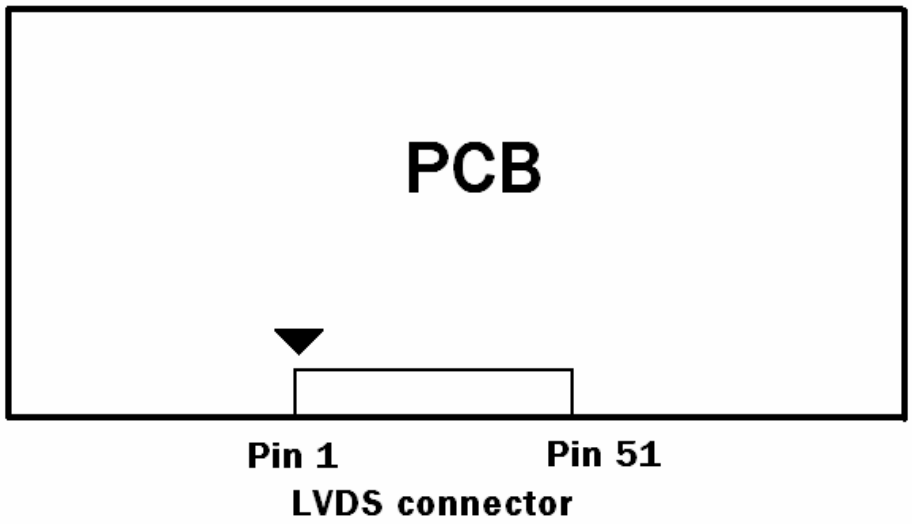
CNF1 Connector Part No.: P-TWO 187059-51221 or equivalent.

Pin	Name	Description	Note
1	NC	No Connection	(3)
2	SCL	I2C Serial Clock (for 3D format selection function)	
3	SDA	I2C Serial Data (for 3D format selection function)	
4	NC	No Connection	
5	L/R_O	Output signal for Left Right Glasses control	
6	GV_SEL	Graphic/Video mode selection	(3)
7	SELLVDS	Input signal for LVDS Data Format Selection	(4)
8	Blanking	Blanking enable	(5)
9	Bit select	8bit/10bit selection	(6)
10	MEMC demo	MEMC demo mode enable	(7)
11	GND	Ground	
12	ORX0-	1st pixel Negative LVDS differential data input. Channel 0	(1)
13	ORX0+	1st pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	1st pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	1st pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	1st pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	1st pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	1st pixel Negative LVDS differential clock input.	(1)
20	OCLK+	1st pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ORX3-	1st pixel Negative LVDS differential data input. Channel 3	(1)
23	ORX3+	1st pixel Positive LVDS differential data input. Channel 3	
24	ORX4-	1st pixel Negative LVDS differential data input. Channel 4	
25	ORX4+	1st pixel Positive LVDS differential data input. Channel 4	
26	NC	No Connection	
27	L/R	Input signal for Left Right synchronous signal	
28	ERX0-	2nd pixel Negative LVDS differential data input. Channel 0	(1)
29	ERX0+	2nd pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	2nd pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	2nd pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	2nd pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	2nd pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	2nd pixel Negative LVDS differential clock input.	(1)
36	ECLK+	2nd pixel Positive LVDS differential clock input	
37	GND	Ground	
38	ERX3-	2nd pixel Negative LVDS differential data input. Channel 3	(1)
39	ERX3+	2nd pixel Positive LVDS differential data input. Channel 3	
40	ERX4-	2nd pixel Negative LVDS differential data input. Channel 4	
41	ERX4+	2nd pixel Positive LVDS differential data input. Channel 4	

42	LD_EN	Input signal for Local Dimming Enable	(8)
43	NC	No Connection	
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	NC	No Connection	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

Note (1) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel

Note (2) LVDS connector pin order defined as follows



Note (3) G/V select. (Default : Graphic mode)

L= Connect to GND, H=Connect to +3.3V or Open

G/V select	Note
L	Video mode
H or Open	Graphic mode

Note (4) SELLVDS. (Default : VESA)

L= Connect to GND or Open, H=Connect to +3.3V

SELLVDS	Note
H or Open	VESA
L	JEIDA

Note (5) Blanking. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

Blanking	Note
L or Open	Disable
H	Enable

Note (6) Bit select. (Default : 10bit)

L= Connect to GND or Open, H=Connect to +3.3V

Bit select	Note
L or Open	10bit
H	8bit

Note (7) MEMC demo. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

MEMC demo	Note
L or Open	Disable
H	Enable

Note (8) LD_EN. (Default : Disable)

L= Connect to GND or Open, H=Connect to +3.3V

LD_EN	Note
L or Open	Disable
H	Enable

5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN3、CN6: 196357-15041-3 (P-TWO)

Pin No.	Symbol	Feature
1	NC	No Connection
2	LED1	Negative of LED String
3	LED2	Negative of LED String
4	LED3	Negative of LED String
5	LED4	Negative of LED String
6	LED5	Negative of LED String
7	LED6	Negative of LED String
8	LED7	Negative of LED String
9	LED8	Negative of LED String
10	NC	No Connection
11	NC	No Connection
12	VCC_LED	Positive of LED String
13	VCC_LED	Positive of LED String
14	VCC_LED	Positive of LED String
15	VCC_LED	Positive of LED String

CN4、CN5: 196357-15041-3 (P-TWO)

Pin No.	Symbol	Feature
1	VCC_LED	Positive of LED String
2	VCC_LED	Positive of LED String
3	VCC_LED	Positive of LED String
4	VCC_LED	Positive of LED String
5	NC	No Connection
6	NC	No Connection
7	LED8	Negative of LED String
8	LED7	Negative of LED String
9	LED6	Negative of LED String
10	LED5	Negative of LED String
11	LED4	Negative of LED String
12	LED3	Negative of LED String
13	LED2	Negative of LED String
14	LED1	Negative of LED String
15	NC	Negative of LED String

5.3 CONVERTER UNIT

CN1: CI0114M1HR0-LA (Cvilux)

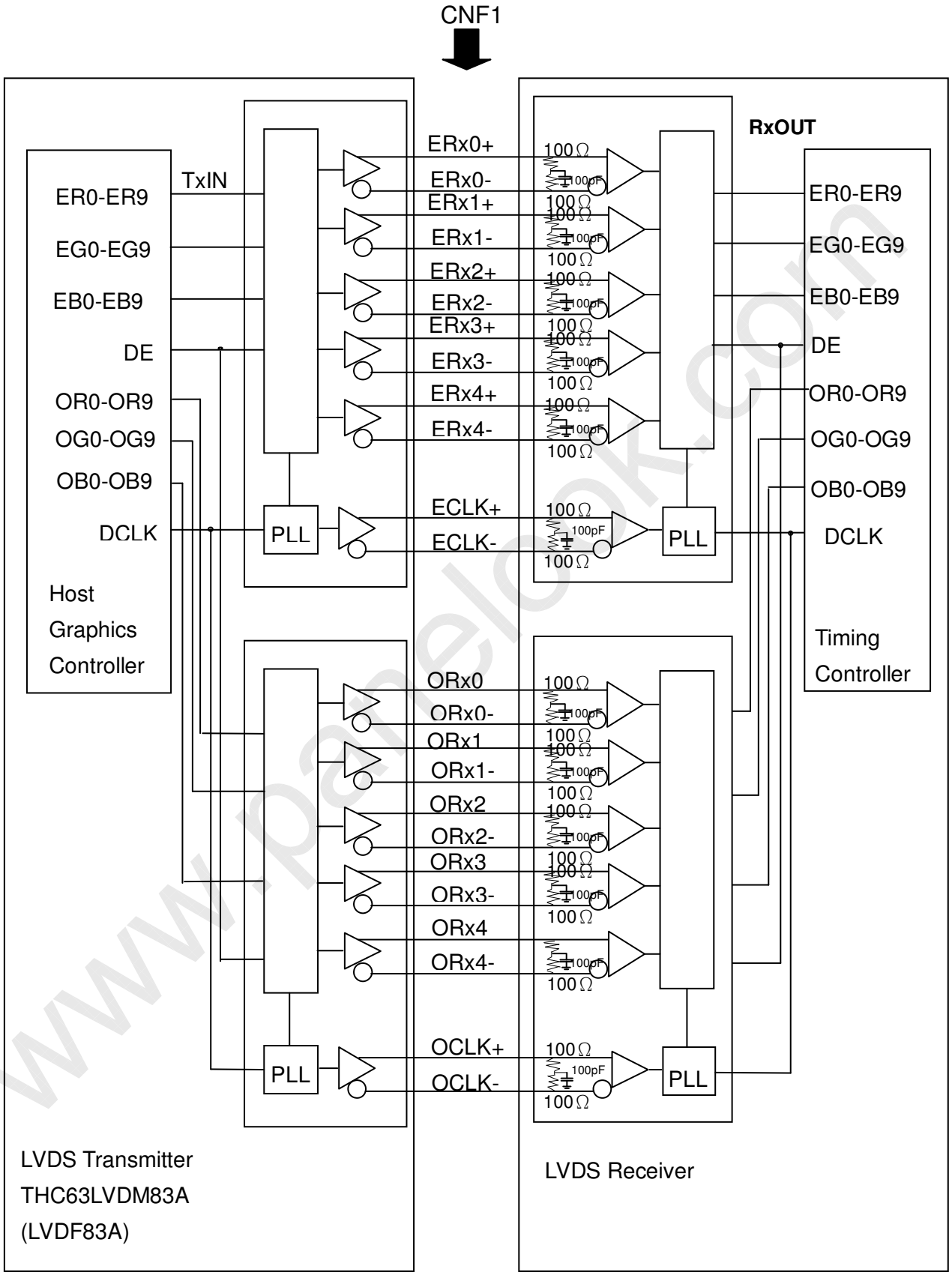
Pin №	Symbol	Feature
1	VLED	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

Notice: 1. If Pin14 is open, E_PWM is 100% duty.

CN2: CI0112M1HR0-LA (Cvilux)

Pin №	Symbol	Feature
1	VLED	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	No Connection
12	NC	No Connection

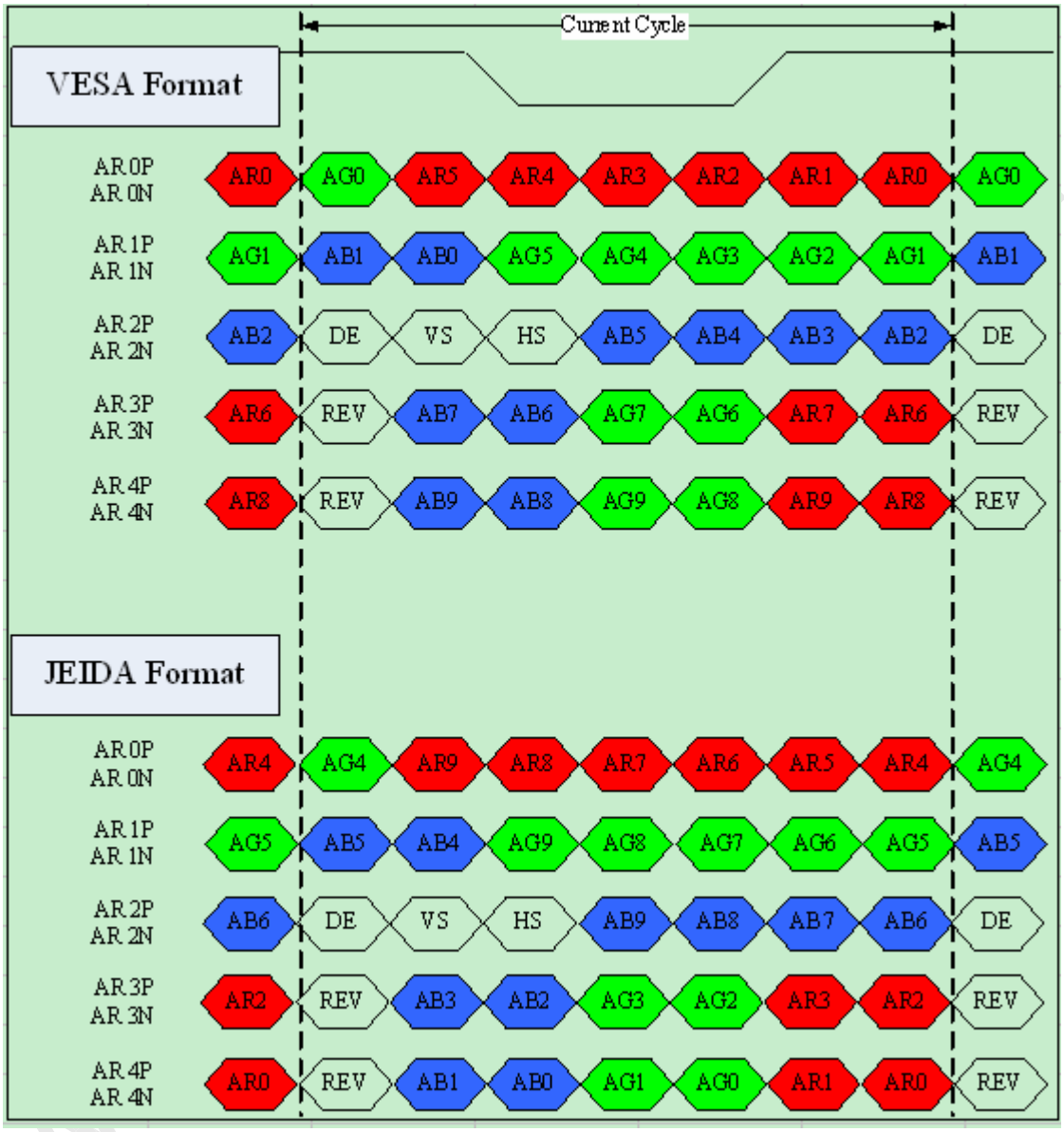
5.4 BLOCK DIAGRAM OF INTERFACE



5.5 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open



R0~R9: Pixel R Data (9; MSB, 0; LSB)

G0~G9: Pixel G Data (9; MSB, 0; LSB)

B0~B9: Pixel B Data (9; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be “H” or “L”.

5.6 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	1	0
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6. 1 INPUT SIGNAL TIMING SPECIFICATIONS

(Ta = 25 ± 2 ºC)

The input signal timing specifications are shown as the following table and timing diagram in the 2D mode.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	68	75	79	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(2)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-3%	—	F_{clkin}+3%	MHz	(3)
	Spread spectrum modulation frequency	F_{SSM}	—	—	150	KHz	(4)
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(5)

6.1.1 Timing spec for Frame Rate = 50Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	47	50	53	Hz	
Vertical Active Display Term	2D Mode	Total	Tv	1115	1350	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080			Th	–
		Blank	Tvb	35	270	315	Th	–
		Front porch	Tvfp	2	–	–	Th	(6)
		Back porch	Tvbp	4	–	–	Th	
		Vsync	Tvswid	1	–	–	Th	
Horizontal Active Display Term		Total	Th	1040	1100	1340	Tc	Th=Thd+Thb
		Display	Thd	960			Tc	–
		Blank	Thb	84	140	380	Tc	–
		Front porch	Thfp	8	–	–	Tc	(6)
		Back porch	Thbp	20	–	–	Tc	
		Hsync	Thswid	8	–	–	Tc	

6.1.2 Timing spec for Frame Rate = 60Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	57	60	63	Hz	
	3D mode		F_{r6}		60		Hz	
Vertical Active Display Term	2D Mode	Total	Tv	1115	1125	1395	Th	Tv=Tvd+Tvb
		Display	Tvd		1080		Th	—
		Blank	Tvb	35	45	315	Th	—
		Front porch	Tvfp	2	—	—	Th	(6)
		Back porch	Tvbp	4	—	—	Th	
		Vsync	Tvswid	1	—	—	Th	
	3D Mdoe	Total	Tv		1125		Th	—
		Display	Tvd		1080		Th	—
		Blank	Tvb		45		Th	—
		Front porch	Tvfp	2	—	—	—	(6)
		Back porch	Tvbp	4	—	—	—	
		Vsync	Tvswid	1	—	—	—	
Horizontal Active Display Term	2D Mode	Total	Th	1040	1100	1340	Tc	Th=Thd+Thb
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	84	140	380	Tc	—
		Front porch	Thfp	8	—	—	Tc	(6)
		Back porch	Thbp	20	—	—	Tc	
		Hsync	Thswid	8	—	—	Tc	
	3D Mdoe	Total	Th	1040	1100	1340	Tc	Th=Thd+Thb
		Display	Thd	960	960	960	Tc	—
		Blank	Thb	84	140	380	Tc	—
		Front porch	Thfp	8	—	—	Tc	(6)
		Back porch	Thbp	20	—	—	Tc	
		Hsync	Thswid	8	—	—	Tc	

6.1.3 Timing spec for 3D 720P

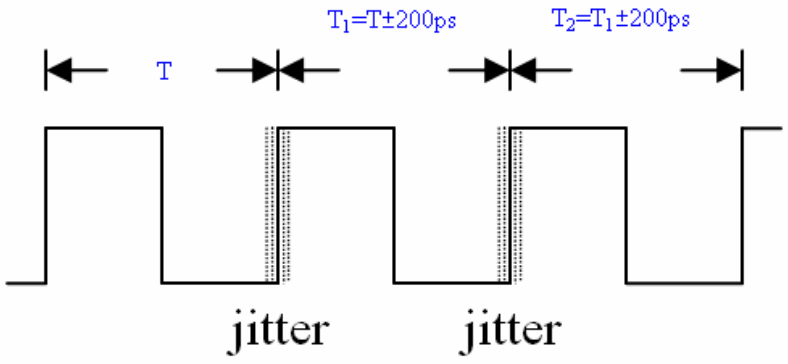
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Vertical Active Display Term	3D Mode	Total	Tv	750	800	860	Th	Tv=Tvd+Tvb
		Display	Tvd	720			Th	—
		Blank	Tvb	20	-	-	Th	—
		Front porch	Tvfp	2			Th	(6)
		Back porch	Tvbp	4			Th	
		Vsync	Tvswid	1			Th	
Horizontal Active Display Term	3D Mode	Total	Th	1600			Tc	Th=Thd+Thb
		Display	Thd	640	640	640	Tc	—
		Blank	Thb	120	-	-	Tc	—
		Front porch	Thfp	24	—	—	Tc	(6)
		Back porch	Thbp	20	—	—	Tc	
		Hsync	Thswid	8	—	—	Tc	

Note (1) Please make sure the range of pixel clock has follow the below equation：

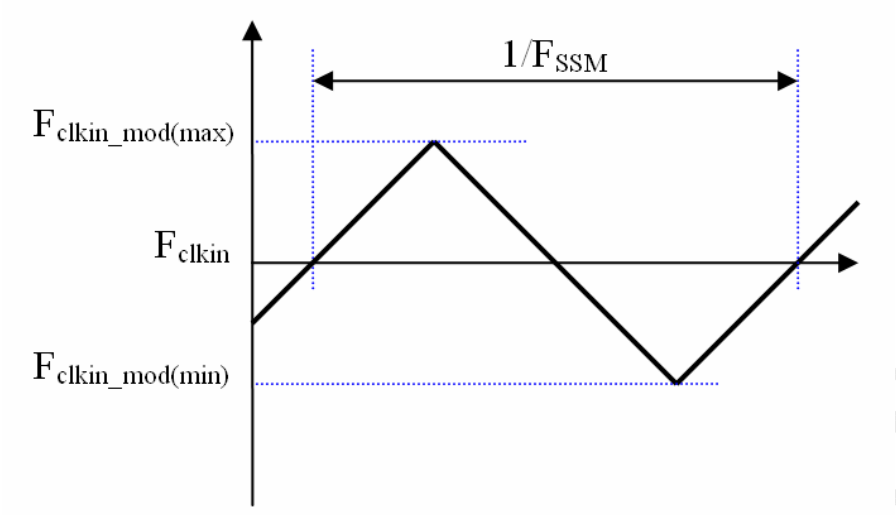
Fclkin(max) ≧ Fr6 ╳ Tv ╳ Th

Fr5 ╳ Tv ╳ Th ≧ Fclkin(min)

Note (2) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note (3) The SSCG (Spread spectrum clock generator) is defined as below figures.

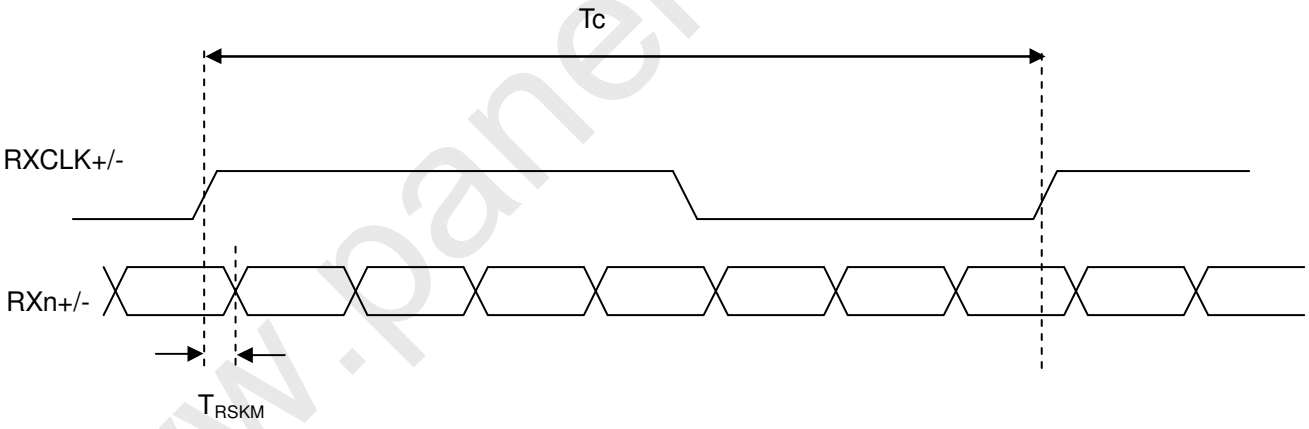


Note (4) Spread spectrum range should be constricted as below.

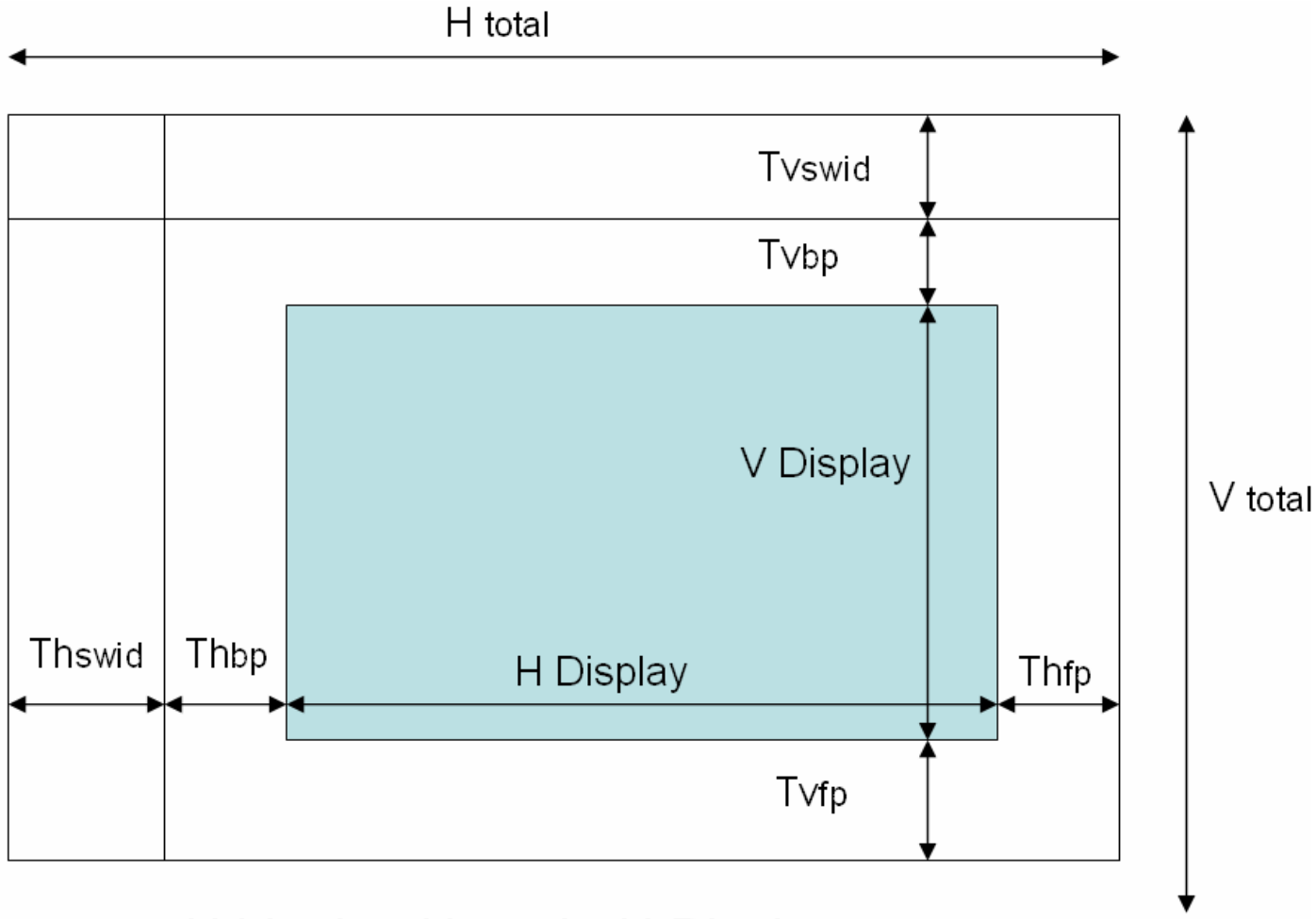
SS Deviation (%) ╳ SS Modulation Frequency (KHz) ≦ 150 (% • KHz)

Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) This module is need Hsync 、Vsync please follow the input signal timing diagram below :



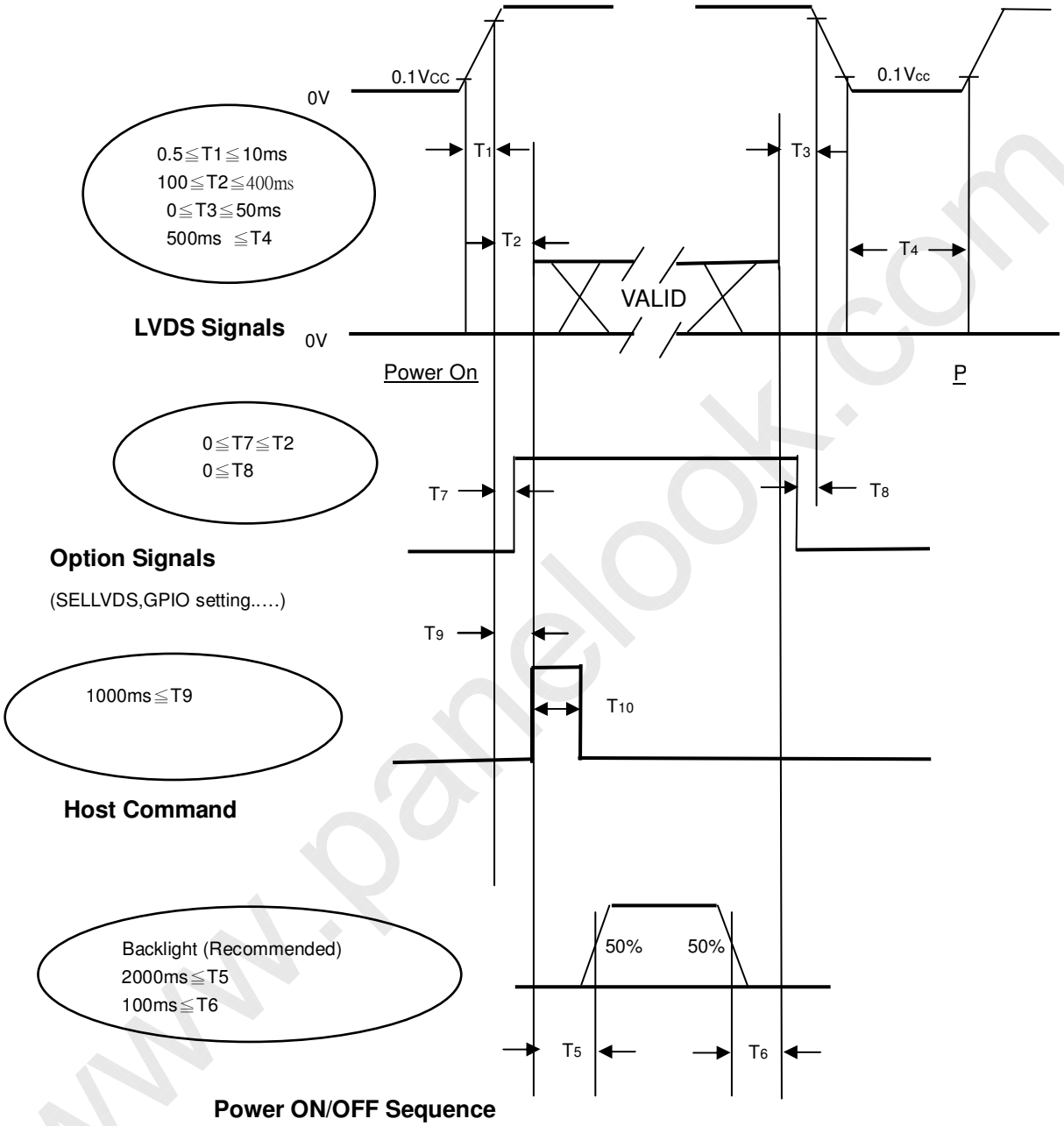
H blank = H total - H Display

V blank = V total - V Display

6.2 POWER ON/OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of VCC is in off level, please keep the level of input signals on the low or high impedance.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

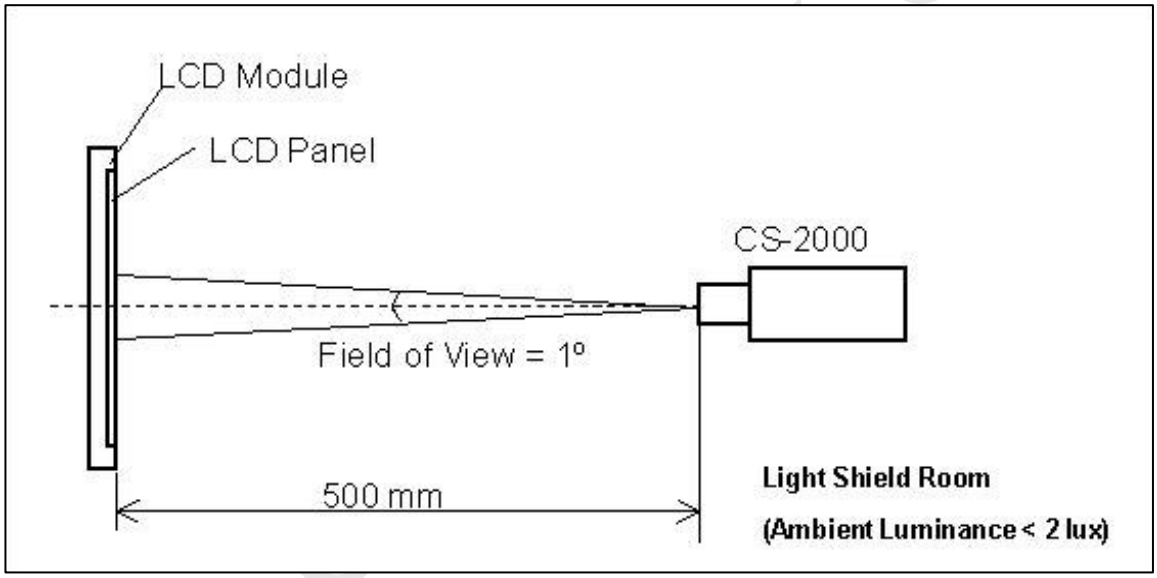
Note (6) T10 depends on the initial setting commands

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	I_L	150± 4.5	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



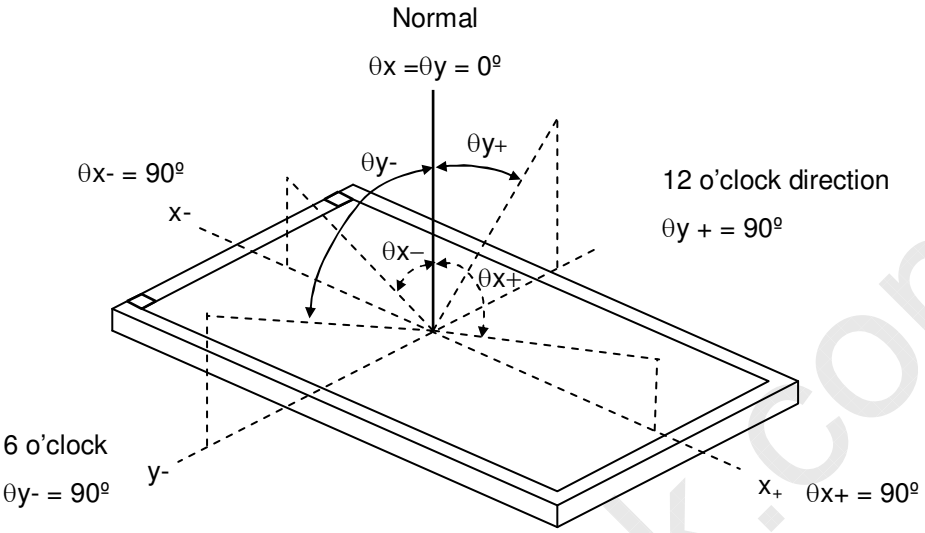
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		θx=0°, θy =0° Viewing angle at normal direction	3000	5000	-	-	(2)
Response Time (VA)		Gray to gray			-	5.5	-	ms	(3)
Center Luminance of White		L_C	2D		320	400	-	cd/m^2	(4)
			3D		-	70	-	cd/m^2	(8)
White Variation		δW			-	-	1.3	-	(6)
Cross Talk		CT	2D		-	-	4	%	(5)
			3D-W		-	4	-	%	(8)
			3D-D		-	11	-	%	(8)
Color Chromaticity	Red	Rx			Typ. -0.03	0.637	Typ. +0.03	-	-
		Ry				0.339		-	
	Green	Gx				0.302		-	
		Gy				0.613		-	
	Blue	Bx				0.151		-	
		By				0.059		-	
	White	Wx				0.280		-	
		Wy				0.290		-	
	Correlated color temperature				-	10000	-	K	-
	Color Gamut	C.G.			-	70	-	%	NTSC
Viewing Angle	Horizontal	θx+		CR≥20 (VA)	80	88	-	Deg.	(1)
		θx-			80	88	-		
	Vertical	θy+			80	88	-		
		θy-			80	88	-		
Transmission direction of the up polarizer		Φ_{up-P}		-	-	90	-	Deg.	(7)

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

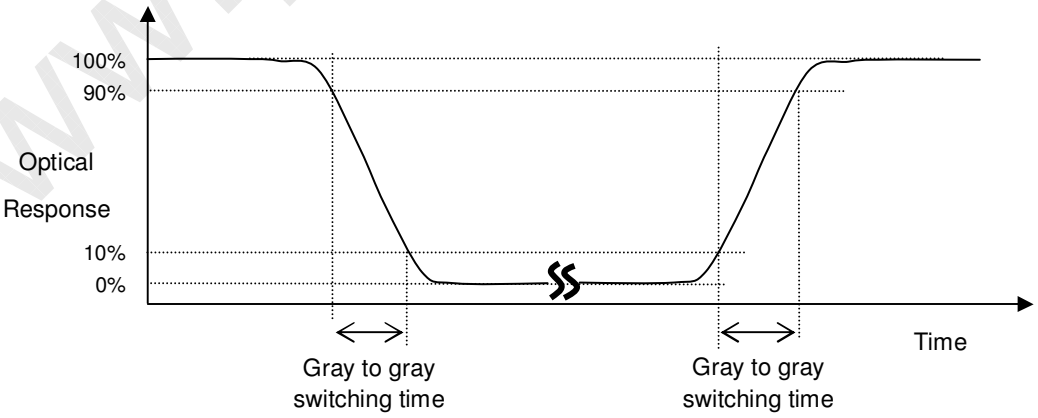
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L255}}{\text{Surface Luminance of L0}}$$

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

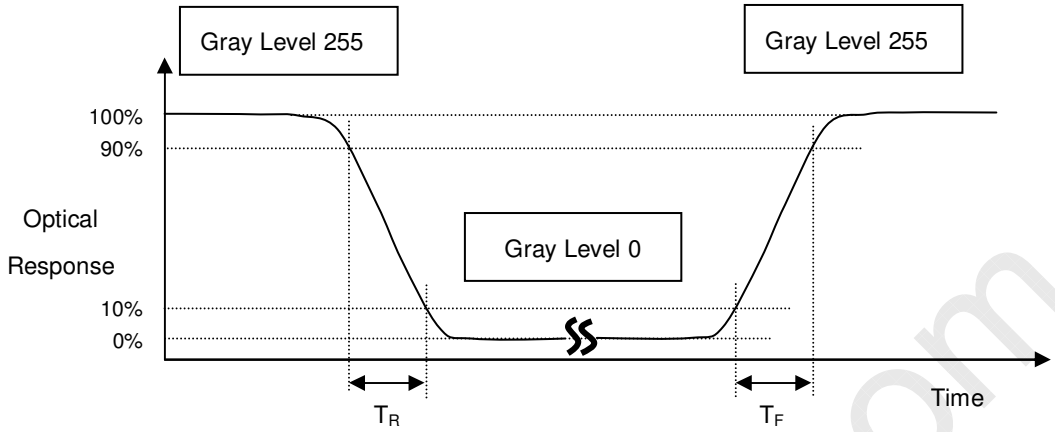
Note (3) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255

Gray to gray average time means the average switching time of gray level 0, 31, 63, 95, 127, 159, 191, 223 and 255 to each other.

Note (3) Definition of Response Time (T_R, T_F):



Note (4) Definition of Luminance of White (L_C):

Measure the luminance of gray level 255 at center point and 5 points

L_C = L (5), where L (X) is corresponding to the luminance of the point X at the figure in Note (6)..

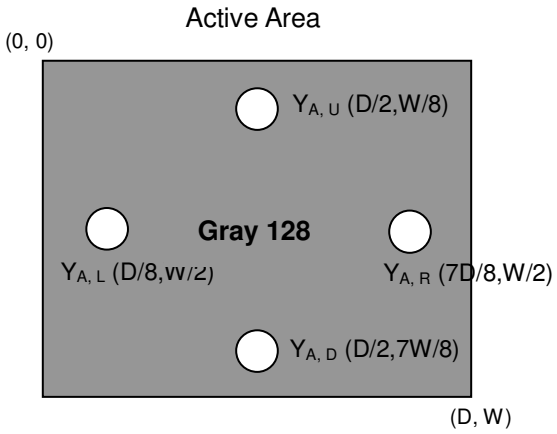
Note (5) Definition of Cross Talk (CT):

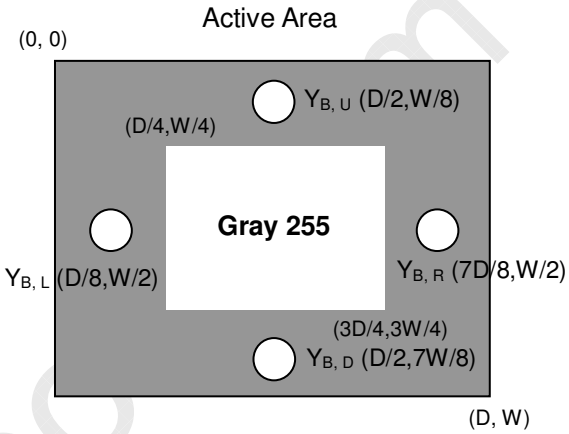
$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where:

Y_A = Luminance of measured location without gray level 255 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m2)

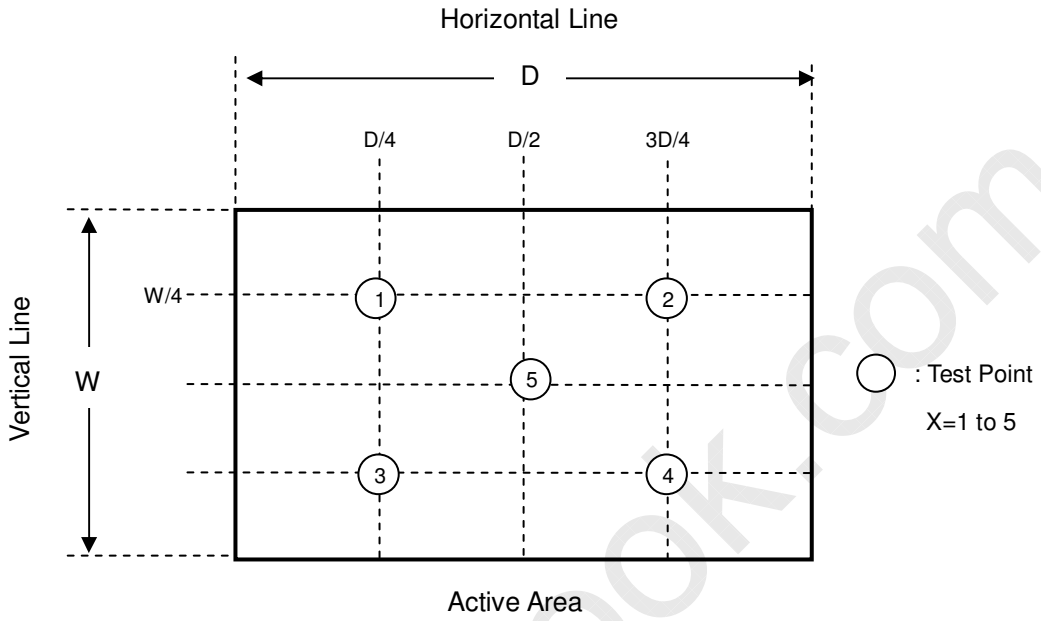




Note (6) Definition of White Variation (δW):

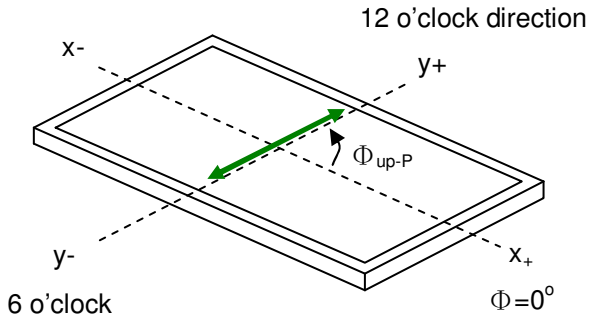
Measure the luminance of gray level 255 at 5 points

δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



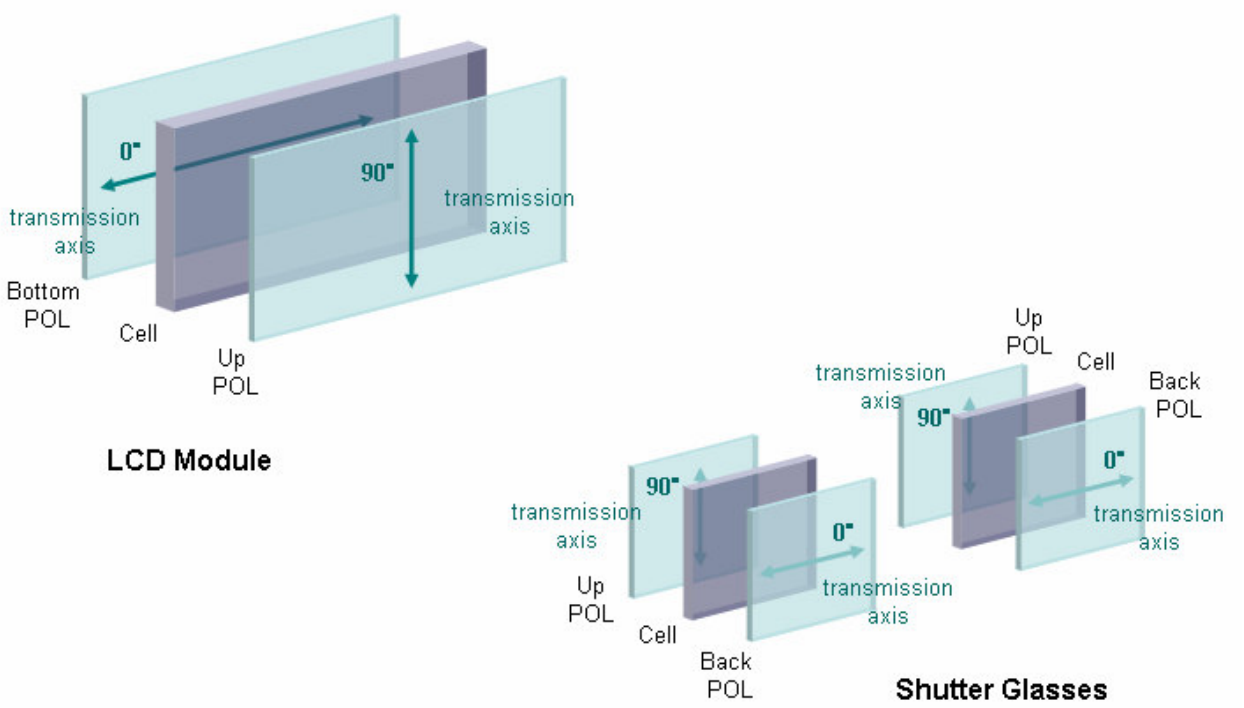
Note (7) This is a reference for designing the shutter glasses of 3D application.

Definition of the transmission direction of the up polarizer($\Phi_{up\text{-}P}$) on LCD Module:



Up Polarizer

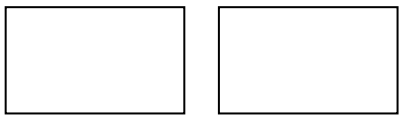
The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



Note (8) Definition of the 3D mode performance (measured under 3D mode, use CMI's shutter glass):

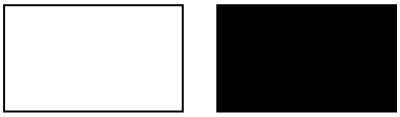
a. Test pattern

Left eye image and right eye image are displayed alternated



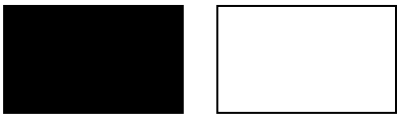
WW

Left eye image: W255; Right eye image: W255



WB

Left eye image: W255; Right eye image: W0

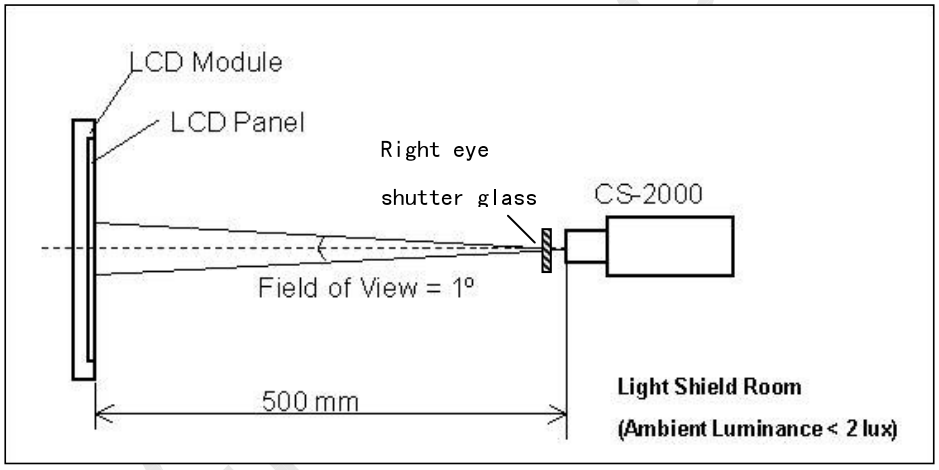


BW

Left eye image: W0; Right eye image: W255

Vertical Line

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation.

The luminance of the test pattern "WW", denoted L(WW); the luminance of the test pattern "WB", denoted L(WB); the luminance of the test pattern "BW", denoted L(BW); the luminance of the test pattern "BB", denoted "L(BB)

c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \left| \frac{L(WB) - L(BB)}{L(WW) - L(BB)} \right|$

Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \left| \frac{L(WW) - L(BW)}{L(WW) - L(BB)} \right|$

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

[3] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[4] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not plug in or pull out the I/F connector while the module is in operation.

[6] Do not disassemble the module.

[7] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

[8] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[9] When storing modules as spares for a long time, the following precaution is necessary.

[9.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

[9.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

8.2 SAFETY PRECAUTIONS

[1] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.

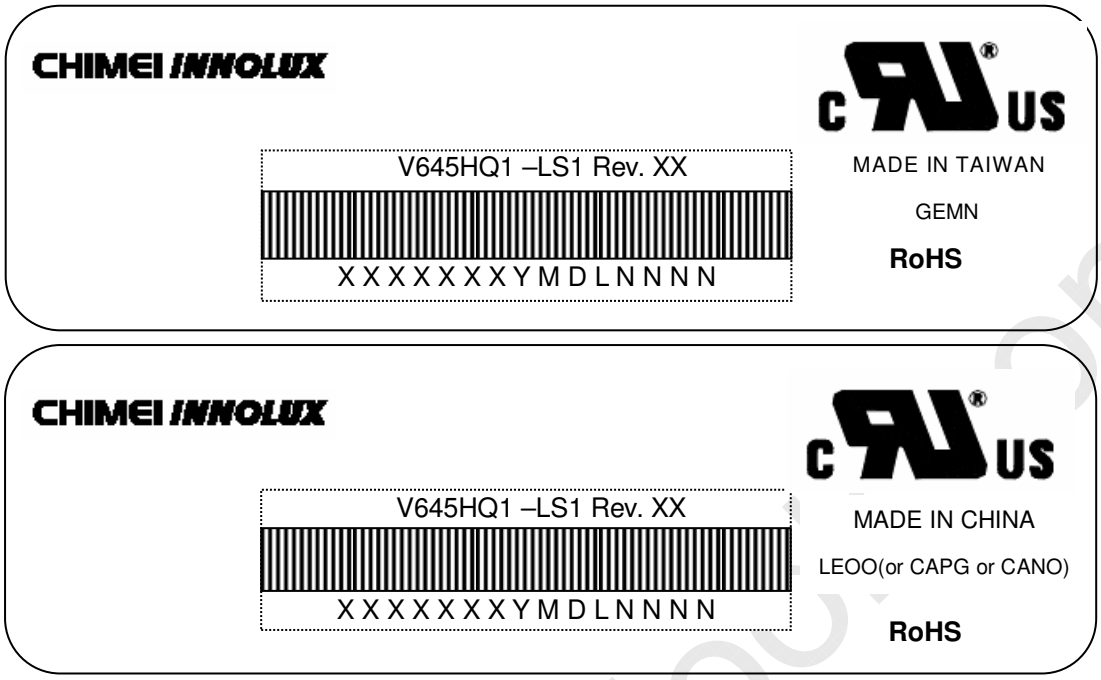
[2] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[3] After the module's end of life, it is not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 CMI MODULE LABEL

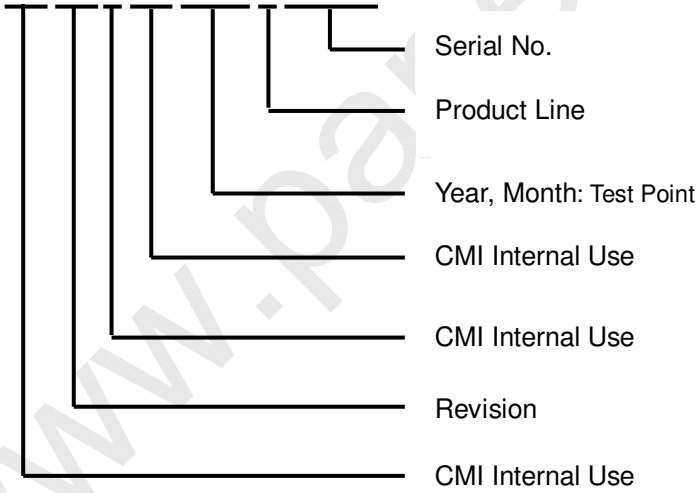
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



Model Name: V645HQ1-LS1

Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID: X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 15 LCD TV modules / 1 Box

(2) Box dimensions : 1637(L)x1128(W)x955(H)mm

(3) Weight : Approx. 480 Kg(15 modules per carton)

10.2 PACKAGING METHOD

Figures 10-1 and 10-2 are the packing method

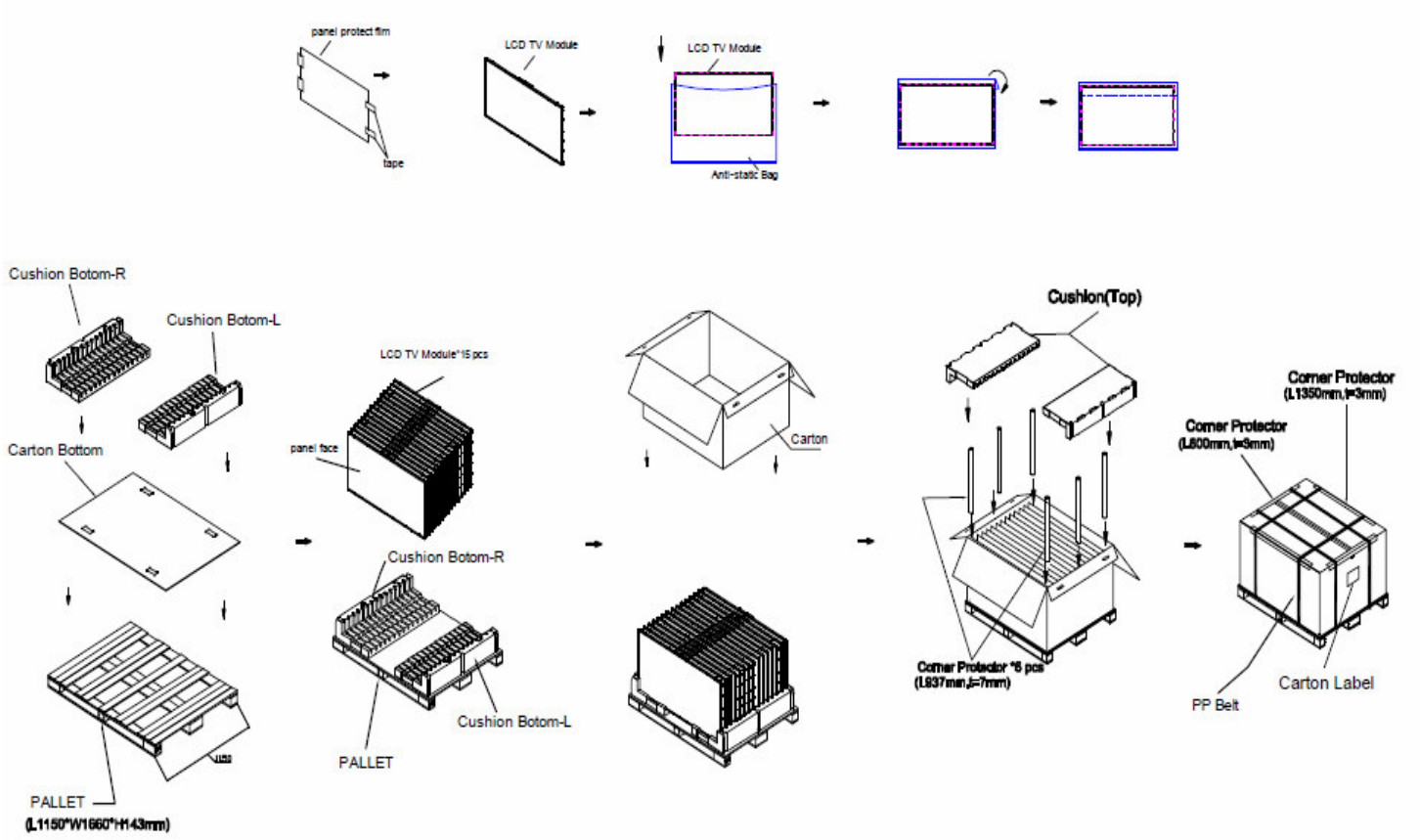
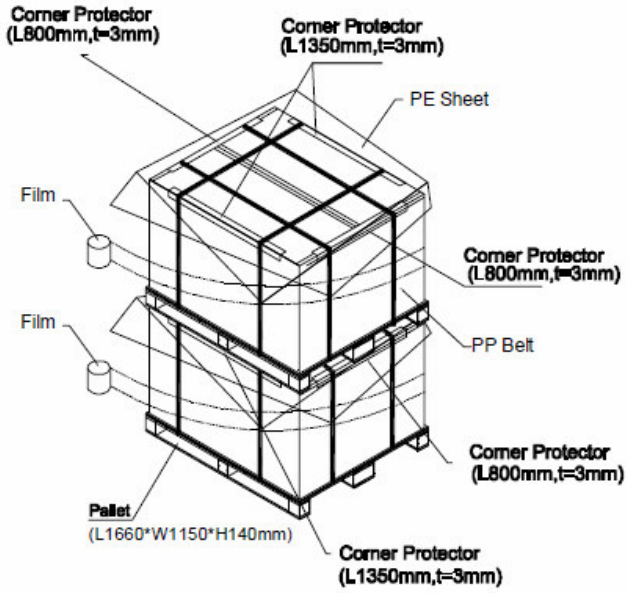
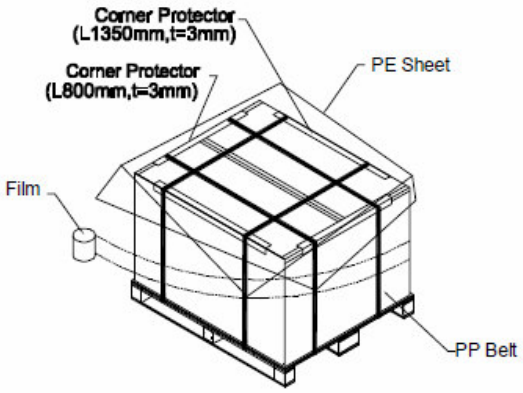


Figure 10-1 packing method

Sea & Land Transportation



Air Transportation



11. MECHANICAL CHARACTERISTIC