□ Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V650HP1

SUFFIX: PS6

Ver. B2

Customer:

APPROVED BY SIGNATURE

Name / Title

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Perry Lin	Chloe Chen

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 2.0	10/11, 2012	All	All	The approval specification was been released.

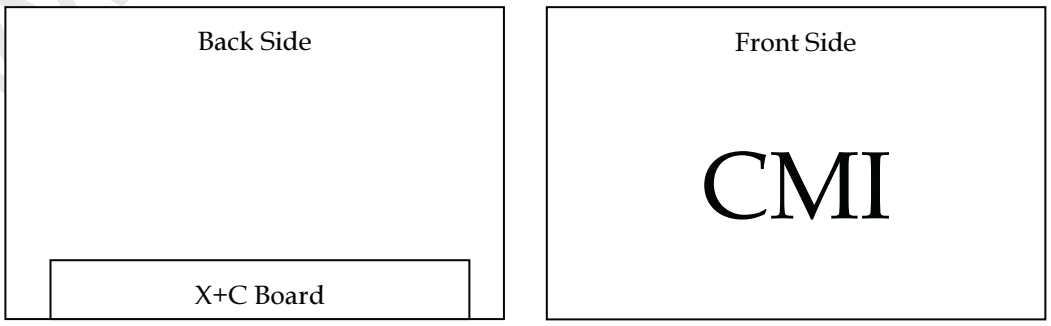
1. GENERAL DESCRIPTION

1.1 OVERVIEW

V650HP1-PS6 is a 65" TFT Liquid Crystal Display product with driver ICs and 4ch-LVDS interface. This product supports 1920 x 1080 HDTV format and can display true 1.07G colors (8-bit+FRC). The backlight unit is not built in.

1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Pixels [lines]	1920 × 1080
Active Area [mm]	1428.48 (H) x 803.52 (V)
Sub-Pixel Pitch [mm]	0.248 (H) x 0.744 (V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	4526
Physical Size [mm]	1455.76 (W) x 856.12(H) x 1.705(D) Typ
Display Mode	Transmissive mode / Normally black
Contrast Ratio	5000:1 Typ. (Typical value measured at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20) (VA Model)	+88/-88(H),+88/-88(V) Typ. (Typical value measured by CMI's module)
Color Chromaticity	R=0.651, 0.329 G=0.265, 0.591 B=0.132, 0.120 W=0.299, 0.351 *Please refer to "color chromaticity" in 7.2
Cell Transparency [%]	6.3%Typ * Please refer to "Center Transmittance" in 7.2
Polarizer Surface Treatment	Anti-Glare coating (Haze 1%)
Rotation Function	Unachievable
Display Orientation	Signal input with "CMI"

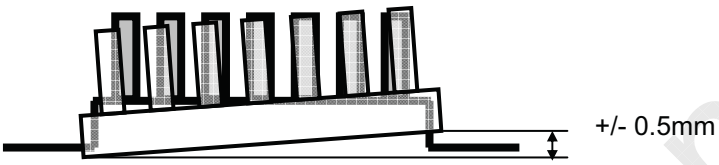


1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight	4222.75	4445	4667.25	g	-
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(2)

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Connector mounting position



2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1), (3)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2), (3)

Note (1) Temperature and relative humidity range is shown in the figure below.

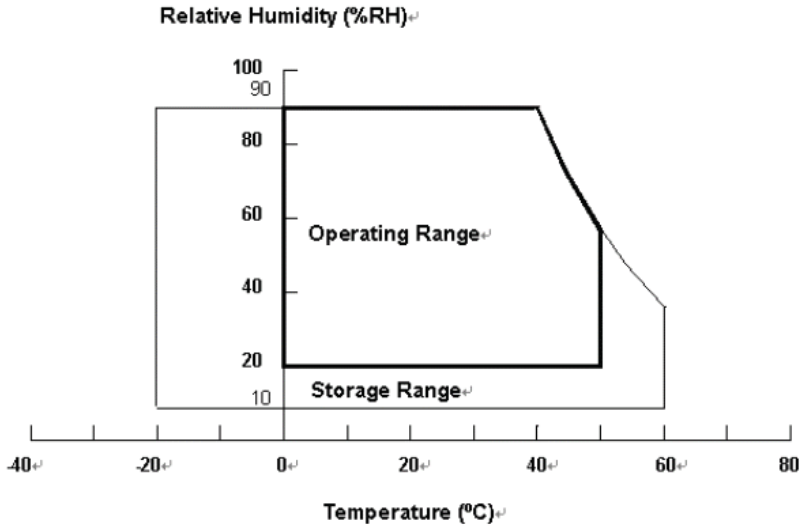
(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

(c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) The rating of environment is base on LCD module. Leave LCD cell alone, this environment condition can't be guaranteed. Except LCD cell, the customer has to consider the ability of other parts of LCD module and LCD module process.



2.2 ABSOLUTE RATINGS OF ENVIRONMENT (OPEN CELL)

Recommended Storage Condition: With shipping package.

Recommended Storage temperature range: 25±5 ℃

Recommended Storage humidity range: 50±10%RH

Recommended Shelf life: a month

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	VCC	-0.3	13.5	V	(1)
Logic Input Voltage	VIN	-0.3	3.6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

3. ELECTRICAL CHARACTERISTICS

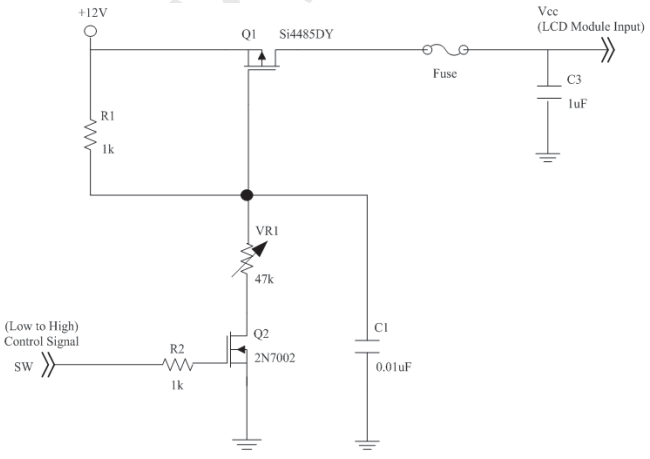
3.1 TFT LCD Module

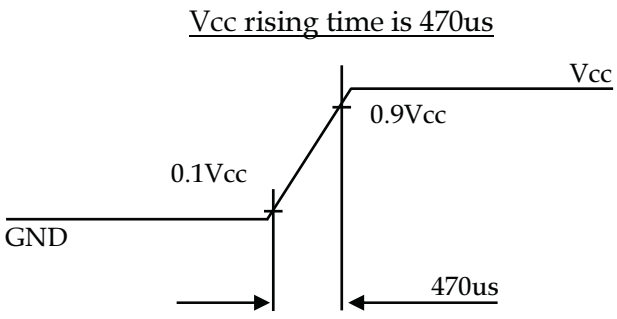
(Ta = 25 ± 2 °C)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	–	–	3.2	A	(2)
Power consumption	White Pattern	P_T	–	7.68	9.24	W	(3)
	Black Pattern	P_T	–	7.56	9.12		
	Horizontal Stripe	P_T	–	14.88	18		
Power Supply Current	White Pattern	P_T	–	0.64	0.77	A	
	Black Pattern	P_T	–	0.63	0.76		
	Horizontal Stripe	P_T	–	1.24	1.5		
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	–	+300	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	-300	–	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	–	600	mV	
	Terminating Resistor	R_T	–	100	–	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	–	3.3	V	–
	Input Low Threshold Voltage	V_{IL}	0	–	0.7	V	–

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.).

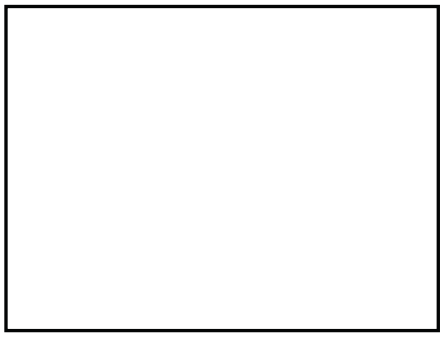
Note (2) Measurement condition :





Note (3) The specified power consumption and power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

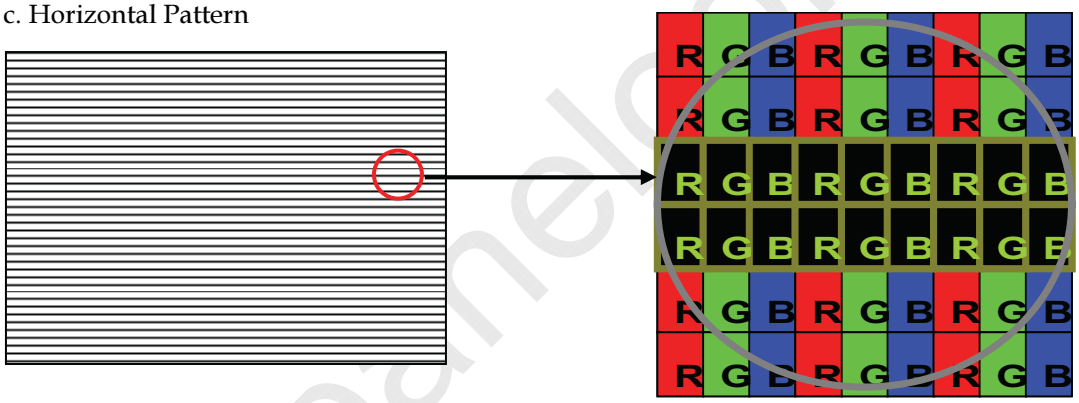


Active Area

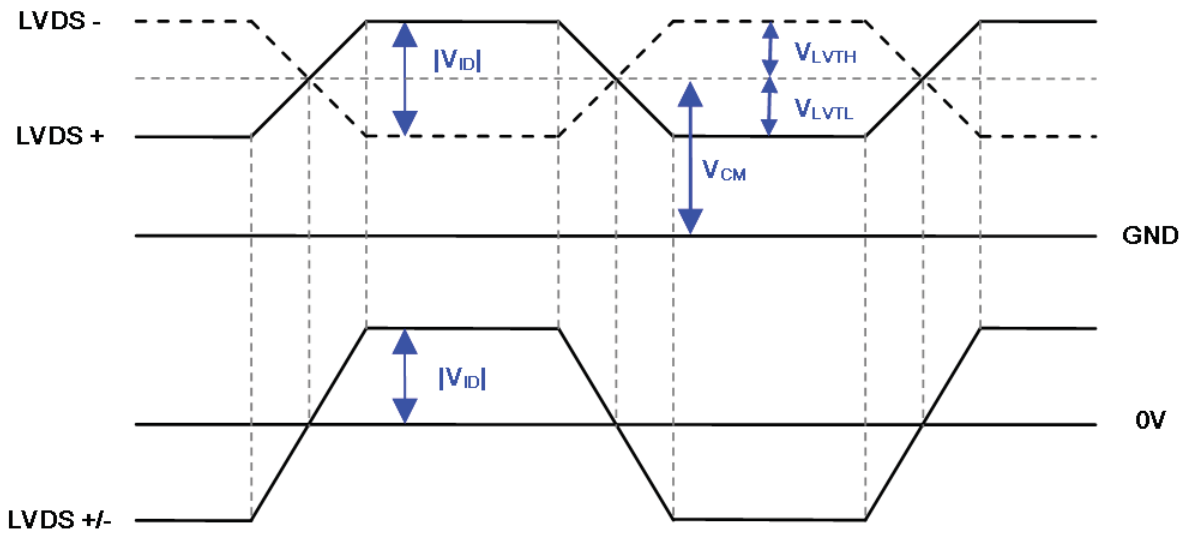
b. Black Pattern

Active Area

c. Horizontal Pattern

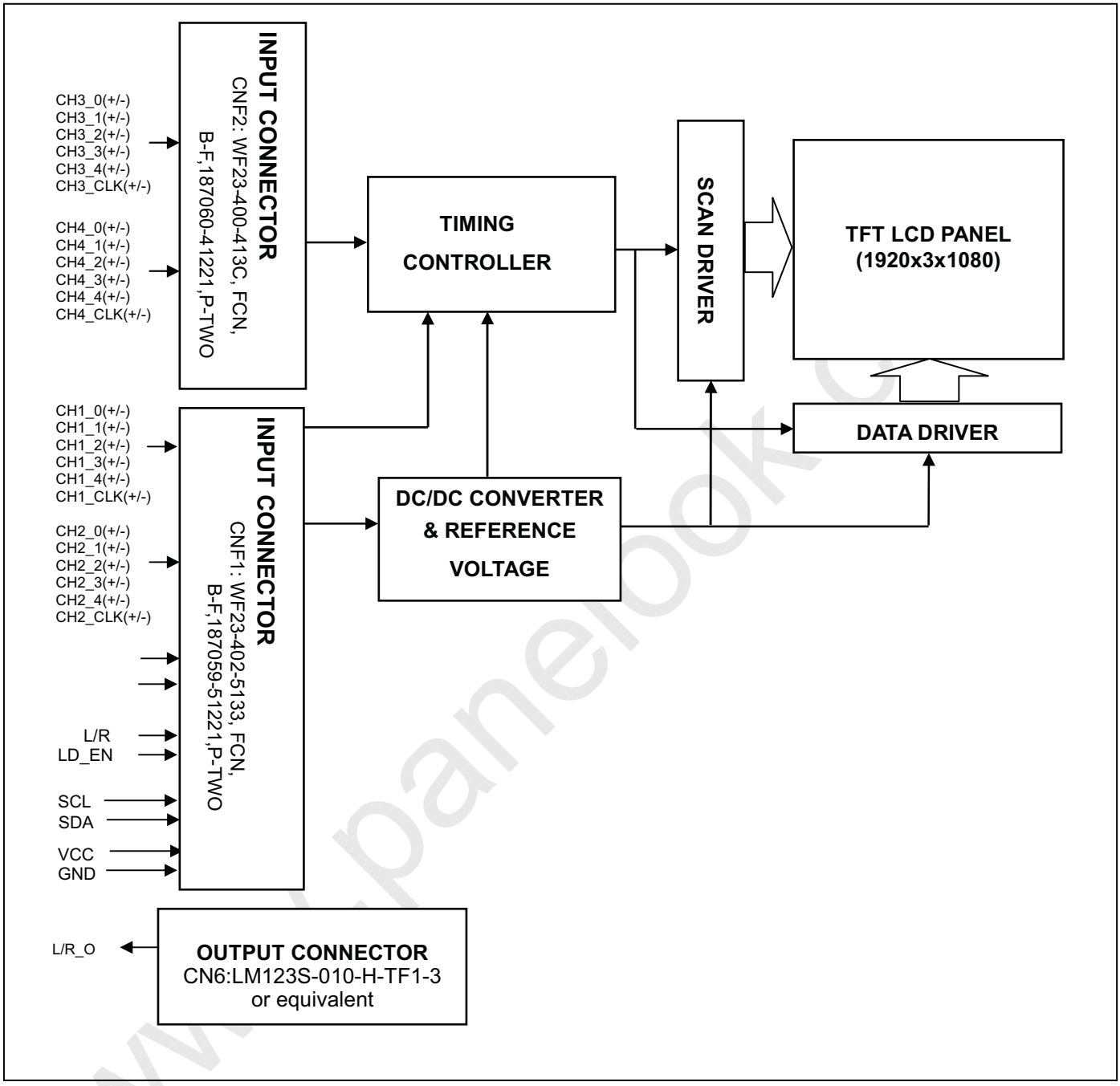


Note (4) The LVDS input characteristics are as follows:



4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5. INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD OPEN CELL

CNF1 Connector pin assignment: (WF23-402-5133 (FCN), B-F,187059-51221(P-TWO)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	EEPROM Serial Clock (for local dimming demo function)	(11)
3	SDA	EEPROM Serial Data (for local dimming demo function)	
4	TST_AGE	Aging Mode	(10)
5	L/R_O	Output signal for Left Right Glasses control	(9)
6	N.C.	No Connection	(1)
7	SELLVDS	Input signal for LVDS Data Format Selection	(2)(6)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	CH1[0]-	First pixel Negative LVDS differential data input. Pair 0	(8)
13	CH1[0]+	First pixel Positive LVDS differential data input. Pair 0	
14	CH1[1]-	First pixel Negative LVDS differential data input. Pair 1	
15	CH1[1]+	First pixel Positive LVDS differential data input. Pair 1	
16	CH1[2]-	First pixel Negative LVDS differential data input. Pair 2	
17	CH1[2]+	First pixel Positive LVDS differential data input. Pair 2	
18	GND	Ground	
19	CH1CLK-	First pixel Negative LVDS differential clock input.	(8)
20	CH1CLK+	First pixel Positive LVDS differential clock input.	
21	GND	Ground	
22	CH1[3]-	First pixel Negative LVDS differential data input. Pair 3	(8)
23	CH1[3]+	First pixel Positive LVDS differential data input. Pair 3	
24	CH1[4]-	First pixel Negative LVDS differential data input. Pair 4	
25	CH1[4]+	First pixel Positive LVDS differential data input. Pair 4	
26	2D/3D	Input signal for 2D/3D Mode Selection(Frame sequence mode)	(3) (7)
27	L/R	Input signal for Left Right eye frame synchronous	(4)(7)
28	CH2[0]-	Second pixel Negative LVDS differential data input. Pair 0	(8)

29	CH2[0]+	Second pixel Positive LVDS differential data input. Pair 0	
30	CH2[1]-	Second pixel Negative LVDS differential data input. Pair 1	
31	CH2[1]+	Second pixel Positive LVDS differential data input. Pair 1	
32	CH2[2]-	Second pixel Negative LVDS differential data input. Pair 2	
33	CH2[2]+	Second pixel Positive LVDS differential data input. Pair 2	
34	GND	Ground	
35	CH2CLK-	Second pixel Negative LVDS differential clock input.	(8)
36	CH2CLK+	Second pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	CH2[3]-	Second pixel Negative LVDS differential data input. Pair 3	(8)
39	CH2[3]+	Second pixel Positive LVDS differential data input. Pair 3	
40	CH2[4]-	Second pixel Negative LVDS differential data input. Pair 4	
41	CH2[4]+	Second pixel Positive LVDS differential data input. Pair 4	
42	LD_EN	Input signal for Local Dimming Enable	(5)(6)
43	N.C.	No Connection	(1)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	(1)
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

CNF2 Connector pin assignment (WF23-400-413C (FCN) B-F,187060-41221(P-TWO)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	N.C.	No Connection	
5	N.C.	No Connection	
6	N.C.	No Connection	

7	N.C.	No Connection	
8	N.C.	No Connection	
9	GND	Ground	
10	CH3[0]-	Third pixel Negative LVDS differential data input. Pair 0	(8)
11	CH3[0]+	Third pixel Positive LVDS differential data input. Pair 0	
12	CH3[1]-	Third pixel Negative LVDS differential data input. Pair 1	
13	CH3[1]+	Third pixel Positive LVDS differential data input. Pair 1	
14	CH3[2]-	Third pixel Negative LVDS differential data input. Pair 2	
15	CH3[2]+	Third pixel Positive LVDS differential data input. Pair 2	
16	GND	Ground	
17	CH3CLK-	Third pixel Negative LVDS differential clock input.	(8)
18	CH3CLK+	Third pixel Positive LVDS differential clock input.	
19	GND	Ground	
20	CH3[3]-	Third pixel Negative LVDS differential data input. Pair 3	(8)
21	CH3[3]+	Third pixel Positive LVDS differential data input. Pair 3	
22	CH3[4]-	Third pixel Negative LVDS differential data input. Pair 4	
23	CH3[4]+	Third pixel Positive LVDS differential data input. Pair 4	
24	GND	Ground	
25	GND	Ground	
26	CH4[0]-	Fourth pixel Negative LVDS differential data input. Pair 0	(8)
27	CH4[0]+	Fourth pixel Positive LVDS differential data input. Pair 0	
28	CH4[1]-	Fourth pixel Negative LVDS differential data input. Pair 1	
29	CH4[1]+	Fourth pixel Positive LVDS differential data input. Pair 1	
30	CH4[2]-	Fourth pixel Negative LVDS differential data input. Pair 2	
31	CH4[2]+	Fourth pixel Positive LVDS differential data input. Pair 2	
32	GND	Ground	
33	CH4CLK-	Fourth pixel Negative LVDS differential clock input.	(8)
34	CH4CLK+	Fourth pixel Positive LVDS differential clock input.	
35	GND	Ground	
36	CH4[3]-	Fourth pixel Negative LVDS differential data input. Pair 3	(8)
37	CH4[3]+	Fourth pixel Positive LVDS differential data input. Pair 3	
38	CH4[4]-	Fourth pixel Negative LVDS differential data input. Pair 4	

39	CH4[4]+	Fourth pixel Positive LVDS differential data input. Pair 4	
40	GND	Ground	
41	GND	Ground	

CN6 Connector pin assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(9)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection. (2D/3D mode is only controlled by this pin)

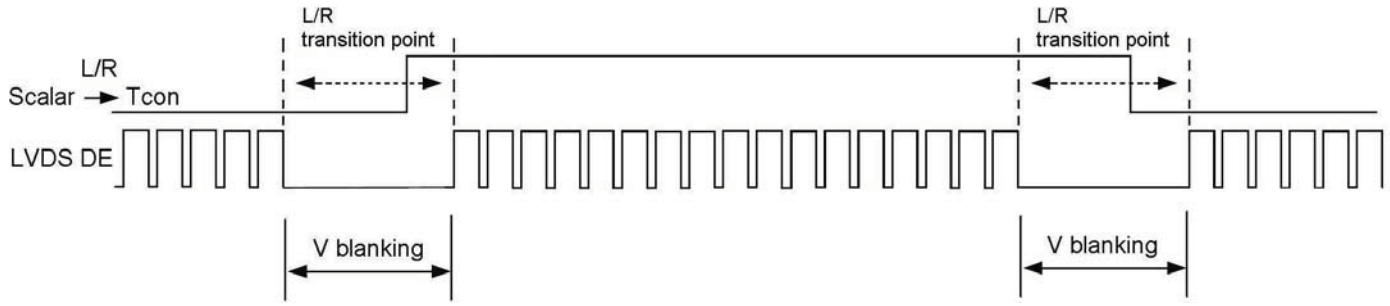
L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

V_{IL}=0V~0.7 V, V_{IH}=2.7V~3.3 V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal



Note (5) Local dimming enable selection.

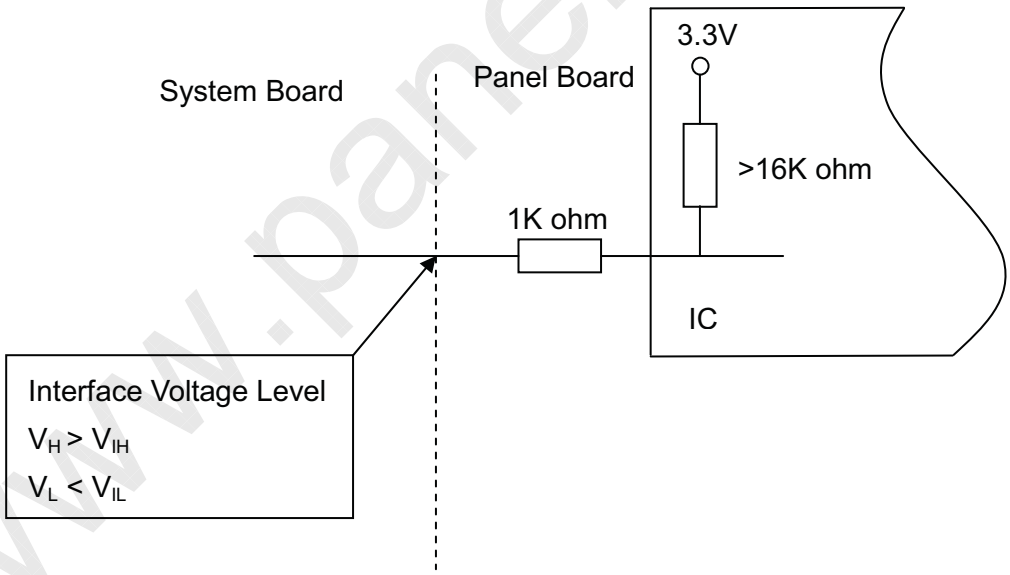
L= Connect to GND , H=Connect to +3.3Vor Open

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

LD_EN enable pin should be set in power on stage.

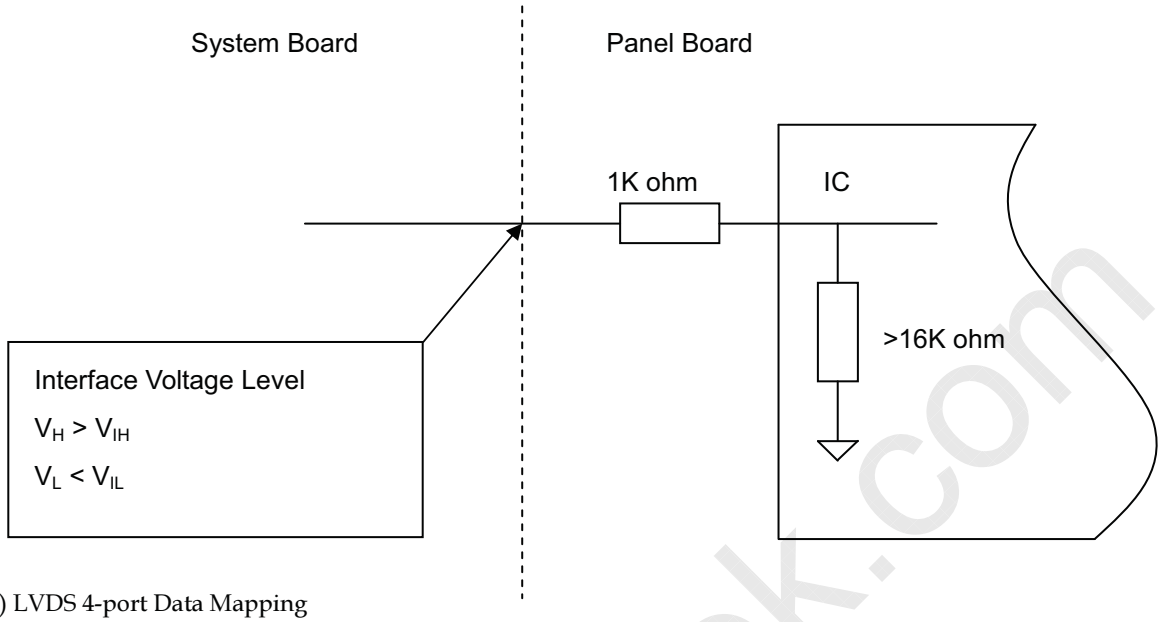
Backlight should be turned off in the period of changing original setting after power on.

Note (6) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (7) Interface optional pin has internal scheme as following diagram.

Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (8) LVDS 4-port Data Mapping

Port	Channel of LVDS	Data Stream
1st Port	First Pixel	1, 5, 9, ……1913, 1917
2nd Port	Second Pixel	2, 6, 10, ….1914, 1918
3rd Port	Third Pixel	3, 7, 11, ….1915, 1919
4th Port	Fourth Pixel	4, 8, 12, ….1916, 1920

Note (9) The definition of L/R_O signal as follows

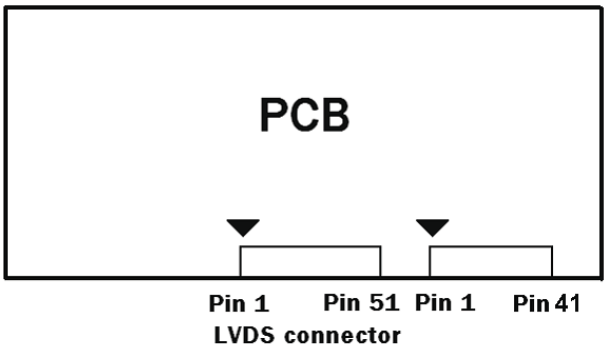
L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on

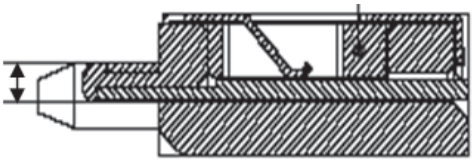
Note (10) Ground or OPEN: Disable, High: Enable.

Note (11) Please reference Appendix A

Note (12) LVDS connector pin order defined as below



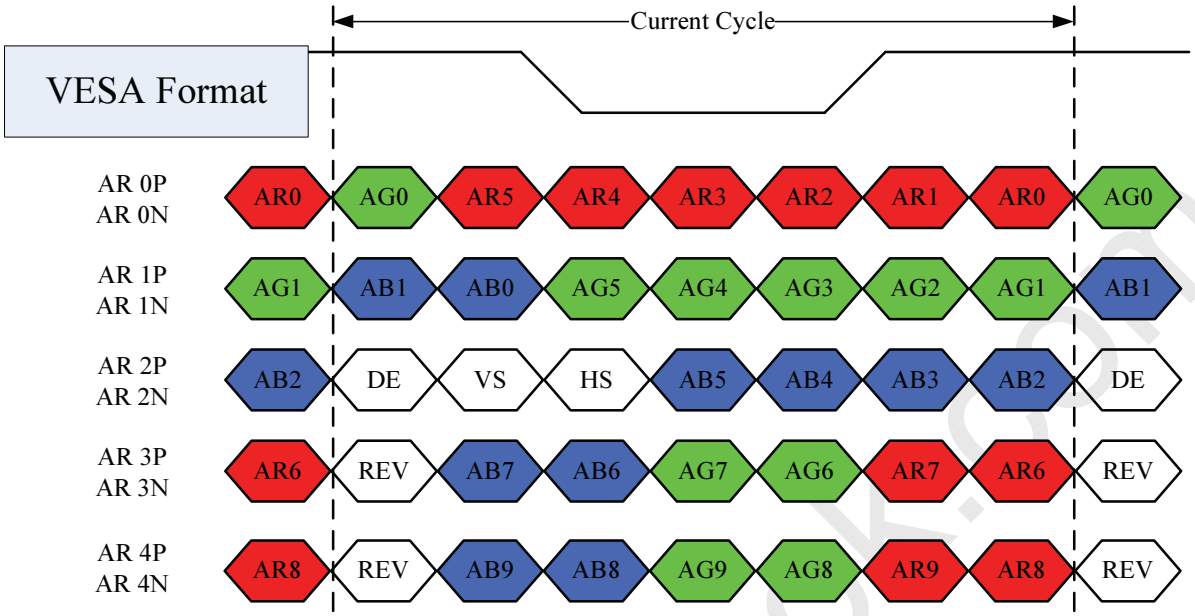
Note (13) LVDS connector mating dimension range request is 0.93mm~1.0mm as below.

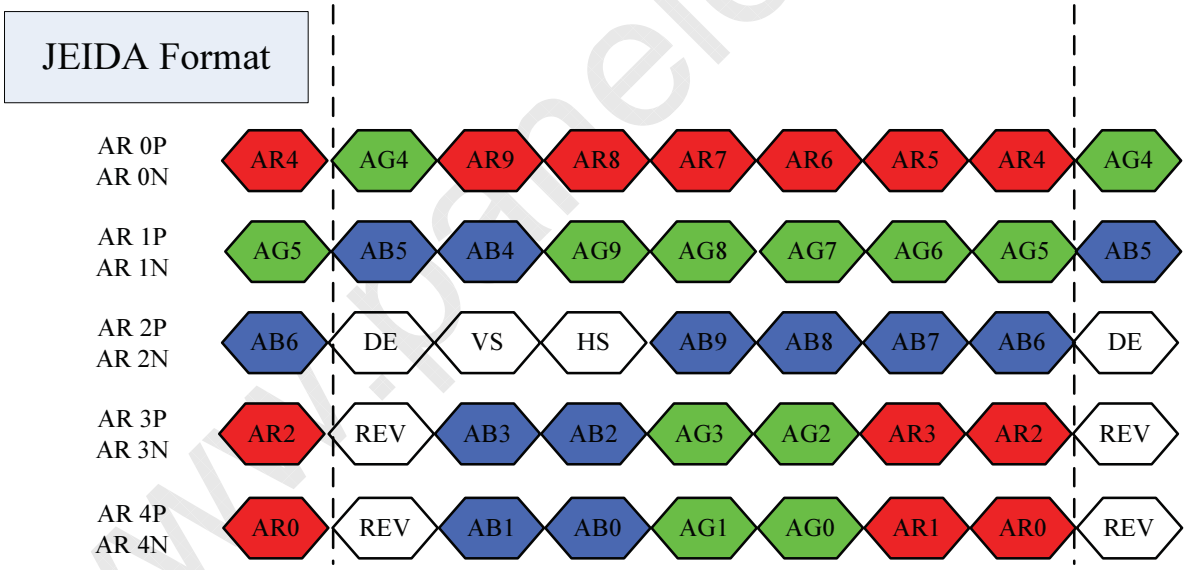


5.2 LVDS INTERFACE

JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open





AR0~AR9	First Pixel R Data (9; MSB, 0; LSB)	DE	Data enable signal
AG0~AG9	First Pixel G Data (9; MSB, 0; LSB)	DCLK	Data clock signal
AB0~AB9	First Pixel B Data (9; MSB, 0; LSB)	RSVD	Reserved

5.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

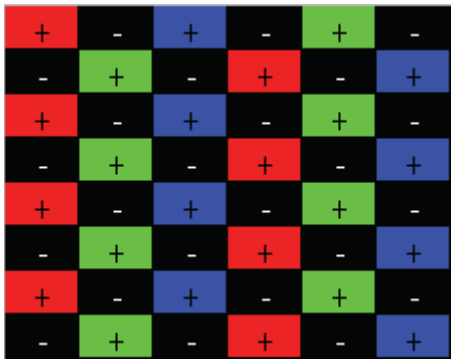
Note (1) 0: Low Level Voltage, 1: High Level Voltage

5.4 FLICKER (Vcom) ADJUSTMENT

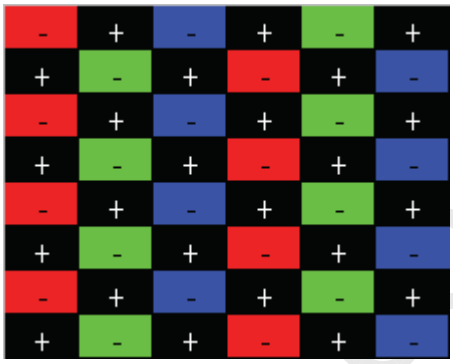
(1) Adjustment Pattern:

Column-inversion pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

Frame N



Frame N+1



(2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com.The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI. Below items is suggested to be ready before Digital V-com adjustment in customer LCM line.

a. USB Sensor Board.

b. Programmable software

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 ℃)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	74.25	80	MHz	—
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}	—	—	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	T_{RSKM}	-400	—	400	ps	(5)

6.1.1 TIMING SPEC FOR FRAME RATE=100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r5}	94	100	106	Hz	(9),(10)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1350	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	270	315	Th	—
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

6.1.2 TIMING SPEC FOR FRAME RATE=120Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F_{r6}	114	120	126	Hz	(9),(10)
	3D mode		F_{r6}	120	120	120	Hz	(7),(9),(10)
Vertical Active Display Term	2D Mode	Total	Tv	1090	1125	1395	Th	Tv=Tvd+Tvb
		Display	Tvd	1080	1080	1080	Th	—
		Blank	Tvb	10	45	315	Th	—
	3D Mdoe	Total	Tv	1125			Th	(6), (8)
		Display	Tvd	1080			Th	
		Blank	Tvb	45			Th	
Horizontal Active Display Term	2D Mode	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—
	3D Mdoe	Total	Th	520	550	670	Tc	Th=Thd+Thb
		Display	Thd	480	480	480	Tc	—
		Blank	Thb	40	70	190	Tc	—

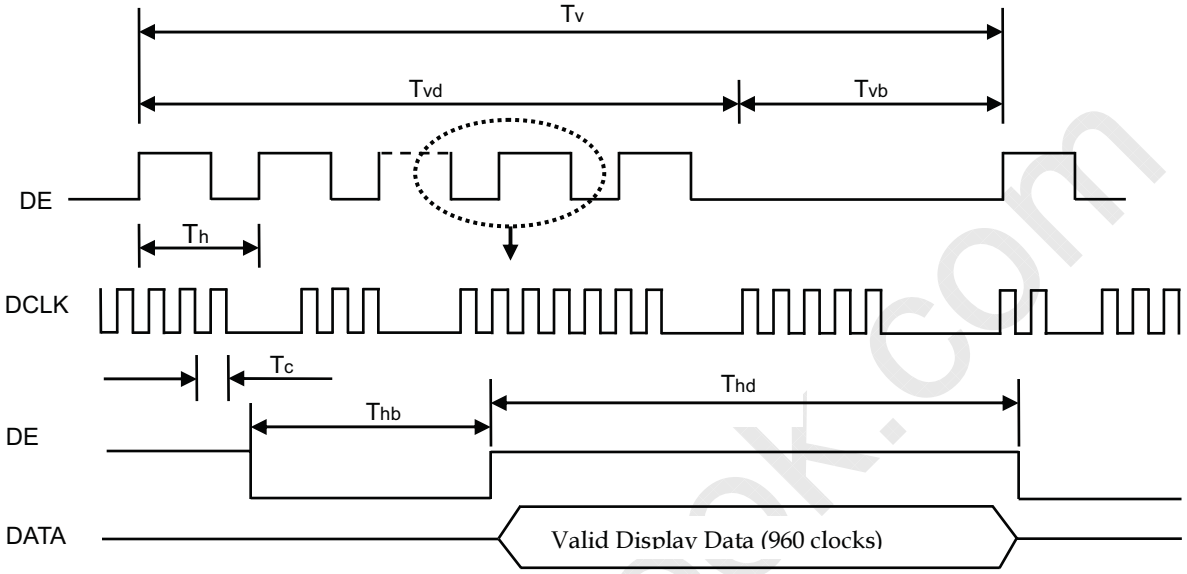
Note (1) Since the module is operated in DE only mode, Hsync and Vsync input signals should be set to low logic level. Otherwise, this module would operate abnormally.

Note (2) Please make sure the range of pixel clock has follow the below equation:

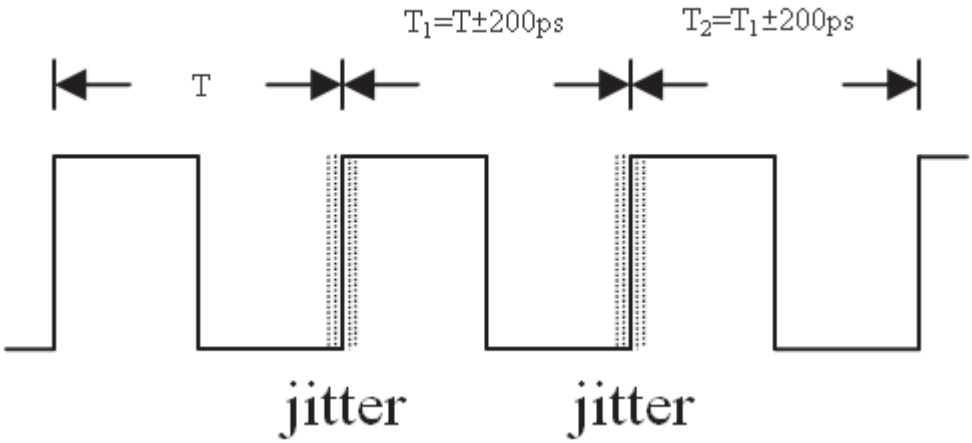
Fclkin(max) ≧ Fr6 ╳ Tv ╳ Th

Fr5 ╳ Tv ╳ Th ≧ Fclkin(min)

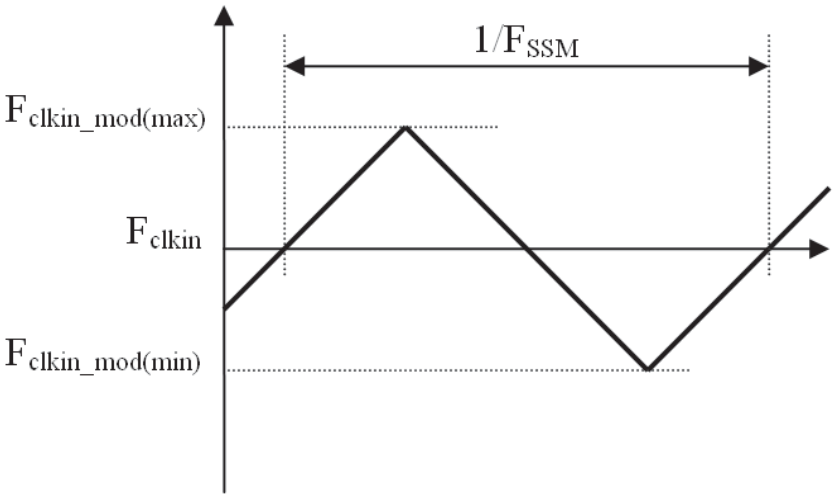
INPUT SIGNAL TIMING DIAGRAM



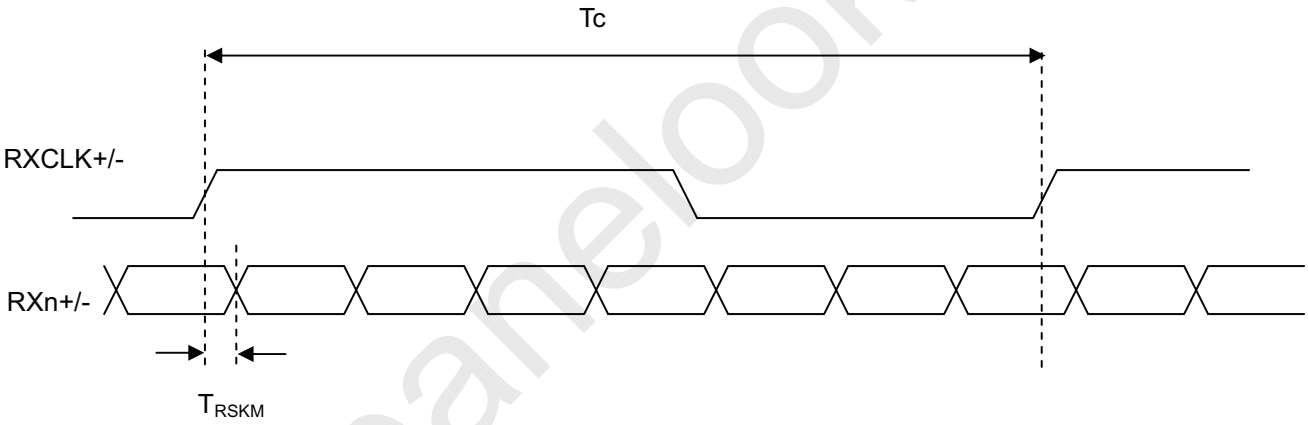
Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = | T_1 – T |



Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and the receiver skew margin is defined and shown in following figure.



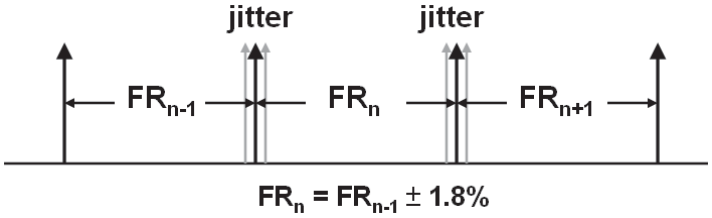
Note (6) Please fix the Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 60Hz 3D mode

Note (7) In 3D mode, the set up Fr5 and Fr6 in Typ. ±3 Hz .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ. ±30.In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

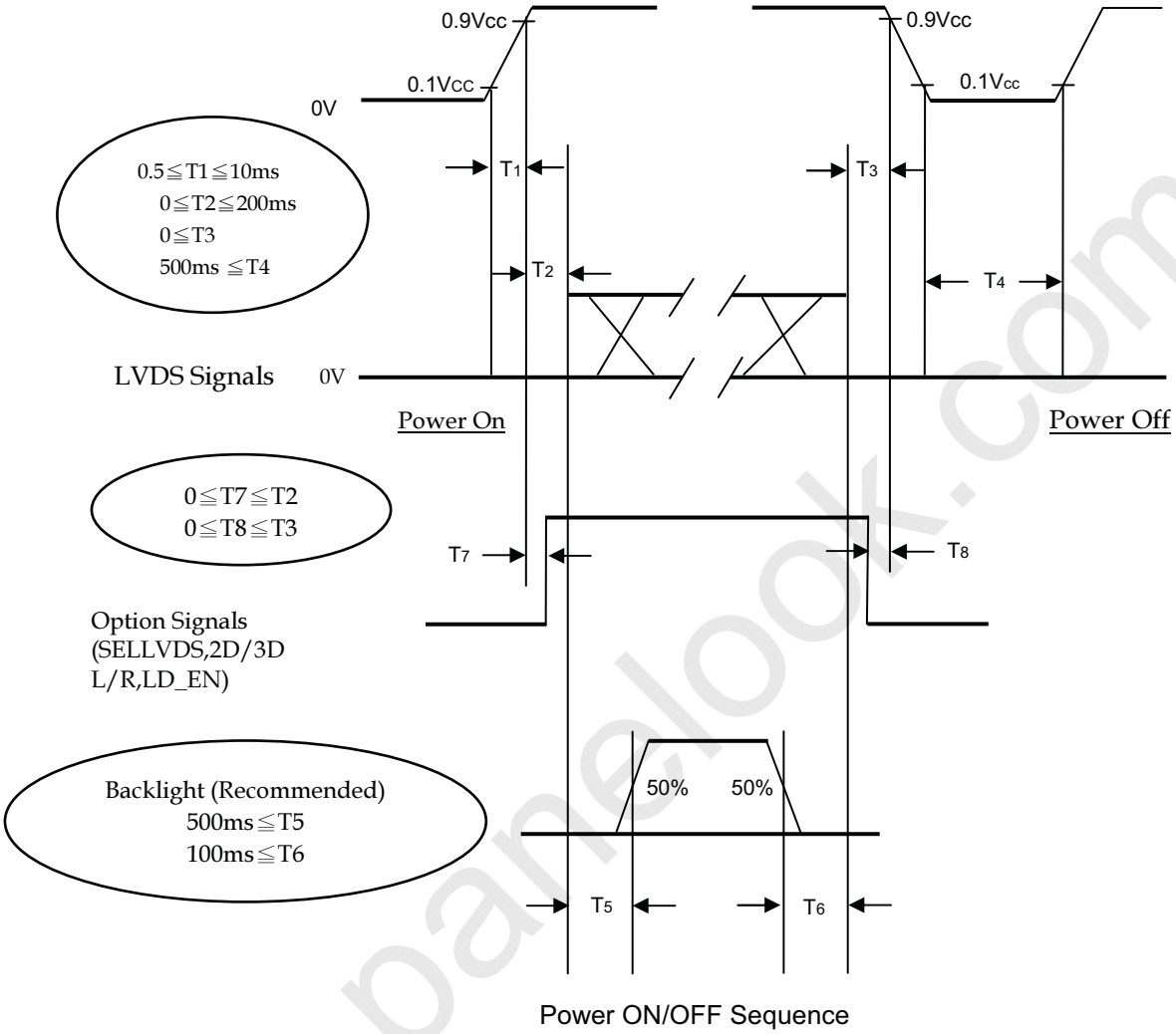
Note (9) The frame-to-frame jitter of the input frame rate is defined as the above figures. FRn = FRn-1 ± 1.8%.

Note (10) The setup of the frame rate jitter > 1.8% may result in the cosmetic LED backlight symptom but the electric function is not affected.

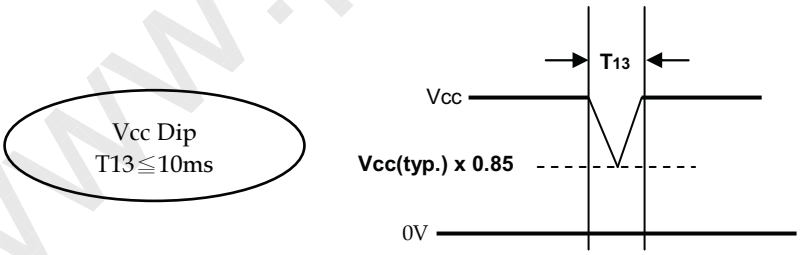


6.2 POWER ON/OFF SEQUENCE

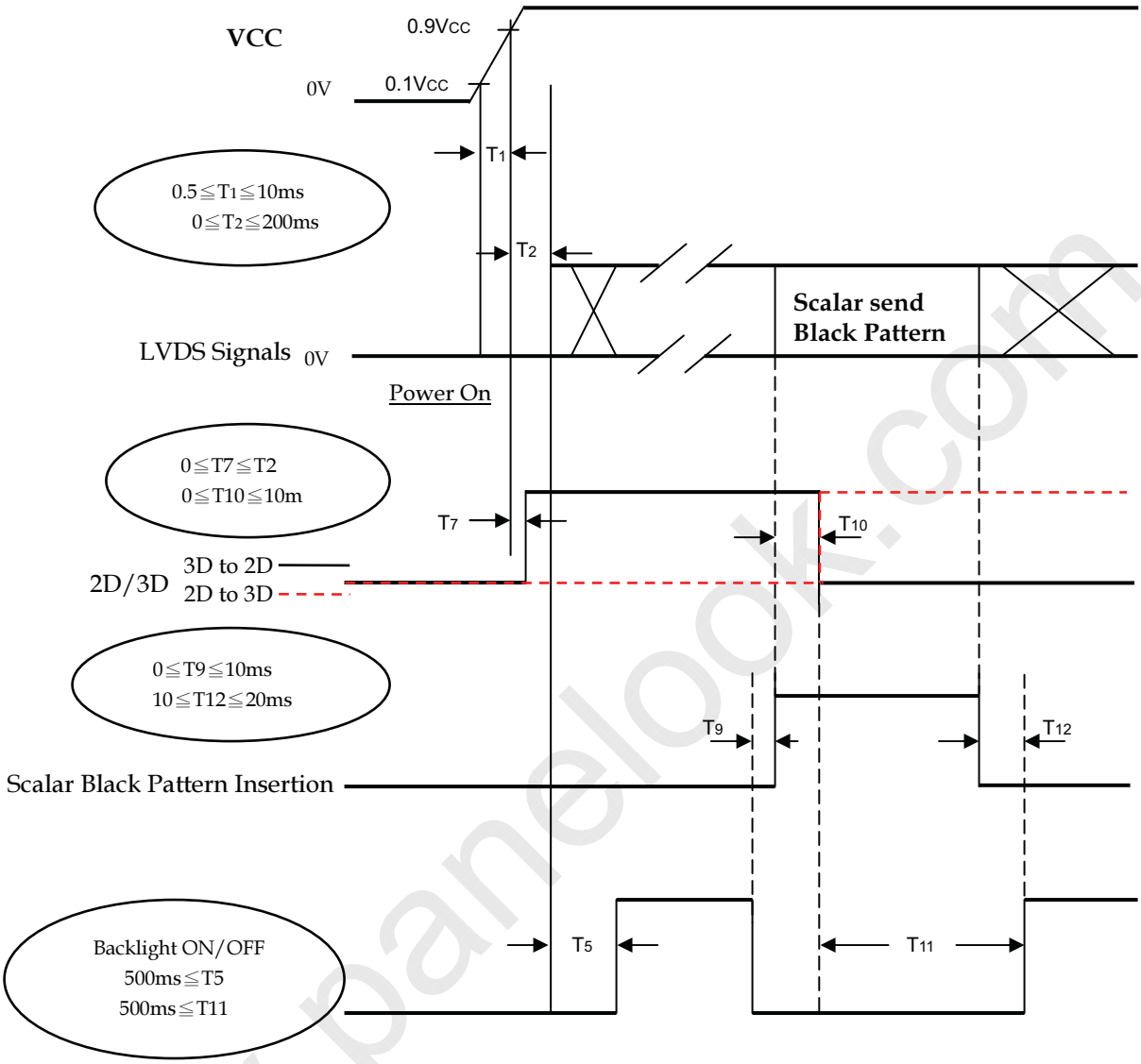
To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below..



Power ON/OFF Sequence



6.3 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

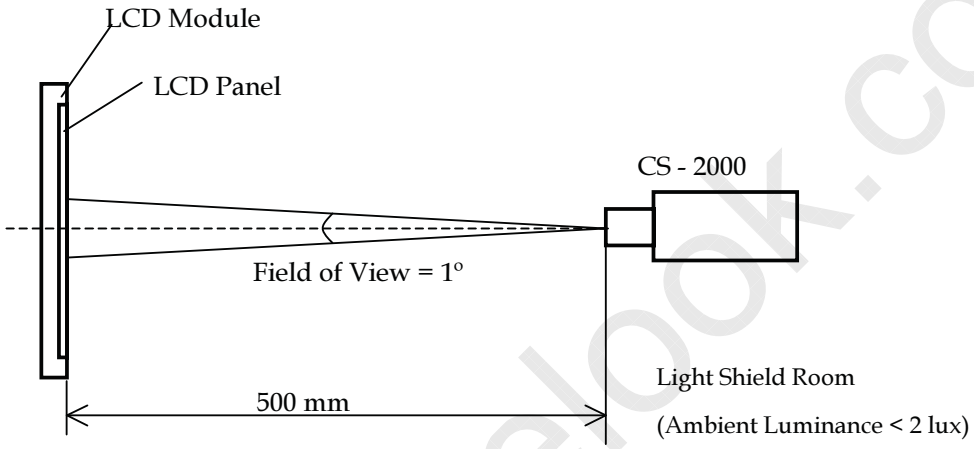
Note (7) Vcc must decay smoothly when power-off.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12V±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	140±4.2	mA

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.



7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown as below. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Color Chromaticity	Red	Rcx	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction Standard light source "C"	Typ. -0.03	0.651	Typ. +0.03	—	(0)
		Rcy			0.329		—	
	Green	Gcx			0.265		—	
		Gcy			0.591		—	
	Blue	Bcx			0.132		—	
		Bcy			0.120		—	
	White	Wcx			0.299		—	
		Wcy			0.351		—	
Transmittance		T%	θ_x=0°, θ_Y =0° with CMI module	—	6.3	—	%	(1),(5)
Transmittance Variation		δT		—	—	1.3	—	(1),(6)
Contrast Ratio		CR		—	5000	—	—	(1),(3)
Response Time		Gray to gray	θ_x=0°, θ_Y =0° with CMI Module	—	6.5	13	ms	(1),(4)
Viewing Angle	Horizontal	θ_x+	CR≥20 With CMI module	—	88	—	Deg.	(1),(2)
		θ_x-		—	88	—		
	Vertical	θ_Y+		—	88	—		
		θ_Y-		—	88	—		

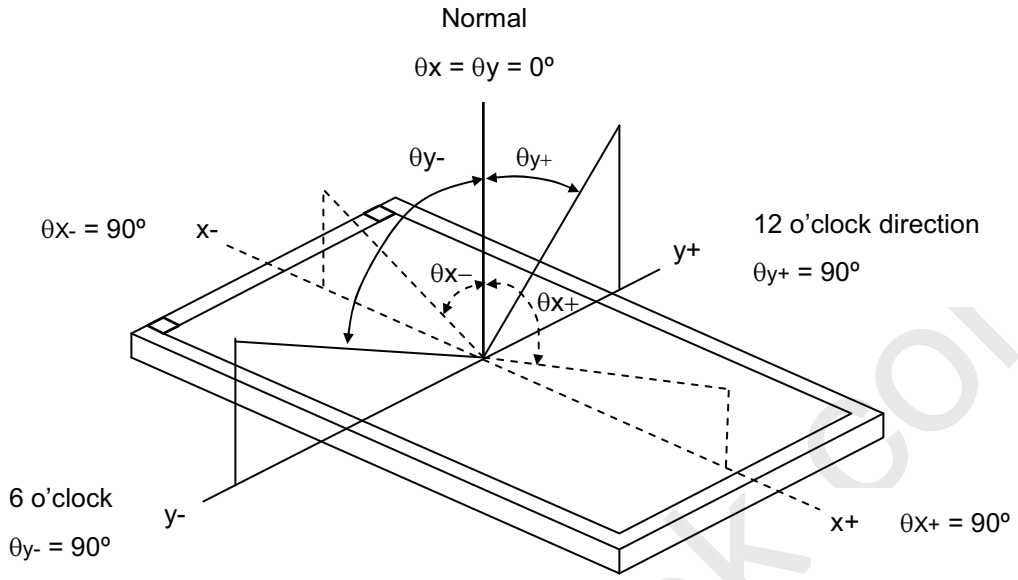
Note (0) Light source is the standard light source "C" which is defined by CIE and driving voltage are based on suitable gamma voltages. The calculating method is as following:

1. Measure Module's and BLU's spectrum at center point. White and R,G,B are with signal input. BLU (for V650HP1-LS6) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C".

Note (1) Light source is the BLU which supplied by CMI and driving voltage are based on suitable gamma voltages.

Note (2) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R)



Note (3) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

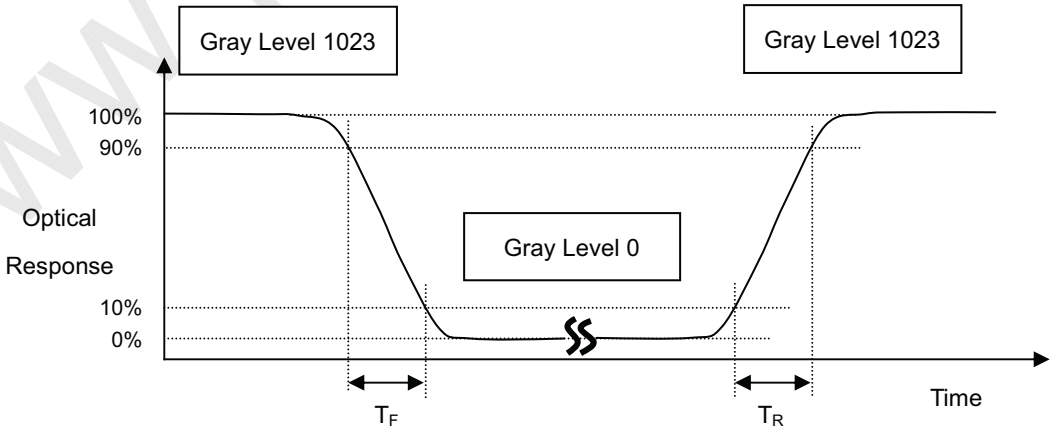
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023 : Luminance of gray level 1023

L0 : Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (5).

Note (4) Definition of Gray-to-Gray Switching Time:



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (5) Definition of Transmittance (T%) :

Measure the luminance of gray level 1023 at 5 points of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{average [L (1), L (2), L (3), L (4), L (5)] of LCD module}}{\text{average [L (1), L (2), L (3), L (4), L (5)] of BLU}} \times 100\%$$

The 5 point is corresponding of the point X at the figure in Note (6).

Note (6) Definition of Transmittance Variation (δT) : (VA Model)

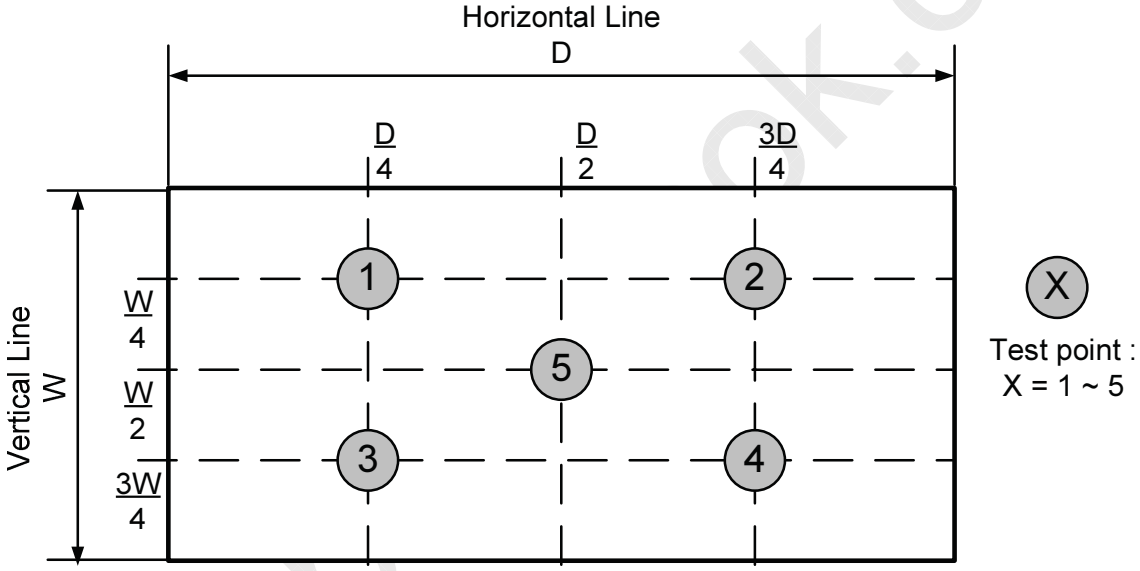
Measure the transmittance at 5 points.

The transmittance of each point can be calculated by the following expression.

T (X) = L1023 (X) of LCD module / Luminance (X) of BLU.

L1023: Luminance of gray level 1023

$$\text{Transmittance Variation (δT)} = \frac{\text{Maximume [T (1), T (2), T (3), T (4), T (5)]}}{\text{Minimum [T (1), T (2), T (3), T (4), T (5)]}}$$



8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply improper or unbalanced force such as bending or twisting to open cells during assembly.

[2] It is recommended to assemble or to install an open cell into a customer's product in clean working areas. The dust and oil may cause electrical short to an open cell or worsen polarizers on an open cell.

[3] Do not apply pressure or impulse to an open cell to prevent the damage.

[4] Always follow the correct power-on sequence when an open cell is assembled and turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[5] Do not design sharp-pointed structure / parting line / tooling gate on the plastic part of a COF (Chip on film), because the burr will scrape the COF.

[6] If COF would be bended in assemble process, do not place IC on the bending corner.

[7] The gap between COF IC and any structure of BLU must be bigger than 2 mm. This can prevent the damage of COF IC.

[8] The bezel opening must have no burr and be smooth to prevent the surface of an open cell scraped.

[9] The bezel of a module or a TV set can not contact with force on the surface of an open cell. It might cause light leakage or scrape.

[10] In the case of no FFC or FPC attached with open cells, customers can refer the FFC / FPC drawing and buy them by self.

[11] It is important to keep enough clearance between customers' front bezel/backlight and an open cell. Without enough clearance, the unexpected force during module assembly procedure may damage an open cell.

[12] Do not plug in or unplug an I/F (interface) connector while an assembled open cell is in operation.

[13] Use a soft dry cloth without chemicals for cleaning, because the surface of the polarizer is very soft and easily scratched.

[14] Moisture can easily penetrate into an open cell and may cause the damage during operation.

[15] When storing open cells as spares for a long time, the following precaution is necessary.

[15.1] Do not leave open cells in high temperature and high humidity for a long time. It is highly recommended to store open cells in the temperature range from 0 to 35℃ at normal humidity without condensation.

[15.2] Open cells shall be stored in dark place. Do not store open cells in direct sunlight or fluorescent light environment.

[16] When ambient temperature is lower than 10ºC, the display quality might be reduced.

[17] Unpacking (Cartons/Tray plates) in order to prevent open cells broken:

[17.1] Moving tray plates by one operator may cause tray plates bent which may induce open cells broken. Two operators carry one carton with their two hands. Do not throw cartons/tray plates, avoid any impact on cartons/tray plates, and put down & pile cartons/tray plates gently.

[17.2] A tray plate handled with unbalanced force may cause an open cell damaged. Trays should be completely put on a flat platform.

[17.3] To prevent open cells broken, tray plates should be moved one by one from a plastic bag.

[17.4] Please follow the packing design instruction, such as the maximum number of tray stacking to prevent the deformation of tray plates which may cause open cells broken.

[17.5] To prevent an open cell broken or a COF damaged on a tray, please follow the instructions below:

[17.5.1] Do not peel a polarizer protection film of an open cell off on a tray

[17.5.2] Do not install FFC or LVDS cables of an open cell on a tray

[17.5.3] Do not press the surface of an open cell on a tray.

[17.5.4] Do not pull X-board when an open cell placed on a tray.

[18] Unpacking (Hard Box) in order to prevent open cells broken:

[18.1] Moving hard boxes by one operator may cause hard boxes fell down and open cells broken by abnormal methods. Two operators carry one hard box with their two hands. Do handle hard boxes carefully, such as avoiding impact, putting down, and piling up gently.

[18.2] To prevent hard boxes sliding from carts and falling down, hard boxes should be placed on a surface with resistance.

[18.3] To prevent an open cell broken or a COF damaged in a hard box, please follow the instructions below:

[18.3.1] Do not peel a polarizer protection film of an open cell off in a hard box.

[18.3.2] Do not install FFC or LVDS cables of an open cell in a hard box.

[18.3.3] Do not press the surface of an open cell in a hard box.

[18.3.4] Do not pull X-board when an open cell placed in a hard box.

[19] Handling – In order to prevent open cells, COFs , and components damaged:

[19.1] The forced displacement between open cells and X-board may cause a COF damaged. Use a fixture tool for handling an open cell to avoid X-board vibrating and interfering with other components on a PCBA & a COF.

[19.2] To prevent open cells and COFs damaged by taking out from hard boxes, using vacuum jigs to take out open cells horizontally is recommended.

[19.3] Improper installation procedure may cause COFs of an open cell over bent which causes damages. As installing an open cell on a backlight or a test jig, place the bottom side of the open cell first on the backlight or the test jig and make sure no interference before fitting the open cell into the backlight/the test jig.

[19.4] Handle open cells one by one.

[20] Avoid any metal or conductive material to contact PCB components, because it could cause electrical damage or defect.

8.2 SAFETY PRECAUTIONS

[1] If the liquid crystal material leaks from the open cell, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[2] After the end of life, open cells are not harmful in case of normal operation and storage.

9. DEFINITION OF LABELS

9.1 OPEN CELL LABEL

The barcode nameplate is pasted on each open cell as illustration for CMI internal control.

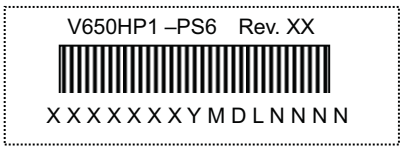
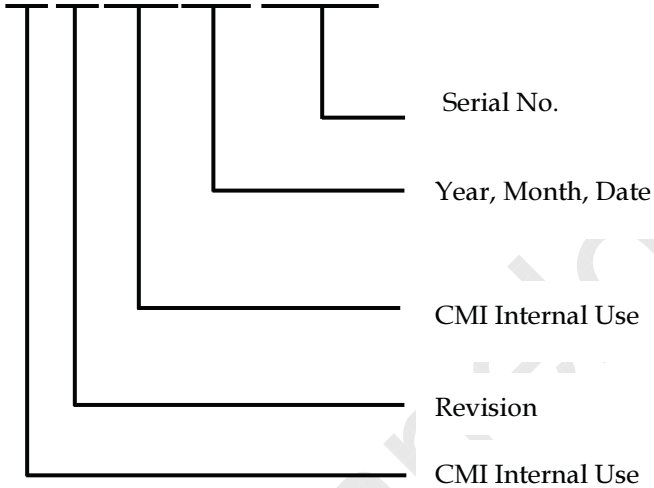


Figure.9-1 Serial No. Label on SPWB

Model Name : V650HP1-PS6

Revision : Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID : X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date :

Year: 2010=0, 2011=1,2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No.: Manufacturing sequence of product

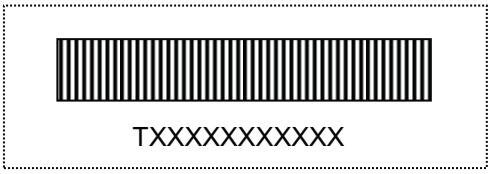


Figure.9-2 Panel ID Label on Cell

Panel ID Label includes the information as below:

Panel ID: T X X X X X X X X X X X

CMI Internal Use

FAB Line: 1~8, for Fab1~Fab8

TFT

10. PACKAGING

10.1 PACKING SPECIFICATIONS

(1) 5 LCD TV Panels / 1 Box

(2) Box dimensions : 1620 (L) X1110 (W) X74 (H)mm

(3) Weight : approximately 40 Kg (5 panels per box)

(4) 70 LCD TV Panels / 1 Group

10.2 PACKING METHOD

Packing method is shown in following figures.

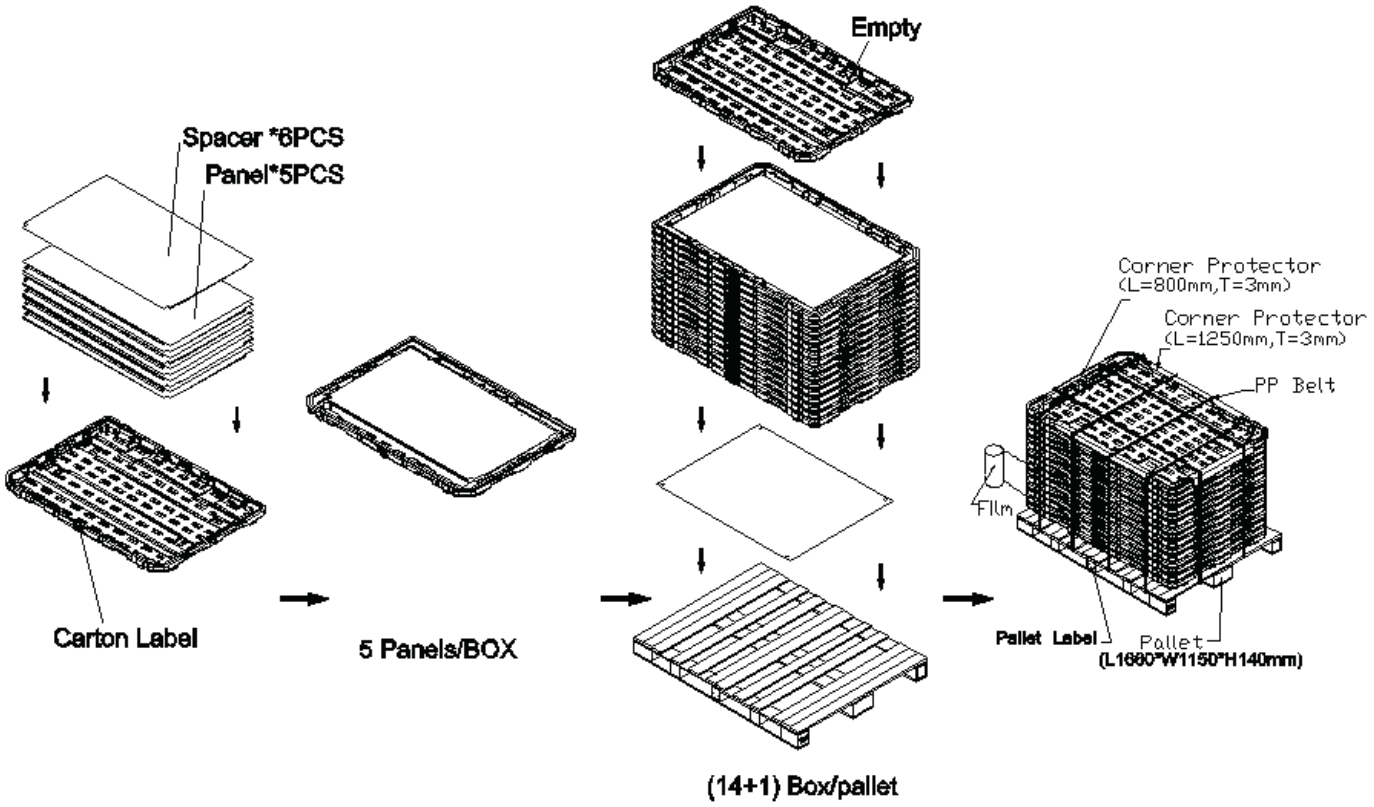
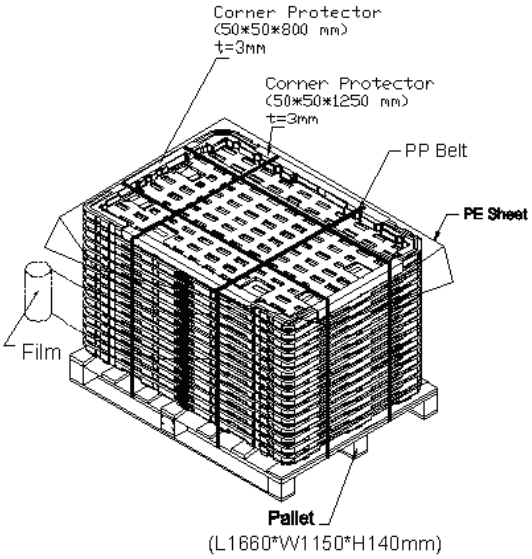


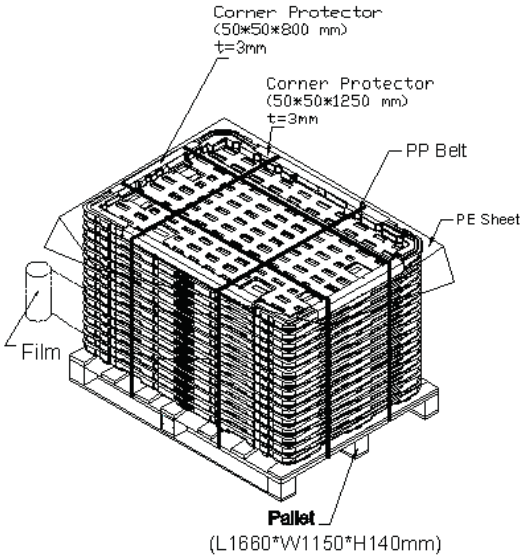
Figure.10-1 packing method

Sea / Land Transportation



(14+1) Box/pallet

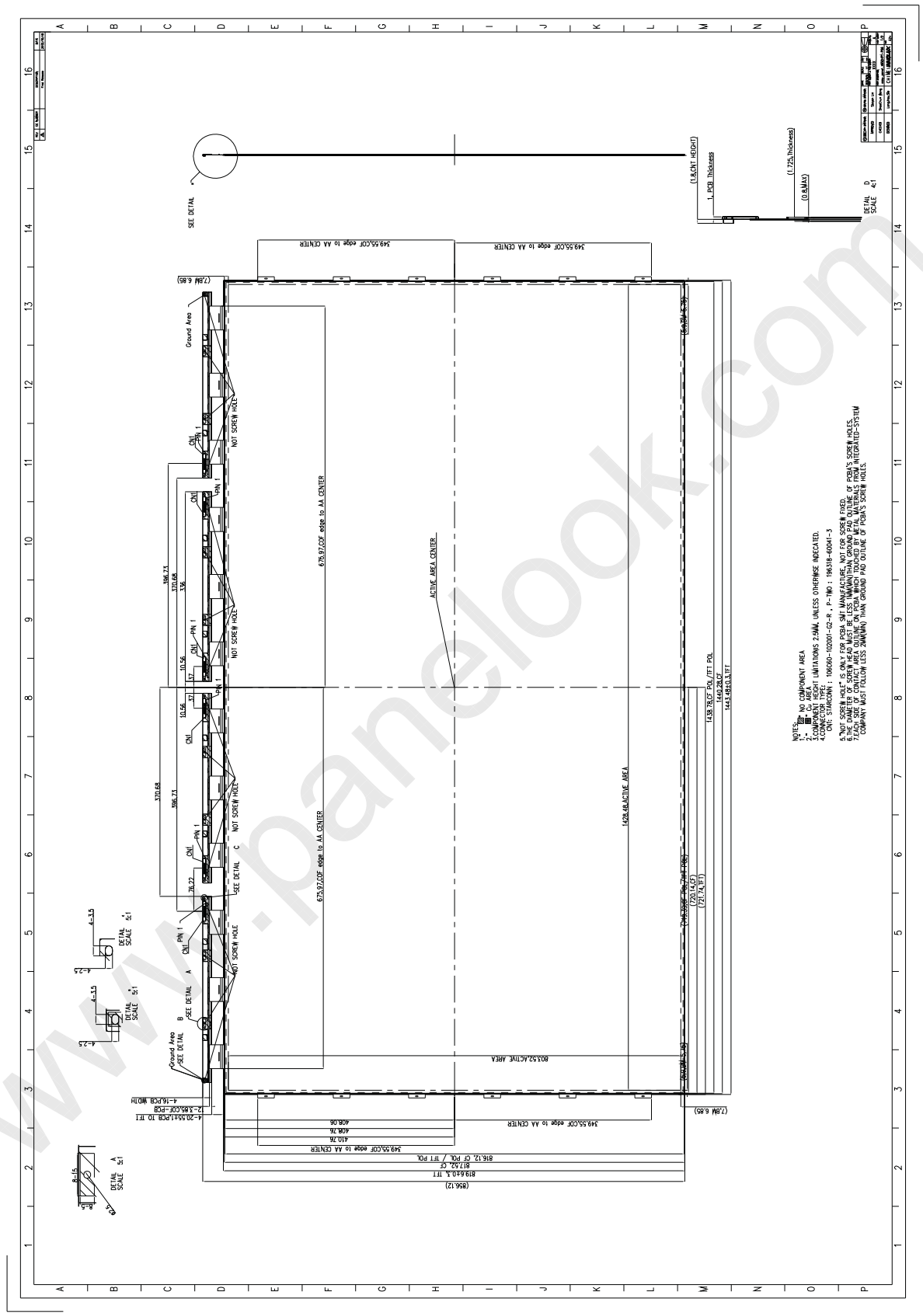
Air Transportation

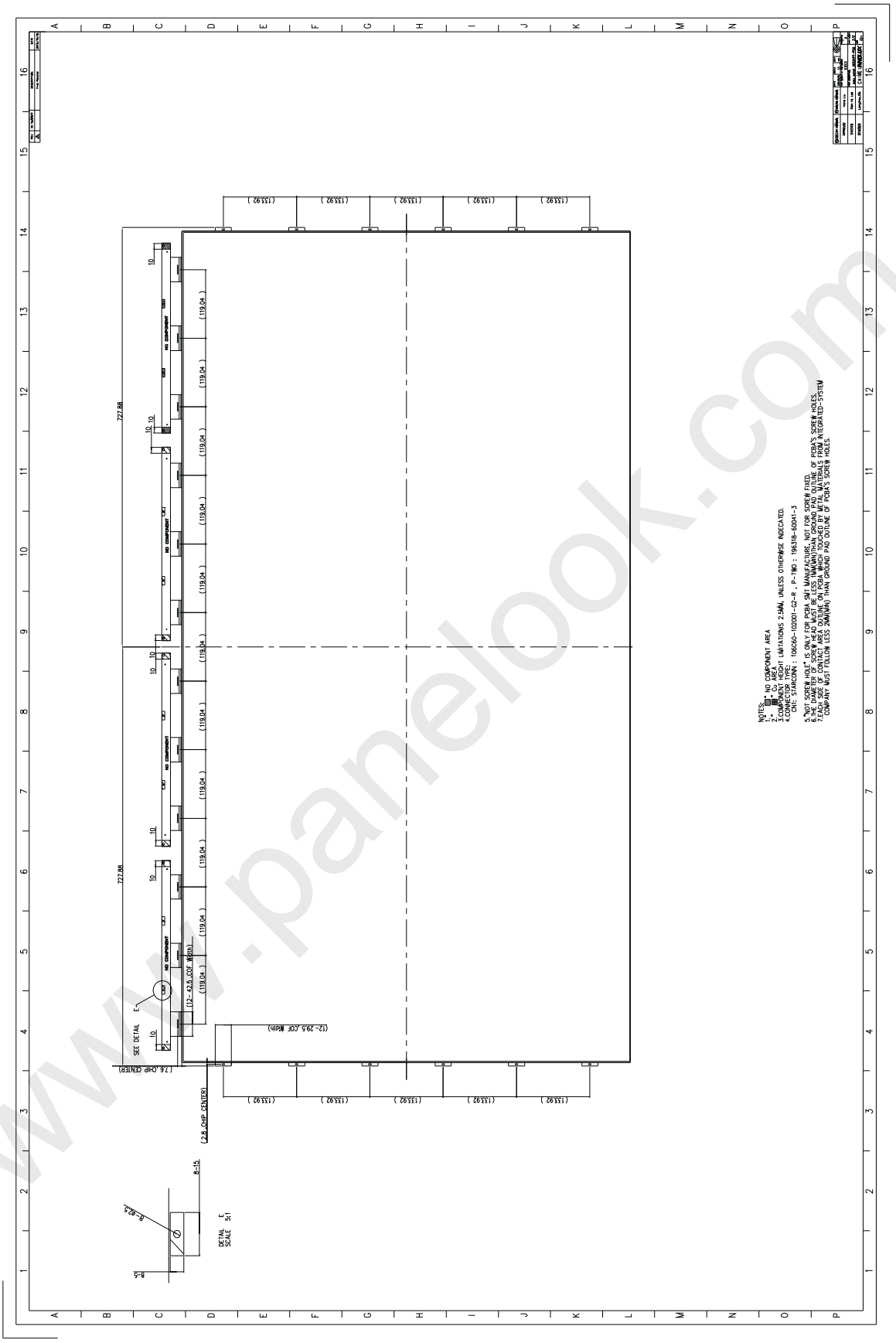


(14+1) Box/pallet

Figure.10-2 packing method

11. MECHANICAL CHARACTERISTIC





Appendix A

Local Dimming demo function

A.1 I2C address and write command

Device address: 0xC2

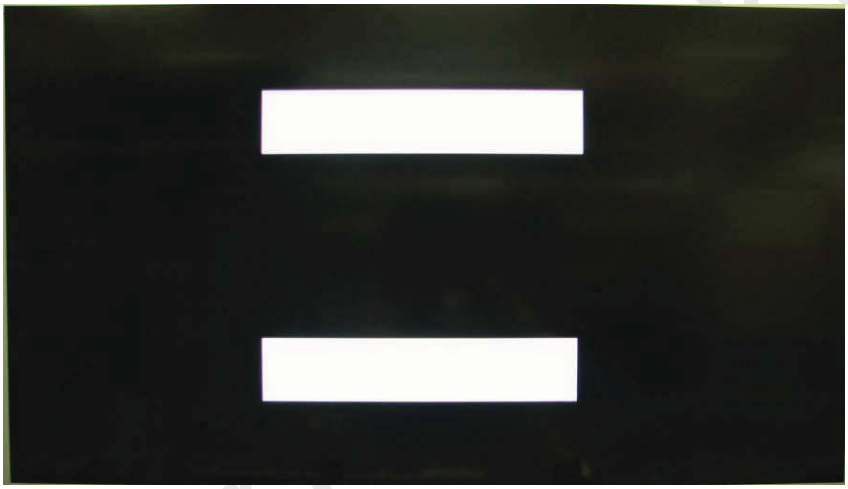
Register address: 0x01

Command data: 0x00: Local Dimming demo mode OFF (Note 1)

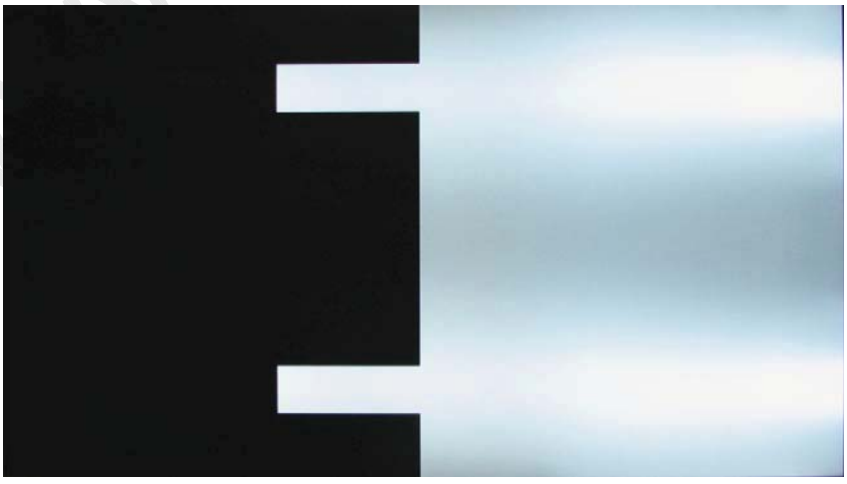
0x01: Local Dimming demo mode ON (Demo in right half screen) (Note 2)

	Device Address		Register Address		Command Data		
START	11000010 (0xC2)	ACK	00000001 (0x01)	ACK	00000001 (0x01)	ACK	STOP

Note 1: Local Dimming demo OFF



Note 2: Local Dimming demo ON



A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns