INNOLUX
群創光電股份有限公司

PRODUCT SPECIFICATION

☐ Tentative Specification
■ Preliminary Specification
☐ Approval Specification

MODEL NO.: V850DK1

SUFFIX: KD1

Revision : B1
Customer :

APPROVED BY SIGNATURE

Name / Title _____ _____
Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Carlos Lee	Greg Wang

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REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver. 0.0	Sept.23, 2013	All	All	The Tentative specification was first issued.
Ver. 0.1	Oct.21, 2013	P 6	1.4	Update MECHANICAL SPECIFICATIONS
		P 13	3.2.1	Update CONVERTER CHARACTERISTICS
		P 14	3.2.2	Update CONVERTER INTERFACE CHARACTERISTICS
		P 17	5.1.1	Update TFT LCD MODULE
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Ver. 0.2	Oct.23, 2013	P 28/29	6	Update INTERFACE TIMING
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Ver 1.0	Dec.25,2013	P 9	3.1	Update TFT LCD MODULE
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		P 28	6.1	Update INPUT SIGNAL TIMING SPECIFICATIONS
			6.1.1	Update Timing spec for Frame Rate = 100Hz
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		P 12/13	3.2.1	Update CONVERTER CHARACTERISTICS
Ver 1.1	Feb 25,2014	P 5	1.2	Update FEATURES
		P 8	2.3.3	Update CD-Link(CDL) INTERFACE
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		P 16/17/18	3.2.3	Update CONVERTER CDL INTERFACE CHARACTERISTICS
		P 20 / 24	5.1	Update TFT LCD MODULE
		P 29	5.3	Update CONVERTER UNIT
		P 31 / 32 / 35 / 38	6	Update INTERFACE TIMING

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V850DK1-KD1 is a 84.5" TFT Liquid Crystal Display module with LED Backlight unit and 16 Lane V-by-one interface. This module supports 3840 x 2160 QF HDTV format and can display true 1.07G colors (8-bit+FRC). The driving board module for backlight is built-in.

1.2 FEATURES

- High brightness (500 nits)
- High contrast ratio (3000 :1)
- Fast response time (Gray to Gray typical : 6.5ms)
- High color saturation (NTSC 100%)
- Quad Full HDTV (3840 x 2160 pixels) resolution, true Quad Full HDTV format
- V-by-One interface
- Optimized response time for 100Hz/120Hz frame rate
- Viewing Angle : 176(H)/176(V) (CR>20) VA technology
- Ultra wide viewing angle: Super MVA technology
- RoHs compliance
- Input frame rate : QFHD 100/120Hz or 4K1K 200/240Hz
  Output frame rate: QFHD 100/120Hz or 4K1K 200/240Hz

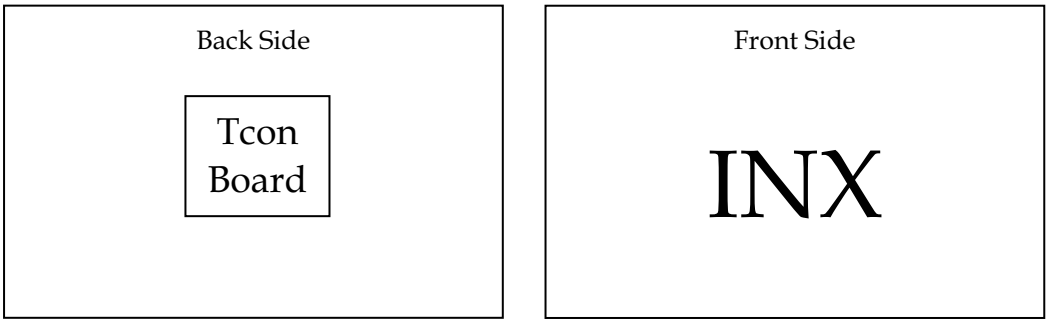
1.3 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	1872(H)*1053(V) (84.5" diagonal)	mm	(1)
Bezel Opening Area	1877.2(H)*1059.0(V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	3840 x R.G.B. x 2160	pixel	-
Pixel Pitch(Sub Pixel)	0.4875 (H) x 0.4875 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	1.07G colors (8-bit+FRC)	color	-
Display Operation Mode	Transmissive mode / Normally black	-	-
Surface Treatment	Anti-Glare coating (Haze 0.5%)	-	(2)
Rotation Function	Unachievable		(3)
Display Orientation	Signal input with "INX"		(3)

Note (1) Please refer to the attached drawings in chapter 9 for more information about the front and back outlines.

Note (2) The spec of the surface treatment is temporarily for this phase. INX reserves the rights to change this feature.

Note (3)



1.4 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal (H)	1900.5	1902.6	1904.7	mm	(1),(2)
	Vertical (V)	1081.5	1083.6	1085.7	mm	(1),(2)
	Depth (D)	40.2	42.2	44.2	mm	To Rear
		49.8	51.8	53.8	mm	To converter cover
Weight			(42,500)		g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

Note (2) Module Depth does not include connectors.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	35	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

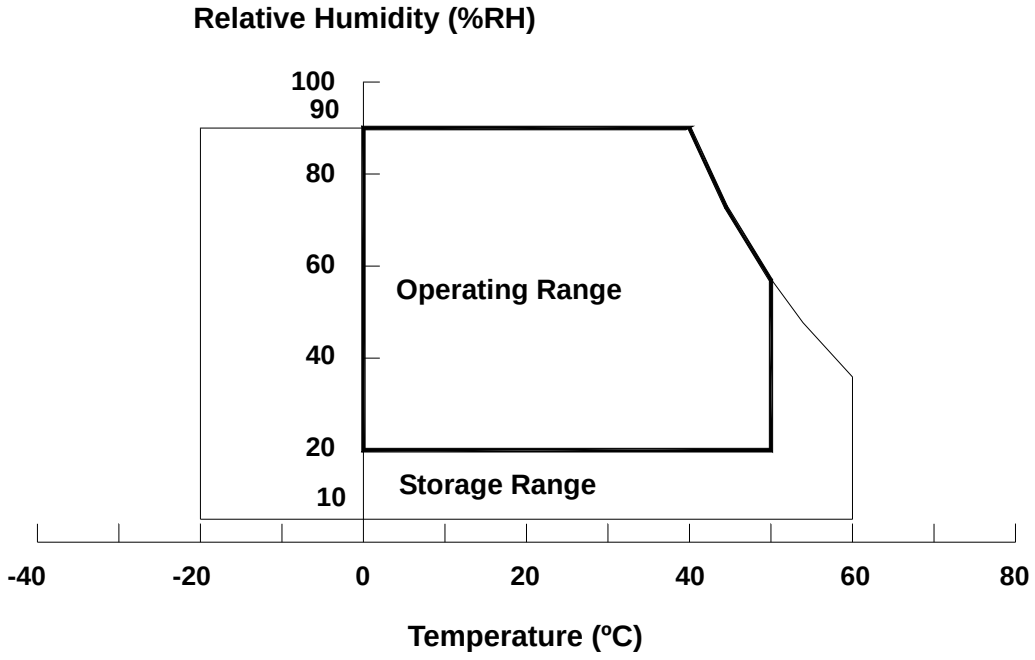
(c) No condensation.

Note (2) Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 70 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 30 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time, It is highly recommended to store the module with temperature from 0 to 35 ℃ at normal humidity without condensation.

(b) The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	13.5	V	(1)
Logic Input Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT CONVERTER UNIT

Item	Symbol	Test Condition	Min.	Type	Max.	Unit	Note
Light Bar Voltage	V_W	Ta = 25 ℃	-	-	60	V_{RMS}	3D Mode
Converter Input Voltage	V_{BL}	-	0	-	30	V	
Control Signal Level	-	-	-0.3	-	6	V	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) No moisture condensation or freezing.

Note (3) The control signals include On/Off Control and External PWM Control.

2.3.3 CD-Link(CDL) INTERFACE

Item	Test Condition	Min.	Type	Max.	Unit	Note
CDL_EN	Ta = 25 ℃	-0.3	-	3.6	V	(4)
CDL_SCK	Ta = 25 ℃	-0.3	-	3.6	V	(5)
VSYNC	Ta = 25 ℃	-0.3	-	3.6	V	(6)
CDL_SDA	Ta = 25 ℃	-0.3	-	3.6	V	(7)

Note (4) Enable pin of CDLink (CDL) Interface. This pin also implies the Vsync information in the same time.

Note (5) Serial clock of CDL interface.

Note (6) The VSYNC pulse width must be larger than 5μs.

Note (7) Serial data input/output for CDL.

3. ELECTRICAL CHARACTERISTICS

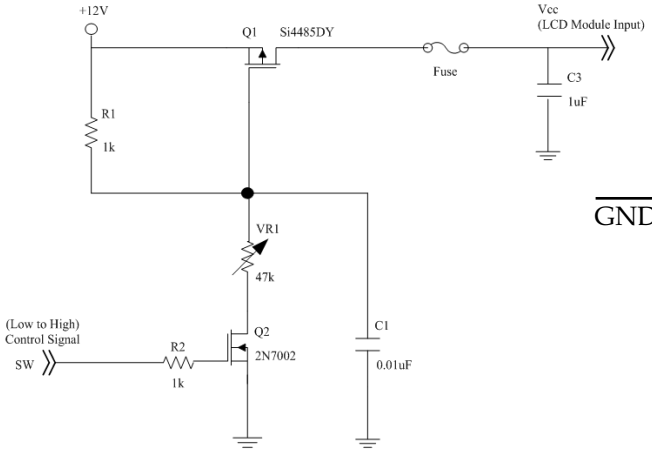
3.1 TFT LCD MODULE

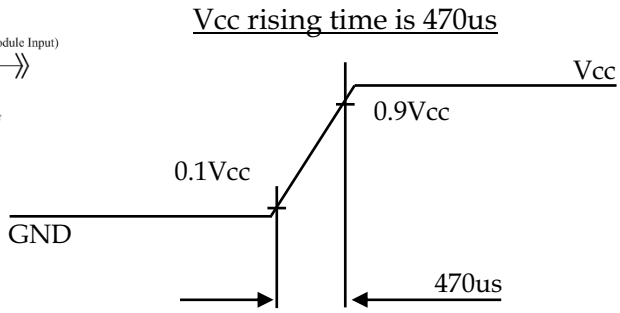
(Ta = 25 ± 2 ºC)

Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	—	—	9.022	A	(2)
Power consumption	White Pattern	P_T	—	26.784	31.98	W	(3)
	Black Pattern	P_T	—	27.072	32.292		
	Heavy Loading pattern 2W2B (by cell and platform)	P_T	—	69.264	84.552		
Power Supply Current	White Pattern	P_T	—	2.232	2.665	A	
	Black Pattern	P_T	—	2.256	2.691		
	Heavy Loading pattern 2W2B (by cell and platform)	P_T	—	5.772	7.046		
VbyOne HS	Differential Input High Threshold Voltage	VLVTH	—	—	+50	mV	(4)
	Differential Input Low Threshold Voltage	VLVTL	-50	—	—	mV	
	Differential Input Resistor	RRIN	80	100	120	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	—	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	—	0.7	V	

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10% of Vcc (Typ.)

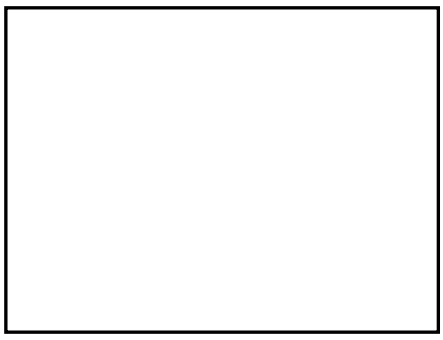
Note (2) Measurement condition :





Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 °C, fv = 120 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

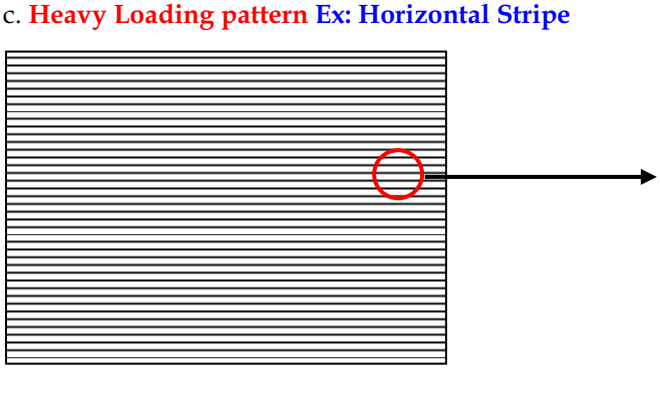


Active Area

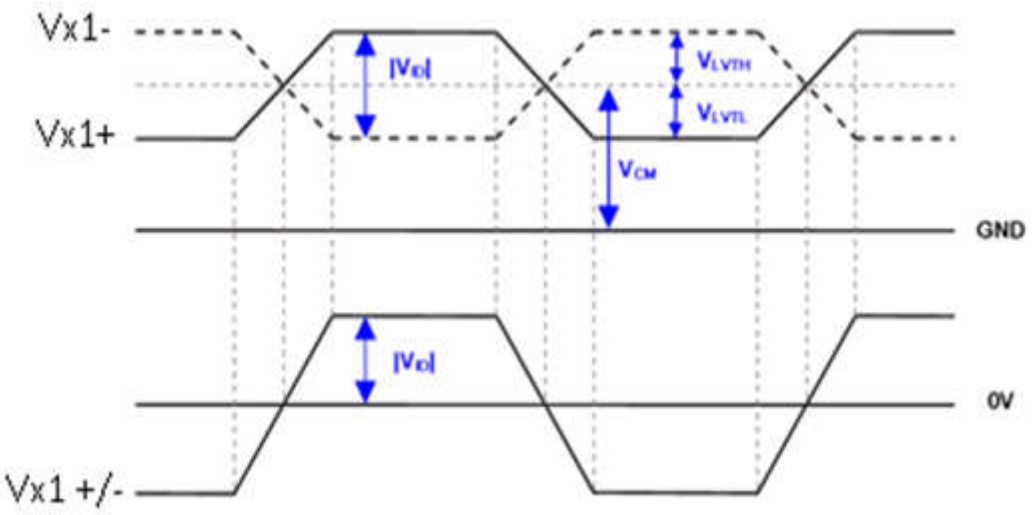
b. Black Pattern

Active Area

c. **Heavy Loading pattern Ex: Horizontal Stripe**



Note (4) The V by One input characteristics are as follows:



3.2 BACKLIGHT UNIT

3.2.1 CONVERTER CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Consumption	$P_{BL(2D)}$	—	(389.6)	(448)	W	(1), (2)
	$P_{BL(3D)}$	—	(333.9)	(367.6)	W	(1), (2)
Converter Input Voltage	VBL	22.8	24.0	25.2	VDC	
Converter Input Current	$I_{BL(2D)}$	—	(16.2)	(18.6)	A	Non Dimming
	$I_{BL(3D)}$	—	(13.9)	(15.3)	A	
Input Inrush Current	$I_{R(2D)}$	—	—	(25.2)	Apeak	V_{BL}=22.8V (3), (6)
	$I_{R(3D)}$	—	—	(48.2)	Apeak	V_{BL}=22.8V (3), (6)
Dimming Frequency	FB	90	160	190	Hz	(5)
Dimming Duty Ratio	DDR	0	-	100	%	(4), (5)
Life Time	-	30,000	-	-	Hrs	(7)

Note (1) The power supply capacity should be higher than the total converter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when converter dimming.

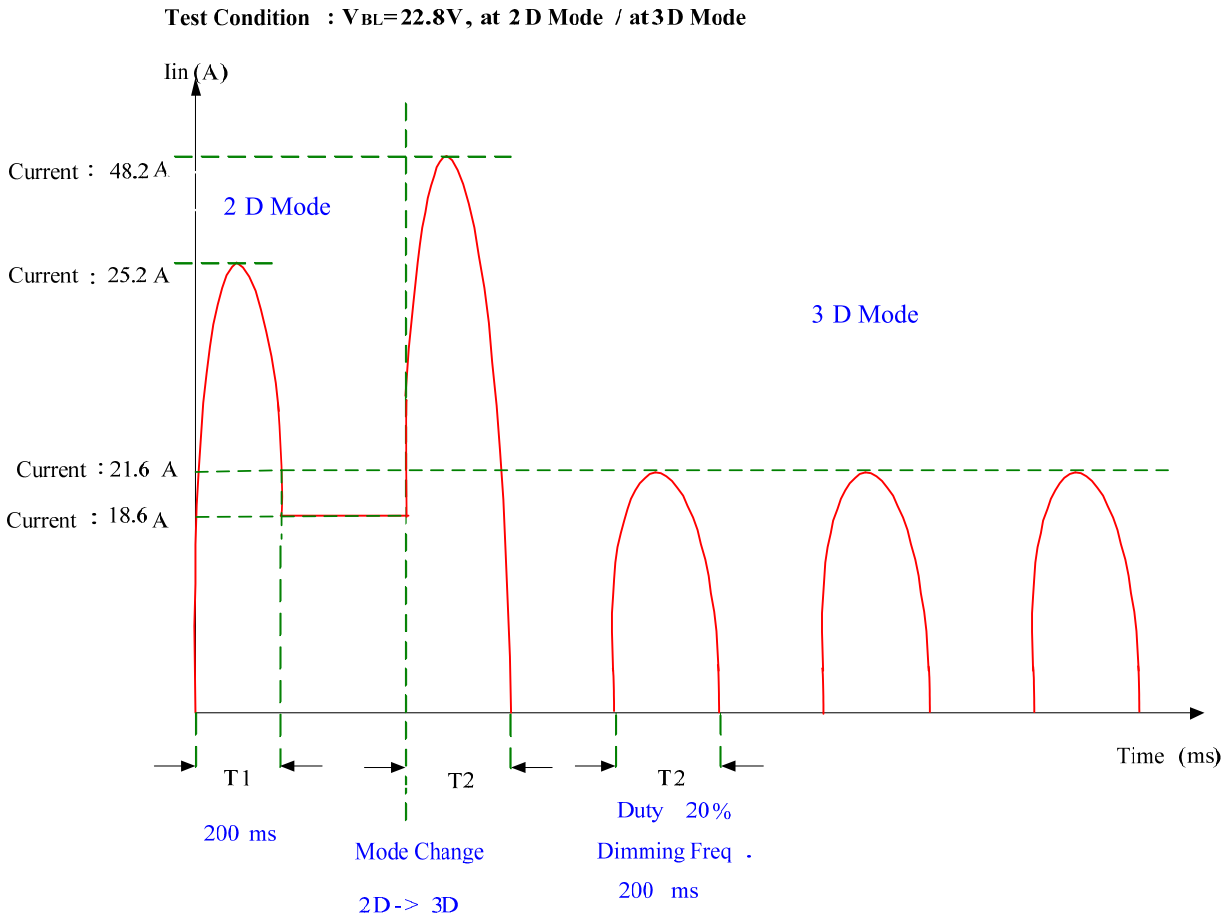
Note (2) The measurement condition of Max. value is based on 84.5" backlight unit under input voltage 24V at 2D/3D Mode and lighting 1 hour later.

Note (3) For input inrush current measure, the VBL rising time from 10% to 90% is about 20ms.

Note (4) EPWM signal have to input available duty range. And , under 5% duty (DDR) IS only valid for electrical operation.

Note (5) FB and DDR are available only at 2D Mode.The dimming frequency follows the frequency of EPWM in 2D normal mode.

Note (6) Below diagram is only for power supply design reference.



Note (7) The lifetime is defined as the time which luminance of the LED decays to 50% compared to the initial value,

Operating condition: Continuous operating at Ta = 25±2℃

3.2.2 CONVERTER INTERFACE CHARACTERISTICS

Parameter		Symbol	Test Condition	Value			Unit	Note	
				Min.	Typ.	Max.			
On/Off Control Voltage	ON	VBLON	—	2.0	—	5.0	V		
	OFF		—	0	—	0.8	V		
External PWM Control Voltage	HI	VEPWM	—	2.0	—	5.25	V	Duty on	(5), (6)
	LO		—	0	—	0.8	V	Duty off	
External PWM Frequency		F_{EPWM}	—	90	160	190	Hz	Normal mode (7)	
Error Signal		ERR	—	—	—	—	—	Abnormal: Open	
VBL Rising Time		Tr1	—	20	—	—	ms	10%-90%V_{BL}	
Control Signal Rising Time		Tr	—	—	—	100	ms		
Control Signal Falling Time		Tf	—	—	—	100	ms		
PWM Signal Rising Time		TPWMR	—	—	—	50	us	(6)	
PWM Signal Falling Time		TPWMF	—	—	—	50	us		
Input Impedance		Rin	—	1	—	—	MΩ	EPWM, BLON	
PWM Delay Time		TPWM	—	100	—	—	ms	(6)	
BLON Delay Time		T_{on}	—	300	—	—	ms		
		T_{on1}	—	300	—	—	ms		
BLON Off Time		Toff	—	300	—	—	ms		

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the external PWM signal during backlight turn on period.

Note (2) The power sequence and control signal timing are shown in the Fig.1. For a certain reason, the converter has a possibility to be damaged with wrong power sequence and control signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL

Note (4) When converter protective function is triggered, ERR will output open collector status. Please refers to Fig.2.

Note (5) The EPWM interface that inserts a pull up resistor to 5V in Max Duty (100%), please refers to Fig.3.

Note (6) EPWM is available only at 2D Mode.

Note (7) EPWM signal have to input available frequency range.

Note (8) [Recommend] EPWM duty ratio is set at 100%(Max. Brightness) in 3D Mode.

Note (9) Used the EPWM signal control user dimming only in L/D OFF. When L/D ON or 2D scan mode. Please reference 5.1 Note(11) and application Note.

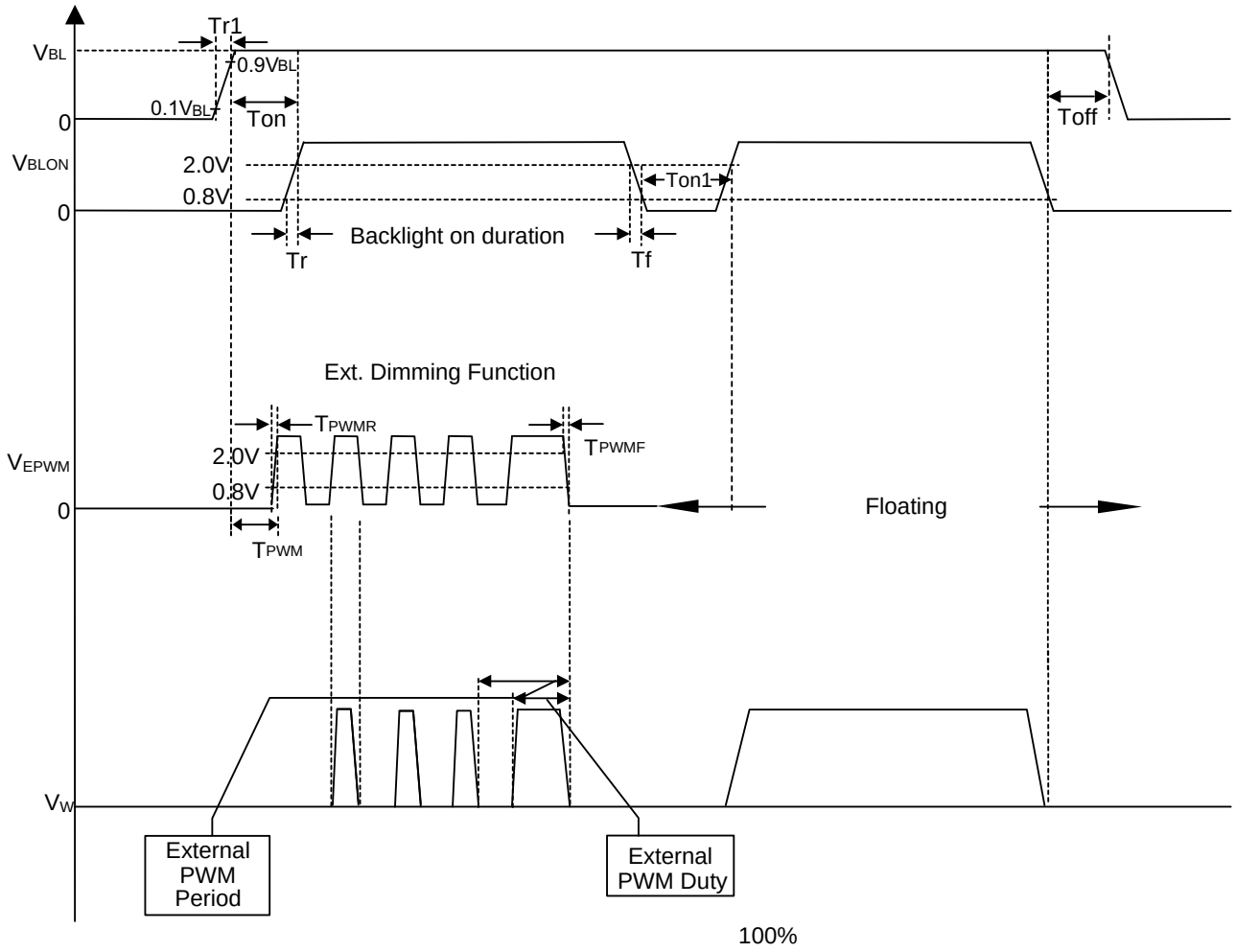


Fig. 1

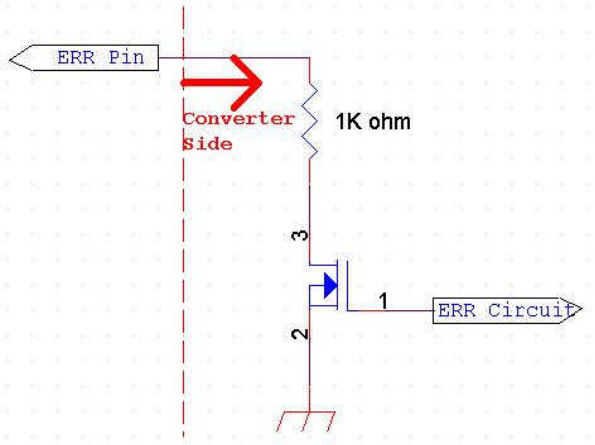


Fig. 2

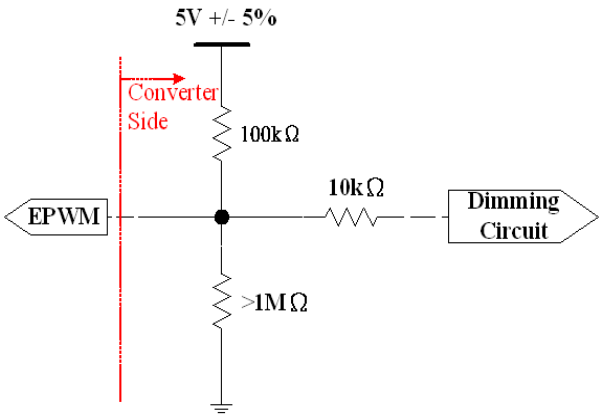
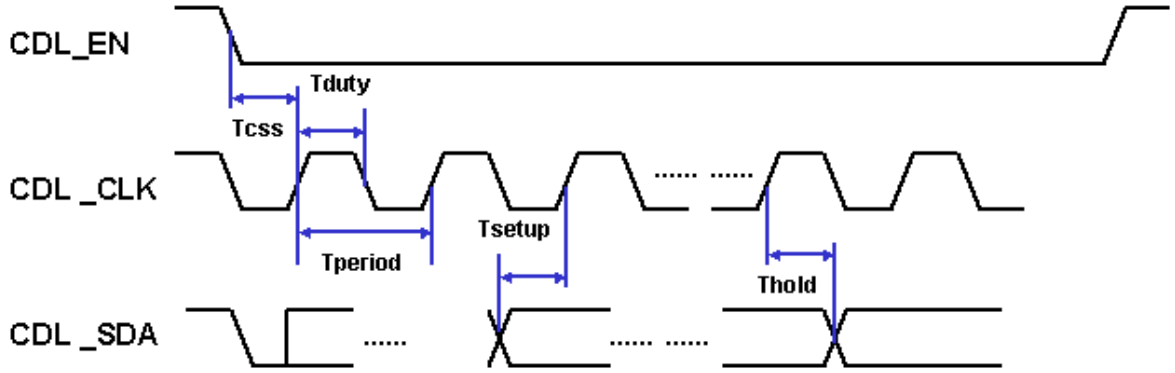


Fig. 3

3.2.3CONVERTER CDL INTERFACE CHARACTERISTICS

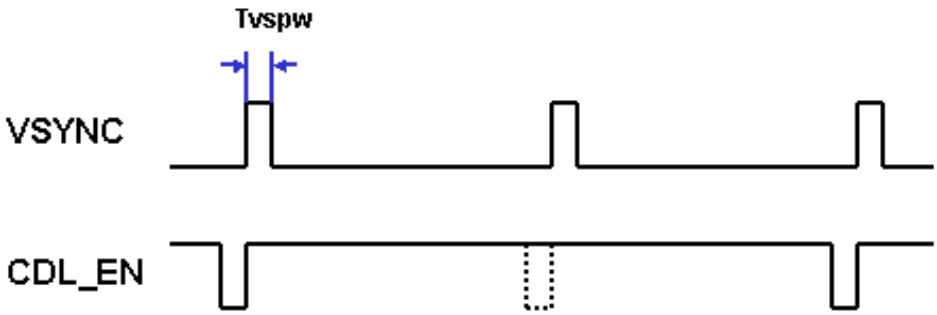
INX CDL setting must follow ***V850DK1-KD1 CDL Application Note-Ver.1 .***

- **CDL Timing Specification: SOC to converter board**



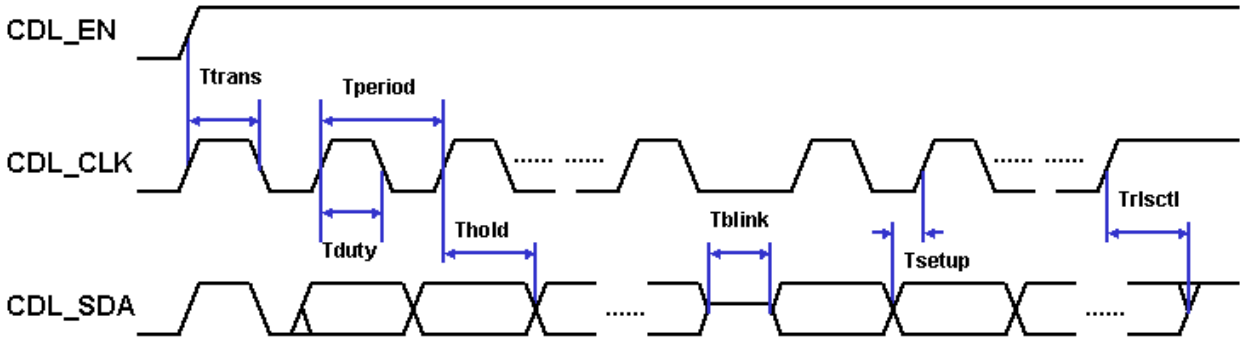
Parameter	Description	SYM	MIN	TYP	MAX	UNIT
SCK cycle time (one CDL connector)	SCK Cycle time	Tperiod	850	1000	1150	ns
CDL_EN to SCK rise	CS setup time	Tcss	1150	-	-	ns
SDA setup time	SDA Setup time	Tsetup	287.5	-	-	ns
SDA Hold time	SDA Hold time	Thold	460	-	-	ns
Duty ratio of SCK	Duty cycle for SCK	Tduty	45	-	55	%
VH	SPI bus high level		2.5	3.3	3.6	V
VL	SPI bus low level		0	0.2	0.6	V

➢ **CDL Timing Specification: VSYNC**



Parameter	Description	SYM	MIN	TYP	MAX	UNIT
VSYNC pulse width	VSYNC pulse width	Tvspw	5.0			us
VSYNC VH	VSYNC high level		3.0	3.3		V
VSYNC VL	VSYNC low level		0		0.6	V

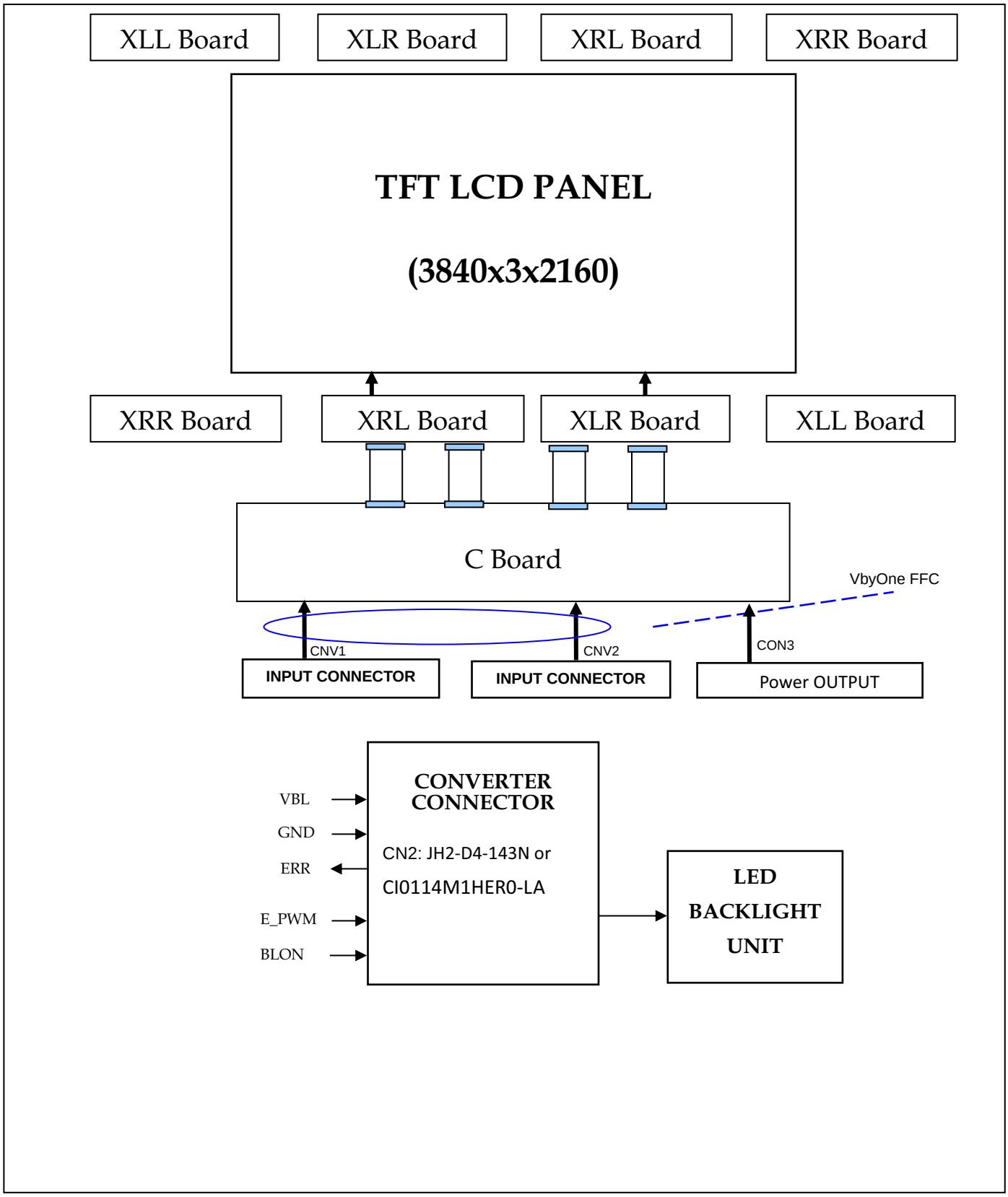
➢ **CDL Timing Specification: Converter board to SOC**



Parameter	Description	SYM	MIN	TYP	MAX	UNIT
SCK cycle time	SCK Cycle time	Tperiod	975	1000	1025	ns
SCK release pulse	TCON releases bus to Converter actives bus	Ttrans	512.5	-	-	ns (rising 2.5V to falling 2.5 V)
SDA setup time	SDA Setup time (SDA 30% VDD to SCK 50% VDD when SDA = 0, SDA 70% VDD to SCK 50% VDD when SDA = 1)	Tsetup	256.25	-	-	ns
SDA Hold time	SDA Hold time (SCK 30% VDD to SDA 50% VDD when SDA = 0, SCK 70% VDD to SDA 50% VDD when SDA = 1)	Thold	410	-	-	ns
Blink of between word	Blink of between word	Tblink	1025		9750	ns
SCK duty cycle	Duty cycle for SCK	Tduty	45	-	55	%
Release control	Release control time	Trlsctl	256.25	-	975	ns
VH	SPI bus high level		2.5	3.3	3.6	V
VL	SPI bus Low level		0	0.2	0.6	V

4. BLOCK DIAGRAM OF INTERFACE

4.1 TFT LCD MODULE



5 .INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

CNV1 Connector Pin Assignment (JAE FI-RE51S-HF/P-Two187059-51221)

Pin	Name	Description	Note
1	N.C.	No Connection(Internal +12V use)	(11)
2	N.C.	No Connection(Internal +12V use)	(11)
3	N.C.	No Connection(Internal +12V use)	(11)
4	N.C.	No Connection(Internal +12V use)	(11)
5	N.C.	No Connection(Internal +12V use)	(11)
6	N.C.	No Connection(Internal +12V use)	(11)
7	N.C.	No Connection(Internal +12V use)	(11)
8	N.C.	No Connection(Internal +12V use)	(11)
9	N.C.	No Connection(Internal +12V use)	(11)
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	N.C.	No Connection	(11)
16	L/R	Input signal for Left/Right synchronous signal.	(3) (8)
17	2D/3D	2D/3D Enable	(2) (8)
18	N.C.	No Connection	(11)
19	N.C.	No Connection	(11)
20	N.C.	No Connection	(11)
21	N.C.	No Connection	(11)
22	N.C.	No Connection	(7)
23	N.C.	No Connection	(11)
24	N.C.	No Connection	(11)
25	HTPDN	Hot plug detect output, Open drain.	
26	LOCKN	Lock detect output, Open drain.	
27	GND	Ground	
28	RX0N	1ST Pixel Negative VbyOne differential data input in area A. Lan 0	(1)
29	RX0P	1ST Pixel Positive VbyOne differential data input in area A. Lan 0	
30	GND	Ground	
31	RX1N	2ND Pixel Negative VbyOne differential data input in area A. Lan 1	(1)
32	RX1P	2ND Pixel Positive VbyOne differential data input in area A. Lan 1	
33	GND	Ground	

34	RX2N	3RD Pixel Negative VbyOne differential data input in area A. Lan 2	(1)
35	RX2P	3RD Pixel Positive VbyOne differential data input in area A. Lan 2	
36	GND	Ground	
37	RX3N	4TH Pixel Negative VbyOne differential data input in area A. Lan 3	(1)
38	RX3P	4TH Pixel Positive VbyOne differential data input in area A. Lan 3	
39	GND	Ground	
40	RX4N	5TH Pixel Negative VbyOne differential data input in area A. Lan 4	(1)
41	RX4P	5TH Pixel Positive VbyOne differential data input in area A. Lan 4	
42	GND	Ground	
43	RX5N	6TH Pixel Negative VbyOne differential data input in area A. Lan 5	(1)
44	RX5P	6TH Pixel Positive VbyOne differential data input in area A. Lan 5	
45	GND	Ground	
46	RX6N	7TH Pixel Negative VbyOne differential data input in area A. Lan 6	(1)
47	RX6P	7TH Pixel Positive VbyOne differential data input in area A. Lan 6	
48	GND	Ground	
49	RX7N	8TH Pixel Negative VbyOne differential data input in area A. Lan 7	(1)
50	RX7P	8TH Pixel Positive VbyOne differential data input in area A. Lan 7	
51	GND	Ground	

CNV2 Connector pin assignment (JAE FI-RE41S-HF/P-Two 187060-41221)

Pin	Name	Description	Note
1	GND	Ground	
2	RX8N	1ST Pixel Negative VbyOne differential data input in area B. Lan 8	(1)
3	RX8P	1ST Pixel Positive VbyOne differential data input in area B. Lan 8	
4	GND	Ground	
5	RX9N	2ND Pixel Negative VbyOne differential data input in area B. Lan 9	(1)
6	RX9P	2ND Pixel Positive VbyOne differential data input in area B. Lan 9	
7	GND	Ground	
8	RX10N	3RD Pixel Negative VbyOne differential data input in area B. Lan 10	(1)
9	RX10P	3RD Pixel Positive VbyOne differential data input in area B. Lan 10	
10	GND	Ground	
11	RX11N	4TH Pixel Negative VbyOne differential data input in area B. Lan 11	(1)
12	RX11P	4TH Pixel Positive VbyOne differential data input in area B. Lan 11	
13	GND	Ground	

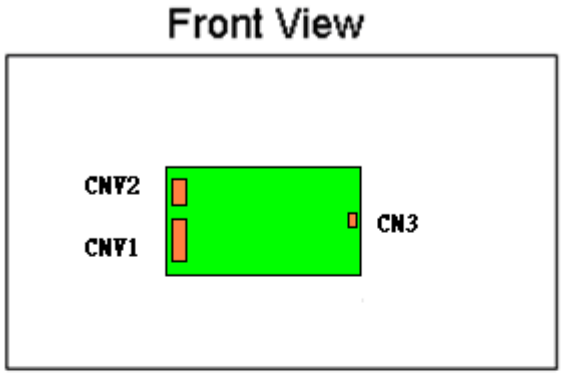
14	RX12N	5TH Pixel Negative VbyOne differential data input in area B. Lan 12	(1)
15	RX12P	5TH Pixel Positive VbyOne differential data input in area B. Lan 12	
16	GND	Ground	
17	RX13N	6TH Pixel Negative VbyOne differential data input in area B. Lan 13	(1)
18	RX13P	6TH Pixel Positive VbyOne differential data input in area B. Lan 13	
19	GND	Ground	
20	RX14N	7TH Pixel Negative VbyOne differential data input in area B. Lan 14	(1)
21	RX14P	7TH Pixel Positive VbyOne differential data input in area B. Lan 14	
22	GND	Ground	
23	RX15N	8TH Pixel Negative VbyOne differential data input in area B. Lan 15	(1)
24	RX15P	8TH Pixel Positive VbyOne differential data input in area B. Lan 15	
25	GND	Ground	
26	N.C.	No Connection	(11)
27	N.C.	No Connection	
28	N.C.	No Connection	
29	N.C.	No Connection	
30	N.C.	No Connection	
31	N.C.	No Connection	
32	N.C.	No Connection	
33	N.C.	No Connection	
34	N.C.	No Connection	
35	N.C.	No Connection	
36	N.C.	No Connection	
37	N.C.	No Connection	
38	N.C.	No Connection	
39	N.C.	No Connection	
40	N.C.	No Connection	
41	N.C.	No Connection	

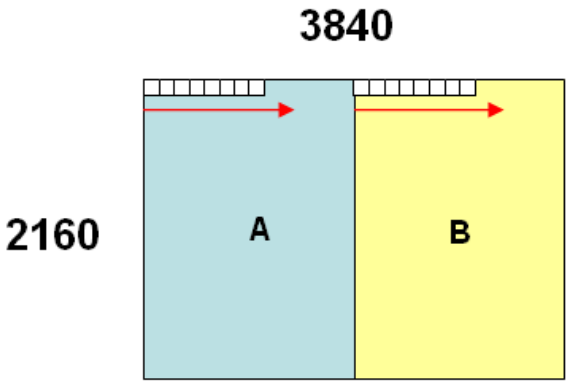
CN3 Connector Pin Assignment (SM05B-PASS-TBT(LF)(SN)(JST))

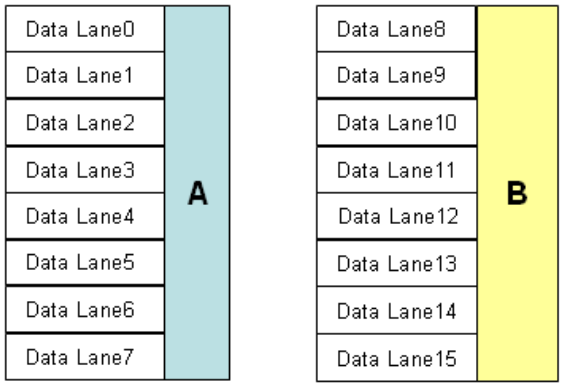
1	GND	Ground	
2	GND	Ground	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	

Note (1) V-by-One® HS Data Mapping

Area	Lane	Data Stream
A	Lane 0	1, 9, 17, ..., 1905, 1913
	Lane 1	2, 10, 18, ..., 1906, 1914
	Lane 2	3, 11, 19, ..., 1907, 1915
	Lane 3	4, 12, 20, ..., 1908, 1916
	Lane 4	5, 13, 21, ..., 1909, 1917
	Lane 5	6, 14, 22, ..., 1910, 1918
	Lane 6	7, 15, 23, ..., 1911, 1919
	Lane7	8, 16, 24, ..., 1912, 1920
B	Lane 8	1921, 1929, 1937, ..., 3825, 3833
	Lane 9	1922, 1930, 1938, ..., 3826, 3834
	Lane 10	1923, 1931, 1939, ..., 3827, 3835
	Lane 11	1924, 1932, 1940, ..., 3828, 3836
	Lane12	1925, 1933, 1941, ..., 3829, 3837
	Lane 13	1926, 1934, 1942, ..., 3830, 3838
	Lane 14	1927, 1935, 1943, ..., 3831, 3839
	Lane 15	1928, 1936, 1944, ..., 3832, 3840







Note (2) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

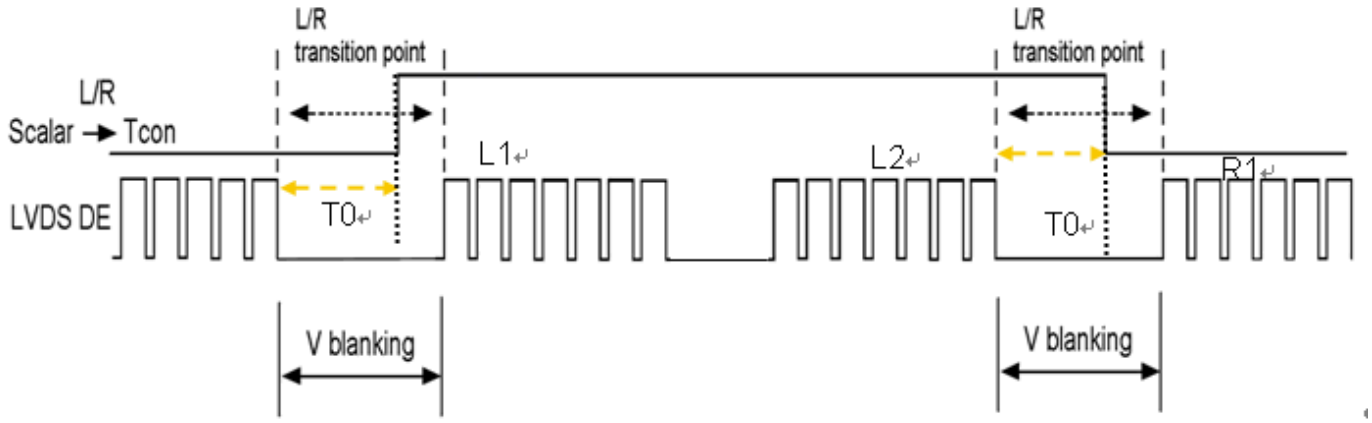
2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (3) Input signal for Left Right eye frame synchronous

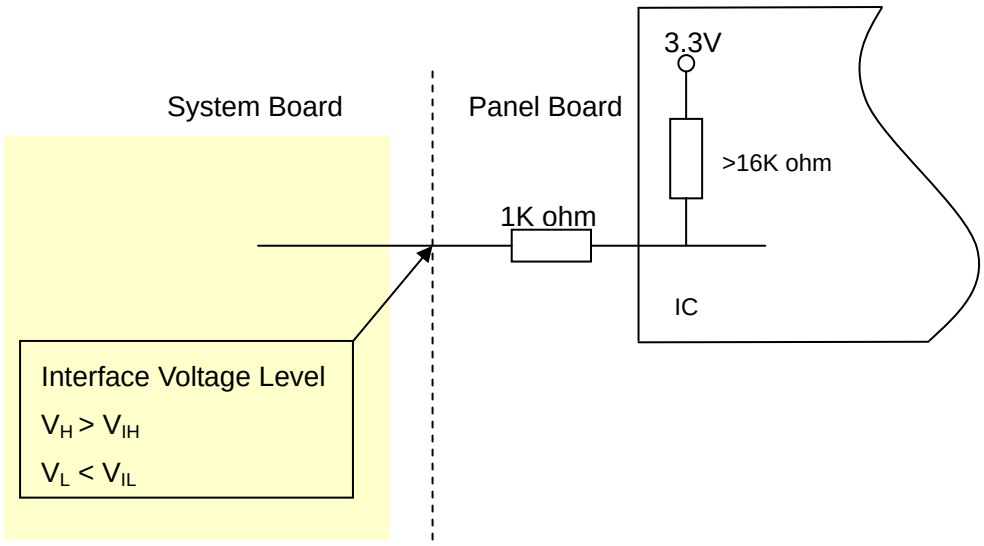
V_{IL}=0~0.8 V, V_{IH}=2.0~3.3 V

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

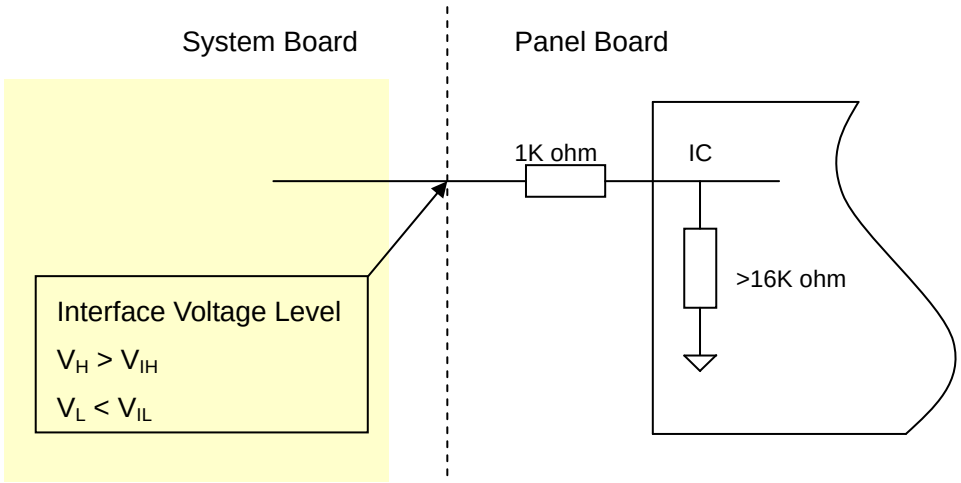
T0>=22line(Video board have to prepare V sync test point of Vx1 transmitter input)



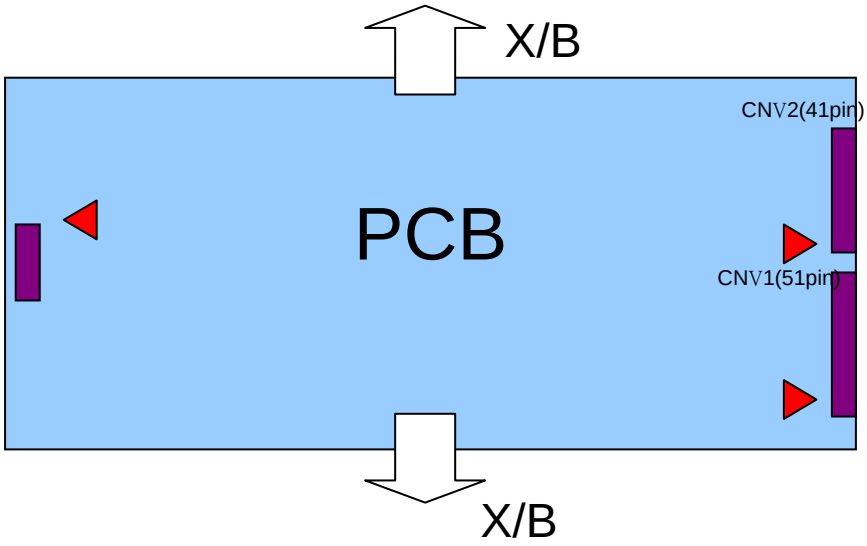
Note (7) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



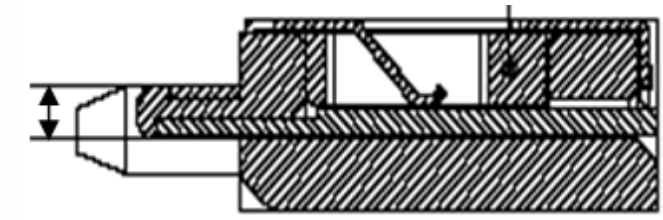
Note (8) Interface optional pin has internal scheme as following diagram. Customer should keep the interface voltage level requirement which including Panel board loading as below.



Note (9) VbyOne HS connector pin order defined as follows



Note (10) V-by-One connector mating dimension range request is 0.93mm~1.0mm as below



Note (11) Reserved for internal use. Please leave it open.

5.2 BACKLIGHT UNIT

The pin configuration for the housing and lead wire is shown in the table below.

CN4,5 : 196388-12041-3 (P-TWO) ; FF01-430-123A(FCN)

Pin №	Symbol	Feature
1	VLED	Positive of LED String
2	VLED	
3	VLED	
4	NC	NC
5	N1	Negative of LED String
6	N2	
7	N3	
8	N4	
9	N5	
10	N6	
11	N7	
12	N8	

CN3,6 : 196388-12041-3 (P-TWO) ; FF01-430-123A(FCN)

Pin №	Symbol	Feature
1	N1	Negative of LED String
2	N2	
3	N3	
4	N4	
5	N5	
6	N6	
7	N7	
8	N8	
9	NC	NC
10	VLED	Positive of LED String
11	VLED	
12	VLED	

5.3 CONVERTER UNIT

CN1 (Header) : CI0114M1HR0-LA (CvilLux) ; JH2-D4-143N(FCN)

Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	ERR	Normal (GND) ; Abnormal (Open collector)
12	BLON	BL ON/OFF
13	NC	NC
14	E_PWM	External PWM Control

CN2 (Header) : CI0112M1HR0-LA (CvilLux) ; JH2-D4-123N(FCN)

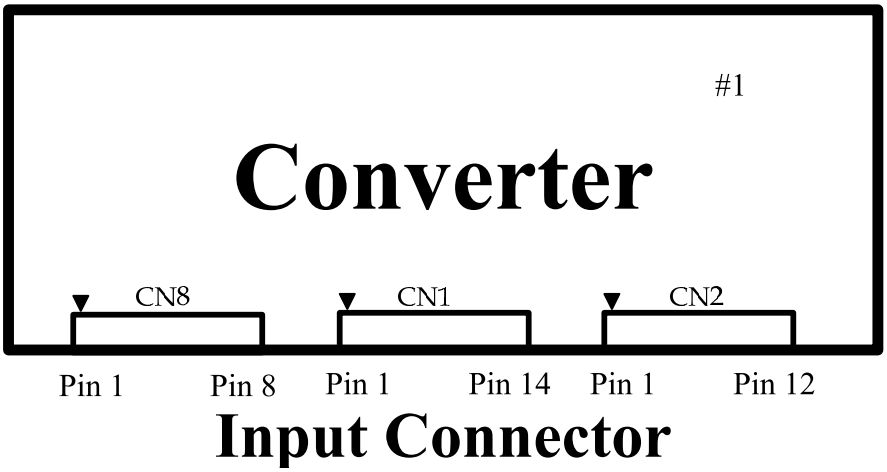
Pin No.	Symbol	Feature
1	VBL	+24V
2		
3		
4		
5		
6	GND	GND
7		
8		
9		
10		
11	NC	NC
12	NC	NC

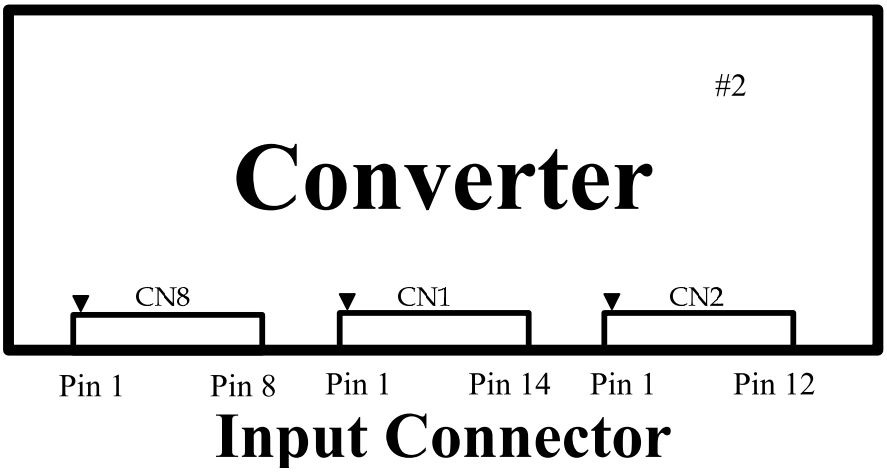
Note (1) If Pin14 is open, E_PWM is 100% duty.

Note (2) Input connector pin order defined as follows

CN8 : 196389-08041-3(P-TWO)

Pin №	Symbol	Description	Direction
1	**CDL_EN**	CDL chip select (R/W)	SOC -> Converter board
2	GND		
3	CDL_SCK	CDL clock to synchronize the data of CDL_SDA	Bi-direction (SOC<-> Converter board)
4	VSYNC	Converter V sync (option, based on platform)	SOC -> Converter board
5	CDL_SDA	CDL data	Bi-direction (SOC <-> Converter board)
6	GND		
7	NA		
8	NA		





5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										Blue									
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:			:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	;	:	:	:	:	:	:	:	:	:
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage，1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram. (Ta = 25 ± 2 ºC)

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
Frequency	Data Clock	1/Tc	70	74.3	80	MHz	(1)
VbyOne Receiver	Data skew between each area (A/B)	Tblock	-0.06	—	0.06	H	(2)
	Intra-Pair skew		-0.3	—	0.3	UI	(3)
	Inter-pair skew		-5	—	5	UI	(4)
	Spread spectrum modulation range	F_{clkin_mod}	1/Tc-0.5%	—	1/Tc+0.5%	MHz	(5)
	Spread spectrum modulation frequency	F_{SSM}	—	—	30	KHz	

6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		Fr5	94	100	106	Hz	(9),(10)
	3D mode		Fr5	188	200	212	Hz	(7),(9),(10)
Vertical Active Display Term (8 Lan,1920X2160 Active Area)	2D Mode	Total	Tv	2200	2700	2790	Th	Tv=Tvd+Tvb
		Display	Tvd	2160	2160	2160	Th	
		Blank	Tvb	40	540	630	Th	
		V back porch	V_back	13	54	61	line	Tvb=V_back+V_front+V_width
		V front porch	V_front	2	476	554	line	
		Vsync width	V_width	1	10	15	line	
	3D Mode	Total	Tv	1116	1125	1396	Th	(6), (8)
		Display	Tvd	1080	1080	1080	Th	
		Blank	Tvb	36	45	316	Th	
		V back porch	V_back	13	15	32	line	Tvb=V_back+V_front+V_width
		V front porch	V_front	22	27	279	line	
		Vsync width	V_width	1	3	5	line	
Horizontal Active Display Term (8 Lan,1920X2160	2D Mode/ 3D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	

		Blank	Thb	30	45	60	Tc	
		H back porch	H_back	10	21	30	Tc	Thb=H_back+H_front+H_width
		H front porch	H_front	4	16	30	Tc	
		Hsync width	H_width	5	8	10	Tc	

6.1.2 Timing spec for Frame Rate = 120Hz

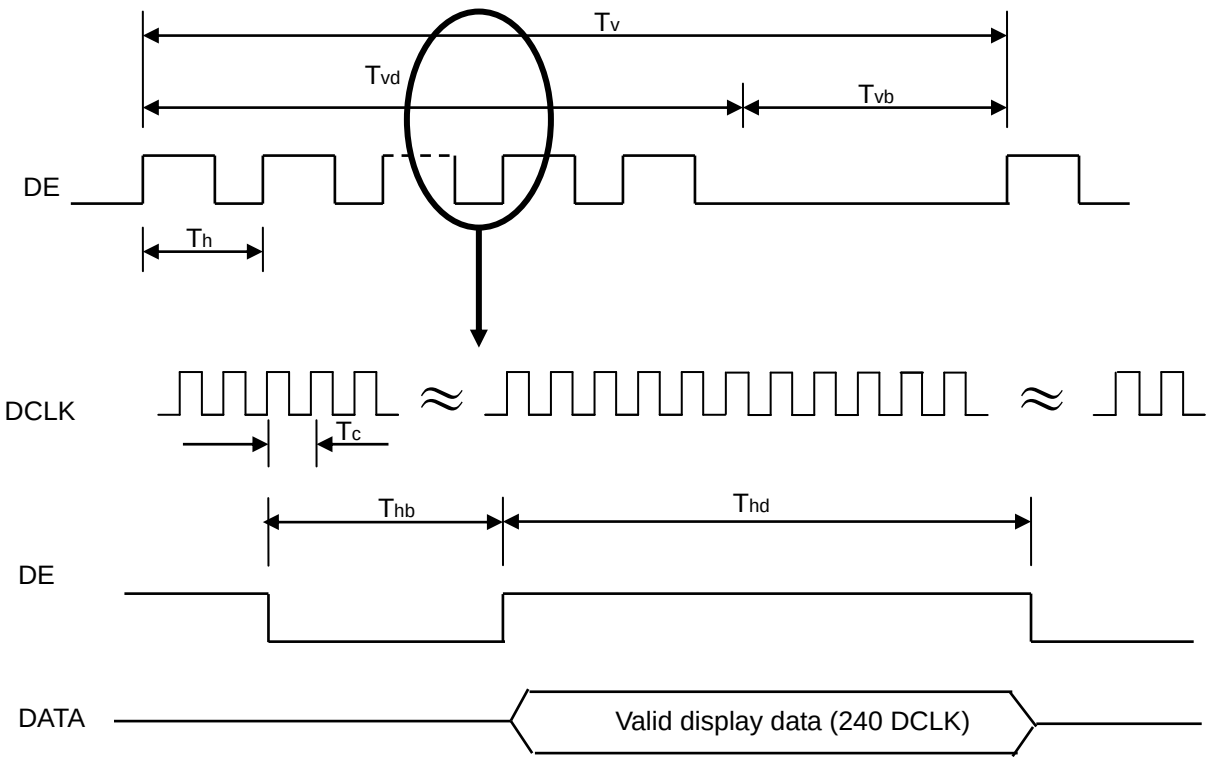
Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		Fr6	114	120	126	Hz	(9),(10)
	3D mode		Fr6	228	240	252	Hz	(7),(9),(10)
Vertical Active Display Term (8 Lan,1920X2160 Active Area)	2D Mode	Total	Tv	2200	2250	2790	Th	Tv=Tvd+Tvb
		Display	Tvd	2160	2160	2160	Th	—
		Blank	Tvb	40	90	630	Th	—
		V back porch	V_back	13	72	115	line	Tvb=V_back+V_front+V_width
		V front porch	V_front	2	8	500	line	
		Vsync width	V_width	1	10	15	line	
	3D Mode	Total	Tv	1116	1125	1200	Th	(6), (8)
		Display	Tvd	1080	1080	1080	Th	
		Blank	Tvb	36	45	120	Th	
		V back porch	V_back	13	15	32	line	Tvb=V_back+V_front+V_width
		V front porch	V_front	22	27	83	line	
		Vsync width	V_width	1	3	5	line	
Horizontal Active Display Term (8 Lan,1920X2160 Active Area)	2D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	—
		Blank	Thb	30	45	60	Tc	—
		H back porch	H_back	10	21	30	Tc	Thb=H_back+H_front+H_width
		H front porch	H_front	4	16	30	Tc	
		Hsync width	H_width	5	8	10	Tc	
	3D Mode	Total	Th	270	285	300	Tc	Th=Thd+Thb
		Display	Thd	240	240	240	Tc	—
		Blank	Thb	30	45	60	Tc	—
		H back porch	H_back	10	21	30	Tc	Thb=H_back+H_front+H_width
		H front porch	H_front	4	16	30	Tc	
		Hsync width	H_width	5	8	10	Tc	

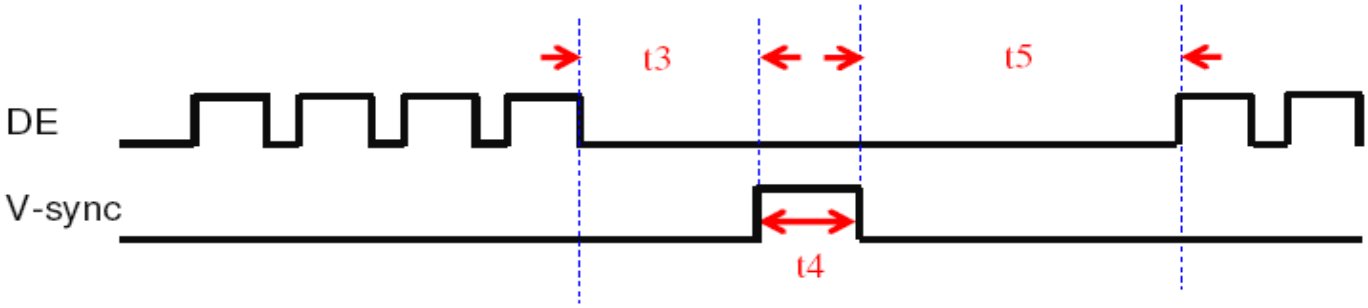
Note (1) Please make sure the range of pixel clock has follow the below equation：

Fclkin(max) ≧ Fr × Tv × Th

Fr × Tv × Th ≧ Fclkin (min)

INPUT SIGNAL TIMING DIAGRAM

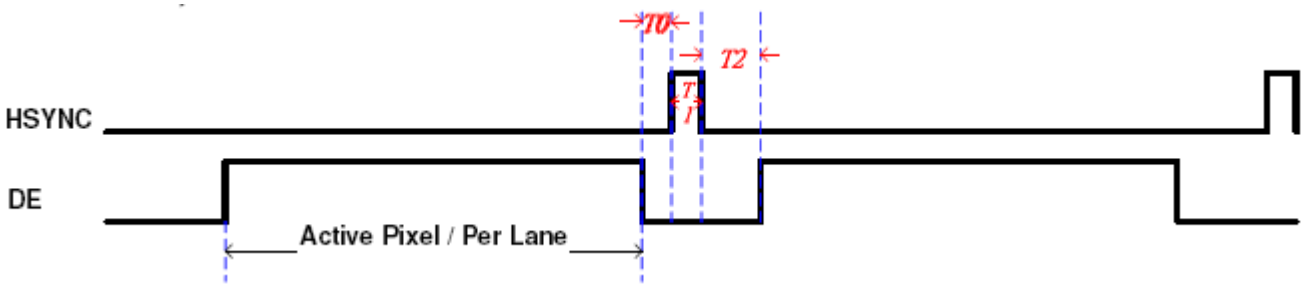




T3>=2H

T4>=1H

T5>=13H

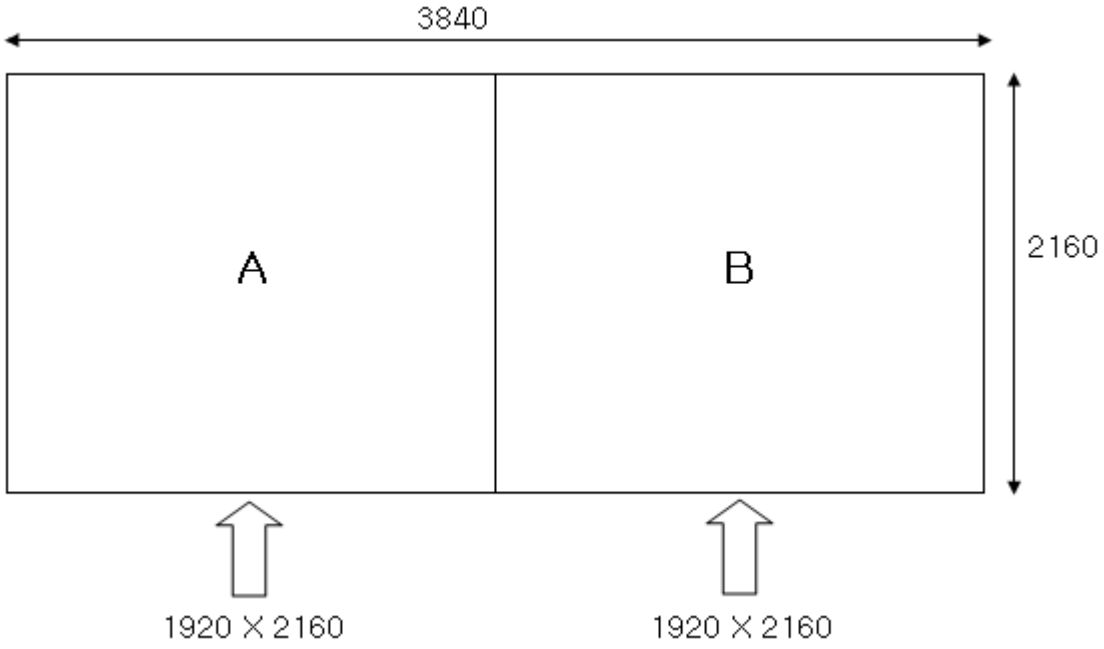


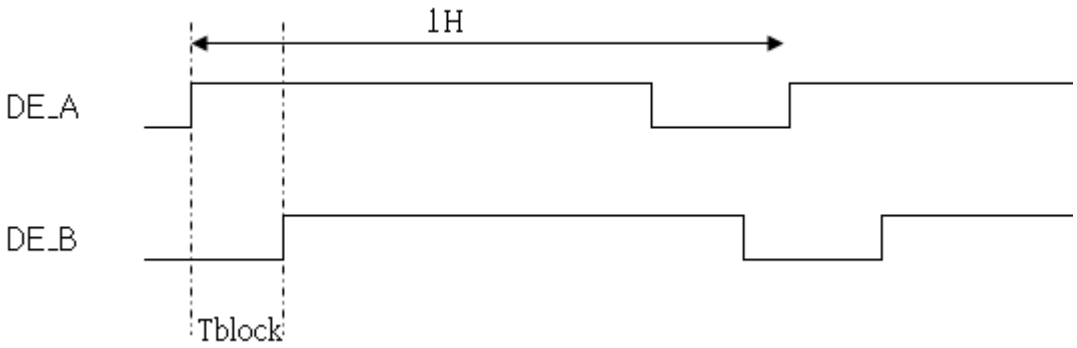
T0>=4 Tc

T1>=5 Tc

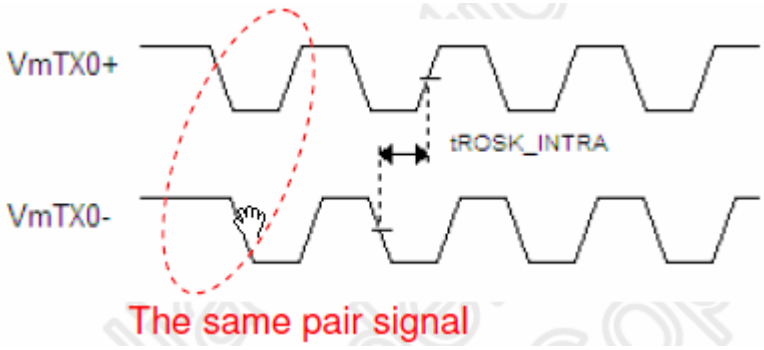
T2>=10 Tc

Note (2) Data skew between areas

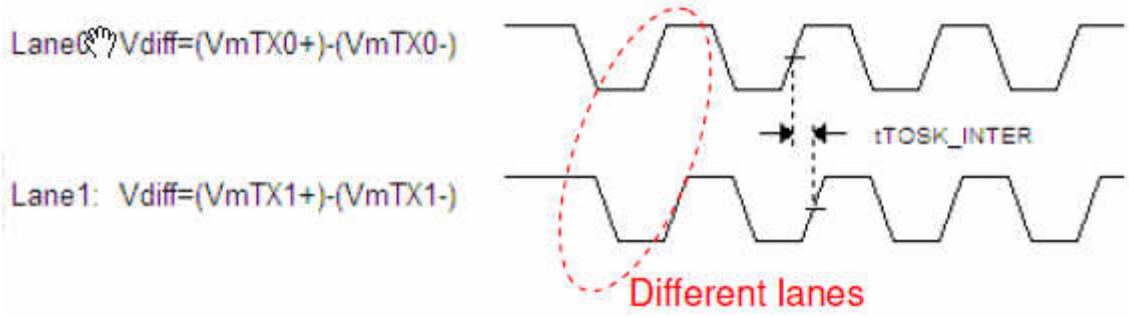




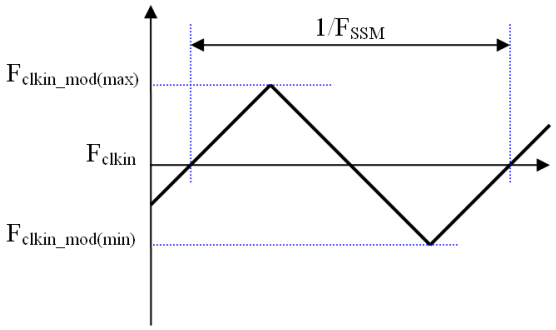
Note (3) VbyOne HS Intra-pair skew



Note (4) VbyOne HS Inter-pair skew.



Note (5) The SSCG (Spread spectrum clock generator) is defined as below figures.



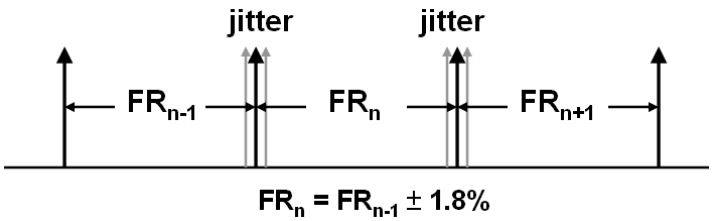
Note (6) Please fix the Vertical timing (Vertical Total =TBD / Display = TBD / Blank = TBD) in 120Hz 3D mode

Note (7) In 3D mode, the set up Fr6 in Typ. ±3 Hz .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ. ±30.In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (9) The frame-to-frame jitter of the input frame rate is defined as the above figures. FRn = FRn-1 ± 1.8%.

Note (10) The setup of the frame rate jitter > 1.8% may result in the cosmetic LED backlight symptom but the electric function is not affected.



6.2 V by One Input Signal Timing Diagram

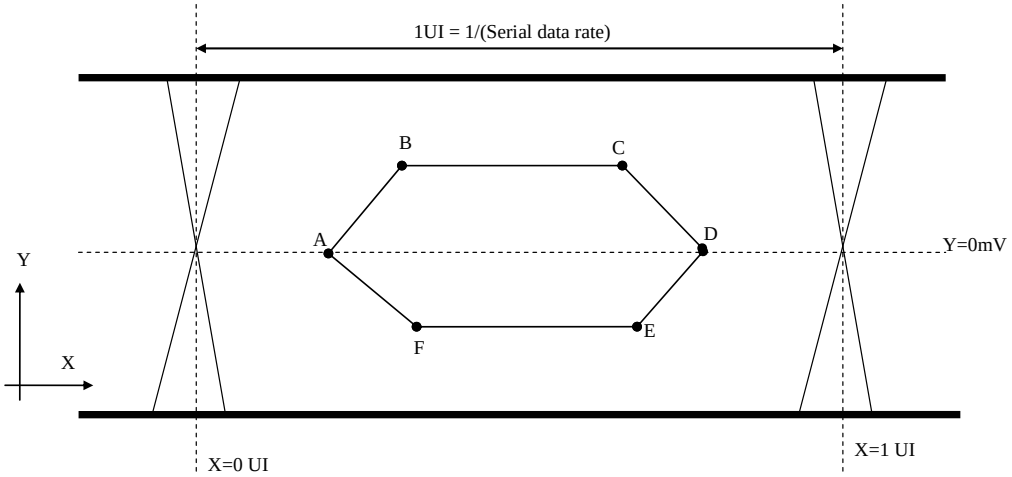


Table 1 Eye Mask Specification

	X [UI]	Y [mV]	Note
A	0.25	0	(1)
B	0.3	50	(1)
C	0.7	50	(1)
D	0.75	0	(1)
E	0.7	-50	(1)
F	0.3	-50	(1)

Note (1) Input levels of V-by-One HS signals are comes from “V-by-One HS Stander Ver.1.4”

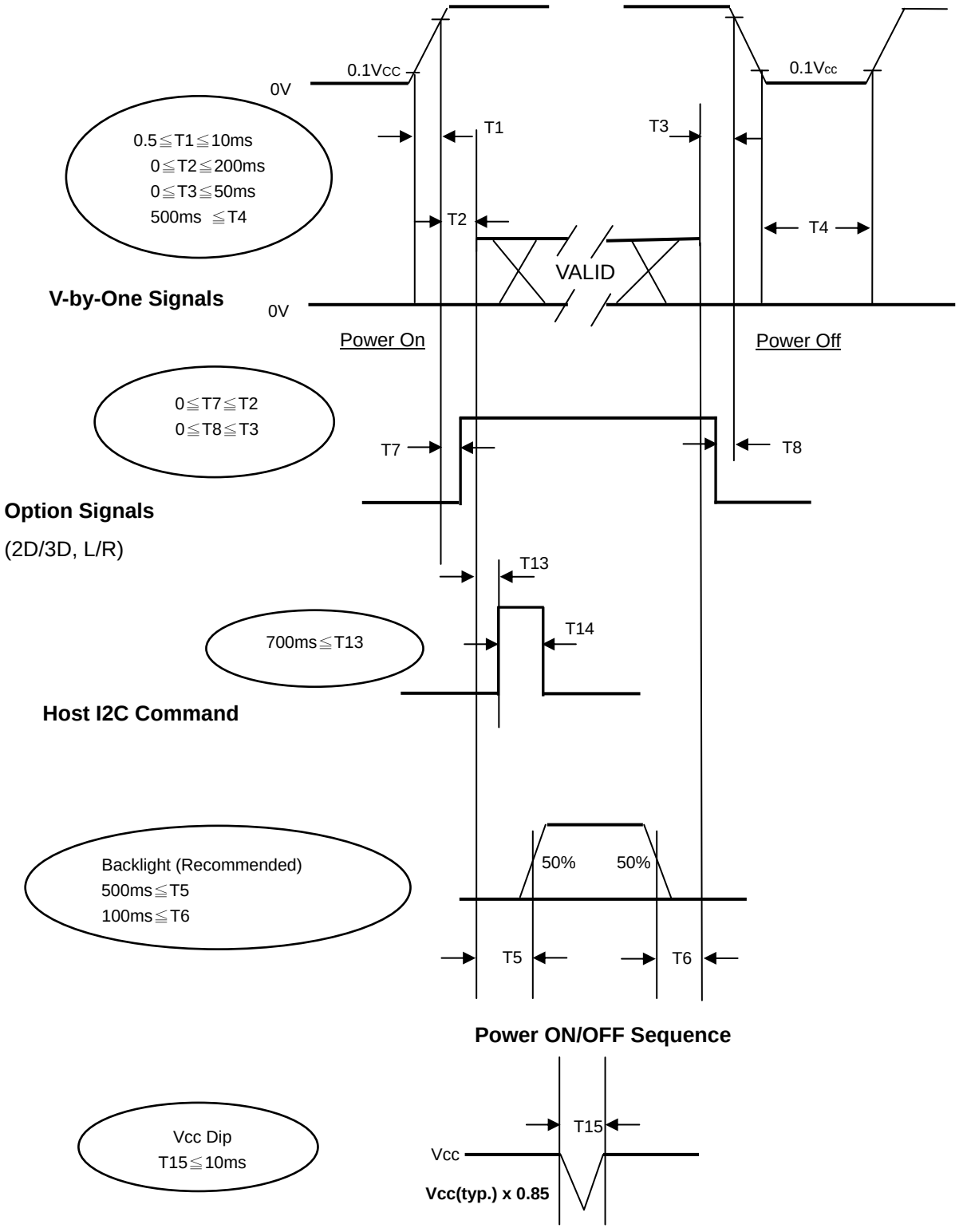
6.3 Byte Length and Color mapping of V-by-One HS

Packer input & Unpacker output		30bpp RGB (10bit)
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]

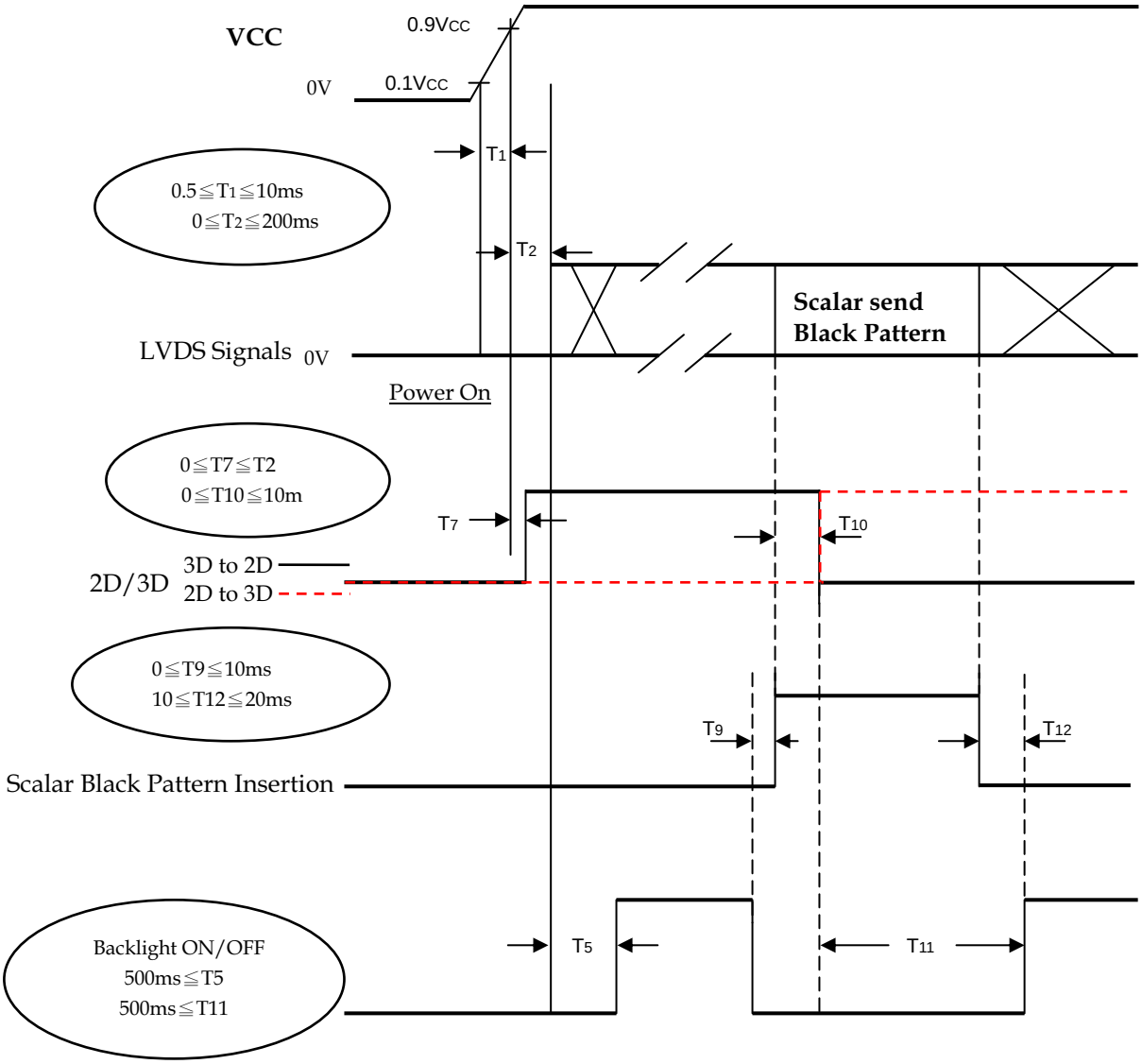
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

6.4 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



6.5 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0,that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

Note (7) Vcc must decay smoothly when power-off.

Note (8) T5 Backlight turn on time depend on T14 command length+T13

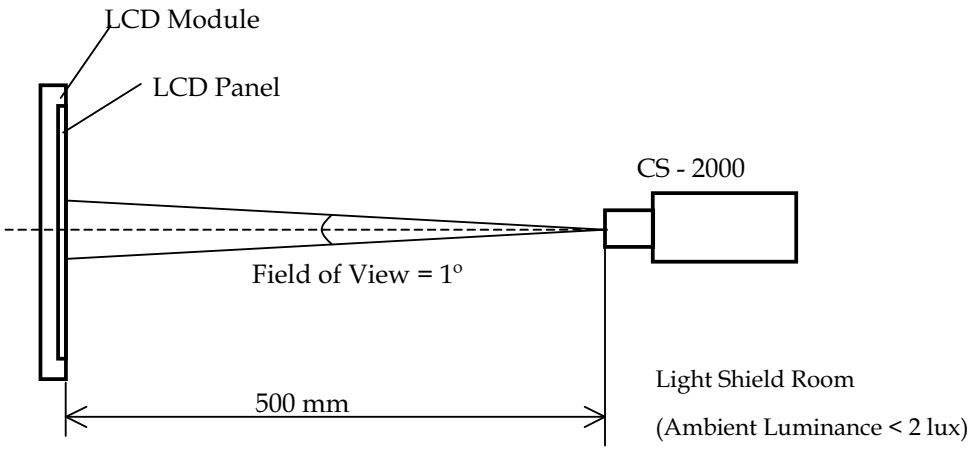
7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12±1.2	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Vertical Frame Rate	Fr	120	Hz

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.

Local Dimming Function should be Disable before testing to get the steady optical characteristics (According to 5.1 CNF1 Connector Pin Assignment, Pin no. "42")



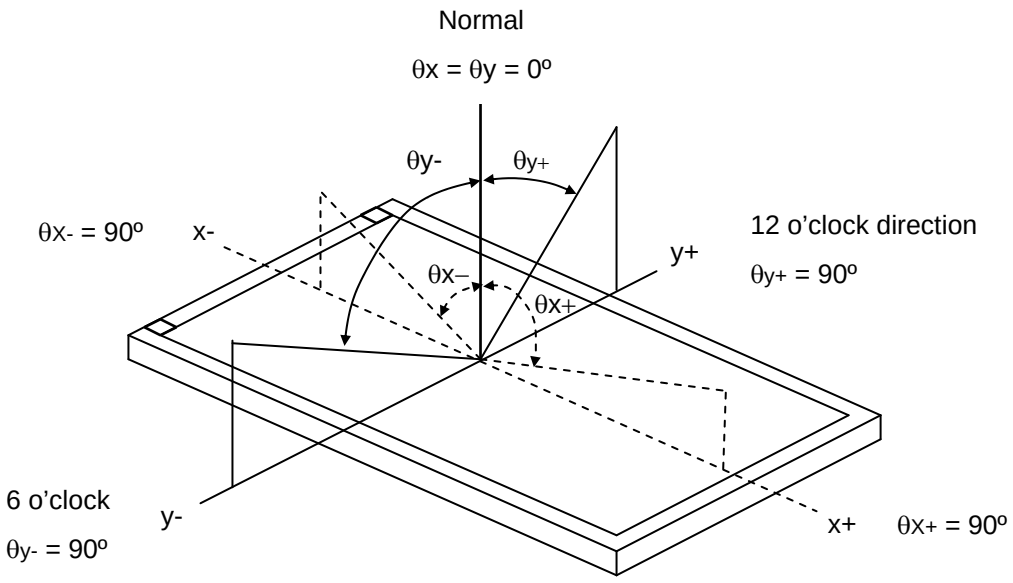
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol		Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR		θ_x=0°, θ_Y =0° Viewing angle at normal direction	2000	3000	-	-	Note (2)
Response Time		Gray to gray				6.5	13	ms	Note (3)
Center Luminance of White		L_C	2D		400	500	-	cd/m²	Note (4)
			3D			60	-	cd/m²	Note (8)
White Variation		δW					1.3	-	Note (6)
Cross Talk		CT	2D		-		4	%	Note (5)
			3D-W			(4)	-	%	Note (8)
			3D-D			(11)	-	%	Note (8)
Color Chromaticity	Red	Rx			Typ.-0.03	(0.683)	Typ.+0.03	-	
		Ry				(0.310)		-	
	Green	Gx				(0.254)		-	
		Gy				(0.695)		-	
	Blue	Bx				(0.151)		-	
		By				(0.055)		-	
	White	Wx				0.280		-	
		Wy				0.290		-	
	Correlated color temperature					10000		K	
	Color Gamut	C.G.			-	100	-	%	NTSC
Viewing Angle	Horizontal	θ_x+		CR≥20	80	88	-	Deg.	(1)
		θ_x-			80	88	-		
	Vertical	θ_Y+			80	88	-		
		θ_Y-			80	88	-		
Transmission direction of the up polarizer		Φ_{up}		-	-	90	-	Deg.	(7)

Note (1) Definition of Viewing Angle (θx, θy) :

Viewing angles are measured by Autronic Conoscope Cono-80 (or Eldim EZ-Contrast 160R).



Note (2) Definition of Contrast Ratio (CR) :

The contrast ratio can be calculated by the following expression.

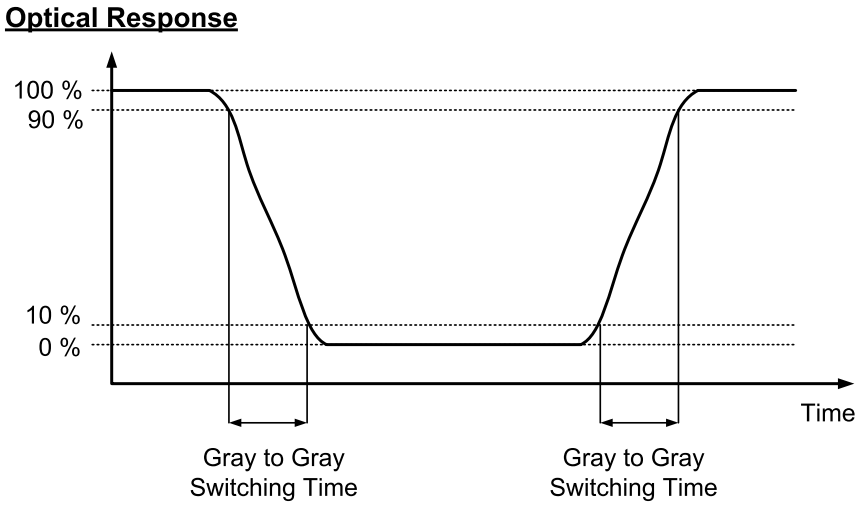
$$\text{Contrast Ratio (CR)} = \frac{\text{Surface Luminance of L1023}}{\text{Surface Luminance of L0}}$$

L1023: Luminance of gray level 1023

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (6).

Note (3) Definition of Gray-to-Gray Switching Time :



The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023 to each other.

Note (4) Definition of Luminance of White (L_C) :

Measure the luminance of gray level 1023 at center point.

L_C = L (5), where L (x) is corresponding to the luminance of the point X at the figure in Note (6).

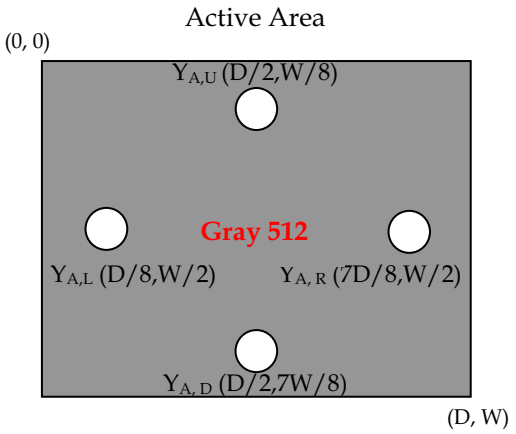
Note (5) Definition of Cross Talk (CT) :

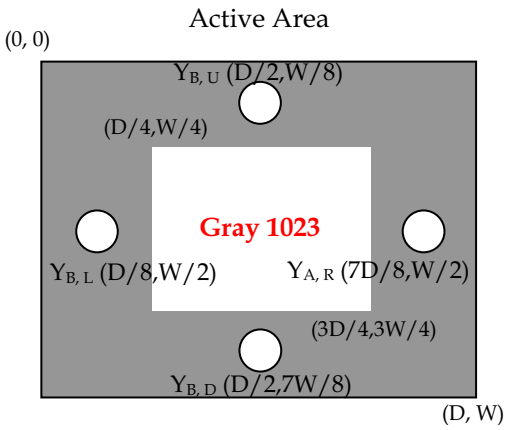
$CT = | Y_B - Y_A | / Y_A \times 100\ (\%)$

Where :

YA = Luminance of measured location without gray level 1023 pattern (cd/m2)

YB = Luminance of measured location with gray level 1023 pattern (cd/m2)

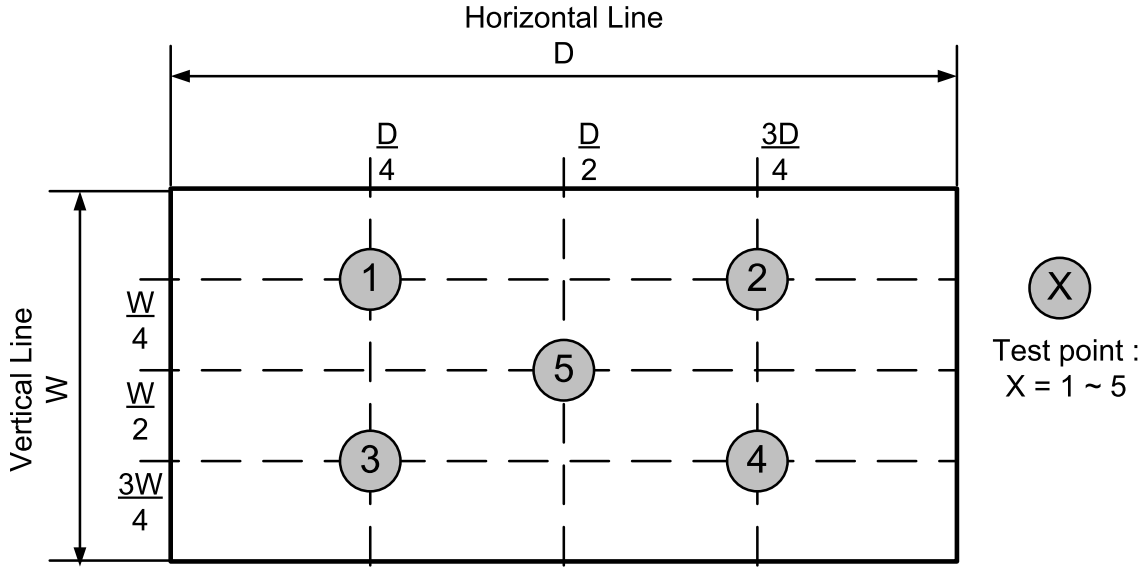




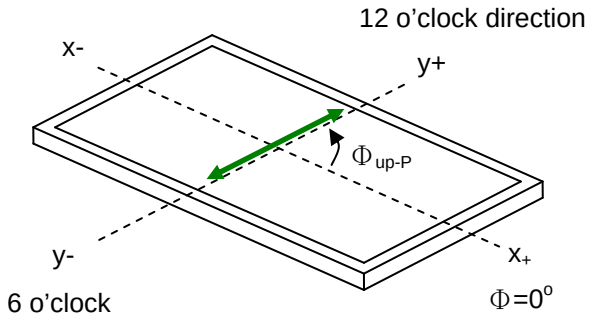
Note (6) Definition of White Variation (δW):

Measure the luminance of gray level 1023 at 5 points

$$\delta W = \frac{\text{Maximum [L (1), L (2), L (3), L (4), L (5)]}}{\text{Minimum [L (1), L (2), L (3), L (4), L (5)]}}$$

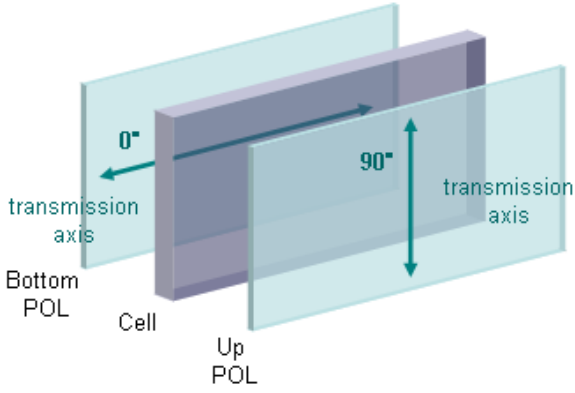


Note (7) This is a reference for designing the shutter glasses of 3D application. Definition of the transmission direction of the up polarizer ($\Phi_{up\text{-}P}$) on LCD Module :

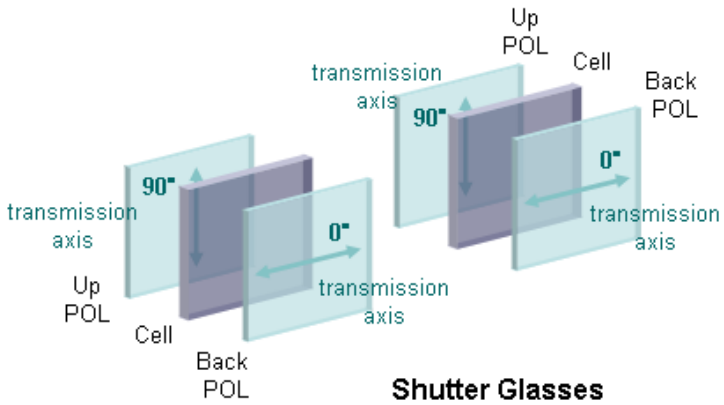


Up Polarizer

The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



LCD Module

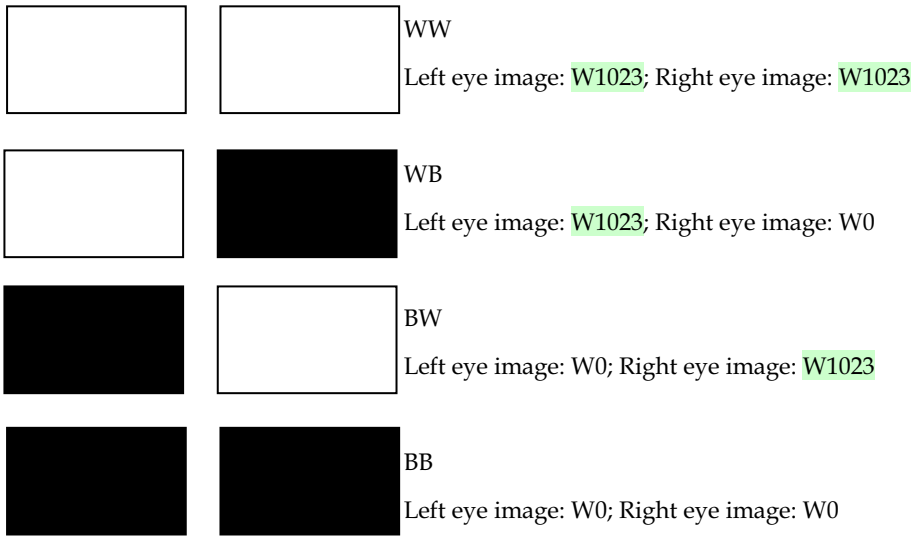


Shutter Glasses

Note (8) Definition of the 3D mode performance (measured under 3D mode, use INX's shutter glass) :

a. Test pattern

Left eye image and right eye image are displayed alternated



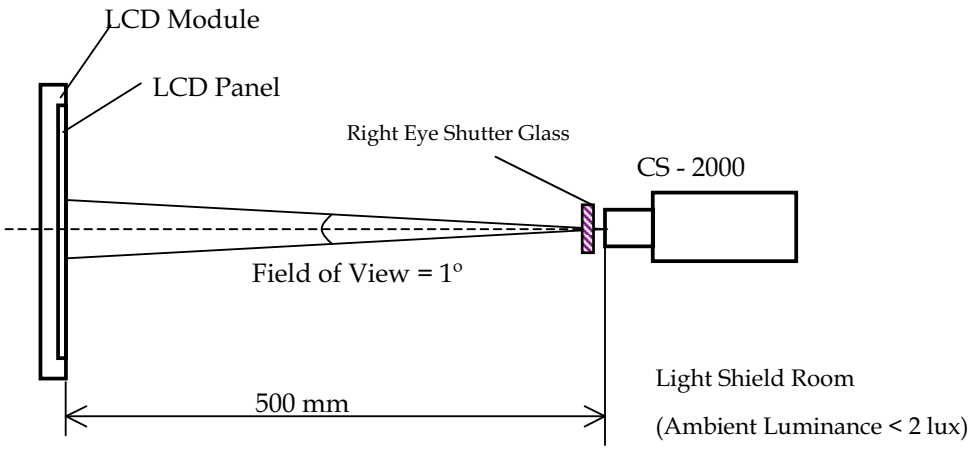
WW
Left eye image: W1023; Right eye image: W1023

WB
Left eye image: W1023; Right eye image: W0

BW
Left eye image: W0; Right eye image: W1023

BB
Left eye image: W0; Right eye image: W0

b. Measurement setup



Shutter glasses are well controlled under suitable timing, and measure the luminance of the center point of the panel through the right eye glass. The transmittance of the glass should be larger than 40.0% under 3D mode operation. The luminance of the test pattern "WW", denoted L(WW); the luminance of the test pattern "WB", denoted L(WB) ; the luminance of the test pattern "BW", denoted L(BW); the luminance of the test pattern "BB", denoted "L(BB)

c. Definition of the Center Luminance of White, Lc (3D) : L(WW)

d. Definition of the 3D mode white crosstalk, CT (3D-W) : $CT(3D-W) \equiv \left| \frac{L(WB)-L(BB)}{L(WW)-L(BB)} \right|$

e. Definition of the 3D mode dark crosstalk, CT (3D-D) : $CT(3D-D) \equiv \left| \frac{L(WW)-L(BW)}{L(WW)-L(BB)} \right|$

8. PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

[1] Do not apply rough force such as bending or twisting to the module during assembly.

[2] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.

[3] Bezel of Set can not press or touch the panel surface. It will make light leakage or scrape.

[4] It should be attached to the system firmly using all mounting holes.

[5] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer, do not press or scratch the surface harder than a HB pencil lead.

[6] Use finger-stalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.

[7] Protection film for polarizer on the module should be slowly peeled off just before use so that the electrostatic charge can be minimized.

[8] Do not disassemble the module.

[9] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

[10] Do not plug in or pull out the I/F connector while the module is in operation, pins of I/F connector should not be touched directly with bare hands. Do not adjust the variable resistor located on the module.

[11] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched. Water, IPA (Isoproyl Alcohol) or Hexane are desirable cleaners. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.

[12] Moisture can easily penetrate into LCD module and may cause the damage during operation.

[13] When storing modules as spares for a long time, the following precaution is necessary.

[13.1] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃ at normal humidity (under 70%) without condensation.

[13.2] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

[14] When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of LED will be higher than that of room temperature.

8.2 SAFETY PRECAUTIONS

To optimize PID module's lifetime and functions, operating conditions should be followed as below

[1] Normal operating condition

[1.1] Temperature : 20±15℃

[1.2] Humidity : 55±20%

[1.3] Well-ventilated place is suggested to set up PID module and system.

[1.4] Display pattern : regular switched patterns or moving pictures.

[1.4.1] Periodical power-off or screen saver is needed after long-term static display.

[1.4.2] Moving picture or black pattern is strongly recommended for screen saver.

[2] Operating requirements of PID modules and systems to prevent uneven display under long-term operating.

[2.1] PID suitable operating time : under 20 hrs a day.

[2.2] Periodical display contents should be changed from static image to moving picture.

[2.2.1] Different background and image colors changed respectively, and changed colors periodically.

[2.2.2] Background and image with large different luminance displayed at the same time should be avoided.

[3] The startup voltage of a Backlight may cause an electrical shock while assembling with the converter. Do not disassemble the module or insert anything into the Backlight unit.

[4] Do not connect or disconnect the module in the "Power On" condition.

[5] Do not exceed the absolute maximum rating value. (supply voltage variation, input voltage variation, variation in part contents and environmental temperature…) Otherwise the module may be damaged.

[6] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

[7] Module should be turned clockwise (regular front view perspective) when used in portrait mode.

[8] Ultra-violet ray filter is necessary for outdoor operation.

[9] Only when PID module is operated under right operating conditions, lifetime in this spec can be guaranteed. After the module's end of life, it is not harmful in case of normal operation and storage.

8.3 SAFETY STANDARDS

The LCD module should be certified with safety regulations as follows:

Regulatory	Item	Standard
Information Technology equipment	UL	UL60950-1:2006 or Ed.2:2007
	cUL	CAN/CSA C22.2 No.60950-1-03 or 60950-1-07
	CB	IEC60950-1:2005 / EN60950-1:2006+ A11:2009
Audio/Video Apparatus	UL	UL60065 Ed.7:2007
	cUL	CAN/CSA C22.2 No.60065-03:2006 + A1:2006
	CB	IEC60065:2001+ A1:2005 / EN60065:2002 + A1:2006+ A11:2008

9. DEFINITION OF LABELS

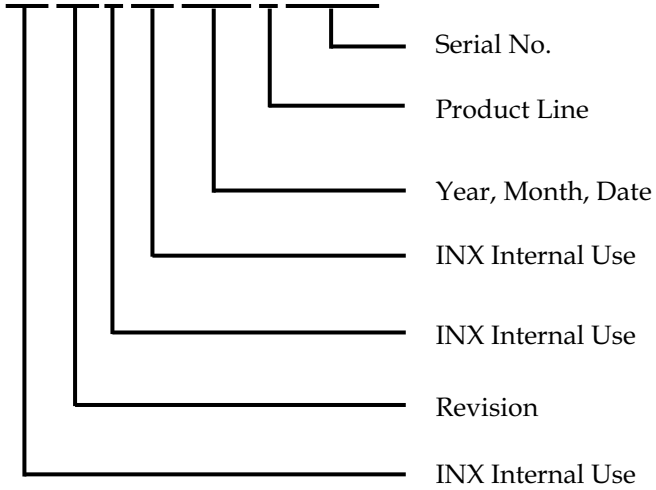
9.1 MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.

Model Name : V85DK1-KD1

Revision : Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

Serial ID : X X X X X X Y M D L N N N N



Serial ID includes the information as below:

Manufactured Date:

Year : 2001=1, 2002=2, 2003=3, 2004=4…2010=0, 2011=1, 2012=2…

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code : Cover all the change

Serial No. : Manufacturing sequence of product

Product Line : 1 → Line1, 2 → Line 2, …etc.

9.2 CARTON LABEL

The barcode nameplate is pasted on each box as illustration, and its definitions are as following explanation.

P.O. NO._____

Parts ID._____

Model Name V850DK1-KD1

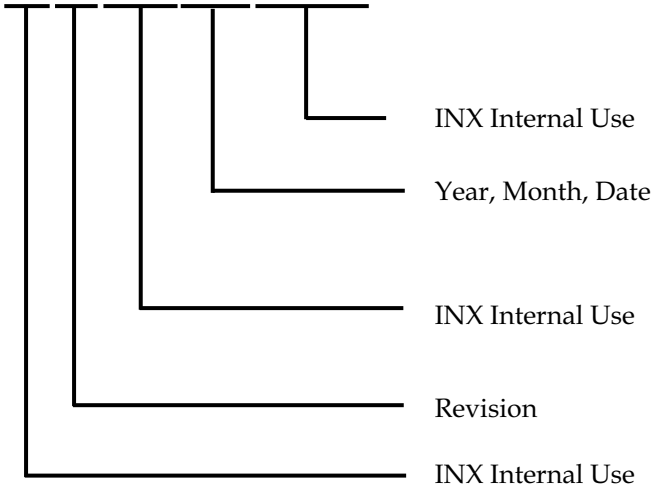
Carton ID._____ Quantities ___

XXXXXXXXXXXXX

Made In Taiwan (Made In China)

Model Name: V850DK1– KD1

Carton ID: X X X X X X X Y M D X X X X



Serial ID includes the information as below :

Manufactured Date:

Year: 2010=0, 2011=1, 2012=2…etc.

Month: 1~9, A~C, for Jan. ~ Dec.

Day: 1~9, A~Y, for 1st to 31st, exclude I ,O, and U.

Revision Code: Cover all the change

10. PACKAGING

10.1 PACKAGING SPECIFICATIONS

(1) 6 LCD TV modules / 1 Box

(2) Box dimensions : 2247(L) X 723 (W) X 1290 (H)

(3) Weight: approximately 350 Kg (6 modules per box)

10.2 PACKAGING METHOD

Packaging method is shown in following figures.

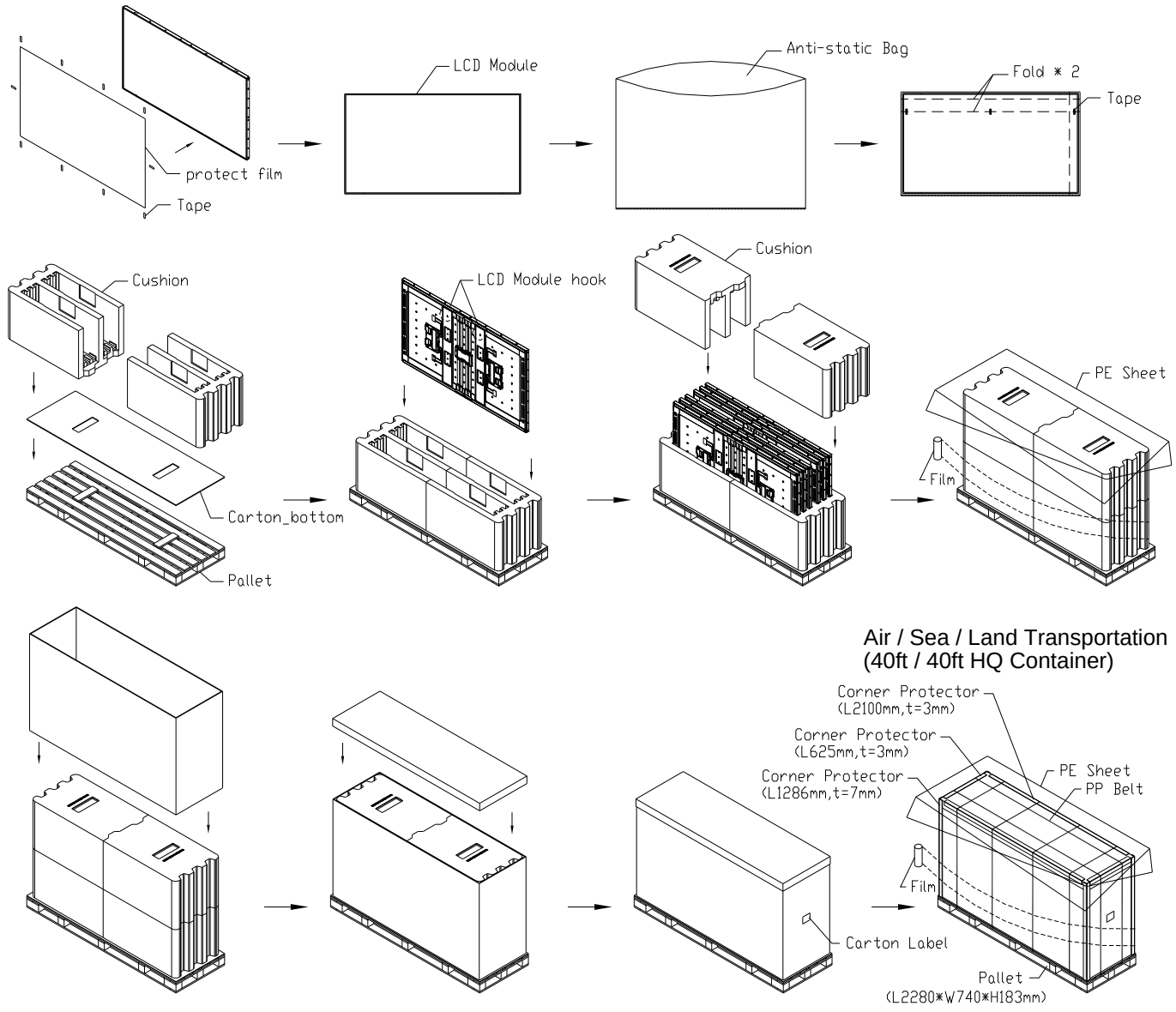


Figure 10-1 packing method

10.3 UN-PACKAGING METHOD

Un-packaging method is shown as following figures.

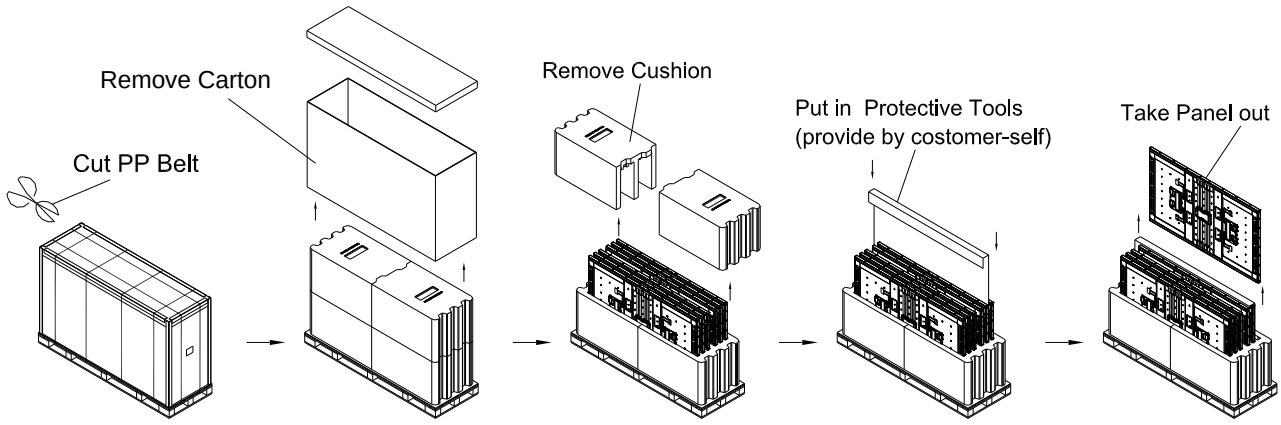
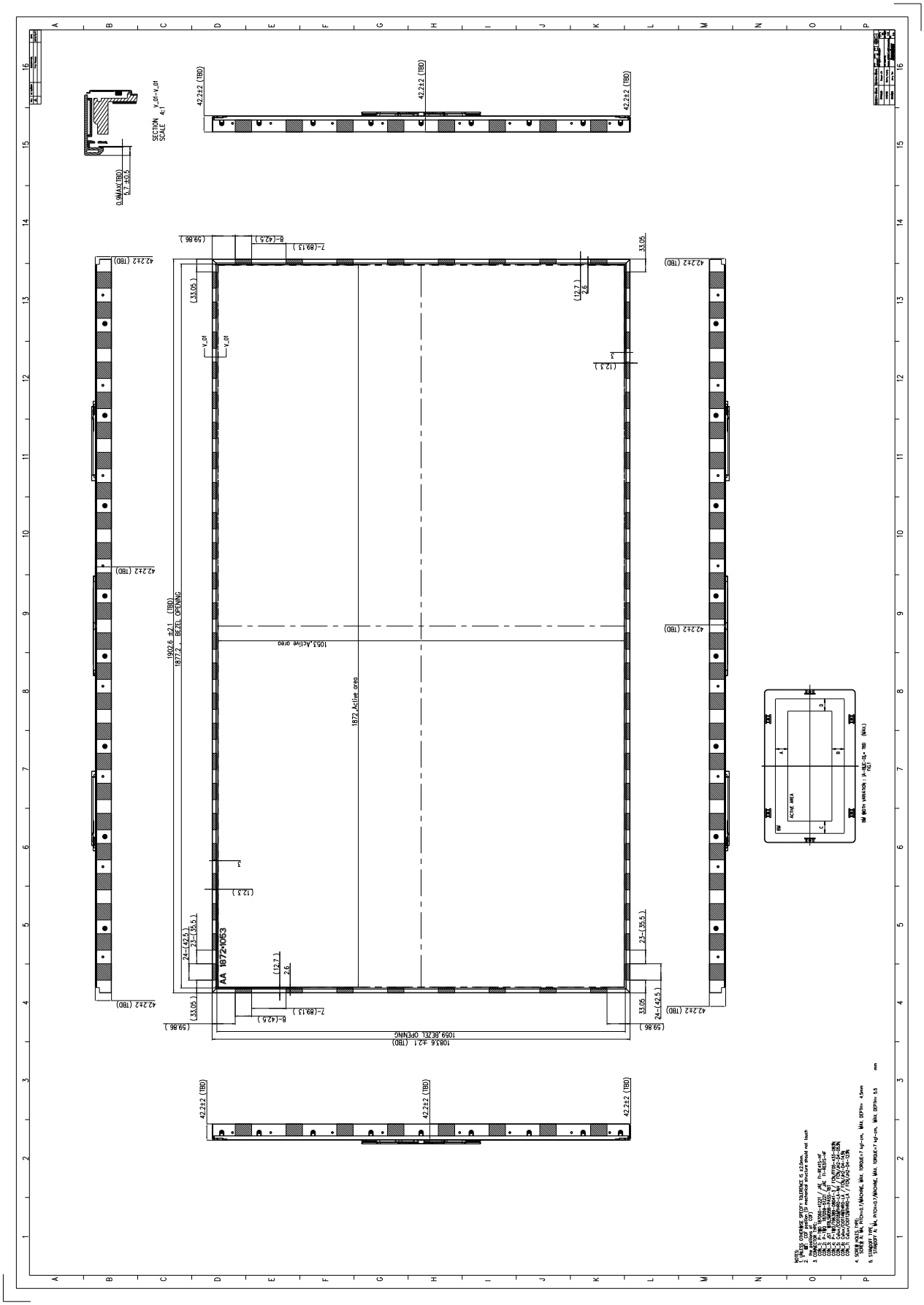
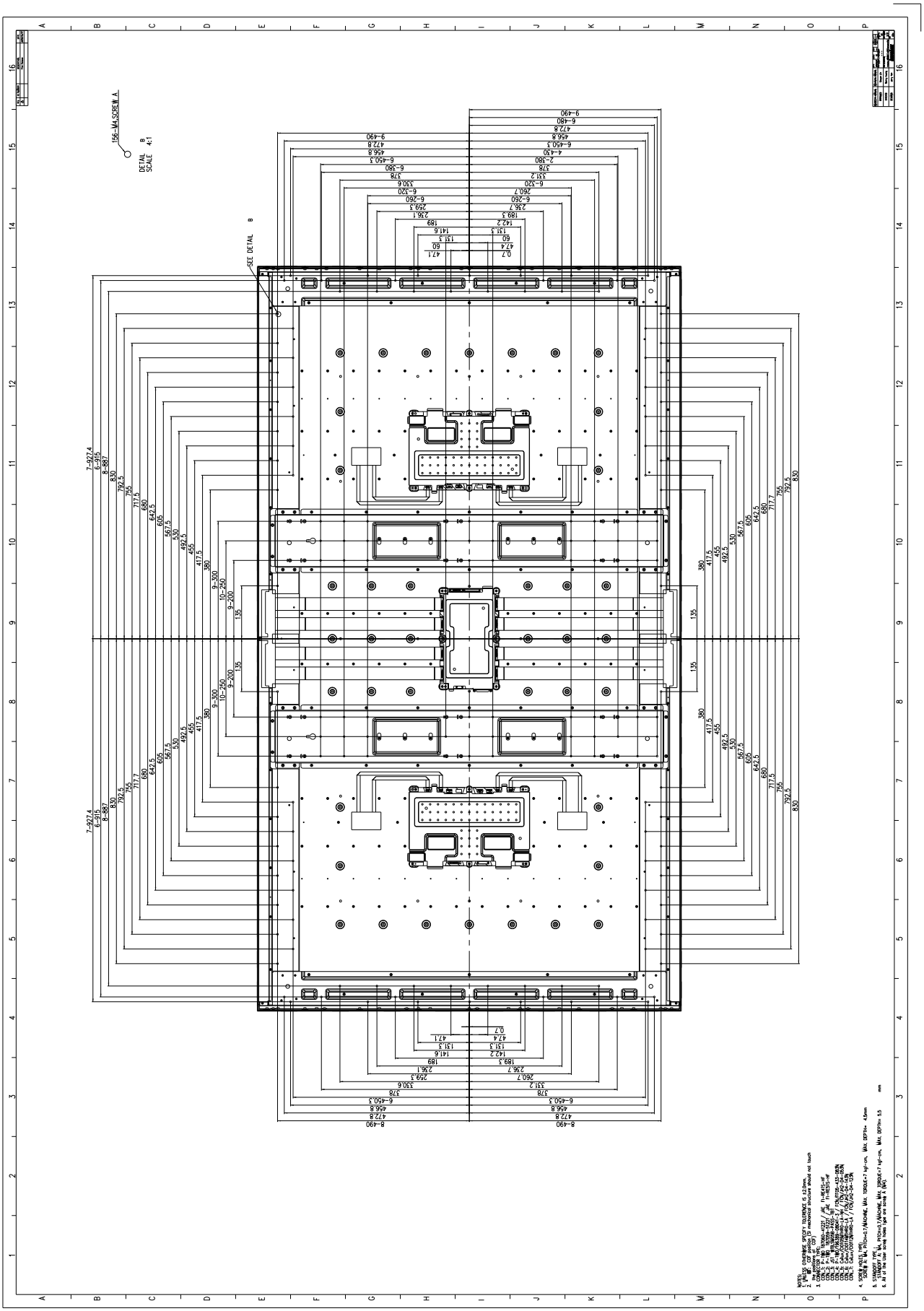
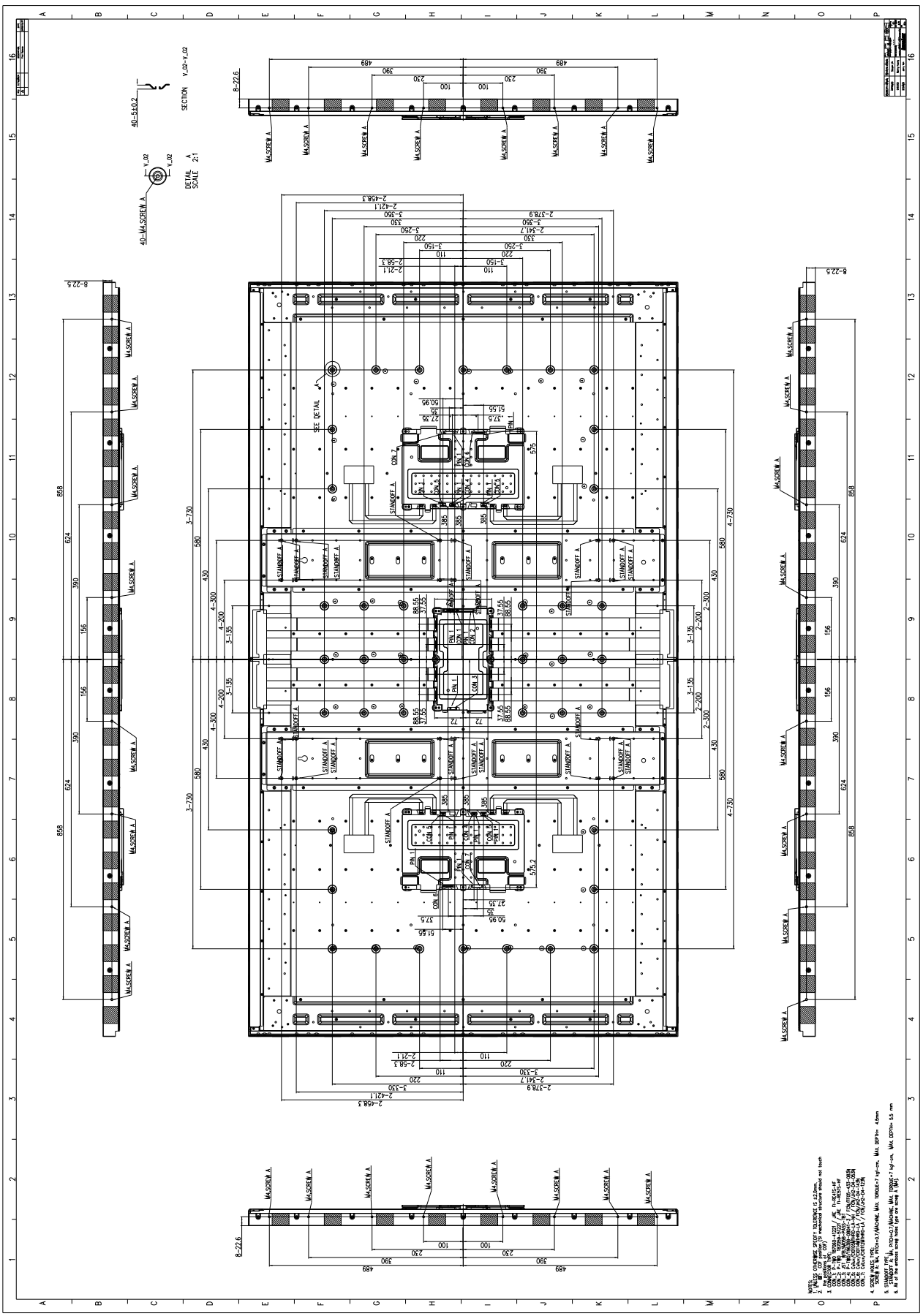


Figure 10-2 un-packing method

11. MECHANICAL CHARACTERISTIC







Appendix A

A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
t_{SU-STA}	Start setup time	250	-	ns
t_{HD-STA}	Start hold time	250	-	ns
t_{SU-DAT}	Data setup time	80	-	ns
t_{HD-DAT}	Data hold time	0	-	ns
t_{SU-STO}	Stop setup time	250	-	ns
t_{BUF}	Time between Stop condition and next Start condition	500	-	ns