

### 3W Filter-less Mono Class D Audio Amplifier

### **General Description**

The VA2101CSG9 is a cost-effective filter-less Class D mono audio power amplifier that operates in wide range of various power supplies. Only three external components space saving offers best performance and minimal occupied area for mobile application such as Pad/Netbook/GPS applications.

VA2101CSG9 is capable of 3.06W high performance output power at  $3\Omega$  load in 5V supply. Other features like 90% efficiency, -70dB PSRR, fully differential design reduces RF interference and allows independent gain settings while summing signals from various audio sources.

VA2101CSG9 also integrates 32ms Anti-Pop, Short Circuit Protection & Over-Heat Protection circuitry to ensure device reliability. These functionalities make it ideal for any portable device which demands more battery life.

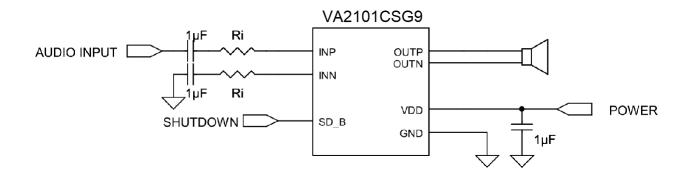
VA2101CSG9 is available with WLCSP-9 RoHS 2.0 and compliant Green or Lead/Halogen-free pack- Applications age.

### **Features**

- Operation Voltage from 2.8V to 5.5V
- Efficiency with an 8Ω speaker: up to 94% @1.6W
- Efficiency with an 3Ω speaker: 80%@3W
- $1.3W@8\Omega$  Load with THD+N < 1%
- $2.1W@4\Omega$  Load with THD+N < 1%
- $3.06W@3\Omega$  Load with THD+N < 10%
- Shutdown current less than 1uA
- Quiescent current less than 6mA
- PSRR, -70dB, No Need For Voltage Regu-
- 32ms delay to eliminate input noise
- Short Circuit and Thermal protection
- RoHS 2.0 compliant WLCSP-9 and Green or Lead/Halogen-free package available

- Portable Multimedia Device
- Pad Device/Netbook/GPS
- IP CAM
- Set-Top Box

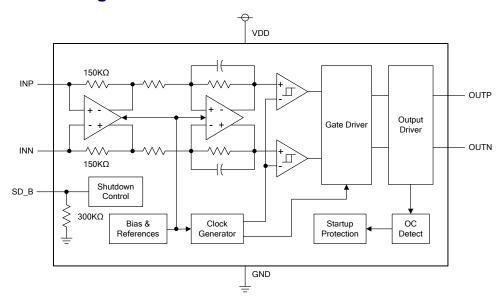
## Typical Application



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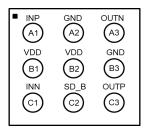


## **Functional Block Diagram**



## **Pin Assignments And Descriptions**

WLCSP-9 Top View



Pin No.	Pin	L / O / D	Function Description
WLCSP	Name	I/O/P	Tunction Description
C2	SD_B	I	Shutdown mode control terminal. Low active.
A1	INP	I	Positive audio signal input.
C1	INN	ı	Negative audio signal input.
C3	OUTP	0	Positive BTL Output.
B1, B2	VDD	Р	Power Supply.
A2 , B3	GND	Р	Power Ground.
A3	OUTN	0	Negative BTL Output.



## **Absolutely Maximum Ratings**

Over operating free-air temperature range, unless otherwise specified (\* 1)

Symbol	Parameter	Limit	Unit
V <sub>DD</sub> (VDD, PVDD)	Supply voltage	-0.3 to 6	V
V <sub>I</sub> (RINN, RINP, LINN, LINP, SD_B)	Input voltage	0 to V <sub>DD</sub>	V
T <sub>A</sub>	Operating free-air temperature range	-40 ~ +85	۰C
T <sub>J</sub>	Operating junction temperature range(* 2)	-40 to +150	۰C
T <sub>STG</sub>	Storage temperature range	-65 to 150	۰C
R <sub>(LOAD)</sub>	Minimum load resistance	3	Ω
Electrostatic discharge	Human body model	±2	kV
Electrostatic discharge	Machine model	±200	V

<sup>(\*1):</sup> Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

## **Recommended Operating Conditions**

Over operating free-air temperature range, unless otherwise specified.

Symbol	Parameter	Test Condition	Specif	Unit	
Syllibol	raiailietei	rest Condition	Min	Max	
$V_{DD}$	Supply Voltage	-	2.8	5.5	V
V <sub>IH</sub>	High Level Input Voltage (SD_B)	V <sub>DD</sub> =5V	2.0	$V_{DD}$	٧
V <sub>IL</sub>	Low Level Input Voltage (SD_B)	V <sub>DD</sub> =5V	-	0.4	٧
Rı	External Input Resistor	GAIN≤20V/V	15	-	kΩ
fosc	PWM Carrier Frequency	$V_{DD} = 5V$	220	300	kHz
V <sub>IC</sub>	Common Mode Input Voltage Range	VDD=2.8V~5.5V, CMRR≤-49dB	0.5	V <sub>DD</sub> -0.8	٧



### **Electrical Characteristics**

 $T_A = 25$ °C,  $V_{DD} = 5$ V,  $R_L = 8\Omega$ , GAIN=10dB, unless otherwise noted.

Symbol	Parameter	Test Condition		Specification			Unit
Syllibol	Jymbol l'alametel		rest Condition		Тур.	Max	Oilit
V <sub>os</sub>	Output Offset Voltage (Measured Differentially)	V <sub>I</sub> =0V, A <sub>V</sub> =20	$V_I$ =0V, $A_V$ =20dB, $R_L$ =8 $\Omega$		1	25	mV
I <sub>IH</sub>	High-Level Input Current	$V_{DD} = 5.5V, V_{I} = 5.8V$				100	μΑ
1112	Low-Level Input Current	$V_{DD} = 5.5 V, V_{I} = -0.3 V$				5	μΑ
PSRR	DC Supply Rejection Ratio		V <sub>DD</sub> =4.5V to 5.5V, Gain=20dB		75	55	dB
CMRR	Common Mode Rejection Ratio $V_{DD} = 2.8 \text{ to } 5.5 \text{V}, V_{IC} = 0.5 \text{V}$ to $V_{DD} - 0.8 \text{V}$			68	49	dB	
		V <sub>DD</sub> =5.5V,no load V <sub>DD</sub> =3.6V			5	6.2	mA
I <sub>DD</sub>	Quiescent Current				4	5	mA
		V <sub>DD</sub> =3.0V			3.5	4	mA
I <sub>DD(SHUTDOWN)</sub>	Supply Current In Shutdown Mode	SD_B=0.4V, V <sub>DD</sub>	n=2.8V~5.5V		0.5	2	μΑ
R <sub>DS(ON)</sub>	Drain-Source ON resistance <sup>1</sup>	V <sub>DD</sub> =5V,	High Side		450	600	mΩ
		I <sub>OUT</sub> =500mA Low Side	Low Side		450	600	
Α	Amplifier Gain	$V_{DD}=2.8$	to 5.5V	285k <u>R</u> 1	300k R <sub>I</sub>	325k R <sub>I</sub>	<u>&gt; </u> >
R <sub>SD-GND</sub>	Resistance from SD_B to GND	to GND			300		kΩ

<sup>(1)</sup> Design center value.



## **Operating Characteristics**

 $T_A=25^{\circ}\!C$  unless otherwise noted.

Symbol Parameter		Test Condition		Specification			linit
				Min	Тур.	Max	Unit
		TUD N 100/ 5 1111	$V_{DD} = 5V$		3.06		
		THD+N=10%, f=1kHz,	$V_{DD} = 3.6V$		1.58		W
		$R_L=3\Omega$	$V_{DD}=2.8V$		0.88		
		THD+N=1%, f=1kHz,	$V_{DD} = 5V$		2.4		
		$R_L=3\Omega$	$V_{DD} = 3.6V$		1.26		[
		N322	$V_{DD}=2.8V$		0.7		
		THD   N = 100/ f = 11/H=	$V_{DD} = 5V$		2.69		
		THD+N=10%, f=1kHz, $R_L=4\Omega$	$V_{DD} = 3.6V$		1.37		W
Po	Output Power	N422	$V_{DD}=2.8V$		0.78		
<b>P</b> 0	Output Power	THD:N 10/ f 11/H=	$V_{DD} = 5V$		2.1		
		THD+N=1%, f =1kHz, $R_L$ =4 $\Omega$	$V_{DD} = 3.6V$		1.09		
			$V_{DD}=2.8V$		0.62		
		THD+N=10%, f=1kHz, $R_L=8\Omega$	$V_{DD} = 5V$		1.68		
			$V_{DD} = 3.6V$		0.84		W
			$V_{DD}=2.8V$		0.49		
		THD+N=1%, f=1kHz, $R_1=8\Omega$	$V_{DD} = 5V$		1.34		w
			$V_{DD} = 3.6V$		0.67		
		$V_{DD} = 2.8V$			0.38		
THD+N	Total Harmonic Dis-	$V_{DD}=5V$ , $P_0=1W$ , $R_L=8\Omega$ , $f=1kHz$			0.1		%
IND+N	tortion Plus Noise	$V_{DD}=3.6V, P_{O}=0.5W, R_{L}=8\Omega, f=1 \text{ kHz}$			0.16		70
K <sub>SVR</sub>	Supply Ripple Rejec- tion Ration	$V_{DD}$ =3.6V, Input AC-Grounded, $C_i$ =1 $\mu$ F, f=215Hz, $V_{(RIPPLE)}$ =0.2 $V_{PP}$			67		dB
SNR	Signal-to-Noise Ra- tio	$V_{DD}=5V$ , $P_0=1W$ , $R_L=8\Omega$			90		dB
V <sub>n</sub>	Output Voltage Noise	V <sub>DD</sub> =5V, f=20Hz to	No Weight		110		μV <sub>RMS</sub>
Vn		Grounded, $C_i=1\mu F$	A Weighted		72		
CMRR	Common Mode Re- jection Ratio	$V_{DD}$ =3.6V, $V_{IC}$ =1 $V_{PP}$	f=217Hz		64		dB
Zı	Input Impedance	,		141	150	159	kΩ
	Start-up time from shutdown	V <sub>DD</sub> =3.6V			32		ms



### **Functional Descriptions**

The basic structure of VA2101CSG9 is a differential amplifier with differential inputs and BTL outputs. The VA2101CSG9 contains one differential amplifier and one common-mode amplifier. The value of differential amplifier output voltage is equal to the value of the differential input voltage multiplied with the set gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around  $V_{\rm DD}/2$  regardless of the common-mode voltage at the input. The VA2101CSG9 can still be used with a single ended input. For some applications such as radio frequency consumer devices, it is recommended to design VA2101CSG9 in differential input configuration to ensure better noise rejection.

### **Input Resistors**

The gain of VA2101CSG9 is set by external resistors  $R_{\rm I}$  shown in Figure 1. Set the gain of the amplifier according to the following equation:

$$Gain = \frac{2 \times 150 k\Omega}{R_{I}} \left(\frac{V}{V}\right) \tag{1}$$

The gain should be set to 2 V/V or lower for best performance. In some cases, lower gain makes the input less susceptible to noise which could be coupled from other circuits or system ground.

Resistor matching is very important criteria in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the input resistors. It is recommended to use 1% tolerance resistor or better for best performance.

The  $R_{\rm I}$  resistors should be placed close to the VA2101CSG9 and keep the input traces close to each other with the same length. Such idea can improve noise rejection because of the high CMRR.

### **Input Capacitors**

The input capacitors may be needed for some applications or when the source is single-ended (See Figure 2). These capacitors will not only block the DC voltage at the amplifier input terminal but also create a high-pass filter together with the input resistors R<sub>I</sub>. The cut-off frequency of the high-pass filter is calculated according to the following equation:

$$f_{C} = \frac{1}{2\pi \times R_{I} \times C_{I}} \quad Hz \tag{2}$$

The value of the input capacitor affects the low frequency performance of the circuit directly. For example, the frequency response of the speaker in mobile phone is usually bad in lower frequency band, so the cut-off frequency should be set to block lower frequency of audio band to avoid the distortion. For another example, the dominant noise frequency in power rail of a GSM mobile phone is at 217Hz. Setting cut-off frequency of high-pass filter above 217Hz can filter out this noise that it is not amplified and heard on the output. Capacitor has 10% tolerance or better is recommended for impedance matching.

### **Differential Circuit Configurations**

The VA2101CSG9 can be used in many circuit input configurations. The simplest and best input configuration is the direct-coupled differential input show in Figure 1. The resistors  $R_{\rm I}$  set the gain of audio amplifier. Refer Equation (1) to calculate. If necessary, the input capacitors can be also used

in the differential input configuration shown in Figure 2. The reason to do so is usually to create the high-pass filter in audio signal input. In case of applying the high-pass filter, equation (1) listed above shall be used to find out the value of the R<sub>1</sub> for a proper gain and then using equation (2) to

# **VA2101CSG9**



obtain the value of  $C_1$  to determine the cut-off frequency.

It is easily to handle multiple audio signal sources with the VA2101CSG9. Figure 3 shows a dual differential input configuration. The gain for each input source can be set independently according to Equation (3) and (4).

Gain 1 = 
$$\frac{2 \times 150 \text{k}\Omega}{R_{\text{TI}}}$$
  $\left(\frac{\text{V}}{\text{V}}\right)$  (3)

Gain 2 = 
$$\frac{2 \times 150 \text{k}\Omega}{R_{12}}$$
  $\left(\frac{V}{V}\right)$  (4)

The input capacitors can be used with one or more input source as well to have different frequency responses depending on the source or if a DC voltage needs to be blocked from the source.

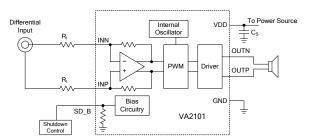


Figure 1. Differential Input Configuration

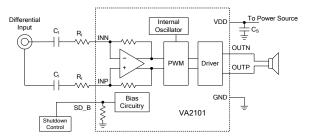


Figure 2. Differential Input Configuration with Input Capacitors

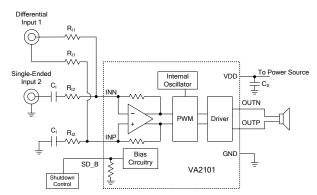


Figure 3. Dual Differential Input Configuration

### Single-Ended Circuit Configurations

The VA2101CSG9 can also be used with single-ended signal sources, but input capacitors shall be added to block DC voltage at the input terminals. The typical single-ended configuration is shown in Figure 4. Use equation (1) to calculate the gain and set the frequency response by equation (2). Hold for the single-ended configuration as shown in Figure 4.

When using more than one single-ended source as shown in Figure 5. The gain and cut-off frequency ( $f_{C1}$  and  $f_{C2}$ ) for each input source can be set independently, shows in Equation (5) ~ Equation (8). Resistor,  $R_{I3}$ , and capacitor,  $C_{I3}$ , are needed on the INP terminal to match the impedance on the INN terminal. Equation (9) and Equation (10) shows how to calculate  $C_{I3}$  and  $R_{I3}$  value. The single-ended inputs must be driven by low impedance source even if one of the inputs is not outputting an AC signal.

Gain 1 = 
$$\frac{2 \times 150 k\Omega}{R_{II}}$$
  $\left(\frac{V}{V}\right)$  (5)

Gain 2 = 
$$\frac{2 \times 150 \text{k}\Omega}{R_{12}}$$
  $\left(\frac{\text{V}}{\text{V}}\right)$  (6)

$$f_{C1} = \frac{1}{2\pi \times R_{II} \times C_{II}} \quad Hz \tag{7}$$





$$f_{C2} = \frac{1}{2\pi \times R_{12} \times C_{12}} \quad Hz \tag{8}$$

$$C_{13} = C_{11} + C_{12} (9)$$

$$R_{I3} = \frac{1}{\left(\frac{1}{R_{I1}} + \frac{1}{R_{I2}}\right)} = \frac{R_{I1} \times R_{I2}}{R_{I1} + R_{I2}}$$
(10)

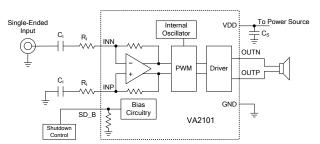


Figure 4. Single-Ended Input Configuration

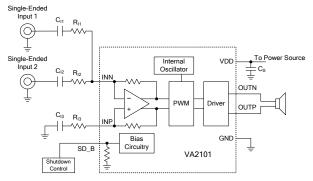


Figure 5. Dual Single-Ended Input Configuration

### **Mixed Input Configurations**

A typical application with one single-ended source and one differential source shows in Figure 6. Ground noise can couple in through INP terminal with this method. It is better to use dual differential inputs. The cut-off frequency of the single-ended input is set by C<sub>I</sub> shows in Equation (13). To assure that each input is balanced, the single-ended input must be driven by a low-impedance source even if the input is not in use.

$$Gain 1 = \frac{2 \times 150 k\Omega}{R_{II}} \left(\frac{V}{V}\right)$$
 (11)

Gain 2 = 
$$\frac{2 \times 150 \text{k}\Omega}{\text{R}_{12}} \left(\frac{\text{V}}{\text{V}}\right)$$
 (12)

$$f_{C2} = \frac{1}{2\pi \times R_{12} \times C_{I}} \quad Hz \tag{13}$$

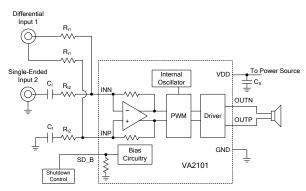


Figure 6. Dual Input with a Single-Ended Input and a Differential Input Configuration

### **Power Efficiency**

The output transistors of VA2101CSG9 act as switches. The amount of power dissipated in the speaker may be estimated by first considering the overall efficiency of the system. The on-resistance of the output transistors is considered to cause the dominant loss in the system, the on-resistance of output transistors is small that the power loss is small and the power efficiency is high. When VA2101CSG9 connects with  $8\Omega$  loads, the power efficiency could be better than 88%.

### Over-Heat Protection

The Over-Heat protection feature on the VA2101 CSG9 prevents damage to the device when the internal die temperature exceeds 150°C. Once the die temperature exceeds the thermal set point, the device enters the shutdown state and the outputs are disabled. The device will be back to normal operation automatically when die temperature is reduced.

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### **Output Short Protection**

The VA2101CSG9 has output short circuit protection circuitry on the outputs that prevents the misconnections such as output to output short, output to GND short and output to VDD short. VA2101CSG9 enters the shutdown state and the outputs are disabled when detects output short. This is a latched fault and must be reset by cycling the voltage on the SD\_B pin to a logic low and back to the logic high, or cycling the power off and then back on. This clears the short–circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry activates again.

### **Low ESR Capacitors**

Low ESR capacitors are highly recommended for this application. In general, a practical capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal capacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

### **Decoupling Capacitors**

VA2101CSG9 requires appropriate power decoupling to minimize the output total harmonic distortion (THD) and improve EMC performance. Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling can be achieved by using two different types of capacitors which target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, three good low ESR ceramic capacitors, for example 1µF, placed as close as possible to every VDD pins works best. For filtering lower frequency noise, a larger low ESR aluminum electrolytic capacitor of 100µF or greater placed

near the audio power amplifier is strongly suggested.

### **Shutdown Operation**

The VA2101CSG9 provides a shutdown mode for reducing supply current to the absolute minimum level during periods of nonuse for battery–power conservation. The VA2101CSG9 has an internal  $300k\Omega$  resistor connected between GND and SD\_B pins. The purpose of this resistor is to eliminate any unwanted state changes when shutdown pin is floating. The SD\_B input pin should be held high during normal operation when the amplifier is in use. Pulling SD\_B low or left floating causes the outputs to mute and the amplifier to enter a low–current state. During the shutdown mode, the DC quiescent current of the circuit does not exceed  $0.5\mu A$ .

### **Output Filters**

Design the VA2101CSG9 without the filter if the lengths of traces plus cables from amplifier to speaker are short enough (< 1 inch). This case is a typical application for applications based with the Class D amplifier without any filter. Some applications such as mobile phone and PDA are good examples for using Class D amplifier without any filter.

However, many applications still require the ferrite bead filter. The ferrite filter reduces EMI around 30 MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires from the amplifier to the speaker.

Figure 7 & 8 show typical L/C and ferrite bead output filters.



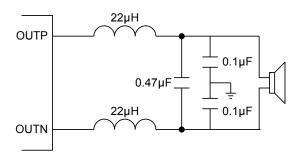


Figure 7. Typical L/C Output Filter

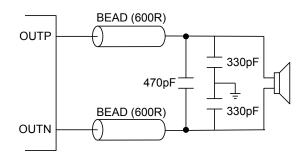


Figure 8. Typical Ferrite Chip Bead Output Filter

## **Typical Characteristics**

### Test Set-Up For Graphs

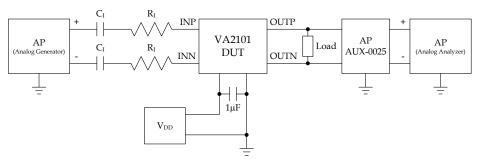


Figure 9. VA2101CSG9 Test Environment



## **Typical Characteristics (cont.)**

 $T_A = 25$ °C, unless otherwise noted.

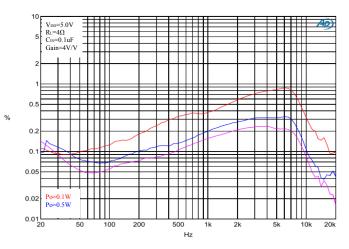


Figure 10. THD+N vs. Frequency

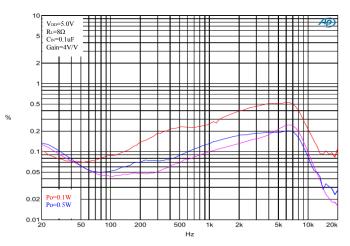


Figure 12. THD+N vs. Frequency

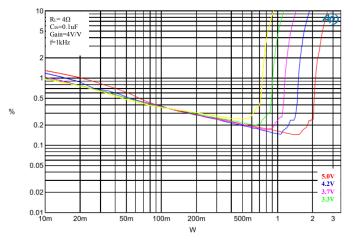


Figure 14. THD+N vs. Output Power

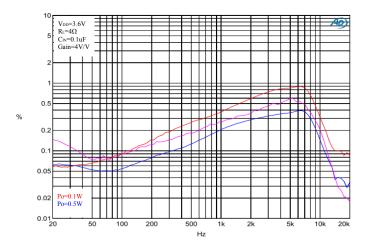


Figure 11. THD+N vs. Frequency

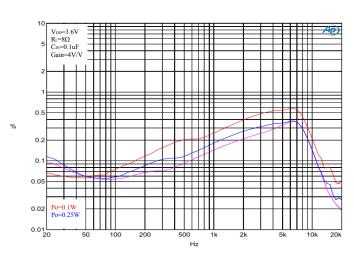


Figure 13. THD+N vs. Frequency

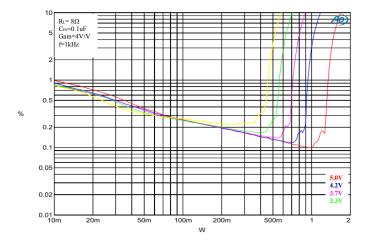


Figure 15. THD+N vs. Output Power



## **Typical Characteristics (cont.)**

 $T_A = 25$ °C, unless otherwise noted.

200u

140

100

60ı

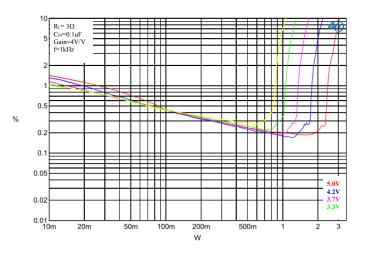


Figure 16. THD+N vs. Output Power

VDD=5V R<sub>L</sub> = 4Q C<sub>D</sub>=0.1uF

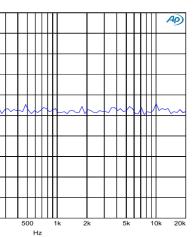


Figure 17. Frequency Response, 5V,  $4\Omega$ 

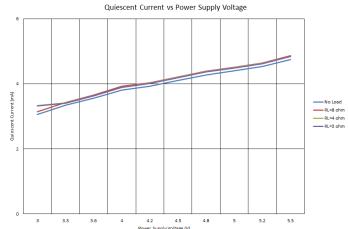


Figure 18. Noise Floor

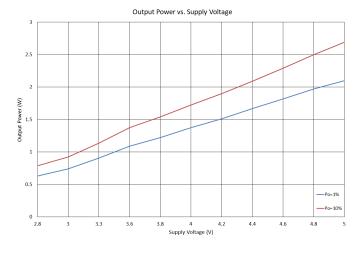


Figure 19. Supply Voltage vs. Quiescent Current

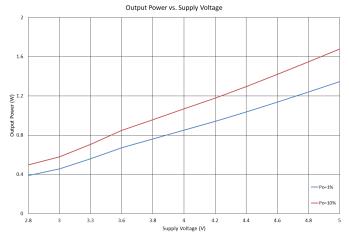


Figure 20. Supply Voltage vs. Output Power\_ $4\Omega$ 

Figure 21. Supply Voltage vs. Output Power\_ $8\Omega$ 



## **Application Information**

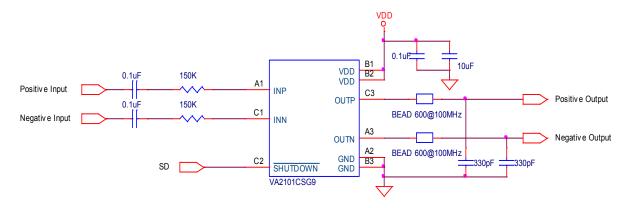


Figure 22. VA2101CSG9 with differential input configuration

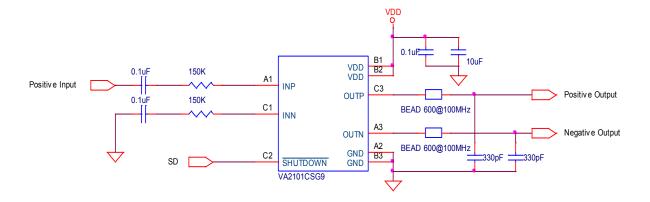
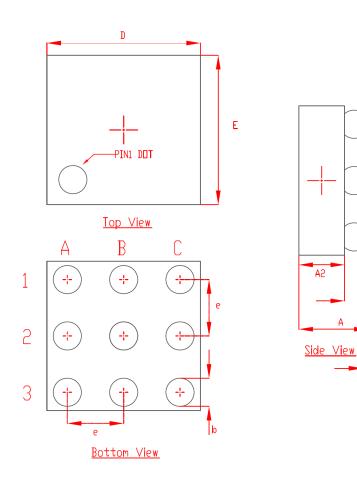


Figure 23. VA2101CSG9 with single-ended input configuration



## **Package Information**

### WLCSP-9 1.06 x1.09



Symbols	Min.	Тур.	Max.
Α	0.46	0.49	0.52
A1	0.15	0.17	0.19
A2	0.31	0.32	0.33
b	0.18	0.2	0.22
D	1.09	1.12	1.15
E	1.06	1.09	1.12
е	0.40 BSC		
QQQ	0.05		

#### Notes:

- Package Outline Unit Description:
  - BSC: Basic. Represents theoretical exact dimension or dimension target.

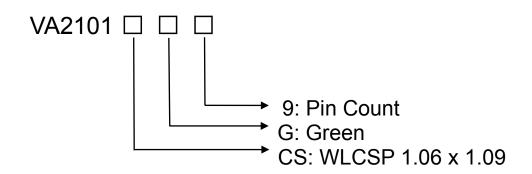
🛆 aaa C SEATING PLANE

- Min: Minimum dimension specified.
- Max: Maximum dimension specified.
- REF: Reference. Represents dimension for reference use only.
- This value is not a device specification.

  Typ: Typical. Provided as a general value. This value is not a device specification.
- 2. Dimensions in Millimeters.



### **Ordering Information**



Part No.	Q`ty/Reel		
VA2101CSG9	2,500		

### **Contact Information**

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