

## Filterless Class D Audio Amplifier

### General Description

The VA2239 is a cost-effective filter-less Class D stereo/PBTL mono audio power amplifier that operates in wide range of various power supplies. VA2239 provide gain control with simple voltage dividers. VA2239 can output 50W per channel into 4Ω load with lower supply current and fewer external components for driving bridged-tied stereo speaker directly. Five different PWM frequency adjustment makes VA2239 is suitable for any consumer electronics especially for high power output audio speakers. With the function of power limit, the speakers could be operated safely and the input signal would be also normalized.

VA2239 operates with high efficiency energy conversion up to 90% (8Ω Load) so that the external heat sink can be eliminated while playing music.

VA2239 also integrates Anti-Pop, Output Short & Over-Heat Protection Circuitry to ensure device reliability. This device also provides the DC detect and protection scheme to prevent the damage of speaker voice coils.

The VA2239 is available in TSSOP-28 green package with exposed pad-up.

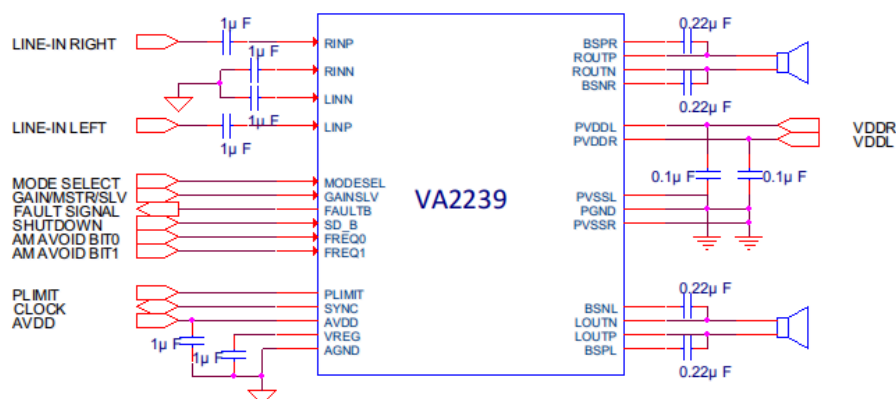
### Features

- Operation Voltage from 4.5V to 26V
- Maximum 90% Efficiency with an 8Ω Speaker
- 2x50W@4Ω, THD+N =10% at 21V
- 2x35W@4Ω, THD+N =1% at 18V
- 1x60W@3Ω, THD+N =1% at 18V (PBTL)
- 1x80W@3Ω, THD+N<1% at 24V (PBTL)
- Multiple Switching Frequencies for AM Avoidance
- Optional Clock Master/Slave Synchronization
- 4 Segments Configurable PWM Frequency: 400kHz/500kHz/600kHz/1MHz
- Voltage-Divider Selectable Gain Settings
- Excellent EMI/EMC Performance
- Scalable Power Limit Function
- Fault Indication Output Terminal
- Speaker DC Detection and Protection
- Parallel BTL Speaker Driving Connection
- Thermal Protection with Auto-Recovery
- Speaker Protection Circuitry
- Short Circuit and Thermal Protection
- RoHS 2.0 compliant TSSOP-28 Green Package with Exposed Pad-Up

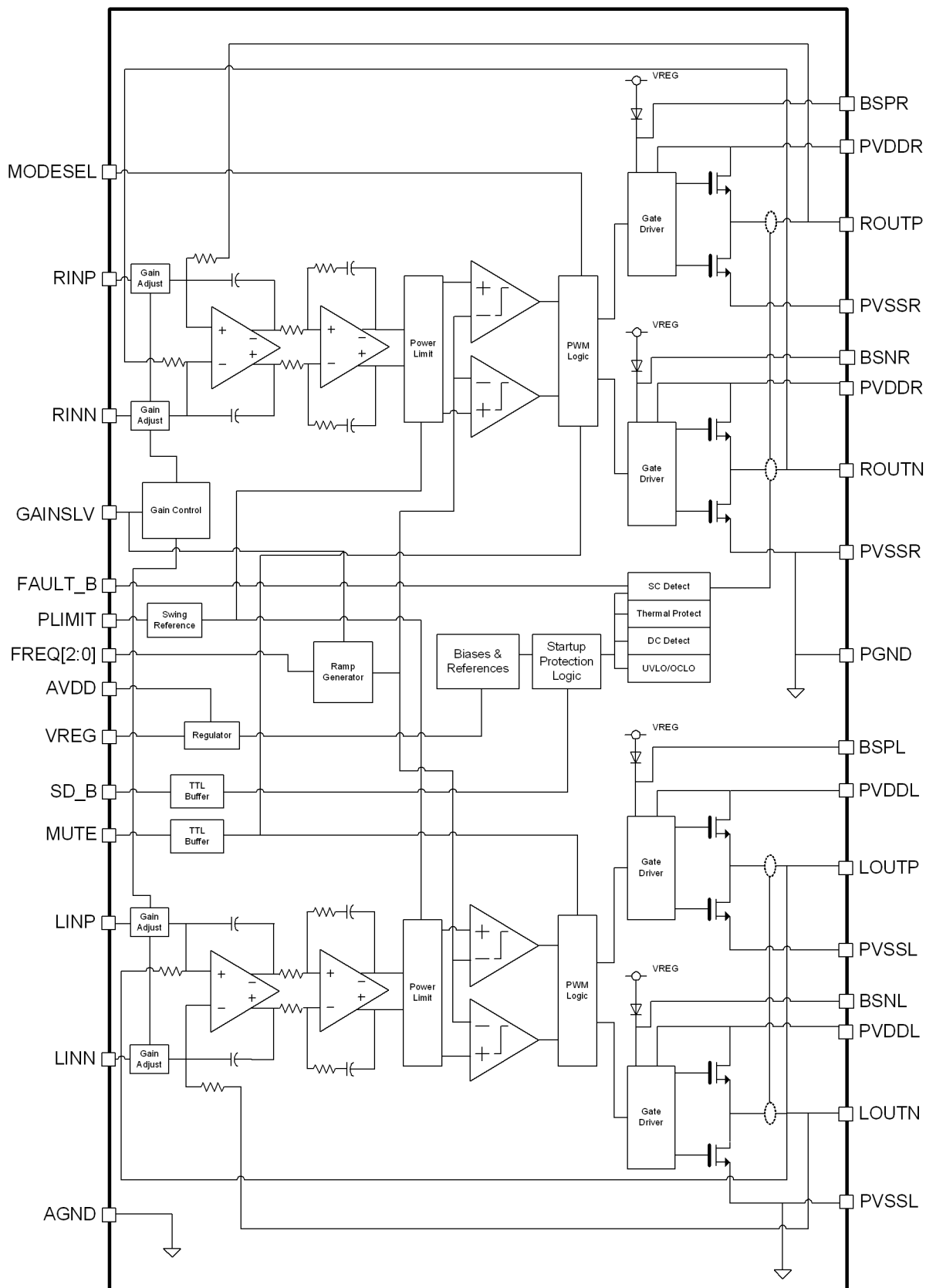
### Applications

- Multimedia Speaker
- Aftermarket Automotive
- Sound Bar and Boombox

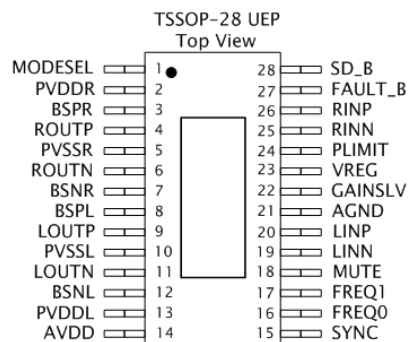
### Typical Application



## Functional Block Diagram



## Pin Assignments And Descriptions



| Pin No. | Pin            | I/O/P | Function Description                                                                                                                                 |
|---------|----------------|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1       | MODESEL        | I     | Mode selection. Low for BD mode, HIGH for 1SPW mode. TTL Logic levels with compliance to AVDD.                                                       |
| 2       | PVDDR          | P     | Power Stage Power Supply.                                                                                                                            |
| 3       | BSPR           | I     | Bootstrap I/O for right channel positive high-side switch.                                                                                           |
| 4       | ROUTP          | O     | Right channel positive output.                                                                                                                       |
| 5       | PVSSR          | P     | Power Stage Ground.                                                                                                                                  |
| 6       | ROUTN          | O     | Right channel negative output.                                                                                                                       |
| 7       | BSNR           | I     | Bootstrap I/O for right channel negative high-side switch.                                                                                           |
| 8       | BSPL           | I     | Bootstrap I/O for left channel positive high-side switch.                                                                                            |
| 9       | LOUTP          | O     | Left channel positive output.                                                                                                                        |
| 10      | PVSSL          | P     | Power Stage Ground.                                                                                                                                  |
| 11      | LOUTN          | O     | Left channel negative output.                                                                                                                        |
| 12      | BSNL           | I     | Bootstrap I/O for left channel negative high-side switch.                                                                                            |
| 13      | PVDDL          | P     | Power Stage Power Supply.                                                                                                                            |
| 14      | AVDD           | I     | Analog Power Supply.                                                                                                                                 |
| 15      | SYNC           | I/O   | Clock Synchronization. Clock input/output for synchronizing multiple class-D devices.                                                                |
| 16      | FREQ0          | I     | Frequency selection Bit 0. TTL logic levels with compliance to AVDD.                                                                                 |
| 17      | FREQ1          | I     | Frequency selection Bit 1. TTL logic levels with compliance to AVDD.                                                                                 |
| 18      | MUTE           | I     | Mute signal for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVDD.               |
| 19      | LINN           | I     | Left channel negative audio signal input. Tie this pin low if need to bridge rear side of outputs.                                                   |
| 20      | LINP           | I     | Left channel positive audio signal input. Tie this pin low if need to bridge rear side of outputs.                                                   |
| 21      | AGND           | P     | Analog Ground.                                                                                                                                       |
| 22      | GAINSLV        | I     | Gain and Master/Slave selection. Use recommended voltage divider network to specify Master/Slave role and gain.                                      |
| 23      | VREG           | O     | Regulated Voltage. For generating high-side MOSFET gate driving bias.                                                                                |
| 24      | PLIMIT         | I     | Power Limit Level Adjust. Connect a resistor divider from VREG to AGND to set power limit. Connect to VREG directly for no power limit.              |
| 25      | RINN           | I     | Right channel negative audio signal input.                                                                                                           |
| 26      | RINP           | I     | Right channel positive audio signal input.                                                                                                           |
| 27      | FAULT_B        | OD    | Fault Indication. Low for fault status and high for normal operation. Open Drain TTL Logic levels with compliance to AVDD.                           |
| 28      | SD_B           | I/O   | Shutdown control terminal. Low active. TTL Logic levels with compliance to AVDD.                                                                     |
| UEP     | Up Thermal Pad | P     | Thermal Pad. Connect to AGND for best system performance. If not connected to AGND, leave floating. Do not short to any other signals or metal case. |

## Absolutely Maximum Ratings

Over operating free-air temperature range, unless otherwise specified (\* 1)

| Symbol                                           | Parameter                                 | Limit                                                                                                               | Unit     |
|--------------------------------------------------|-------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------|
| $V_{DD}(PVDDL, PVDDR, AVDD)$                     | Supply voltage                            | -0.3 to 30                                                                                                          | V        |
| $V_I(\text{FREQ0, FREQ1, MODESEL, MUTE, SD\_B})$ | Input voltage                             | -0.3 to $V_{DD}+0.3$                                                                                                | V        |
| $V_I(\text{PLIMIT, GAINSLV, SYNC})$              | Input voltage                             | -0.3 to $V_{REG}+0.3$                                                                                               | V        |
| $V_I(\text{LINN, RINN, LINP, RINP})$             | Analog Input voltage                      | -0.3 to 6.5                                                                                                         | V        |
| $T_A$                                            | Operating free-air temperature range      | -40 ~ +85                                                                                                           | °C       |
| $T_J$                                            | Operating junction temperature range(* 2) | -40 to +150                                                                                                         | °C       |
| $T_{STG}$                                        | Storage temperature range                 | -65 to 150                                                                                                          | °C       |
| $R_{(LOAD)}$                                     | Minimum load resistance                   | 4 (BTL Stereo)<br>4 (PBTL mode $\geq 12V$ )<br>(Heatsink Required)<br>2 (PBTL mode $< 12V$ )<br>(Heatsink Required) | $\Omega$ |
| Electrostatic discharge                          | Human body model                          | $\pm 2$                                                                                                             | kV       |
| Electrostatic discharge                          | Machine model                             | $\pm 200$                                                                                                           | V        |

(\*1): Stress beyond those listed at "absolute maximum rating" table may cause permanent damage to the device. These are stress rating ONLY. For functional operation are strongly recommend follow up "recommended operation conditions" table.

## Recommended Operating Conditions

Over operating free-air temperature range, unless otherwise specified.

| Symbol     | Parameter                                                             | Test Condition                                               | Specification |     | Unit    |
|------------|-----------------------------------------------------------------------|--------------------------------------------------------------|---------------|-----|---------|
|            |                                                                       |                                                              | Min           | Max |         |
| $V_{DD}$   | Supply voltage                                                        | PVDDL, PVDDR, AVDD                                           | 4.5           | 26  | V       |
| $V_{IH}$   | High level input voltage<br>(FREQ0, FREQ1, MODESEL, MUTE, SD_B, SYNC) | $V_{DD}=24V$                                                 | 2             |     | V       |
| $V_{IL}$   | Low level input voltage<br>(FREQ0, FREQ1, MODESEL, MUTE, SD_B, SYNC)  | $V_{DD}=24V$                                                 |               | 0.8 | V       |
| $V_{OL}$   | Low level output voltage (FAULT_B)                                    | $V_{DD}=24V, R_{PULL}=100k\Omega$                            |               | 0.8 | V       |
| $I_{IH}$   | High level input current                                              | $V_{DD}=18V, V_I=2V$ , for FREQ0, FREQ1, MODESEL, MUTE, SD_B |               | 50  | $\mu A$ |
| $L_{LOAD}$ | Minimum load inductance                                               |                                                              | 1             |     | $\mu H$ |
| $T_A$      | Operating free-air temperature                                        |                                                              | -40           | 85  | °C      |

## Electrical Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_{DD} = 12\text{V}$ ,  $R_L = 4\Omega$ ,  $\text{GAIN} = 20\text{dB}$ , unless otherwise noted.

| Symbol          | Parameter                                       | Test Condition                                               | Specification |      |      | Unit             |
|-----------------|-------------------------------------------------|--------------------------------------------------------------|---------------|------|------|------------------|
|                 |                                                 |                                                              | Min           | Typ. | Max  |                  |
| $ V_{OS} $      | Output offset voltage (measured differentially) | $V_I = 0\text{V}$                                            |               | 1.5  | 15   | mV               |
| $I_Q$           | Quiescent current                               | $SD\_B = 2\text{V}$ , No load                                |               | 25   | 40   | mA               |
| $I_{SD}$        | Shutdown current                                | $SD\_B = 0.8\text{V}$ , No load                              |               | 250  | 500  | $\mu\text{A}$    |
| $t_{ON}$        | Shutdown turn-on time                           | $SD\_B = 2\text{V}$                                          |               | 15   |      | ms               |
| $t_{OFF}$       | Shutdown turn-off time                          | $SD\_B = 0.8\text{V}$                                        |               | 2    |      | $\mu\text{s}$    |
| $f_{OSC}$       | Internal oscillation frequency                  | $FREQ0 = 0$ , $FREQ1 = 0$                                    |               | 400  |      | kHz              |
|                 |                                                 | $FREQ0 = 1$ , $FREQ1 = 0$                                    |               | 500  |      |                  |
|                 |                                                 | $FREQ0 = 0$ , $FREQ1 = 1$                                    |               | 600  |      |                  |
|                 |                                                 | $FREQ1 = 1$ , $FREQ0 = 1$                                    |               | 1000 |      |                  |
| $A$             | Amplifier gain                                  | $R_{DOWN} = 5.6\text{k}\Omega$ , $R_{UP} = \text{Open}$      |               | 20   |      | dB               |
|                 |                                                 | $R_{DOWN} = 27\text{k}\Omega$ , $R_{UP} = 100\text{k}\Omega$ |               | 26   |      |                  |
|                 |                                                 | $R_{DOWN} = 39\text{k}\Omega$ , $R_{UP} = 100\text{k}\Omega$ |               | 32   |      |                  |
|                 |                                                 | $R_{DOWN} = 47\text{k}\Omega$ , $R_{UP} = 75\text{k}\Omega$  |               | 36   |      |                  |
| $R_{DS(ON)}$    | Drain-Source ON resistance <sup>1</sup>         | $V_{DD} = 12\text{V}$ , $I_{OUT} = 500\text{mA}$             | High Side     | 100  |      | $\text{m}\Omega$ |
|                 |                                                 |                                                              | Low Side      | 100  |      |                  |
| $V_{REG}$       | Regulator output                                | $I_{VREG} = 100\mu\text{A}$ , $V_{DD} = 4.5 \sim 26\text{V}$ | 5.55          | 5.75 | 5.95 | V                |
| $t_{DC-DET}$    | DC detect time                                  |                                                              |               | 420  |      | ms               |
| $t_{TRIP}$      | Over-temperature threshold                      |                                                              |               | 170  |      | $^\circ\text{C}$ |
| $t_{HYSTERSIS}$ | OTP hysteresis                                  |                                                              |               | 20   |      | $^\circ\text{C}$ |
| $I_{OCP}$       | Over-current trap threshold                     |                                                              |               | 8    |      | A                |

(1) Design center value.

## Operating Characteristics

$V_{DD} = 12\text{V}$ ,  $A_V = 20\text{dB}$ ,  $T_A = 25^\circ\text{C}$  unless otherwise noted.

| Symbol      | Parameter                            | Test Condition                                                                                                 | Specification           |      |     | Unit                |
|-------------|--------------------------------------|----------------------------------------------------------------------------------------------------------------|-------------------------|------|-----|---------------------|
|             |                                      |                                                                                                                | Min                     | Typ. | Max |                     |
| $P_O$       | Output power                         | THD+N=10%, $f=1\text{kHz}$ , $R_L=4\Omega$                                                                     | $V_{DD} = 21\text{V}^1$ | 58   |     | W                   |
|             |                                      |                                                                                                                | $V_{DD} = 18\text{V}^1$ | 43   |     |                     |
|             |                                      | THD+N=1%, $f=1\text{kHz}$ , $R_L=4\Omega$                                                                      | $V_{DD} = 21\text{V}^1$ | 45   |     |                     |
|             |                                      |                                                                                                                | $V_{DD} = 18\text{V}^1$ | 35   |     |                     |
|             |                                      | THD+N=10%, $f=1\text{kHz}$ , $R_L=3\Omega$ , PBTl, $V_{DD} = 24\text{V}^1$                                     |                         | 100  |     |                     |
| THD+N       | Total harmonic distortion plus noise | $V_{DD} = 12\text{V}$ , $P_O = 10\text{W}$ , $R_L = 4\Omega$ , $f = 1\text{kHz}$                               |                         | 0.03 |     | %                   |
| $ V_{OS} $  | Offset voltage                       |                                                                                                                |                         | 20   |     | mV                  |
| $ K_{SVR} $ | Supply ripple rejection ration       | Input AC-Grounded, $C_i = 1\mu\text{F}$ , $f = 1\text{kHz}$                                                    |                         | 70   |     | dB                  |
| $ SNR $     | Signal-to-Noise ratio                | A-weighted, THD+N=1%, $R_L = 8\Omega$                                                                          |                         | 97   |     | dB                  |
| $V_n$       | Output voltage noise                 | $C_i = 1\mu\text{F}$ , $A = 26\text{dB}$ , $f = 20\text{Hz}$ to $20\text{kHz}$ , A-weighted, Input AC-Grounded |                         | 80   |     | $\mu\text{V}_{RMS}$ |
| $ CMRR $    | Common mode rejection ratio          | $V_{DD} = 12\text{V}$ , $V_{IC} = 1\text{V}_{PP}$                                                              | $f = 120\text{Hz}$      | 68   |     | dB                  |
| $Z_i$       | Input impedance                      | Gain=20dB                                                                                                      |                         | 60   |     | $\text{k}\Omega$    |
| Crosstalk   | Channel separation                   | $V_O = 1\text{W}$ , $f = 1\text{kHz}$ , Gain=20dB                                                              |                         | 93   |     | dB                  |

(1) Heat-sink is required.

## Functional Descriptions

### Gain Settings

The gain of the VA2239 can be simply set by the voltage divider connected to GAINSLV terminal. The gain, resistor ratios and corresponding input impedance are listed in Table 1. Please note that the gain setting can not be change on the fly, that is, if the gain setting is changed and the VA2239 needs to be power-recycled to take effect.

The input resistance is depended on the gain setting. Since the gain setting is determined by the ratio of the internal feedback resistive network, the variation of the gain is small. But the absolute value of the input resistance may shift by  $\pm 20\%$  at the same gain. In actual design cases, 80% of nominal value should be assumed as the input resistance of VA2239 in the input network of whole amplifier.

| Mode   | Gain | R <sub>DOWN</sub> | R <sub>UP</sub> | Input Impedance |
|--------|------|-------------------|-----------------|-----------------|
| Master | 20dB | 5.6k $\Omega$     | OPEN            | 60k $\Omega$    |
| Master | 26dB | 27k $\Omega$      | 100k $\Omega$   | 30k $\Omega$    |
| Master | 32db | 39k $\Omega$      | 100k $\Omega$   | 15k $\Omega$    |
| Master | 36dB | 47k $\Omega$      | 75k $\Omega$    | 9k $\Omega$     |
| Slave  | 20dB | 51k $\Omega$      | 51k $\Omega$    | 60k $\Omega$    |
| Slave  | 26dB | 75k $\Omega$      | 47k $\Omega$    | 30k $\Omega$    |
| Slave  | 32dB | 100k $\Omega$     | 39k $\Omega$    | 15k $\Omega$    |
| Slave  | 36dB | 100k $\Omega$     | 16k $\Omega$    | 9k $\Omega$     |

Table 1. Gain Setting vs. Resistor Network

The VA2239 can be operated in either clock master mode or clock slave mode in multiple class D amplifier usage. In clock master mode, the SYNC pin is clock source. In clock slave mode the SYNC pin is an clock input terminal. TTL logic levels with compliance to VREG.

### Amplifier Input Impedance

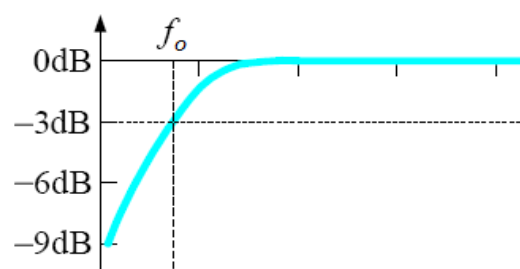


Figure 1. Cut-off point of high-pass filter

In most cases, no extra resistor needs to be added on the input of VA2239. The actual input resistor is already determined while selecting the gain. If a single capacitor is used in the input high-pass filter, the cut-off frequency  $f_o$  may vary with the change of gain setting. The -3dB point of the cut-off frequency can be calculated by the following equation,

$$f_o = \frac{1}{2\pi \times R_I \times C_I}$$

,where the  $R_I$  values is given in Table 1.

### Power Timing Sequence

Most pop noises during power on/off period are caused by the charging/discharging of input capacitors. Input capacitors are being charged while the SD\_B terminal is pulled up. Therefore an appropriate power on/off sequence is required with the control of SD\_B and MUTE.

Initially the SD\_B terminal shall be pulled low and the MUTE terminal shall be pulled high. After the powered up, the SD\_B should be pulled-up first, delay for a while, and then pull low the MUTE terminal to enable audio output. With this sequence the pop noise can be eliminated.

To shutdown the amplifier, the MUTE terminal shall be pulled-up to mute the output first, delay for a while, and then pull down the SD\_B terminal

## Functional Descriptions (cont.)

to enter the shut down state. To prevent the pop noise caused by improper power off sequence, the SD\_B terminal is forced no function when the MUTE terminal is pulled low (aka. unmute). The amplifier needs to be muted and then SD\_B would be functional.

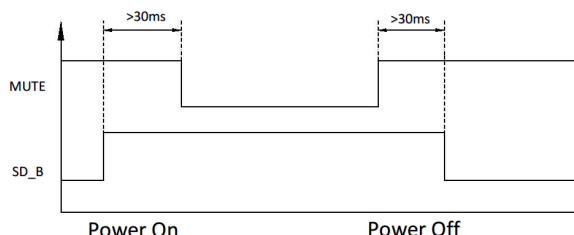


Figure 2. Recommended Power On/Off Sequence

## Shutdown Operation

The VA2239 employs a state of shutdown mode to reduce supply current to the absolute minimum level during periods of nonuse for power conservation. This terminal should be held high during normal operation when the amplifier is in normal operating. Pulling low causes the output drivers shutdown and the amplifier to enter a low-current state. Do not leave it unconnected, because there is no weakly pulling resistor inside the amplifier.

Remember that to place the amplifier in the shutdown state prior to removing the power supply voltage so that power-off pop noise can be eliminated.

## VREG Supply

The V<sub>REG</sub> Supply is used to bias the gates of the output full-bridge upper half MOSFETs. It could be used to supply the PLIMIT pin and related voltage divider circuit. Add at least 1  $\mu$ F decoupling capacitor to ground at this terminal.

## Fault Recovery Operation

The VA2239 builds in many protection schemes such as output short-circuit protection, over temperature protection and DC detection protection. Once any protection traps, the FAULT\_B pin would be pulled low and usually the output driver will be shut down and enter to a high impedance state.

Since the fault latches the output, if automatic recovery from the fault condition is desired, the FAULT\_B pin should be connected to the SD\_B pin directly. This makes the FAULT\_B pin to pull low the SD\_B pin in fault condition and try to reset the amplifier. If the fault case is removed, the FAULT\_B pin would be normally high after reset.

## Speaker Protection

Due to the nature of Class D amplifiers, the speakers may have DC current if the audio inputs get DC voltage in any case. An output DC fault will shuts down the audio amplifier and change the state of output into high impedance.

To resolve the case of DC input, it is good to treat it as very low frequency sine wave much lower than audio band such as 2Hz. Based on this criteria, a DC detect fault shall be issued when the output differential duty-cycle of either channel exceeds 14% for more than 420ms at the same polarity. This feature protects the speakers away from large currents.

The minimum differential input DC voltages required to trigger the DC detection fault are listed in the Table 2.

## Functional Descriptions (cont.)

| $A_v$ (dB) | $V_{IN}$ (mV, Differential) |
|------------|-----------------------------|
| 36         | 17                          |
| 32         | 28                          |
| 26         | 56                          |
| 20         | 112                         |

Table 2. DC detect fault threshold

To resume the normal operation, it is necessary to power off the amplifier and then power on, cycling SD\_B can not resume normal operation.

### Short Circuit Protection

VA2239 has protection from over-current conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the FAULT\_B pin as a low state. The amplifier outputs are switched to a high impedance state when the short circuit protection latch is engaged. The latch can be cleared by cycling the SD\_B pin through the low state.

### Thermal Protection

Thermal protection on the VA2239 prevents damage to the device when the internal die temperature exceeds 170°C. There is a  $\pm 20^\circ\text{C}$  tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 20°C. VA2239 will be back to normal operation at this point with no external system interaction.

### Power Limit Operation

The voltage at PLIMIT terminal can be used to limit

the power to levels below that which is possible based on the supply rail. Add a resistor divider from VREG to ground to set the voltage at the PLIMIT terminal. An external reference may also be used if precise limitation is required. Also add a 1  $\mu\text{F}$  capacitor from this pin to ground.

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to fixed maximum value. This limit can be thought of as a “virtual” voltage rail which is lower than the supply connected to power rail. This “virtual” rail is 5 times the voltage at the PLIMIT pin. This output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

$$P_{OUT} = \frac{\left( \left( \frac{R_L}{R_L + 2 \times R_S} \right) \times V_P \right)^2}{2 \times R_L}$$

$$V_P = 5 \times \text{PLIMIT voltage if PLIMIT} < 5 \times V_P$$

$$P_{OUT} (\text{with 10\% THD}) = 1.25 \times P_{OUT}$$

where  $R_S$  is the total series resistance including  $r_{DS(ON)}$  and any resistance in the output filter.  $R_L$  is the load resistance.  $V_P$  is the peak amplifier of the output possible within the supply rail.

### AM Radio EMI Reduction

For most countries the AM radio band is located in 522kHz~1701kHz. Due to the intrinsic of the switching topology, the fundamental frequency of switching frequency and its second harmonic would interfere the corresponding AM radio station seriously. To achieve both of the advantage of switching amplifier and AM radio receiving performance, the VA2239 provides 4 selectable switching frequencies to change on demand to prevent the

## Functional Descriptions (cont.)

interfere. See Table 3 for recommended frequencies.

(units: kHz)

| US        | EU/China  | Japan     | Switch Freq. | FREQ1  | FREQ0 |
|-----------|-----------|-----------|--------------|--------|-------|
| 530~540   | 531~540   | 531~540   | 400          | 0      | 0     |
| 540~910   | 540~909   | 540~909   | 500          | 0      | 1     |
| 920~1120  | 918~1116  | 918~1116  | 600 or 400   | 1 or 0 | 0     |
| 1130~1370 | 1125~1368 | 1125~1368 | 500          | 0      | 1     |
| 1380~1550 | 1377~1548 | 1377~1548 | 600 or 400   | 1 or 0 | 0     |
| 1560~1710 | 1557~1602 | 1557~1629 | 600 or 400   | 1 or 0 | 0     |

Table 3. Recommended switching frequencies

## Application Information

### Output Filter

Many applications require a ferrite bead filter at least. The ferrite filter reduces EMI above 30MHz. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies, be aware of its maximum current limitation.

Use an LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and there are long wires from the amplifier to the speaker.

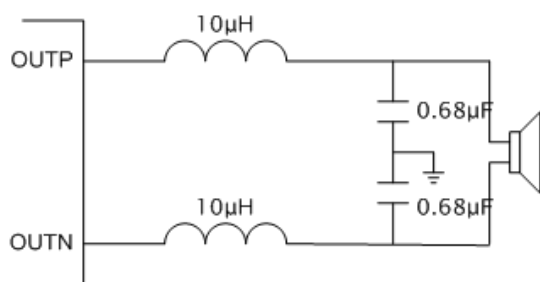


Figure 3. Typical LC Output Filter, Speaker Impedance=8Ω

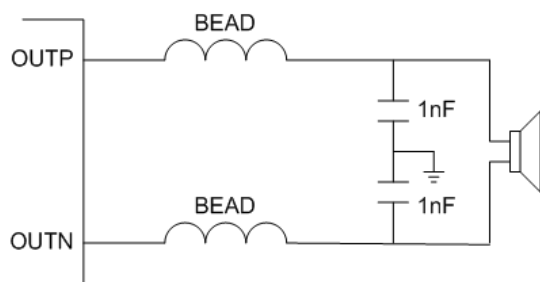


Figure 4. Typical Ferrite Chip Bead Output Filter

Inductors used in LC filters must be selected carefully. A significant change in inductance at the peak output current of the VA2239 will cause increased distortion. The change of inductance at currents up to the peak output current must be less than 0.1µH per amp to avoid this. Also note that smaller inductors than 10µH may cause an increase in distortion above what is shown in preceding graphs of THD versus frequency and output power. In all cases, avoid using inductors which value are less

than 10µH.

Like the selection of the inductor in LC filters, the capacitor must be selected carefully, too. A significant change in capacitance at the peak output voltage of the VA2239 will cause increased distortion. LC filter capacitors should be double of DC voltage ratings of the peak application voltage (the power supply voltage) at least. In general, it is strongly recommended using capacitors with good temperature performance like X5R series.

### Output Snubbers

In Figure 5, the 10nF capacitors in series with 3.3Ω resistors connected with the outputs of the VA2239 are snubber circuits. They smooth switching transitions and reduce overshoot and ringing. With these networks, THD+N can be improved at lower power levels and EMC can be reduced 2~4 dB at middle frequencies. They increase quiescent current by 3mA~11mA depending on supply voltage.

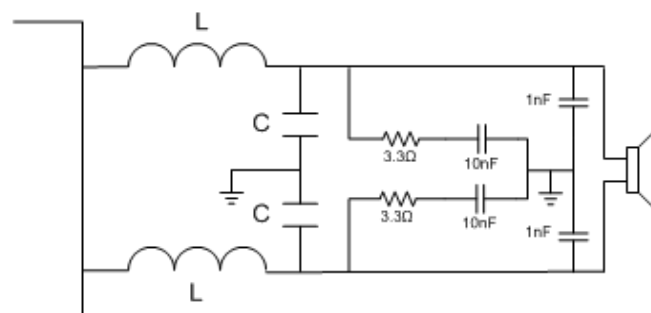


Figure 5. Output Snubber Circuits

### Low ESR Capacitors

Low ESR capacitors are highly recommended for this application. In general, a practical capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this unwanted resistor can eliminate the effects of the ideal ca-

## Application Information (cont.)

pacitor. Place low ESR capacitors on supply circuitry can improve THD+N performance.

### Boot-Strap Capacitors

The full H-bridge output stages use only MOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22 $\mu$ F ceramic capacitor, rated for at least 25V, must be connected from each output to its corresponding boot-strap input. Specifically, one 0.22 $\mu$ F capacitor must be connected from OUTP to BSP, and one 0.22 $\mu$ F capacitor must be connected from OUTN to BSN.

The bootstrap capacitors connected between the BSP or BSN pins and corresponding output function as a floating power supply for the high side N-channel power MOSFET gate drive circuitry. During each high side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

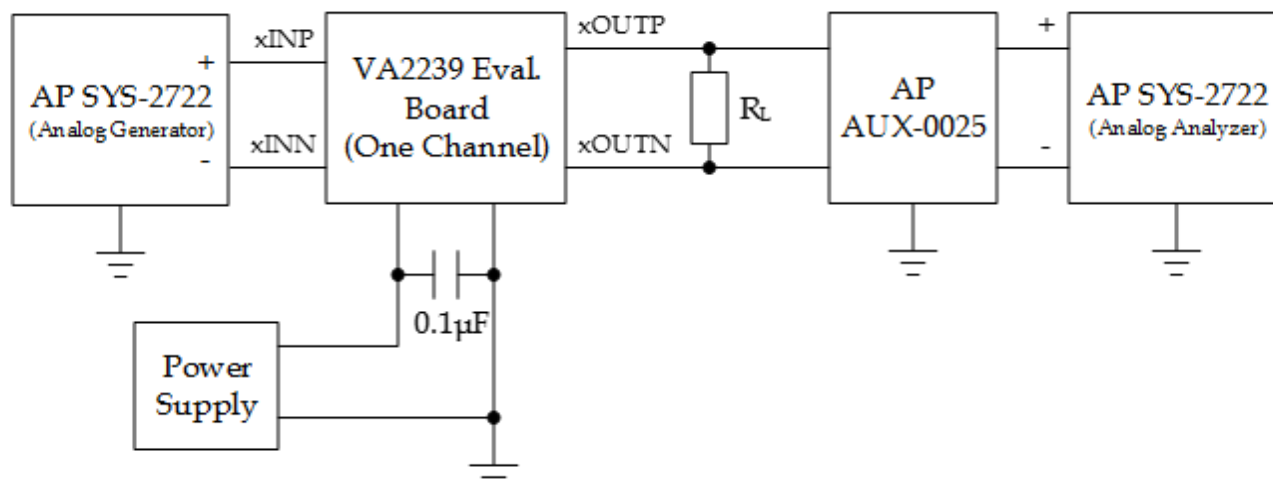
### Decoupling Capacitors

VA2239 requires appropriate power decoupling to minimize the output total harmonic distortion (THD) and improves EMC performance. Power supply decoupling also prevents intrinsic oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling can be achieved by using two different types of capacitors which target different types of noise on the power supply lines. For higher frequency spikes, or digital hash on the rail, a good low ESR ceramic capacitor, for example 0.1 $\mu$ F to 10 $\mu$ F, placed as close as possible to PVDDR and PVDDL pins works best. For filtering lower frequency noise, a larger low ESR aluminum electrolytic capacitor of 470 $\mu$ F or greater placed near the audio power amplifier is suggested. The 470 $\mu$ F capacitor also serves as local storage ca-

pacitor for supplying current during heavy power output on the amplifier outputs. The PVDDR and PVDDL terminals provide the power to the output transistors, so a 470 $\mu$ F or larger capacitor should be placed by PVDDR and PVDDL terminals as near as possible. A 10 $\mu$ F ceramic capacitor on each PVDDR/PVDDL terminal is also recommended.

## Typical Characteristic

### Test Setup Connection Diagram



\* Remove all L/C (BEAD) filter components on board before performing all measurements.

\*\* Connection diagram is for one-channel configuration.

| Figure No. | Description                                     |
|------------|-------------------------------------------------|
| 6          | THD+N vs. Output Power, 8Ω load (BTL) 8V~18V    |
| 7          | THD+N vs. Output Power, 8Ω load (BTL) 21V , 24V |
| 8          | THD+N vs. Output Power, 4Ω load (BTL) 8V~24V    |
| 9          | THD+N vs. Output Power, 4Ω load (BTL) 21V , 24V |
| 10         | Noise, 24V, 4Ω load                             |
| 11         | Noise, 24V, 8Ω load                             |
| 12         | THD+N vs. Frequency, 24V, 8Ω load (BTL)         |
| 13         | THD+N vs. Frequency, 24V, 4Ω load (BTL)         |
| 14         | Frequency Response, 24V, 8Ω load                |
| 15         | Frequency Response, 24V, 4Ω load                |
| 16         | Efficiency, 4Ω load / 2ch (BTL)                 |
| 17         | Efficiency, 8Ω load / 2ch (BTL)                 |

## Typical Characteristic (cont.)

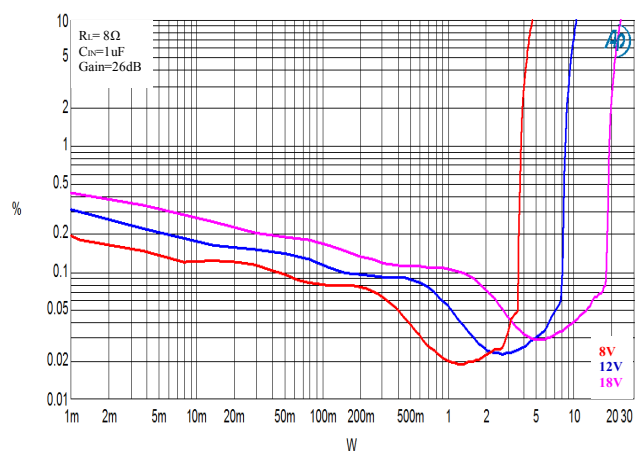


Figure 6. THD+N vs. Output Power, 8Ω load (BTL)

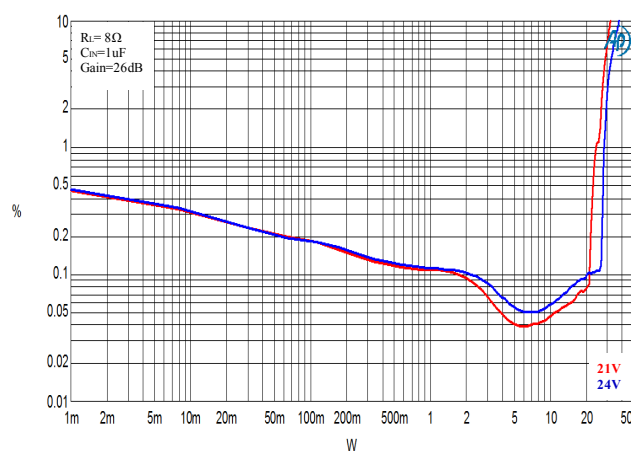


Figure 7. THD+N vs. Output Power, 8Ω load (BTL)

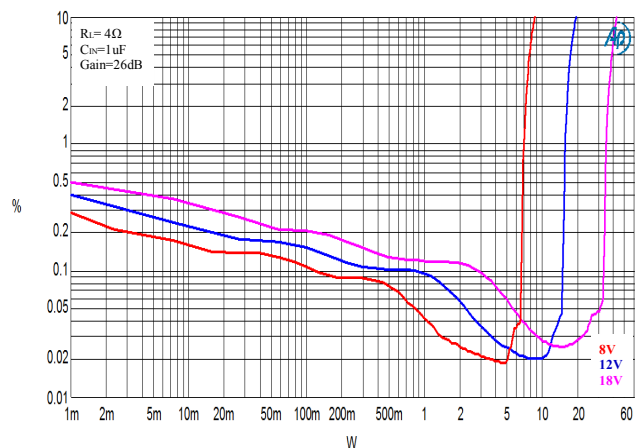


Figure 8. THD+N vs. Output Power, 4Ω load (BTL)

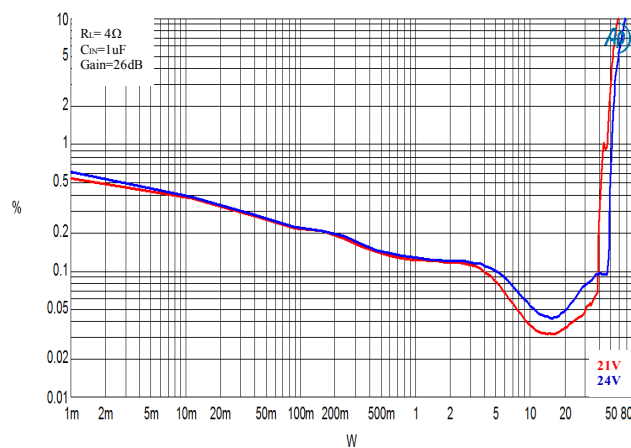


Figure 9. THD+N vs. Output Power, 4Ω load (BTL)

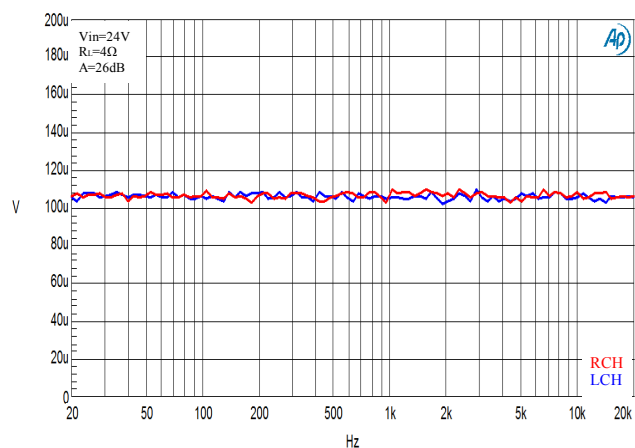


Figure 10. Noise, 24V, 4Ω load

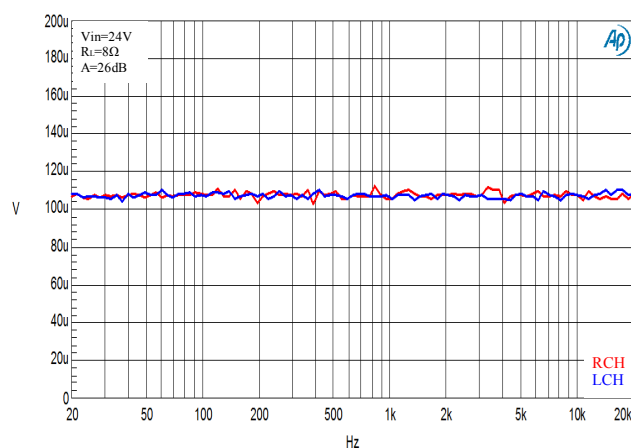


Figure 11. Noise, 24V, 8Ω load

## Typical Characteristic (cont.)

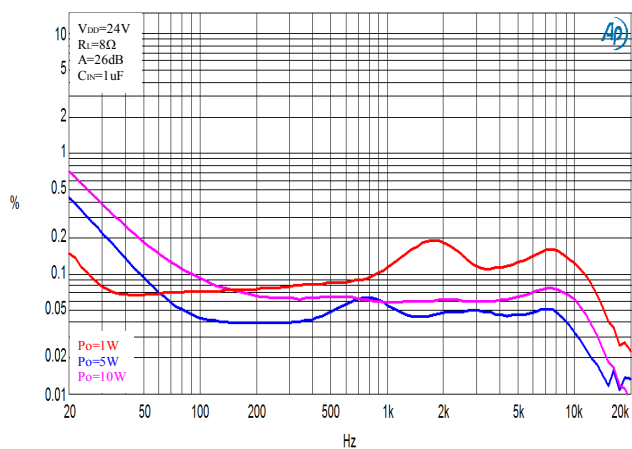


Figure 12. THD+N vs. Frequency, 24V, 8Ω load (BTL)

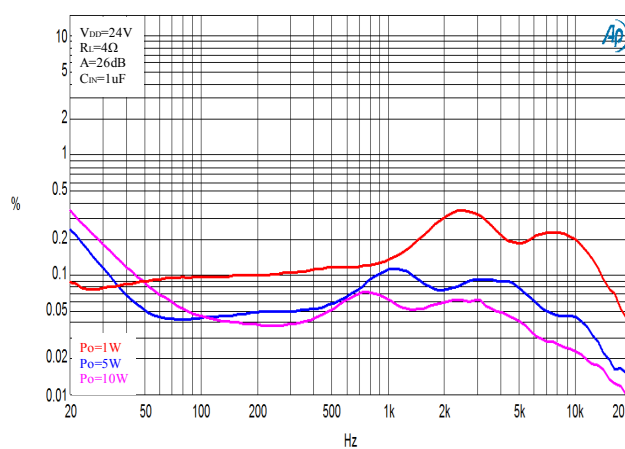


Figure 13. THD+N vs. Frequency, 24V, 4Ω load (BTL)

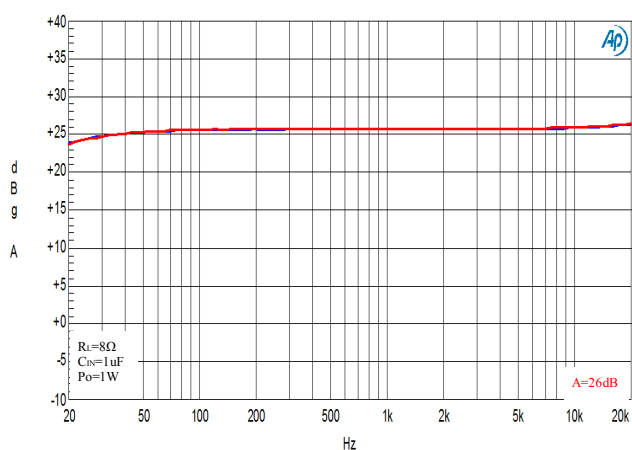


Figure 14. Frequency Response, 24V, 8Ω load

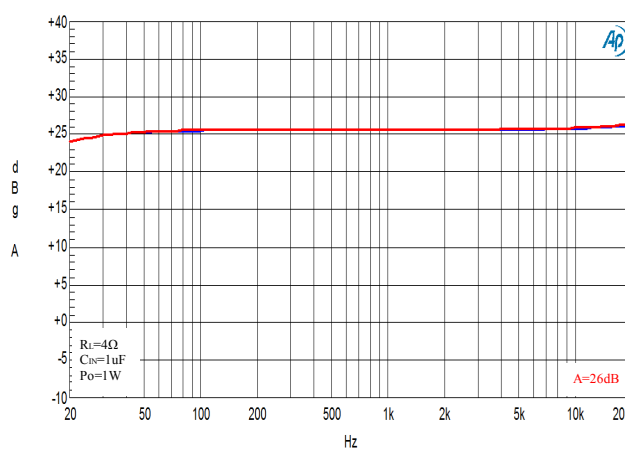


Figure 15. Frequency Response, 24V, 4Ω load

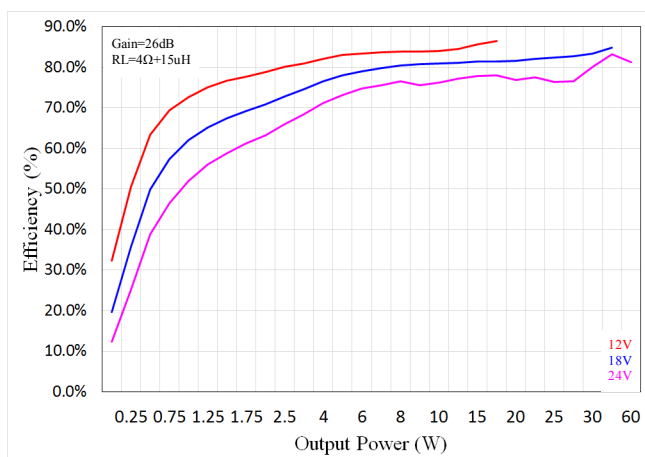


Figure 16. Efficiency, 4Ω load / 2ch (BTL)

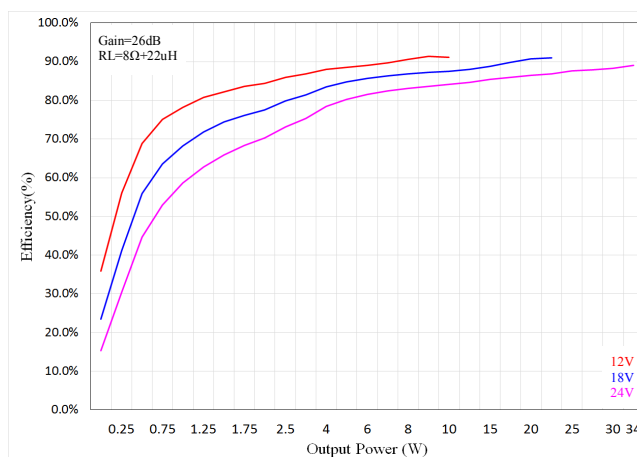


Figure 17. Efficiency, 8Ω load / 2ch (BTL)

## Application Circuit

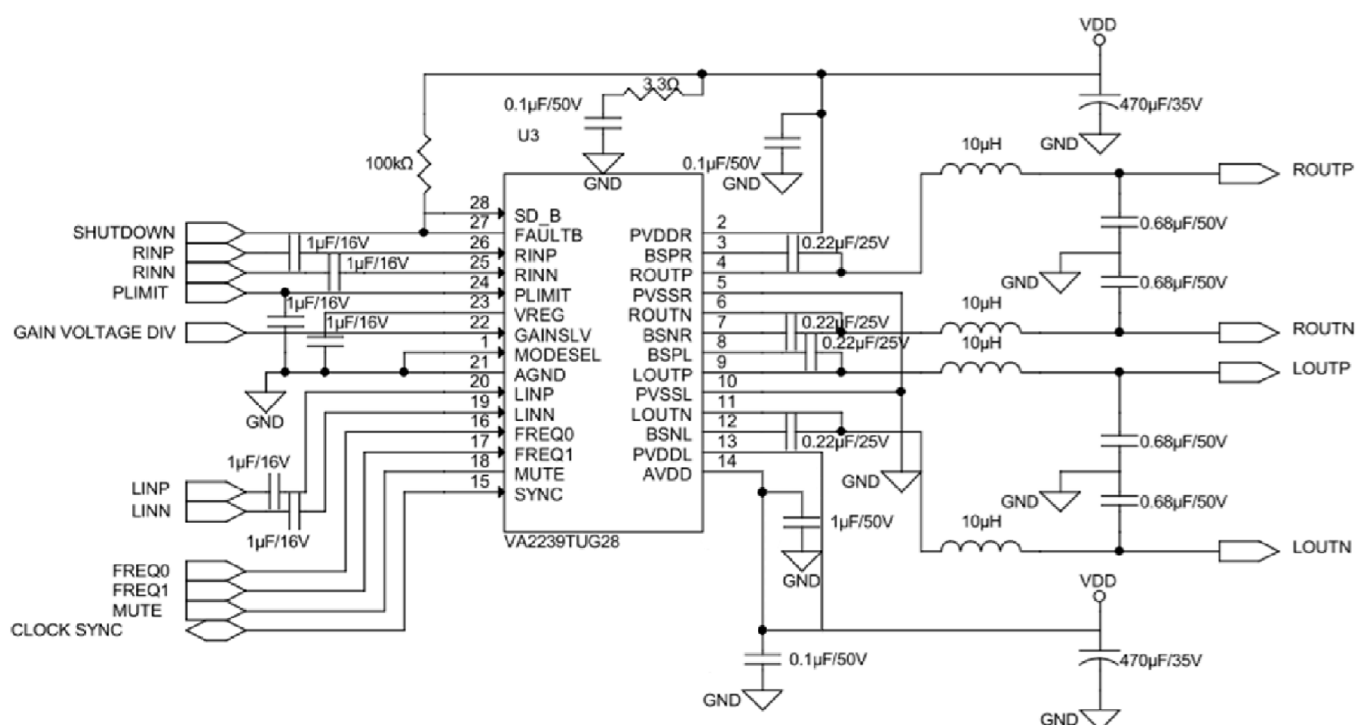


Figure 6. VA2239 Stereo Reference Application

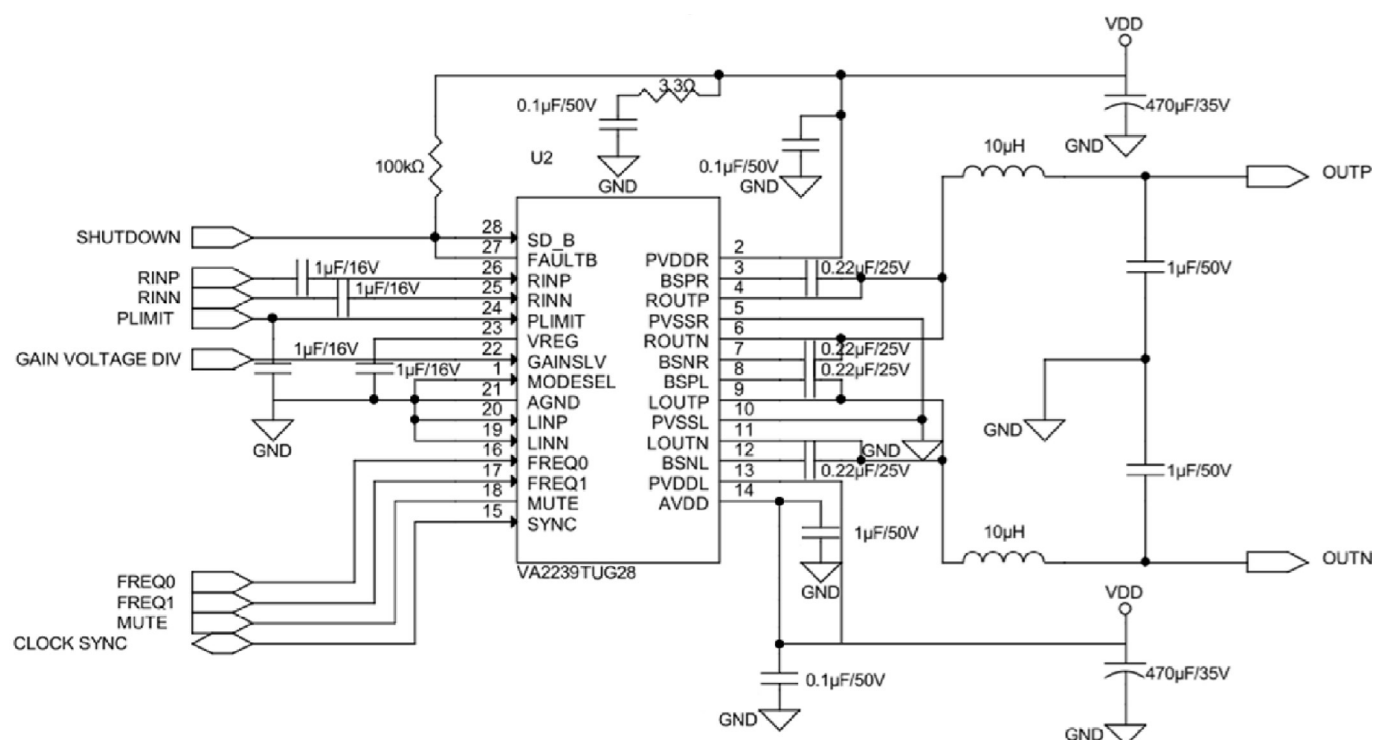
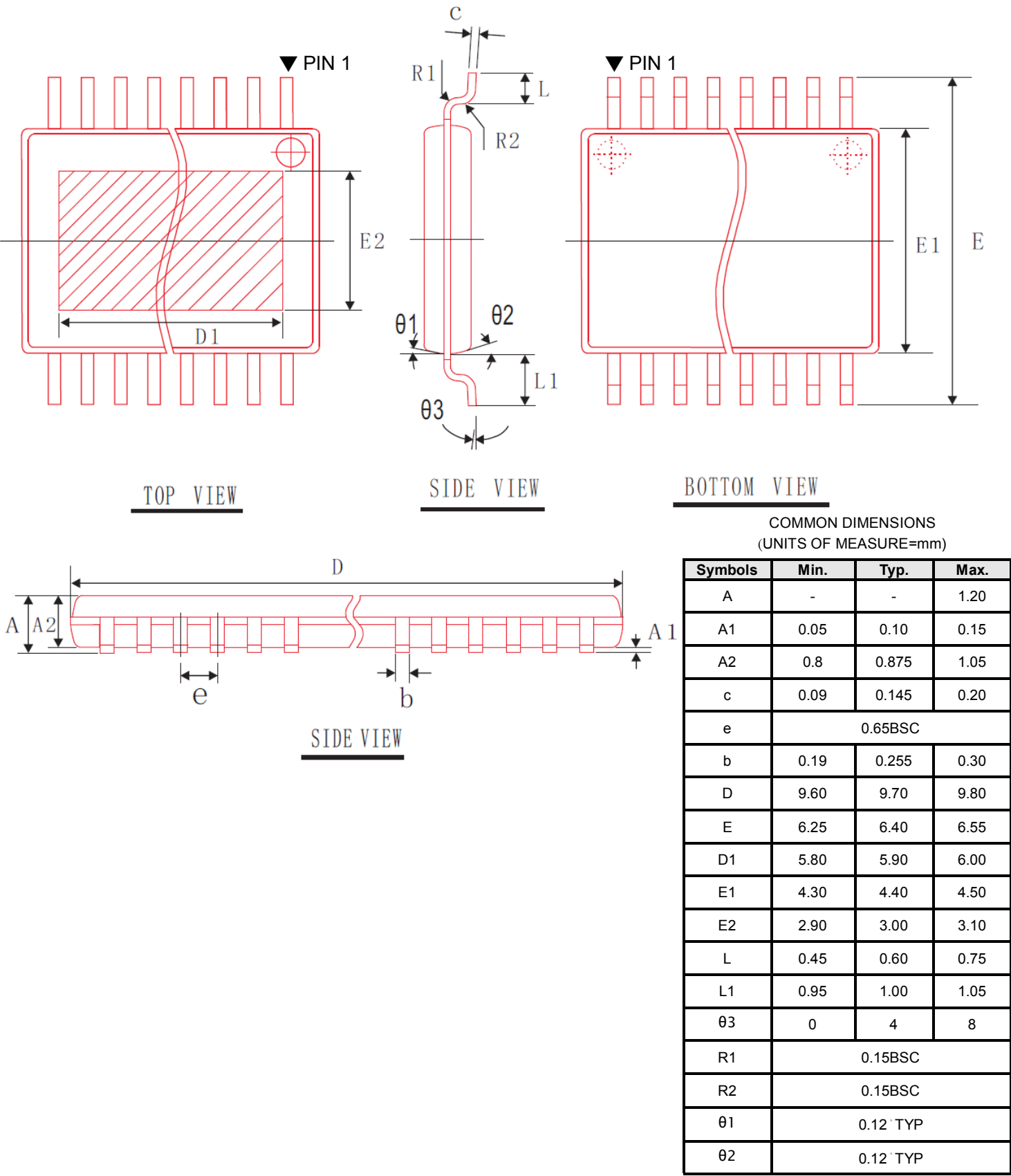


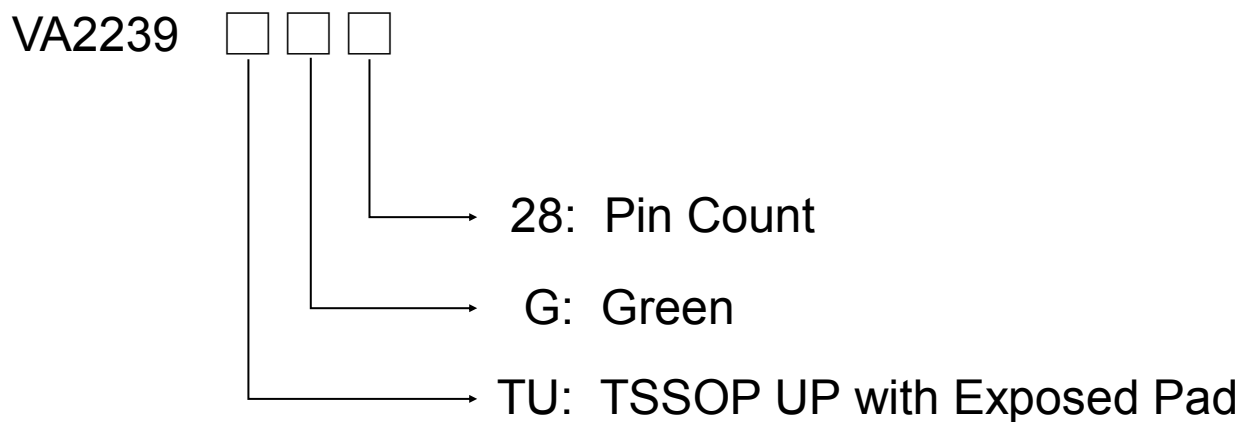
Figure 7. VA2239 Mono Reference Application

## Package Information

### TSSOP-28UEP



## Ordering Information



| Part No.    | Q`ty/Reel |
|-------------|-----------|
| VA2239TUG28 | 4,000     |

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