VTC Incorporated

VA2705

T-79-07-20

DUAL HIGH-SPEED PRECISION OPERATIONAL AMPLIFIER

FEATURES

- Dual Version of VA705 Fast-Settling Op Amp
- Fast Settling Time: ±0.1% in 250ns
- High Slew Rate: 35V/μs
- Wide Gain Bandwidth: 25MHz
- Low Offset Voltage: 3mV
- Minimal Crosstalk: >90dB Separation
- Large Output Current: ±50mA
- Short Circuit Protection
- Industry-Standard Pinout
- Available in Commercial Versions

DESCRIPTION

The VA2705 offers the high-speed (35V/μs), precision advantages of theVA705 in a dual package configuration. The small offsets and open-loop gain (10k V/V) make the amplifier ideal for video processing and signal conditioning applications where accuracy is at a premium. The VA2705 is offered in an 8-pin CERDIP.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages .... ±6V
Differential Input Voltage .... ±9V
Common Mode Input Voltage .... $|V_S|$ -0.5V
Power Dissipation (T_A=70°C, Note 1) 450mW
Output Short Circuit Current Duration (Note 2) ...... Indefinite
Operating Temperature Range:
Commercial (2705 J, K) .... 0° to 70°C
Storage Temperature Range .... -65° to +150°C
Lead Temperature (Soldering to 60 Sec.) .... 300°C

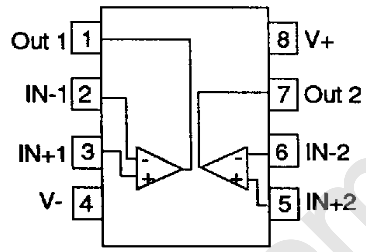
Note 1: Power derating above T_A = 70°C to be based on a maximum junction temperature of 150°C and the following thermal resistance factors:

Note 2: Continuous short circuit protection is allowed on one amplifier per time up to the following case and ambient temperatures:

PKGE.	θ_{JC} (°C/W)	θ_{JA} (°C/W)	T_C (°C)	T_A (°C)
DIP	75	180	100	30

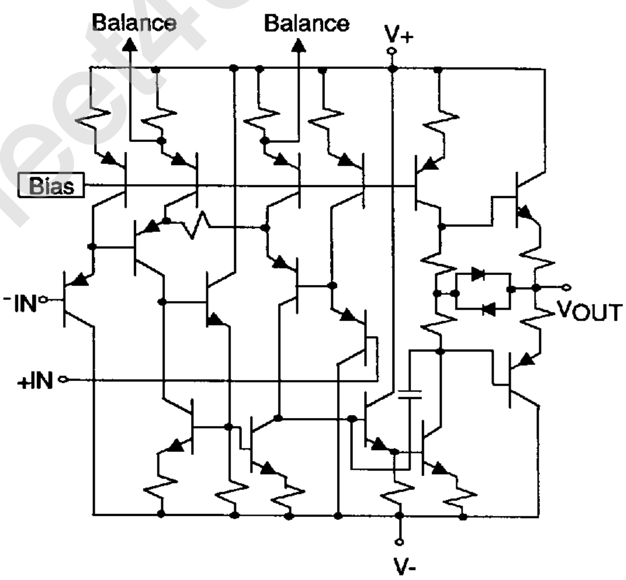
CONNECTION DIAGRAMS

8-Lead Dual In-Line Package



Top View

SIMPLIFIED SCHEMATIC



PACKAGE TYPES AVAILABLE

- 8-Pin Plastic DIP
- 8-Pin CERDIP

DISCONTINUED

4088 E-09

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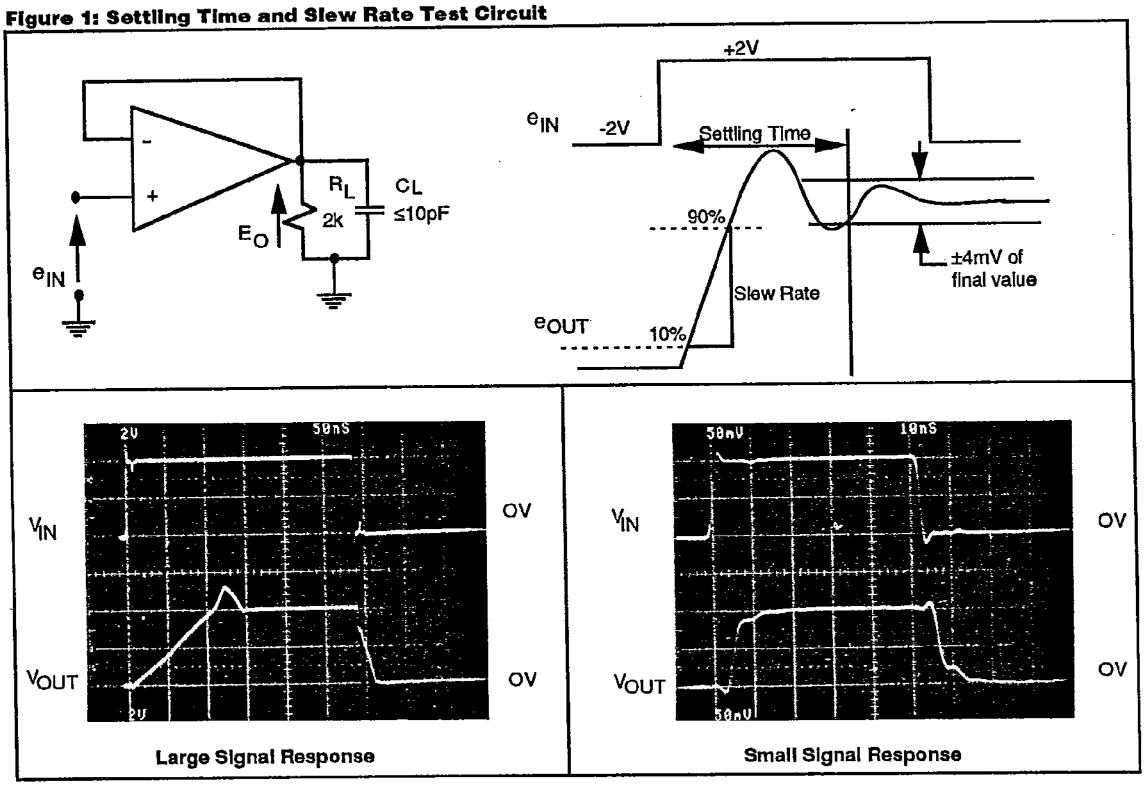
ELECTRICAL CHARACTERISTICS ($V_S = \pm5V$, $T_A = 25°C$ unless otherwise stated) (each amplifier)

PARAMETER	SYMBOL	CONDITIONS	VA2705J MIN	VA2705J TYP	VA2705J MAX	VA2705K MIN	VA2705K TYP	VA2705K MAX	UNITS
Input Offset Voltage	V_{OS}			6	12		3	6	mV
T_{Min} to T_{Max}		$0° \le T_A \le 70°C$		9	16		5	10	
		$-55 \le T_A \le 125°C$							
Average Offset Voltage Drift	$\frac{\Delta V_{OS}}{\Delta T}$	$0° \le T_A \le 70°C$		20			20		µV/°C
		$-55 \le T_A \le 125°C$							
Input Bias Current	I_B			650	1100		650	900	nA
T_{Min} to T_{Max}		$0° \le T_A \le 70°C$			1700			1400	
		$-55 \le T_A \le 125°C$							
Input Offset Current	I_{OS}			35	100		25	50	nA
Input Common Mode Range	V_{CM}		+3 -4	+3.5 -4.5		+3 -4	+3.5 -4.5		V
Differential Input Resistance	R_{IND}	(Note 1)	3	10		3	10		MΩ
Common Mode Input Resistance	R_{INC}	(Note 1)	4	8		4	8		MΩ
Differential Input Capacitance	C_{IND}	(Note 1)		2					pF
Common Mode Input Capacitance	C_{INC}	(Note 1)		3			3		pF
Input Voltage Noise	e_N	BW = 10Hz to 100KHz		12			12		µVRMS
Open Loop Voltage Gain	A_V	$V_{OUT} = \pm3V$ $R_L = 2k\Omega$	2	5		4	10		V/mV
Output Voltage Swing	V_{OUT}	$R_L = 2k\Omega$	±3.5	+4 -4.2		±3.5	+4 -4.2		V
		$R_L = 51\Omega$	±2.0			±2.5			
Power Supply Current (Both Amplifiers)	I_S			15	20		15	20	mA
Common Mode Rejection Ratio	CMRR	$V_{CM} = \pm2V$	60	70		60	70		dB
Power Supply Rejection Ratio	PSRR	$\Delta V_{PS} = \pm0.5V$	60	66		60	66		dB
Slew Rate	SR	10-90% of Leading Edge (Figure 1)	30	35		30	35		V/µs
Settling Time	t_S	To ±0.1% (±4mV) of Final Value (Figure 1, Note 1)		250	300		250	300	ns
Gain Bandwidth Product	GBW			25			25		MHz
Small Signal Rise/Fall Time	t_r/t_f	$e_O = \pm50mV$ 10-90% (Figure 1)		7			7		ns
Full Power Bandwidth	BW_{FP}	$R_L = 2k\Omega$ $C_L = 50pF$ $V_{OUT} = 6Vp\text{-}p$		1.8			1.8		MHz
Amplifier to Amplifier Crosstalk		Input Referenced f=10KHz (Figure 2)		-96			-96		dB

Notes: 1. Not tested, guaranteed by design

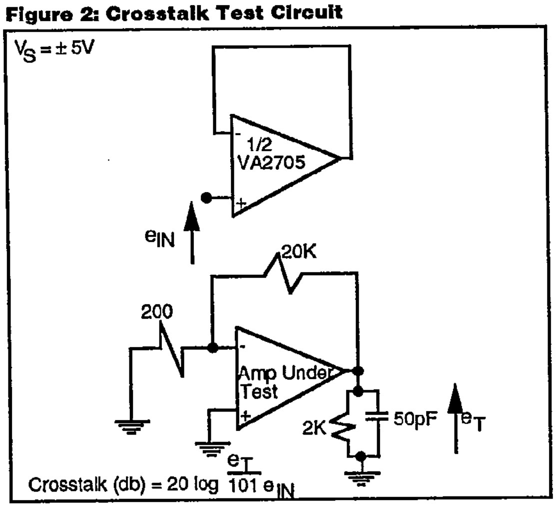
Figure 1: Settling Time and Slew Rate Test Circuit



Large Signal Response

Small Signal Response

Figure 2: Crosstalk Test Circuit



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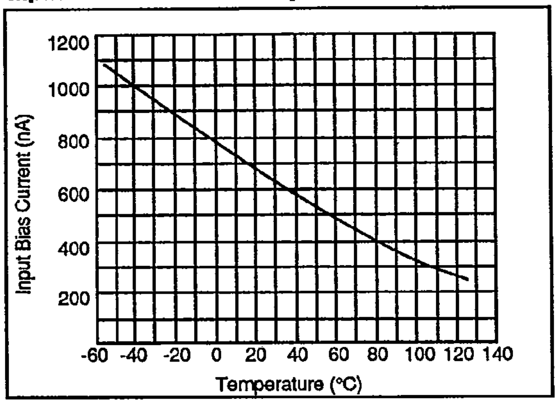
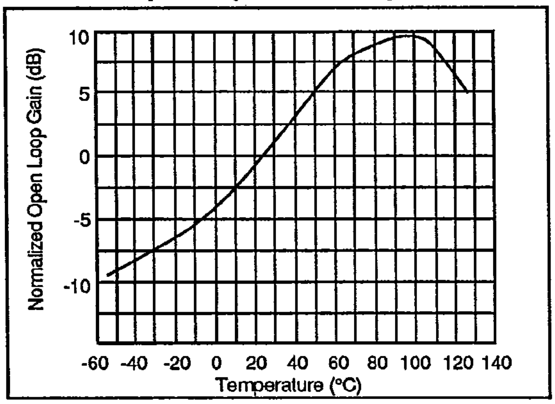
TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A = 25° C unless otherwise stated)

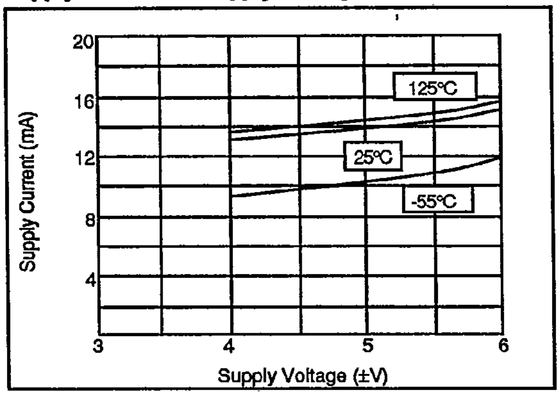
Input Bias Current vs Temperature



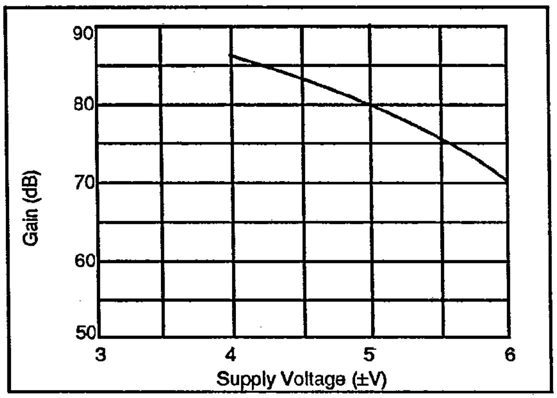
Normalized Open Loop Gain vs Temperature



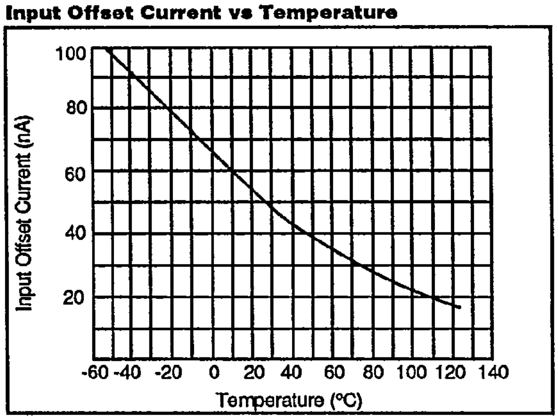
Supply Current vs Supply Voltage



Open Loop Gain vs Supply Voltage

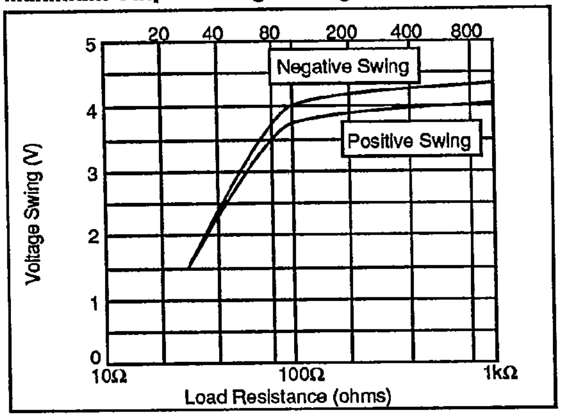


Input Offset Current vs Temperature

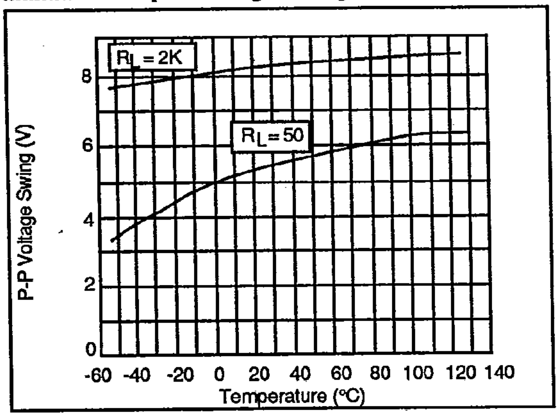


TYPICAL PERFORMANCE CHARACTERISTICS ($V_S = \pm 5V$, $T_A = 25°C$ unless otherwise stated)

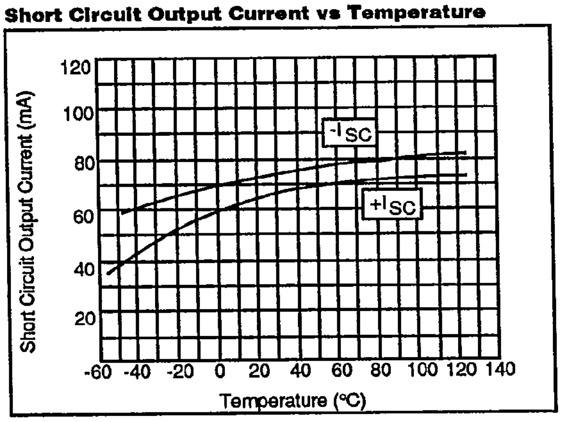
Maximum Output Voltage Swing vs Load Resistance



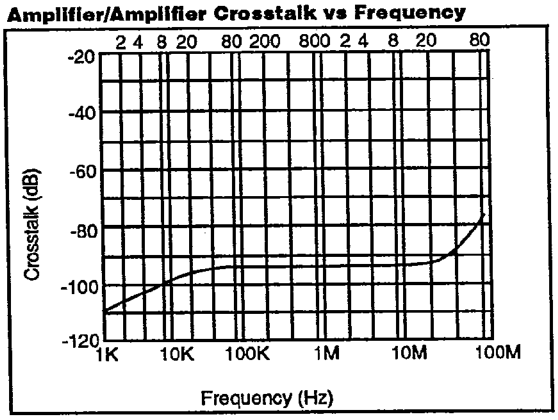
Maximum Output Voltage Swing vs Temperature



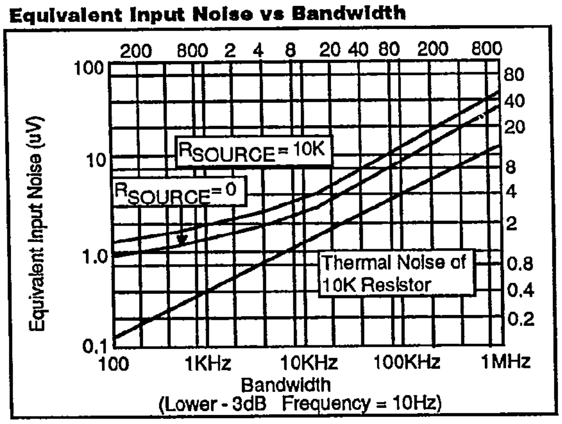
Short Circuit Output Current vs Temperature



Amplifier/Amplifier Crosstalk vs Frequency



Equivalent Input Noise vs Bandwidth



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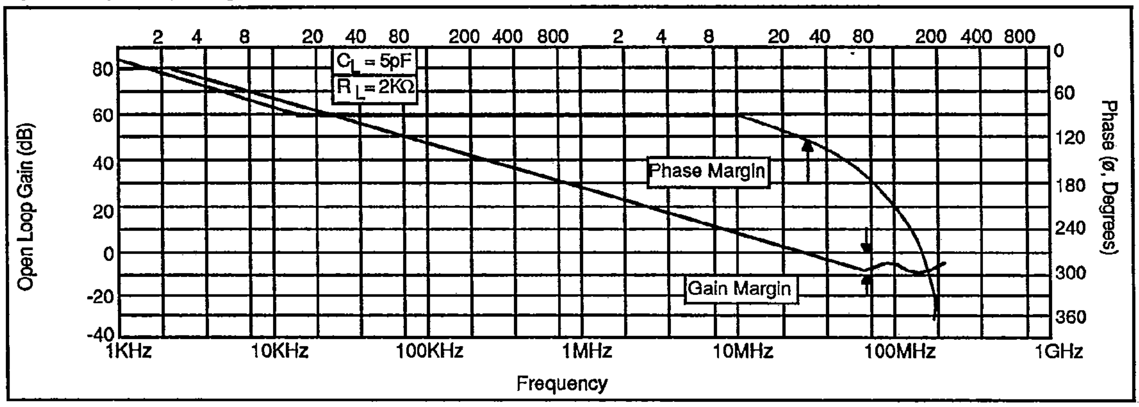
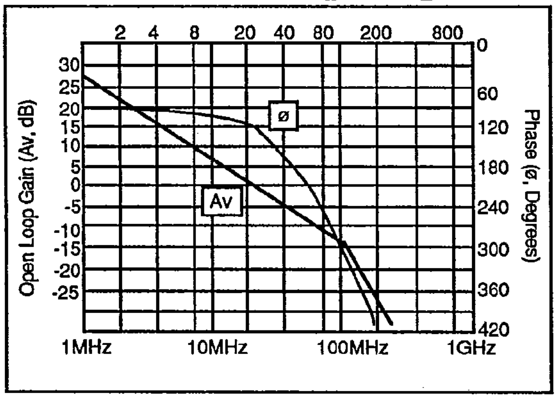
TYPICAL PERFORMANCE CHARACTERISTICS (V_S= ±5V, T_A = 25° C unless otherwise stated)

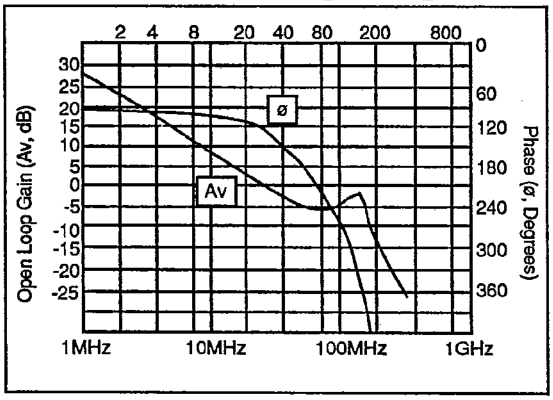
Open Loop Frequency Response



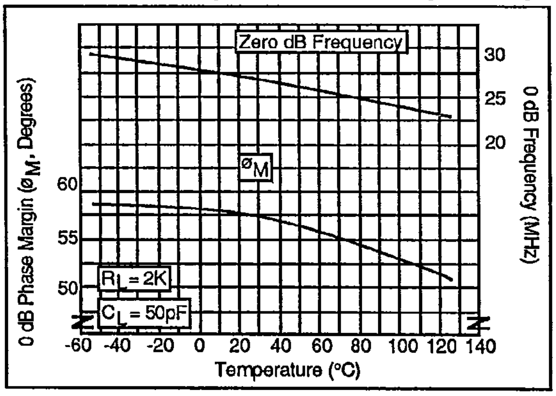
Open Loop Freq. Response, R_L= 50Ω, C_L= 50pF



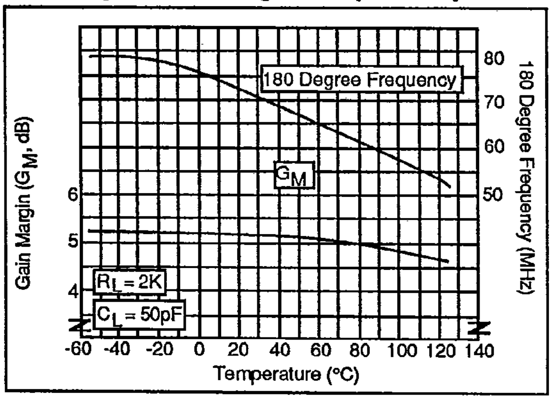
Open Loop Freq. Response, R_L= 2KΩ, C_L= 50pF



Zero dB Phase Margin and Zero dB Freq. vs Temp.



Gain Margin and 180 Degree Freq. vs Temp.



APPLICATION INFORMATION

AC Characteristics

The 28MHz 0dB crossover point of the VA2705 is achieved without feed forward compensation, a technique which can produce long tails in the recovery characteristic. The single pole rolloff follows the classic 20dB/decade slope to frequencies approaching 50MHz. The phase margin of 58°, even with a capacitive load of 50pF, gives stable and predictable performance down to unity gain follower configurations.

At frequencies beyond 50MHz, the 20dB/decade slope is disturbed by an output stage zero, the damping factor of which is dependent upon the load capacitor. This results in loss of gain margin (gain at loop phase = 360°) at frequencies of 70 to 100MHz which at a gain margin of 5dB (R_L = 2k, C_L = 50pF) results in a 10dB peak in the unity gain follower closed loop characteristic (Figure 3).

Figure 3 shows a blow up of the open loop characteristics in the 10MHz to 200MHz frequency range as well as the corresponding unity gain follower characteristics at similar load conditions. It is seen that the output stage zero results in bandwidth extension beyond the 28MHz, 0dB crossover point. In fact, with the proper choice of the R_L,C_L load, the unity gain follower can be "tweaked" to give flat small signal response to 100MHz.

Figure 4 shows corresponding time domain response for a small signal step. As expected there is a strong 80MHz ring for R_L = 2kΩ, C_L = 50pF which disappears at R_L = 50Ω, C_L = 5pF.

Layout Considerations

As with any high-speed wideband amplifier, certain layout considerations are necessary to ensure stable operation. All connections to the amplifier should be kept as short as possible, and the power supplies bypassed with 0.1μF capacitors to signal ground. It is suggested that a ground plane be considered as the best method for ensuring stability because it minimizes stray inductance and unwanted coupling in the ground signal paths.

To minimize capacitive effects, resistor values should be kept as small as possible, consistent with the application.

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Figure 3: Unity Gain Follower Frequency Characteristics

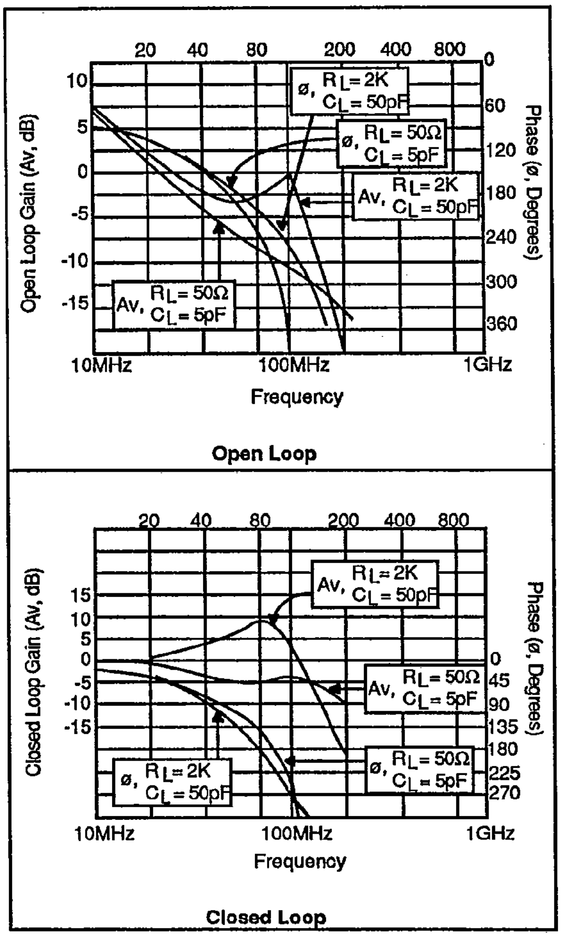

Figure 4: Unity Gain Follower Step Response