VAR-SOM-SD600
System on Module (SoM)
Data Sheet
(Provisional)

Version 1.0

May 14

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Part No. VAR-SoM-SD600

This document describes theVariscite System on Module (SoM) implementation of a multipurpose multimedia processor based on the Qualcomm Snapdragon™ 600 (APQ8064) 1.7 GHz quad Krait™ CPU.

This document specifies the electrical, mechanical and thermal parameters of the VAR-SOM-SD600 System on Module (SoM) and is intended for design engineers incorporating the SoM into its company's products.

Its initial chapter can be used as an overview of the VAR-SOM-SD600 by management and non-technical staff.

Document Revision History

Revision	Date	Notes
1.0	May 7, 2014	Initial

Table of Contents

1 About this Document

1.1 Scope

This document describes the Variscite System on Module (SoM) implementation of a multipurpose multimedia processor based on the Qualcomm Snapdragon™ 600 (APQ8064) 1.7 GHz quad Krait™ CPU.

1.2 Reference Documents

The following documents can be used for reference:

- SD600 SDK Carrier Board Developer's Guide
- VAR-SOM-SD600 Schematics

Contact Variscite support services for further information: mailto:support@variscite.com.

2 Overview

The VAR-SOM-SD600 is a high performance System-on-Module that leverages cutting edge mobile computing for embedded and industrial product designs, based on the Qualcomm Snapdragon™ 600 (APQ8064) 1.7 GHz quad Krait™ CPU.

The VAR-SOM- SD600 provides an ideal building block for simple integration with a wide range of products in target markets requiring rich multimedia functionality, powerful graphics processing and video capabilities, as well as high-processing power, in a compact, cost effective SoM with low power consumption. The VAR-SOM-SD600 boasts a wide range of peripheral interfaces, which are routed to the 314-pin edge connector.

Variscite also provides a carrier board with a socket for the VAR-SOM-SD600, and various connectors for additional interfaces for potential devices to interface to such as audio, video, Wi-Fi antennas, etc.

The VAR-SOM- SD600 supports the following operating systems:

- Android
- Linux (coming soon)

2.1 SD600 (APQ8064) features summary

Qualcomm Snapdragon™ 600 (APQ8064)

- High performance 1.7 GHz Quad Krait™ up to 22,400 DMIPS
- Highly efficient DMIPS/in the middle of the window performance
- Enhanced ARMv7 compliant architecture
- Adreno 320 GPU providing 2D/3D graphics acceleration
- Full HD 1080p video encoding/ decoding capability
- Up to 4GB DDR3
- Up to 64GB eMMC storage

Networking

- Gigabit Ethernet
- Dual Band Wi-Fi 802.11a/b/g/n with MIMO option
- Bluetooth: 4.0 + BLE

Audio

- Digital stereo microphone
- Analog microphone (line-in)
- Stereo headphone output
- 2 x line out , I2S output

Display Support

- Dual LVDS, HDMI 1.4, Dual MIPI-DSI
- Up to QXGA 2048 x 1536 x 24 bpp

USB

- USB OTG with integrated PHY
- 2 x USB 2.0 Host with integrated PHYs
- 1 x HSIC for external PHY-less connection

Camera

- 2 x Camera MIPI CSI up to 20MP

Other Interfaces

- PCIe
- SATA
- UART, I2C, SPI, SD/MMC, JTAG
- Backlight PWM

2.2 SoM Block diagram

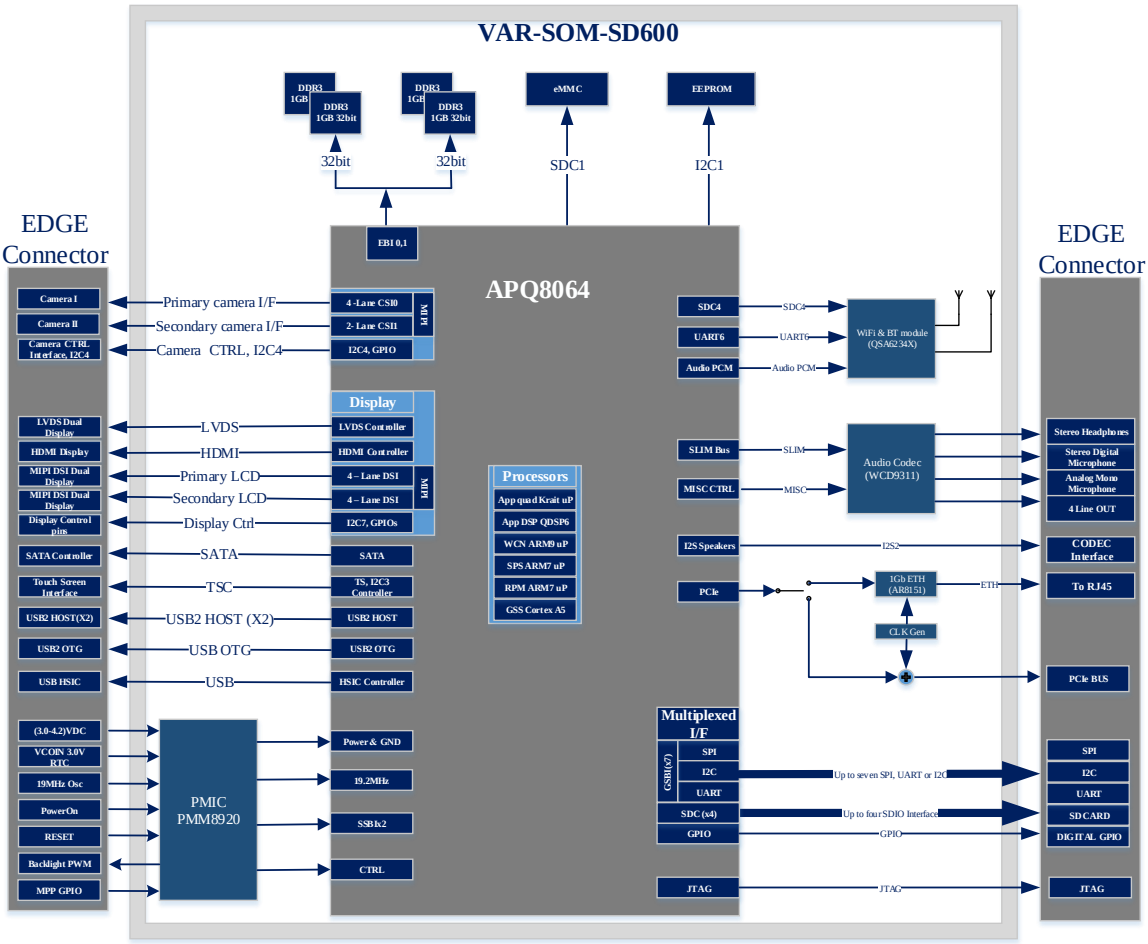

Figure 2-1: SoM Block diagram

2.3 Applications

The VAR-SOM-SD600 SoM is used in a wide range of products across many different target markets. Some of the typical applications are:

- Portable (battery powered) and Mains powered products
- Medical
- Military and Aerospace
- Consumer electronics
- Communications
- Video Conferencing and Surveillance
- Industrial Control
- Optical inspection

2.4 SOM's components and layout

The VAR-SOM-SD600 comprises the following main HW components:

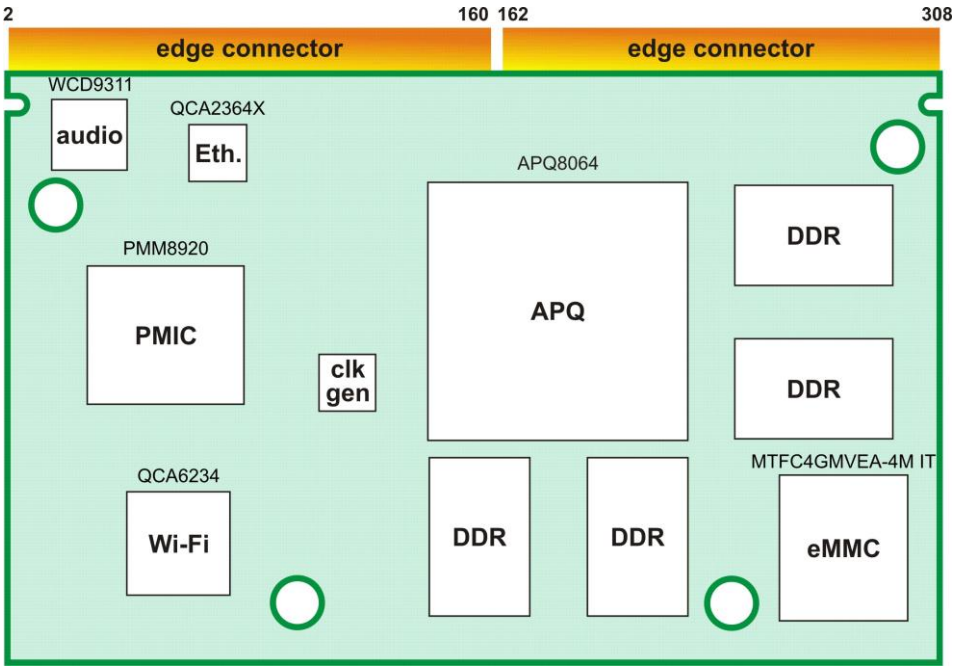

Figure 2-2: Main functional blocks of the SoM

Table 2-1: Main functional blocks

Block	Part Number	Description
APQ	APQ8064	Qualcomm Snapdragon™ 600 1.7 GHz quad Krait™ APQ-8064-0-784FCBGA-TR-02-0-AB
PMIC	PMM8920	Power management IC

Eth	AR8151	PCIe Gigabit Ethernet
Audio	WCD9311	Low-power, stereo audio CODEC, to supply headphones, digital microphone and line OUT I/F
Wi-Fi	QCA6234	Dual-Band 2.4/5.0 GHz IEEE 802.11 a/b/g/n WLAN plus Bluetooth 4.0 combo solution. Supplied by on-board antenna sockets.
DDR		Up to 4GB
eMMC		Up to 64 GB Flash disk
EEPROM	24AA01T-I/LT	Up to 1Kb, I2C EEPROM (I2C1)
Edge connector		Compatible with a standard MXM3.0 314-pin connectors.

3 Main Hardware Components and Interfaces

The VAR-SOM-SD600 supplies a broad selection of interfaces, available mainly via its edge connector. The Wi-Fi and Bluetooth interfaces are supplied via on-SOM antenna connectors.

3.1 SD600 (APQ8064) main Features

- Four Krait application processors, with up to 1.7 GHz, 2 MB L2 cache, TrustZone support, VeNum 128-bit SIMD multimedia coprocessor.
- Powerful QDSP6 core (500 MHz) for application support, within the low-power audio subsystem, 512 kB TCM/L2 memory.
- ARM7 resource and power manager (RPM) processor
- Smart peripheral subsystem (SPS) for improved secure digital (SD) and USB transfer rates
- RPM for improved efficiency

Memory support features

- 64bit , Dual-rank, dual-channel PCDDR3 SDRAM
- Secure Digital supports eMMC Flash

Multimedia features

- High camera resolution—20 MP with inline JPEG
- Mobile Industry Processor Interface (MIPI) support for cameras and displays
- 4-lane primary camera serial interface (CSI); 2-lane secondary CSI; 1-lane 3D CSI
- 4-lane primary display serial interface (DSI); 4-lane secondary DSI

Audio codec via the WCD9311

- I2S busses or SLIMbus
- Up to six digital microphones, two speakers, and seven DACs

Low-power audio (LPA)

- Low complexity, low power dissipation
- 7.1 surround sound
- Versatile post processing
- Supports large variety of audio playback and voice modes
  - Encoders for audio recording and FM recording
  - Many concurrency modes are supported

Audio codecs and audio CMX are supported

- Audio – MP3, AAC, aacPlus, eAAC, AMR-NB, AMR-WB, G.711, WMA 9/10 Pro
- CMX – 128 voices, 512 kB wavetable

Enhanced audio

- Dolby 5.1 and 7.1 Surround (AC-3)

- Fluence™ noise cancellation
- QAudioFX™/QConcert™/QEnsemble

Audio/visual (A/V) outputs

- High Definition Multimedia Interface (HDMI Rev. 1.4a)
- Integrated HDMI Tx core and HDMI PHY
- 1080p at 60 Hz refresh; 24-bit RGB color
- Up to 8-channel audio for 7.1 surround sound
- Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
- HDMI alternate – Mobile Hi-Definition Link (MHL)

Display support – up to two concurrent displays

- Dual display with up to 60 Hz refresh
- Primary via dual-link MIPI DSI, 1 Gbps per lane, up to QXGA (2048 × 1536)
- Secondary via 4-lane MIPI DSI, 1 Gbps per lane, up to QHD (960 × 540)
- Simultaneous dual-display, primary MIPI DSI or LVDS up to QXGA (2048 × 1536), and secondary up to QHD (960 × 540)
- Alternative primary display via dual LVDS, up to QXGA (2048 × 1536)
  - HDMI (see A/V bullets above)
  - TV output via HDMI
  - Color depth: 24-bit pp

3.2 Connectivity Features

- There are seven general serial bus interface (GSBI) ports, each up to 4-bits wide with the configuration options: UART, UIM, I2C, SPI, or GPIO bits
- Universal Serial Bus (USB)—Three USB 2.0 HS ports with built-in PHY (480 Mbps), as a peripheral or embedded host Full-speed USB port for UICC.
- High-speed inter-chip (HSIC)
- PCI Express (PCIe) interface—2.0 port, 1x lane
- SATA interface port

3.3 Audio

The audio interface on the SoM board comprises a Qualcomm WCD9311 CODEC and I2S interface for connecting a DAC, ADC, CODEC etc. The SoM supports audio over Bluetooth through the PCM interface between the APQ8064 and the QCA6234X module.

3.3.1 Audio Features

- I2S busses or Serial Low-power Inter-chip Media bus (SLIMbus)
- Up to two digital microphones, analogue microphone, four line out, and headphones.
- Versatile post processing

- Audio codecs and audio CMX are supported
  - Audio—MP3, AAC, aacPlus, eAAC, AMR-NB, AMR-WB, G.711, WMA 9/10 Pro
  - CMX—128 voices, 512 kB wavetable
- Enhanced audio
  - Dolby 5.1 and 7.1 Surround (AC-3)
  - Fluence™ noise cancellation
  - QAudioFX™/QConcert™/QEnsemble
- Audio/visual (A/V) outputs

The Internal CODEC connections support:

- Stereo single-ended headphone outputs (16 or 32 Ω)
- Four single-ended line outputs (600 Ω)
- Digital microphones
- Electret microphone

3.3.2 WCD9311 Features

The WCD9311 IC is a standalone audio CODEC

- Serial Low-power Inter-chip Media bus (SLIMbus) for access to on-chip digital audio channels with fewer pins relative to inter-IC sound (I2S) bus
- Seven analog input ports and eight analog output ports
- Six digital microphone inputs (three clock/data pairs)
- Sidetone sample rate converter and infinite impulse response (IIR) filters for better performance and lower latency
- 100 dB signal-to-noise ratio (SNR) (minimum) with 2.2 V analog supply and 0 dB gain mode
- SLIMbus interface that supports resolutions of 12, 16, 20, and 24 bits
- Input programmable gain settings of 0, 6, 12, and 18 dB
- Four microphone bias circuits that can be used to power analog and DMICs
- Three independent pulse-code modulation (PCM) rates to support voice, music, and ultrasonic rates concurrently
- ANC path that is selectable from any ADC or digital microphone
- Digital gain control from -80 to +40 dB in 0.5 dB increments, plus mute
- Digital DC blocking filter with a selectable corner frequency of 3, 75, or 150 Hz
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz
- 2 mW stereo record at 48 kHz sample rate
- Stereo single-ended headphone outputs (16 or 32 □)
- Four single-ended line outputs (600 □) (can be used as stereo differential)

- Click and pop suppression:
  - -80 dBVpp A-weighted (maximum) on the headphone outputs
  - -60 dBVpp A-weighted (maximum) on earpiece and line outputs

Table 3-1: Audio signals pin out

# on Edge Connector	Signal Name	GPIO functionality	*Type	Group
21	CDC_IN2_P		AI	CODEC
23	CDC_IN2_N		AI	
22	CDC_HPH_LP		AO	
24	CDC_HPH_REF		PWR	
26	CDC_HPH_RM		AO	
27	CDC_DMIC_BIAS2		PWR	
29	CDC_DMIC_CK0		DO	
31	CDC_DMIC_D0		DI	
33	LINE_OUT4		AO	
35	LINE_OUT3		AO	
34	GPIO_49	SPKR_I2S_DOUT	DIO	External CODEC
209	GPIO_48	SPKR_I2S_WS	DIO	
219	GPIO_50	SPKR_I2S_MCLK_BOOT_CONFIG_1	DIO	
261	GPIO_37	CDC_MIC_I2S_DIN0	DIO	
263	GPIO_35	CDC_MIC_I2S_SCK	DIO	
265	GPIO_36	CDC_MIC_I2S_WS	DIO	
266	GPIO_38	CDC_MIC_I2S_DIN1	DIO	
271	GPIO_47	SPKR_I2S_SCK	DIO	

- For elaboration of the various Types, see chapter 4.5.1

3.4 Camera

The SoM provides two MIPI-CSI camera interfaces, Primary and Secondary, with complementary timing signals, I2C and control signals.

- CSI0 Primary—via 4-lane MIPI_CSI)—supports CMOS and CCD sensors. Up to 20 MP in-line JPEG encode at 15 fps.
  - 60 fps WXGA viewfinder frame rate
  - A wide variety of pixel manipulation, camera modes, image effects, and post-processing techniques are supported, including defective pixel correction
  - VFE raw dump of CSI data at line rate (4 Gbps) to PCDDR3
  - SMIA++ support, plus inter-integrated circuit (I2C) or SPI control
- CSI1 Secondary—via 2-lane MIPI_CSI)—provides webcam functions. Up to 8 MP.
- Additional QCamera features:
  - 3D camera (via 1-lane MIPI_CSI)—up to 8 MP
  - In-line JPEG processing
    - No external RAM requirement for image snapshot processing
    - Reduced shot-to-shot latency for multishot photos video applications
  - Qcamcorder—30 fps at 1080p (H.264/MPEG4); 30 fps at D1 (H.263)
  - Qtv (video decoding)
    - Playback—30 fps at 1080p (H.264/MPEG2/MPEG4/DivX/VC-1); 30 fps at D1 (H.263)
    - Streaming—30 fps at 1080p (H.264/MPEG2/MPEG4/DivX/VC-1); 30 fps at D1 (H.263)
  - Qvideophone (VT)—15 fps at QCIF (MPEG4/H.263)

Table 3-2: Camera signals pin out

# on Edge Connector	Signal Name	GPIO functionality	Type	Group
186	CLK_500M_MIPI_CSI0_P		DS	CSI0
188	CLK_500M_MIPI_CSI0_N		DS	
180	MIPI_CSI0_LANE3_P		DS	
182	MIPI_CSI0_LANE3_N		DS	
177	MIPI_CSI0_LANE2_P		DS	
179	MIPI_CSI0_LANE2_N		DS	
183	MIPI_CSI0_LANE1_P		DS	
185	MIPI_CSI0_LANE1_N		DS	

189	MIPI_CSI0_LANE0_P		DS	
191	MIPI_CSI0_LANE0_N		DS	
198	CLK_500M_MIPI_CSI1_P		DS	CSI1
200	CLK_500M_MIPI_CSI1_N		DS	
204	MIPI_CSI1_LANE1_P		DS	
206	MIPI_CSI1_LANE1_N		DS	
192	MIPI_CSI1_LANE0_P		DS	
194	MIPI_CSI1_LANE0_N		DS	
92	CAM_MCLK0			
203	GPIO_04	CAM_MCLK1_BOOT_CONFIG_6	DIO	CAMERA
280	GPIO_03	FLASH_CTRL_EN0	DIO	
286	GPIO_01	FLASH_NOW	DIO	

3.5 Display

The VAR-SOM- SD600 provides three display interfaces on its edge connector:

- MIPI-DSI
- HDMI
- Dual LVDS

The SoM supports two concurrent displays.

- Dual display with up to 60 Hz refresh rate @ 1080p
  - Primary via dual-link MIPI DSI, 1 Gbps per lane, up to QXGA (2048 × 1536)
  - Secondary via 4-lane MIPI DSI, 1 Gbps per lane, up to QHD (960 × 540)
  - Simultaneous dual-display, primary MIPI DSI or LVDS up to QXGA (2048 × 1536) Secondary display up to QHD (960 × 540)
  - Alternative primary display via dual LVDS, up to QXGA (2048 × 1536)
    - HDMI
    - Color depth: 24-bit pp
    - Types: TFT, LTPS, CSTN, and OLED

3.5.1 MIPI-DSI

- 4-lane primary display serial interface (DSI) via dual-link MIPI DSI, 1 Gbps per lane, up to QXGA (2048 × 1536).
- 4-lane secondary DSI via 4-lane MIPI DSI, 1 Gbps per lane, up to QHD (960 × 540)

Table 3-3: DSI signals pin out

# on Edge Connector	Signal Name	Type	Group
127	CLK_500M_MIPI_DSI0_P	DS	DSI0
129	CLK_500M_MIPI_DSI0_N	DS	
171	MIPI_DSI0_LANE3_P	DS	
173	MIPI_DSI0_LANE3_N	DS	
165	MIPI_DSI0_LANE2_P	DS	
167	MIPI_DSI0_LANE2_N	DS	
174	MIPI_DSI0_LANE1_P	DS	
176	MIPI_DSI0_LANE1_N	DS	
157	MIPI_DSI0_LANE0_P	DS	
159	MIPI_DSI0_LANE0_N	DS	
144	CLK_500M_MIPI_DSI1_P	DS	DSI1
146	CLK_500M_MIPI_DSI1_N	DS	

150	MIPI_DSI1_LANE3_P	DS	
152	MIPI_DSI1_LANE3_N	DS	
168	MIPI_DSI1_LANE2_P	DS	
170	MIPI_DSI1_LANE2_N	DS	
156	MIPI_DSI1_LANE1_P	DS	
158	MIPI_DSI1_LANE1_N	DS	
162	MIPI_DSI1_LANE0_P	DS	
164	MIPI_DSI1_LANE0_N	DS	

3.5.2 HDMI

- 1080p at 60 Hz refresh, 24-bit RGB color high-definition and integrated high-definition multimedia interface
- Up to 8-channel audio for 7.1 surround sound
- Dolby Digital Plus, Dolby True-HD, and DTS-HD Master
- Integrated HDMI Tx core and HDMI PHY

Table 3-4: HDMI signals pin out

# on Edge Connector	Signal Name	GPIO functionality	Type	APQ Pin
97	CLK_165M_HDMI_P		DS	AH14
99	CLK_165M_HDMI_N		DS	AG14
115	HDMI_TX2_P		DS	AB15
117	HDMI_TX2_N		DS	AC15
109	HDMI_TX1_P		DS	AH15
111	HDMI_TX1_N		DS	AG15
103	HDMI_TX0_P		DS	AB14
105	HDMI_TX0_N		DS	AA14

3.5.3 Dual LVDS

The LVDS may be both single and dual channel.

- Alternative primary display via dual LVDS, up to QXGA (2048 × 1536)
- Simultaneous dual-display, primary MIPI DSI or LVDS up to QXGA (2048 × 1536), and secondary up to QHD (960 × 540)

Table 3-5: Dual LVDS signals pin out

# on Edge Connector	Signal Name	Type	APQ Pin
108	CLK_170M_0_LVDS_P	DS	AG11
110	CLK_170M_0_LVDS_N	DS	AH11
114	CLK_170M_1_LVDS_P	DS	AH12
116	CLK_170M_1_LVDS_N	DS	AG12
138	LVDS_TX7_P	DS	AG13
140	LVDS_TX7_N	DS	AH13
132	LVDS_TX6_P	DS	AE13
134	LVDS_TX6_N	DS	AF13
126	LVDS_TX5_P	DS	AC13
128	LVDS_TX5_N	DS	AD13
120	LVDS_TX4_P	DS	AB13
122	LVDS_TX4_N	DS	AC14
151	LVDS_TX3_P	DS	AF11
153	LVDS_TX3_N	DS	AE11
145	LVDS_TX2_P	DS	AD12
147	LVDS_TX2_N	DS	AC11
139	LVDS_TX1_P	DS	AA12
141	LVDS_TX1_N	DS	Y12
133	LVDS_TX0_P	DS	AA11
135	LVDS_TX0_N	DS	Y1

3.6 PCI Express/Ethernet

The VAR-SOM-SD600 is preconfigured with **either** a PCIe **or** Ethernet (PHY) interface.

3.6.1 ETHERNET

The SoM has an optional Gigabit Ethernet LAN Controller with Integrated Transceiver mounted on board. The AR8151L-B combines a 10/100/1000BASE-T GbE media access controller (MAC), a triple-speed Ethernet physical layer transceiver (PHY) and a PCI Express bus interface. In the case of an on-board Ethernet usage the PCIe bus is disconnected from SoM connector.

The AR8151L-B is compliant with IEEE 802.3u specification for 10/100 Mbps Ethernet and IEEE 802.3ab specification for 1000 Mbps Ethernet. The AR8151L-B device combines pulse shaping, Tx/Rx PCS, echo canceller, NEXT canceller, equalizer, decoder, and timing recovery functions to deliver robust signal performance in noisy environments.

The AR8151L-B GbE controller supports checksum offload features for IP, TCP, and UDP, lowering CPU utilization and optimizing network performance.

Table 3-6: PCIe/Ethernet signals pin out

# on Edge Connector	Signal Name	Type	Group
43	PCIE_RX_P_CON	DS	PCIe
45	PCIE_RX_N_CON	DS	
49	PCIE_TX_P_CON	DS	
51	PCIE_TX_N_CON	DS	
55	CLK_100M_PCIE_N	DS	PCI Gen
57	CLK_100M_PCIE_P	DS	PCI Gen.
61	ETH_TRX3_N	DS	Ethernet
63	ETH_TRX3_P	DS	
67	ETH_TRX2_N	DS	
69	ETH_TRX2_P	DS	
73	ETH_TRX1_N	DS	
75	ETH_TRX1_P	DS	
79	ETH_TRX0_N	DS	
81	ETH_TRX0_P	DS	

3.7 SATA

The VAR-SOM-SD600 SoM has one serial ATA (SATA) interface connected from the APQ directly to the edge connector.

Table 3-7: SATA 1.0 port signals pin out

# on Edge Connector	Signal Name	Type	APQ Pin

96	CPU_SATA_RX_P	DS	AG17
98	CPU_SATA_RX_N	DS	AH17
102	CPU_SATA_TX_P	DS	AH16
104	CPU_SATA_TX_N	DS	AG16
121	CLK_100M_CPU_SATA_CLK_P	DS	AF16
123	CLK_100M_CPU_SATA_CLK_N	DS	AE16

3.8 JTAG

The SoM includes a JTAG interface to provide a debug and test control. Seven signals are routed from the APQ directly to the edge connector.

Table 3-8: JTAG signals pin out

# on Edge Connector	Signal Name	Type	APQ Pin
294	CPU_JTAG_RTCK	DO	K21
296	CPU_JTAG_TMS	DI	D25
298	CPU_JTAG_TDI	DI	F24
300	CPU_JTAG_TCK	DI	L21
302	CPU_JTAG_SRST#	DI	D26
304	CPU_JTAG_TDO	DO	D28
306	CPU_JTAG_TRST#	DI	D27

4 Serial Interfaces

The VAR-SOM-SD600 utilizes all seven of the APQ's serial interfaces. Interface number 6 as well as half of interface number 1 are used internally by the SoM. The remaining interfaces can be configured as shown in Table 4-1:

*Table 4-1: Serial interface options – default in **bold***

I/f #	# of Bits	Usage Options (1 only) n/a	UART[1]	I2C[2]	SPI[3]	Comments
1	2	✓	-	-	-	Not user configurable, used as I2C1 internally by SoM
	2	-	✓	-	-	
2	4	-	✓	✓	✓	
3	4	-	✓	✓	✓	
4	4	-	✓	✓	✓	
5	4	-	✓	✓	✓	
6	4	✓	-	-	-	Not user configurable, used as BT-UART internally by SoM
7	2	-	✓	✓	✓	Carrier board uses bits 3 and 2 used for debug UART (no flow control). Bits 1 and 0 are used for I2C7 interface. If the debug interface is not used, the channel may be configured to any mode.
	2	-				

[1] EIA RS232-C

[2] II2C Specification, version 2.1, January 2000 (Philips Semiconductor document number 9398 393 40011)
Not supported: High-speed mode (3.4 Mbps), 10-bit addressing, Fast mode plus (1 Mbps)

[3] Master only. Max SPI clock frequency 52 MHz.

*Table 4-2: Detailed serial interface pin outs – default in **bold***

No.	Serial Channel/bit	4-pin UART	4-pin SPI	3-pin UIM + GPIO	I2C + 2-pin UART	UIM + I2C	4 GPIOs
282	GSBI1[2]_GPIO_19	UART_TX	-	-		-	GPIO_19
284	GSBI1[3]_GPIO_18	UART_RX	-	-		-	GPIO_18
275	GSBI2[3]_GPIO_22	**UART_TX**	SPI_CLK	GPIO_25	I2C_SCL	I2C_SCL	GPIO_22
277	GSBI2[2]_GPIO_23	**UART_RX**	SPI_CS_N	UIM_RESET_N	I2C_SDA	I2C_SDA	GPIO_23
279	GSBI2[1]_GPIO_24	**UART_CTS**	SPI_DATA_MISO	UIM_CLK	UART_RX	UIM_CLK	GPIO_24
281	GSBI2[0]_GPIO_25	**UART_RTS**	SPI_DATA_MOSI	UIM_DATA	UART_TX	UIM_DATA	GPIO_25
229	GSBI3[3]_GPIO_6	UART_TX	SPI_DATA_MOSI	UIM_DATA	**UART_TX**	UIM_DATA	GPIO_6
227	GSBI3[2]_GPIO_7	UART_RX	SPI_DATA_MISO	UIM_CLK	**UART_RX**	UIM_CLK	GPIO_7
223	GSBI3[1]_GPIO_08	UART_CTS	SPI_CS_N	UIM_RESET_N	**I2C_SDA**	I2C_SDA	GPIO_08
225	GSBI3[0]_PIO_09	UART_RTS	SPI_CLK	GPIO_25	**I2C_SCL**	I2C_SCL	GPIO_09
289	GSBI4[3]_GPIO_10	UART_TX	SPI_DATA_MOSI	UIM_DATA	**UART_TX**	UIM_DATA	GPIO_10
291	GSBI4[2]_GPIO_11	UART_RX	SPI_DATA_MISO	UIM_CLK	**UART_RX**	UIM_CLK	GPIO_11
285	GSBI4[1]_GPIO_12	UART_CTS	SPI_CS_N	UIM_RESET_N	**I2C_SDA**	I2C_SDA	GPIO_12
287	GSBI4[0]_GPIO_13	UART_RTS	SPI_CLK	GPIO_25	**I2C_SCL**	I2C_SCL	GPIO_13
254	GSBI5[3]_GPIO_51	**UART_TX**	SPI_DATA_MOSI	UIM_DATA	UART_TX	UIM_DATA	GPIO_51
256	GSBI5[2]_GPIO_52	**UART_RX**	SPI_DATA_MISO	UIM_CLK	UART_RX	UIM_CLK	GPIO_52
211	GSBI5[1]_GPIO_53	**UART_CTS**	SPI_CS_N	UIM_RESET_N	I2C_SDA	I2C_SDA	GPIO_53
36	GSBI5[0]_GPIO_54	**UART_RTS**	SPI_CLK	GPIO_25	I2C_SCL	I2C_SCL	GPIO_54
255	GSBI7[3]_GPIO_82	UART_TX	SPI_DATA_MOSI	UIM_DATA	**UART_TX**	UIM_DATA	GPIO_82
253	GSBI7[2]_GPIO_83	UART_RX	SPI_DATA_MISO	UIM_CLK	**UART_RX**	UIM_CLK	GPIO_83
251	GSBI7[1]_GPIO_84	UART_CTS	SPI_CS_N	UIM_RESET_N	**I2C_SDA**	I2C_SDA	GPIO_84
249	GSBI7[0]_GPIO_85	UART_RTS	SPI_CLK	GPIO_25	**I2C_SCL**	I2C_SCL	GPIO_85

4.1 USB

The VAR-SOM-SD600 SoM provides three USB 2.0 HS ports with built-in PHY (480 Mbps) and one HSIC port. USB1 is used as OTG, and USB3 and USB4 are used as host interfaces. USB2 port is routed via HSIC to the edge connector.

Universal Serial Bus (USB) implementation features:

- Three USB 2.0 HS ports with built-in PHY (480 Mbps), as a peripheral or embedded host
- High-speed inter-chip (HSIC)

Table 4-3: USB signals pin out

# on Edge Connector	Signal Name	GPIO functionality	Type	Group

17	USB1_VBUS_IN_CONN		PWR	USB OTG
195	CPU_USB1_ID		DI	USB1
197	USB_PORT1_ID		DI	
220	CPU_USB1_D_P		DS	
222	CPU_USB1_D_N		DS	
232	CPU_USB3_D_P		DS	USB3
234	CPU_USB3_D_N		DS	
299	USB_PORT3_VBUS		PWR	
226	CPU_USB4_D_P		DS	USB4
228	CPU_USB4_D_N		DS	
301	USB_PORT4_VBUS		PWR	
288	GPIO_88	USB2_HSIC _STROBE	DIO	USB2_HSIC
290	GPIO_89	USB2_HSIC _DATA	DIO	

4.2 Secure Digital

The VAR-SOM-SD600 SoM provides four secure digital controller (SDC) ports.

- SDC1: eMMC Flash memory support
- SDC2: Optional. Supports 1.8 voltage interface. It may be used for MMC, SD card, eMMC and eSD connections or a GPIO function. Routed to edge connector
- SDC3: support dual-voltage (1.8 V and 2.9 V) SD card interface. Routed to edge connector
- SDC4: WLAN on-board support for both SD version 3.0 and MMC version 4.4.1/4.5

Table 4-4: SD signals pin out

# on Edge Connector	Signal Name	GPIO functionality	Type	Group
235	GPIO_57	SDC2_CMD	DIO	SDC2
237	GPIO_59	SDC2_CLK		
239	GPIO_58	SDC2_DAT3		
241	GPIO_60	SDC2_DAT2		
243	GPIO_61	SDC2_DAT1		
245	GPIO_62	SDC2_DAT0		
238	SDC3_CMD		DIO	SDCARD
248	SDC3_CLK			

246	SDC3_DAT3			
240	SDC3_DAT2			
250	SDC3_DAT1			
244	SDC3_DAT0			

4.3 APQ8064 GPIOs

The VAR-SOM-SD600 provides IO pins for use as GPIOs.

GPIO features of the APQ8064 are as follows:

- 90 GPIO pins (GPIO_0 to GPIO_89)
- Input configurations: pull-up, pull-down, keeper, or no-pull
- Output configurations: programmable drive current

4.3.1 GPIO Function Configuration

GPIO pins can support multiple functions. To assign GPIOs to a particular function, you must identify all of the application's requirements and map each GPIO to its function, to avoid conflicts in GPIO assignments.

Table 4-5: APQ8064 GPIO signals pin out

# on e.c	Signal Name	GPIO functionality	Type	Group
86	GPIO_72	HDMI_HPD#	DIO	HDMI
91	GPIO_71	HDMI_DDC_DATA	DIO	HDMI
92	GPIO_05	CAM_MCLK0	DIO	Camera
93	GPIO_70	HDMI_DDC_CLK	DIO	HDMI
203	GPIO_04	CAM_MCLK1_BOOT_CONFIG_6	DIO	Camera
207	GPIO_56	FLASH_CTRL_EN1	DIO	
209	GPIO_48	SPKR_I2S_WS	DIO	EX.CODEC
211	GSBI5[1]_GPIO_53		DIO	GSBI5
217	GPIO_87	BOOT_CONFIG_0	DIO	BOOT
219	GPIO_50	BOOT_CONFIG_1	DIO	EX.CODEC
231	GPIO_26	TS_PENIRQ_N	DIO	TOUCH
227	GSBI3[2]_GPIO_7	TS_EOC	DIO	
229	GSBI3[3]_GPIO_6	TS_SSBI	DIO	

# on e.c	Signal Name	GPIO functionality	Type	Group
223	GSBI3[1]_GPIO_08	I2C3_SDA	DIO	GSBI3
225	GSBI3[0]_GPIO_09	I2C3_SCL	DIO	GSBI3
235	GPIO_57	SDC2_CMD	DIO	SDC
237	GPIO_59	SDC2_CLK	DIO	
239	GPIO_58	SDC2_DAT3	DIO	
241	GPIO_60	SDC2_DAT2	DIO	
243	GPIO_61	SDC2_DAT1	DIO	
245	GPIO_62	SDC2_DAT0	DIO	
242	GPIO_29	SD_CARD3_DET#	DIO	SDC
249	GSBI7[0]_GPIO_85		DIO	GSBI7
251	GSBI7[1]_GPIO_84		DIO	
253	GSBI7[2]_GPIO_83		DIO	GSBI7
254	GSBI5[3]_GPIO_51		DIO	GSBI5
255	GSBI7[3]_GPIO_82		DIO	GSBI7
256	GSBI5[2]_GPIO_52		DIO	GSBI5
259	GPIO_0		DIO	GPIO
260	GPIO_77	V3P3_BOOST_EN	DIO	PWR CTR
261	GPIO_37	CDC_MIC_I2S_DIN0	DIO	Audio
262	GPIO_34	CAM1_RST#	DIO	Camera
263	GPIO_35	CDC_MIC_I2S_SCK	DIO	Audio
264	GPIO_69	HDMI_CEC	DIO	HDMI
265	GPIO_36	CDC_MIC_I2S_WS	DIO	Audio
266	GPIO_38	CDC_MIC_I2S_DIN1	DIO	Audio
271	GPIO_47	SPKR_I2S_SCK	DIO	Audio
275	GSBI2[3]_GPIO_22		DIO	GSBI2
276	GPIO_28	SD_CARD2_DET#	DIO	SDC
277	GSBI2[2]_GPIO_23		DIO	UART2
280	GPIO_03	FLASH_CTRL_EN0	DIO	CAMERA
281	GSBI2[0]_GPIO_25		DIO	GSBI2
282	GSBI1[2]_GPIO_19		DIO	GSBI1
284	GSBI1[3]_GPIO_18		DIO	GSBI1
285	GSBI4[1]_GPIO_12		DIO	CAMERA
286	GPIO_01	FLASH_NOW	DIO	
287	GSBI4[0]_GPIO_13		DIO	
288	GPIO_88	USB2_HSIC_STROBE	DIO	USB HSIC
289	GSBI4[3]_GPIO_10		DIO	CAMERA

# on e.c	Signal Name	GPIO functionality	Type	Group
290	GPIO_89	USB2_HSIC_DATA	DIO	USB HSIC
291	GSBI4[2]_GPIO_11		DIO	CAMERA
307	GPIO_33	EXP_GPIO_33_CON	DIO	

Table 4-6: GPIO PMIC signals pin out

# on e.c	Signal Name	GPIO functionality	Type	Group
58	PMIC_GPIO_31	CAM0_STANDBY	DIO	
60	PMIC_GPIO_28	CAM0_RST#	DIO	
62	PMIC_GPIO_42		DIO	
64	PMIC_GPIO_5		DIO	
66	PMIC_GPIO_18		DIO	
70	PMIC_GPIO_26	BACKLIGHT_PWM_EN	PWM	DISPLAY
72	PMIC_GPIO_20		DIO	
74	PMIC_GPIO_27	TS_LDO_EN	DIO	
76	PMIC_GPIO_30	TS_XRES	DIO	
78	PMIC_GPIO_36	DISP_PWR_EN_N	DIO	
90	PMIC_GPIO_19		DIO	
199	PMIC_GPIO_32	USB3_PWR_FAULT_N	DIO	USB3
201	PMIC_GPIO_38	USB4_PWR_FAULT_N	DIO	USB4
205	PMIC_GPIO_23	CAM1_STANDBY	DIO	Camera
213	PMIC_GPIO_07	5V_BOOST_EN	DIO	PWR CTR
215	PMIC_GPIO_40	PCIE_CLK_PWR_EN	DIO	PCIe
230	PMIC_GPIO_37	USB3_PWR_EN	DIO	USB
268	PMIC_GPIO_29	UIM1_M_CLK	DIO	

4.4 Wi-Fi and Bluetooth

The VAR-SOM-SD600 SoM includes a QCA6234 Integrated Dual-Band 802.11 a/b/g/n WLAN + Bluetooth 4.0, Class 1.5 module, optimized for low-power.

The QCA6234 integrates the complete transmit/receive RF paths including baluns, switches, and reference oscillator. The device is also pre-calibrated, eliminating the need for customer production calibration.

Near zero power consumption in idle and stand-by enables users to leave WLAN and BT "always on."

The QCA6234 is a System in Package (SiP) small form factor IEEE 802.11 a/b/g/n MAC/baseband/radio optimized+BT4.0 for low-power mobile applications.

4.4.1 QCA6234 Features

- Two stream (2x2) 802.11n provides highest throughput and superior RF performance for handheld devices
- Advanced 2x2 802.11n features:
  - 40MHz channels at 5GHz
  - Space Time Block Coding (STBC) Rx for improved downlink robustness over range
  - Low Density Parity Check (LDPC) encoding for improved uplink and downlink robustness over range
  - Maximum Ratio Combining (MRC)
  - Maximum Likelihood (ML) Decoder
- Supports popular interfaces used in embedded designs:
  - SDIO 2.0 (50MHz, 4-bit and 1-bit) for WLAN
  - USB/HSIC for WLAN
  - High-speed UART (up to 4 Mbps)
  - Bluetooth low energy (BT4.0) ready
  - Class 1.5 Bluetooth with integrated Tx/Rx switch
- All WLAN RF transmitters are pre-calibrated
- Near zero power consumption in idle and stand-by enables users to leave WLAN and BT "always on."
- Advanced BT/WLAN coexistence and concurrent RX for superior rate-over-range and very low latency.
- Best in class Rx sensitivity for superior throughput rate-over-range performance
- Integrated Sleep Clock eliminates the need for expensive bulky 32 kHz real-time clock

4.5 Edge Connector

The VAR-SOM-SD600 SoM exposes a 314-pin MXM 3.0 PCB edge connector.

Recommended Mating connector for baseboard interfacing is JAE MM70-314-310B1-x or FOXCONN AS0B82x-S55x-xH_317-AP00-1743_A, or a mechanical and electrical equivalent.

4.5.1 Signal Types

The signal types in the following section are as follows:

Table 4-7: Signals types

Type	Description
DI	Digital Input (CMOS)
DO	Digital Output (CMOS)
DIO	Digital Input / Output
DS	Differential Signal

Type	Description
AO	Analog Output
AI	Analog Input
AIO	Analog Input / Output
PWR	Power

Table 4-8: Edge connector signals pin out

No.	Signal Name	Alternate Function	Type
1	VPH		PWR
2	GND		PWR
3	VPH		PWR
4	GND		PWR
5	VPH		PWR
6	GND		PWR
7	GND		PWR
8	GND		PWR
9	GND		PWR
10	GND		PWR
11	V5P0_VREG_OTG		PWR
12	VCOIN		PWR
13	VREG_5V		PWR
14	V2P8_VREG_L16		PWR
15	V2P95_VREG_L6		PWR
16	V1P8_VREG_S4		PWR
17	USB1_VBUS_IN_CONN		PWR
18	V1P8_VREG_L23		PWR
19	GND		PWR
20	GND		PWR
21	CDC_IN2_P		AI
22	CDC_HPH_LP		AO
23	CDC_IN2_N		AI
24	CDC_HPH_REF		PWR
25	GND		PWR
26	CDC_HPH_RM		AO
27	CDC_DMIC_BIAS2		PWR
28	GND		PWR
29	CDC_DMIC_CK0		DO
30	GPIO_30	SPI5_CS1A	DIO
31	CDC_DMIC_D0		DI
32	GPIO_32	SPI5_CS3A	DIO
33	LINE_OUT4		AO
34	GPIO_49	SPKR_I2S_DOUT	DIO
35	LINE_OUT3		AO

No.	Signal Name	Alternate Function	Type
36	GSBI5[0]_GPIO_54		DIO
37	LINE_OUT2		AO
38	PMIC_ GPIO_33		DIO
39	LINE_OUT1		AO
40	PMIC_GPIO_35		DIO
41	GND		PWR
42	NC		
43	PCIE_RX_P_CON		DS
44	GND		PWR
45	PCIE_RX_N_CON		DS
46	V1P7_ETH_VDDCT		PWR
47	GND		PWR
48	V3P075_VREG_L3		PWR
49	PCIE_TX_P		DS
50	NC		
51	PCIE_TX_N		DS
52	PMIC_GPIO_06	PCIE_WAKE#	DIO
53	GND		PWR
54	GSBI1[0]_GPIO_21		DIO
55	CLK_100M_PCIE_N		DS
56	GSBI1[1]_GPIO_20		DIO
57	CLK_100M_PCIE_P		DS
58	PMIC_GPIO_31	PCIE_WAKE#	DIO
59	GND		PWR
60	PMIC_GPIO_28	CAM0_RST#	DIO
61	ETH_TRX3_N		DS
62	PMIC_GPIO_42 [2]		DIO
63	ETH_TRX3_P		DS
64	PMIC_GPIO_5		DIO
65	GND		PWR
66	PMIC_GPIO_18		DIO
67	ETH_TRX2_N		DS
68	GND		PWR
69	ETH_TRX2_P		DS
70	PMIC_GPIO_26	BACKLIGHT_PWM_EN	PWM

No.	Signal Name	Alternate Function	Type
71	GND		PWR
72	PMIC_GPIO_20		DIO
73	ETH_TRX1_N		DS
74	PMIC_GPIO_27	TS_LDO_EN	DIO
75	ETH_TRX1_P		DS
76	PMIC_GPIO_30	TS_XRES	DIO
77	GND		PWR
78	PMIC_GPIO_36	DISP_PWR_EN_N	DIO
79	ETH_TRX0_N		DS
80	PMIC_MPP_8821_02	DISP_RST#	
81	ETH_TRX0_P		DS
82	NC		
83	GND		PWR
84	PMIC_LED_DRV0_N		DIO
85	PWRBTN#		DI
86	GPIO_72	HDMI_HPD#	DIO
87	RSTBTN#		DI
88	PMIC_VIB_DRV_N		PWM
89	GND		PWR
90	PMIC_GPIO_19		DIO
91	GPIO_71		DIO
92	CAM_MCLK0		DIO
93	GPIO_70	HDMI_DDC_CLK	DIO
94	GND		PWR
95	GND		PWR
96	CPU_SATA_RX_P		DS
97	CLK_165M_HDMI_P		DS
98	CPU_SATA_RX_N		DS
99	CLK_165M_HDMI_N		DS
100	GND		PWR
101	GND		PWR
102	CPU_SATA_TX_P		DS
103	HDMI_TX0_P		DS
104	CPU_SATA_TX_N		DS
105	HDMI_TX0_N		DS

No.	Signal Name	Alternate Function	Type
106	GND		PWR
107	GND		PWR
108	CLK_170M_0_LVDS_P		DS
109	HDMI_TX1_P		DS
110	CLK_170M_0_LVDS_N		DS
111	HDMI_TX1_N		DS
112	GND		PWR
113	GND		PWR
114	CLK_170M_1_LVDS_P		DS
115	HDMI_TX2_P		DS
116	CLK_170M_1_LVDS_N		DS
117	HDMI_TX2_N		DS
118	GND		PWR
119	GND		PWR
120	LVDS_TX4_P		DS
121	CLK_100M_CPU_SATA_P		DS
122	LVDS_TX4_N		DS
123	CLK_100M_CPU_SATA_N		DS
124	GND		PWR
125	GND		PWR
126	LVDS_TX5_P		DS
127	CLK_500M_MIPI_DSI0_P		DS
128	LVDS_TX5_N		DS
129	CLK_500M_MIPI_DSI0_N		DS
130	GND		PWR
131	GND		PWR
132	LVDS_TX6_P		DS
133	LVDS_TX0_P		DS
134	LVDS_TX6_N		DS
135	LVDS_TX0_N		DS
136	GND		PWR
137	GND		PWR
138	LVDS_TX7_P		DS
139	LVDS_TX1_P		DS
140	LVDS_TX7_N		DS

No.	Signal Name	Alternate Function	Type
141	LVDS_TX1_N		DS
142	GND		PWR
143	GND		PWR
144	CLK_500M_MIPI_DSI1_P		DS
145	LVDS_TX2_P		DS
146	CLK_500M_MIPI_DSI1_N		DS
147	LVDS_TX2_N		DS
148	GND		PWR
149	GND		PWR
150	MIPI_DSI1_LANE3_P		DS
151	LVDS_TX3_P		DS
152	MIPI_DSI1_LANE3_N		DS
153	LVDS_TX3_N		DS
154	GND		PWR
155	GND		PWR
156	MIPI_DSI1_LANE1_P		DS
157	MIPI_DSI0_LANE0_P		DS
158	MIPI_DSI1_LANE1_N		DS
159	MIPI_DSI0_LANE0_N		DS
160	GND		PWR
161	GND		PWR
162	MIPI_DSI1_LANE0_P		DS
163	GND		PWR
164	MIPI_DSI1_LANE0_N		DS
165	MIPI_DSI0_LANE2_P		DS
166	GND		PWR
167	MIPI_DSI0_LANE2_N		DS
168	MIPI_DSI1_LANE2_P		DS
169	GND		PWR
170	MIPI_DSI1_LANE2_N		DS
171	MIPI_DSI0_LANE3_P		DS
172	GND		PWR
173	MIPI_DSI0_LANE3_N		DS
174	MIPI_DSI0_LANE1_P		DS
175	GND		PWR

No.	Signal Name	Alternate Function	Type
176	MIPI_DSI0_LANE1_N		DS
177	MIPI_CSI0_LANE2_P		DS
178	GND		PWR
179	MIPI_CSI0_LANE2_N		DS
180	MIPI_CSI0_LANE3_P		DS
181	GND		PWR
182	MIPI_CSI0_LANE3_N		DS
183	MIPI_CSI0_LANE1_P		DS
184	GND		PWR
185	MIPI_CSI0_LANE1_N		DS
186	CLK_500M_MIPI_CSI0_P		DS
187	GND		PWR
188	CLK_500M_MIPI_CSI0_N		DS
189	MIPI_CSI0_LANE0_P		DS
190	GND		PWR
191	MIPI_CSI0_LANE0_N		DS
192	MIPI_CSI1_LANE0_P		DS
193	GND		PWR
194	MIPI_CSI1_LANE0_N		DS
195	CPU_USB1_ID		DI
196	GND		PWR
197	USB_PORT1_ID		DI
198	CLK_500M_MIPI_CSI1_P		DS
199	PMIC_GPIO_32	USB3_PWR_FAULT_N	DIO
200	CLK_500M_MIPI_CSI1_N		DS
201	PMIC_GPIO_38	USB4_PWR_FAULT_N	DIO
202	GND		PWR
203	GPIO_04	CAM_MCLK1_BOOT_CONFIG_6	DIO
204	MIPI_CSI1_LANE1_P		DS
205	PMIC_GPIO_23	CAM1_STANDBY	DIO
206	MIPI_CSI1_LANE1_N		DS
207	GPIO_56	FLASH_CTRL_EN1	DIO
208	USB3_TX		DS
209	GPIO_48	SPKR_I2S_WS	DIO
210	USB3_TY		DS

No.	Signal Name	Alternate Function	Type
211	GSBI5[1]_GPIO_53		DIO
212	GND		PWR
213	PMIC_GPIO_07	5V_BOOST_EN	DIO
214	USB3_RX		DS
215	PMIC_GPIO_40	PCIE_CLK_PWR_EN	DIO
216	USB3_RY		DS
217	GPIO_87	BOOT_CONFIG_0	DIO
218	GND		PWR
219	GPIO_50	SPKR_I2S_MCLK_BOOT_CONFIG_1	DIO
220	CPU_USB1_D_P		DS
221	GND		PWR
222	CPU_USB1_D_N		DS
223	GSBI3[1]_GPIO_08		DIO
224	PMIC_GPIO_22	USB4_PWR_EN	DIO
225	GSBI3[0]_GPIO_09		DIO
226	CPU_USB4_D_P		DS
227	GSBI3[2]_GPIO_7	TS_EOC	DIO
228	CPU_USB4_D_N		DS
229	GSBI3[3]_GPIO_6	TS_SSBI	DIO
230	PMIC_GPIO_37		DIO
231	GPIO_26	TS_PENIRQ_N	DIO
232	CPU_USB3_D_P		DS
233	GND		PWR
234	CPU_USB3_D_N		DS
235	GPIO_57	SDC2_CMD	DIO
236	GND		PWR
237	GPIO_59	SDC2_CLK	DIO
238	SDC3_CMD		DIO
239	GPIO_58	SDC2_DAT3	DIO
240	SDC3_DAT2		DIO
241	GPIO_60	SDC2_DAT2	DIO
242	GPIO_29	SD_CARD3_DET#	DIO
243	GPIO_61	SDC2_DAT1	DIO
244	SDC3_DAT0		DIO
245	GPIO_62	SDC2_DAT0	DIO

No.	Signal Name	Alternate Function	Type
246	SDC3_DAT3		DIO
247	GND		PWR
248	SDC3_CLK		DIO
249	GSBI7[0]_GPIO_85		DIO
250	SDC3_DAT1		DIO
251	GSBI7[1]_GPIO_84		DIO
252	GND		PWR
253	GSBI7[2]_GPIO_83		DIO
254	GSBI5[3]_GPIO_51		DIO
255	GSBI7[3]_GPIO_82		DIO
256	GSBI5[2]_GPIO_52		DIO
257	GND		PWR
258	GND		PWR
259	GPIO_0		DIO
260	GPIO_77	V3P3_BOOST_EN	DIO
261	GPIO_37	CDC_MIC_I2S_DIN0	DIO
262	GPIO_34	CAM1_RST#	DIO
263	GPIO_35	CDC_MIC_I2S_SCK	DIO
264	GPIO_69	HDMI_CEC	DIO
265	GPIO_36	CDC_MIC_I2S_WS	DIO
266	GPIO_38	CDC_MIC_I2S_DIN1	DIO
267	GND		PWR
268	PMIC_GPIO_29	PMIC_UIM1_M_CLK	DIO
269	NC		
270	ETH_LED0		DO
271	GPIO_47	SPKR_I2S_SCK	DIO
272	ETH_LED1		DO
273	GND		PWR
274	ETH_LED2		DO
275	GSBI2[3]_GPIO_22		DIO
276	GPIO_28	SD_CARD2_DET#	DIO
277	GSBI2[2]_GPIO_23		DIO
278	GND		PWR
279	GSBI2[1]_GPIO_24		DIO
280	GPIO_03	FLASH_CTRL_EN0	DIO

No.	Signal Name	Alternate Function	Type
281	GSBI2[0]_GPIO_25		DIO
282	GSBI1[2]_GPIO_19		DIO
283	GND		PWR
284	GSBI1[3]_GPIO_18		DIO
285	GSBI4[1]_GPIO_12		DIO
286	GPIO_01	FLASH_NOW	DIO
287	GSBI4[0]_GPIO_13		DIO
288	GPIO_88	USB2_HSIC_STROBE	DIO
289	GSBI4[3]_GPIO_10		DIO
290	GPIO_89	USB2_HSIC_DATA	DIO
291	GSBI4[2]_GPIO_11		DIO
292	GND		PWR
293	GND		PWR
294	CPU_JTAG_RTCK		DO
295	V3P3V		PWR
296	CPU_JTAG_TMS		DI
297	V3P3V		PWR
298	CPU_JTAG_TDI		DI
299	USB_PORT3_VBUS		AI
300	CPU_JTAG_TCK		DI
301	USB_PORT4_VBUS		AI
302	CPU_JTAG_SRST#		DI
303	JTAG_PS_HOLD		DI
304	CPU_JTAG_TDO		DO
305	NC		
306	CPU_JTAG_TRST#		DI
307	EXP_GPIO_33_CON		IO
308	GND		PWR
309	CPU_RESOUT_N		DO
311	GND		PWR

The edge connector table includes default state that make the SoM compatible with the Variscite Carrier board. A user can change the definition of some pins in conformity with Pin Mux tables as it appears in this data sheet.

5 Boot Sequence

Two pins on the SoM set up the boot sequence options of the VAR-SOM-SD600, these are:

Table 5-1: Boot sequence configuration

Pin 217 GPIO_87	Pin 219 GPIO_50	Boots from:
0	0	SD, USB
0	1	SD, eMMC
1	0	SD, SD2
1	1	eMMC

The selection is preconfigured when you order the SoM.

The optional carrier board has two switches that enable user selection of the boot source:

- SW1 / GPIO_87
- SW2 / GPIO_50

6 Clock and Reset Architecture

6.1 Clock Distribution

The SoM has several onboard system clocks sources and interconnection:

- 27MHz crystal of APQ8064
- 19MHz oscillator of PMM8920
- 32.768kHz of PMM8920
- 25MHz of PCIe Generator

7 Power

7.1 Power Management

The SoM includes the PMM8920 PMIC that generates the required power domains for the APQ chip. The PMIC functionality is partitioned into five major blocks to simplify discussion:

- Input power management
- Output power management
- General housekeeping
- User interfaces
- IC interfaces.

7.2 Power Domains

- The PMIC on SOM is supplied with DC Input 3.0V÷4.3V from a Li-Ion/Polymer battery or Power supply.
- USB OTG power input is supplied with DC 5.0V±5%. Net VREG_5V, J1 pin 13

Table 7-1: Connector power supplies pinout

# on e.c	Signal Name	Type	Max[V]	Min[V]	Description
1, 2, 3, 4, 5, 6	VPH	PWR In	4.3	3.0	PMIC Supply voltage.
295, 297	V3P3V		3.46	3.14	Supply voltage for WLAN module, Ethernet controller and PCIe clock generator.
13	VREG_5V		5.25	4.35	USB OTG power input.
12	VCOIN		3.25	2.0	RTC
11	V5P0_VREG_OTG	PWR Out	5.25	4.75	500mA max.
15	V2P95_VREG_L6		2.8	3.1	600mA
14	V2P8_VREG_L16		2.95	2.66	150mA
16	V1P8_VREG_S4		1.85	1.75	1500ma
18	V1P8_VREG_L23		1.85	1.75	150mA
46	V1P7_ETH_VDDCT		1.45	1.31	10Ma

Table 7-2: Connector Digital Ground pin out

# on edge connector	Signal Name	Type
7, 8, 9, 10, 19, 20, 25, 28, 41, 44, 47, 53, 59, 65, 68, 71, 77, 83, 89, 94, 95, 100, 101, 106, 107, 112, 113, 118, 119, 124, 125, 130, 131, 136, 137, 142, 143, 148, 149, 154, 155, 160, 161, 163, 166, 169, 172, 175, 178, 181, 184, 187, 190, 193, 196, 202, 208, 218, 221, 233, 236, 247, 252, 257, 258, 267, 273, 278, 283, 292, 293, 308, 311	GND	PWR

7.3 Power Consumption

Table 7-3: Max APQ power consumption

Task	SoM VPH=3.7V [mW]
Idle (~10% CPU) @ 400MHz	92
FHD Video playback	644
100% CPU Dhrystone test—Quad core	~3Watt

Table 7-4: Max Peripheral power usage

Task	SoM V3P3V @3.3V [mW]
WLAN transmission	1,388
AR8151 PCIe to Ethernet IC (1000Mbps active)	319.4

8 Absolute Maximum Ratings

8.1 Voltages

Table 8-1: Absolute maximum voltage ratings

Power Supply	Min	Max	Unit
Main Power Supply, VPH	2.7	4.5	V
Supply for on SoM components	3	3.6	V

WARNING: Stresses above those listed as absolute maximum ratings may cause permanent damage. Functionality AT or ABOVE these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

9 DC Electrical Specifications

9.1 Normal Operational Conditions

Unless otherwise specified, all DC and AC specifications in this data sheet are valid for the following voltages ranges.

Table 99-1: typical voltage ratings

Power Supply	Min	Max	Unit
Main Power Supply, VPH one cell Li-Io battery	3	4.3	V
Supply for on SoM components	3.135	3.465	V

Table 99-2: Digital I/O characteristics for VDD_P3 =VDD_P4 = 1.8 V nominal

Parameter	Min	Max	Unit	Group
VIH	1.2	2.1	V	GSBI, Peripheral I/Os, EMMC, EEPROM, JTAG, CODEC digital I/Os, QCA6234X digital I/Os.
VIL	-0.3	0.63	V	
VOH	1.4	1.8	V	
VOL	0	0.45	V	

Table 99-3: Digital I/O characteristics for VDD_P2 = 2.85 V nominal

Parameter	Min	Max	Unit	Group
VIH	1.9	3.15	V	SD card interface
VIL	-0.3	0.9975	V	
VOH	2.4	2.85	V	
VOL	0	0.45	V	

Table 99-4: APQ-specific USBPHY specifications

Parameter	Min	Max	Unit	Group
VIH	1.27	-	V	USB Interface
VIL	-	0.6	V	

Table 99-5: Audio codec analog I/O characteristics

Parameter	Min	Max	Unit	Comment
HPH output	26.4	33.3	mW	16 OHm load
	25.8	33.1	mW	32OHm load
LINE output	0.47	0.53	V	Full-scale output voltage
	0.80	0.90	V	Output common mode voltage
		1M	Ohm	Output load Single ended
Microphone bias voltage	1.70	2.85	V	Normal operation
Microphone bias current		3.0	mA	Two microphone loads of 1 to 1.5 mA each
Analog Max. input voltage	0.47	0.53	Vrms	Single-ended , through AUX_PGA

10 Mechanical Specifications

10.1 Package Description

10.1.1 Approved Materials

All materials and components to be used in the system are RoHS compliant.

10.1.2 SOM Mounting Holes

The SoM has four mounting holes. The required bolts, spacers, washers, and nuts in order to mount the SoM to the carrier board or the custom hardware, are attached in the development kit. On the top side of the SoM, a heat plate could be assembled on the same mounting holes.

10.1.3 SoM Mounting Dimensions

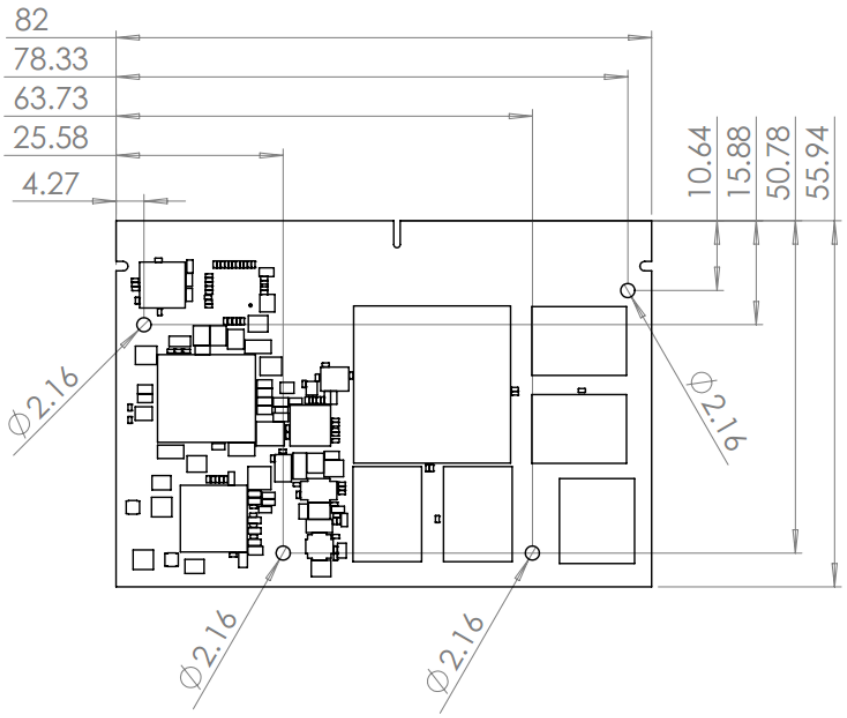

Figure 10-1: SoM mounting dimensions (mm)

11 Thermal and Environmental Specifications

The SoM has two assembly options to provide different temperature compliance:

- **Commercial**—ICs used will withstand temperature range of: 0°C to +70°C
- **Extended** —ICs used will withstand temperature range of: -20°C to +85°C
  This product is designed to operate over a wide temperature range when used with a heat sink and is suited for industrial applications such as outside plant equipment.

11.1 Heat Spreader

The VAR-SOM-SD600, based on the Qualcomm SD600, is a high-performance SOM.

Most applications use the 1.7 GHz at bursts of a few seconds, upon demand. In such case there is no need for special thermal heat dissipation or heat spreader.

The heat spreader is used only for applications that continuously utilize the 1.7 GHz quad core at 100% CPU utilization. In this scenario the SoM may require the use of a heat spreader.

The heat spreader can be used for mounting a proprietary heat sink or spreading the heat in any other way. It is fitted on the VAR-SOM-SD600 board top side. By thermally coupling the SD600 SoC to a relatively large aluminum plain, the time period in which the VAR-SOM-DS600 can operate in a very high frequency can be extended significantly.

As part of the end-product thermal design, the customer can:

- Use the heat spreader as is. Variscite can deliver the heat spreader in high volumes.
- Mount a heat sink on top of the heat spreader or thermally connect it to the device casing to improve heat dissipation.
- Design a custom head spreader. All the CAD data required for such a design is available on Variscite web site.

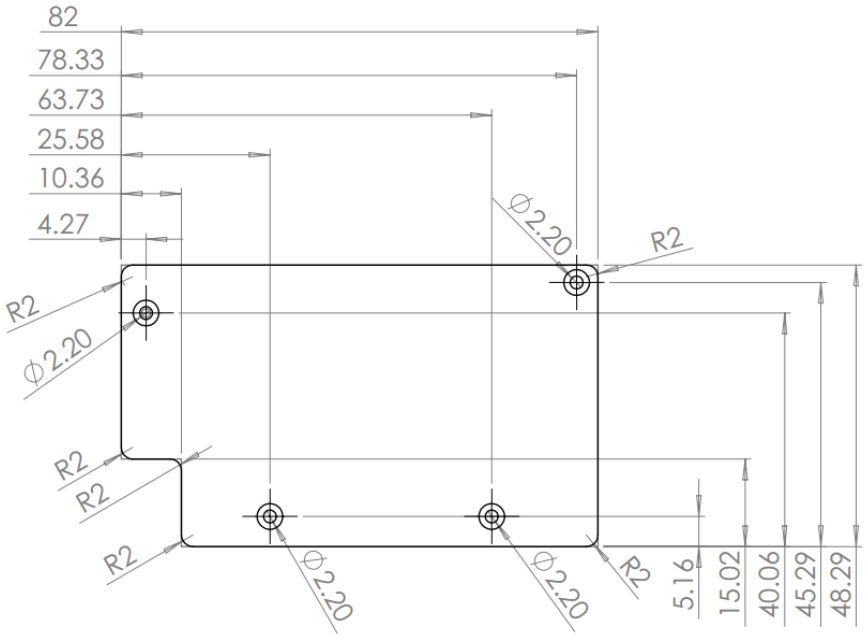

Figure 11-4: Variscite Heat plate dimensions

12 Ordering Information

Please refer to http://www.variscite.com/products/system-on-module-som/cortex-a15-krait/var-som-sd600-cpu-qualcomm-snapdragon600

13 Warranty Terms

Variscite guarantees hardware products against defects in workmanship and material for a period of one (1) year from the date of shipment. Your sole remedy and Variscite's sole liability shall be for Variscite, at its sole discretion, to either repair or replace the defective hardware product at no charge or to refund the purchase price. Shipment costs in both directions are the responsibility of the customer. This warranty is void if the hardware product has been altered or damaged by accident, misuse or abuse.

13.1 Disclaimer of Warranty

THIS WARRANTY IS MADE IN LIEU OF ANY OTHER WARRANTY, WHETHER EXPRESSED, OR IMPLIED, OF MERCHANTABILITY, FITNESS FOR A SPECIFIC PURPOSE, NON-INFRINGEMENT OR THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION, EXCEPT THE WARRANTY EXPRESSLY STATED HEREIN. THE REMEDIES SET FORTH HEREIN SHALL BE THE SOLE AND EXCLUSIVE REMEDIES OF ANY PURCHASER WITH RESPECT TO ANY DEFECTIVE PRODUCT.

13.2 Limitation on Liability

UNDER NO CIRCUMSTANCES SHALL VARISCITE BE LIABLE FOR ANY LOSS, DAMAGE OR EXPENSE SUFFERED OR INCURRED WITH RESPECT TO ANY DEFECTIVE PRODUCT. IN NO EVENT SHALL VARISCITE BE LIABLE FOR ANY INCIDENTAL OR CONSEQUENTIAL DAMAGES THAT YOU MAY SUFFER DIRECTLY OR INDIRECTLY FROM USE OF ANY PRODUCT.

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15 Appendix A—Glossary

The following table describes the terms and abbreviations used in this document.

Table 15-1: Terms and abbreviations

Term	Description
CAN Bus	Controller Area Network Bus
CSI	Camera Serial Interface
DMIC	Digital Microphone
DSI	Display Serial Interface
EMAC	Ethernet Media Access Controller
ESD	Electro Static Discharge
FFC	Flexible Flat Cable
HDMI	High Definition Multimedia Interface
HSIC	High-Speed Inter-Chip
I2C	Inter-Integrated Circuit bus
I2S	Inter-IC Sound
LCD	Liquid Crystal Display
LVDS	Low Voltage Differential Signaling
MIPI	Mobile Industry Processor Interface
MMC/SD	Multi Media card /Secure Digital card
MPP	Multi-purpose pins
OTG	On-the-Go USB interface
PCIe	Peripheral Component Interconnect Express
PHY	Physical Layer
PMIC	Power Management IC
SATA	Serial Advanced Technology Attachment
SoC	System on Chip
SDK	Software Development Kit
SoM	System on Module
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UFL	Miniature coaxial RF connector for high-frequency signals
USB	Universal Serial Bus