

Power MOSFET

PRODUCT SUMMARY

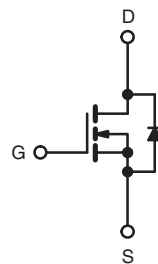
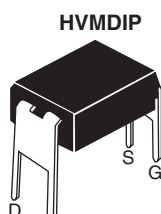
V_{DS} (V)	200	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.80
Q_g (Max.) (nC)	14	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	7.9	
Configuration	Single	

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
 COMPLIANT



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^\circ\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V _{DS}	200	V
Gate-Source Voltage			V _{GS}	± 20	
Continuous Drain Current	V _{GS} at 10 V	T _A = 25 °C	I _D	0.80	A
		T _A = 100 °C		0.50	
Pulsed Drain Current ^a			I _{DM}	6.4	W/°C
Linear Derating Factor				0.0083	
Single Pulse Avalanche Energy ^b			E _{AS}	260	mJ
Repetitive Avalanche Current ^a			I _{AR}	5.2	A
Repetitive Avalanche Energy ^a			E _{AR}	0.10	mJ
Maximum Power Dissipation	T _A = 25 °C		P _D	1.0	W
Peak Diode Recovery dV/dt ^c			dV/dt	5.0	V/ns
Operating Junction and Storage Temperature Range			T _J , T _{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 152\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 1.6\text{ A}$ (see fig. 12).
- $I_{SD} \leq 5.2\text{ A}$, $dI/dt \leq 95\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA		-	0.29	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 160 V, V _{GS} = 0 V, T _J = 125 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 0.48 A ^b	-	0.80	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = 50 V, I _D = 0.48 A ^b		0.60	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5		-	260	-	pF
Output Capacitance	C _{oss}			-	100	-	
Reverse Transfer Capacitance	C _{rss}			-	30	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 4.8 A, V _{DS} = 160 V, see fig.6 and 13 ^b	-	-	14	nC
Gate-Source Charge	Q _{gs}			-	-	3.0	
Gate-Drain Charge	Q _{gd}			-	-	7.9	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 4.8 A, R _g = 18 Ω, R _D = 19 Ω, see fig. 10 ^b		-	7.2	-	ns
Rise Time	t _r			-	22	-	
Turn-Off Delay Time	t _{d(off)}			-	19	-	
Fall Time	t _f			-	13	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode		-	-	0.80	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	6.4	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 0.80 A, V _{GS} = 0 V ^b		-	-	1.8	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 4.8 A, dI/dt = 100 A/μs ^b		-	150	300	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.91	1.8	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

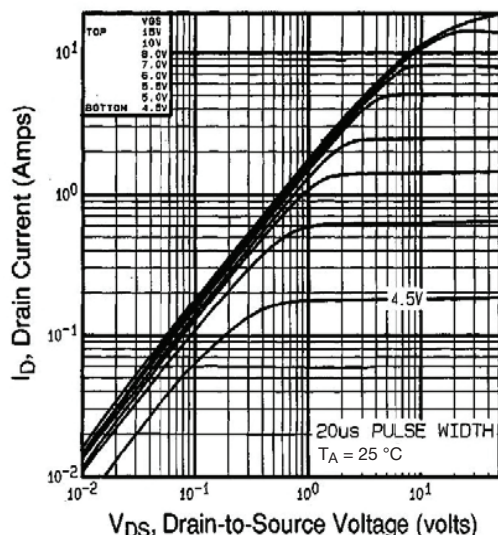
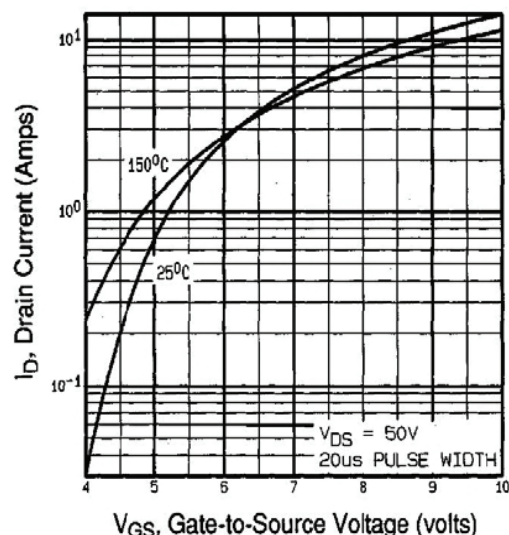
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)
Fig. 1 - Typical Output Characteristics, $T_A = 25\text{ }^{\circ}\text{C}$ 

Fig. 3 - Typical Transfer Characteristics

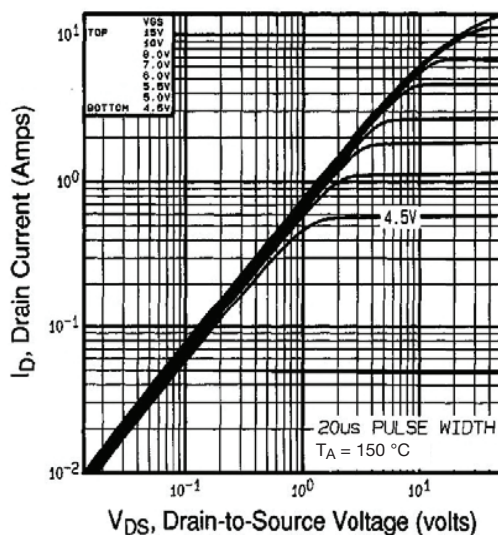
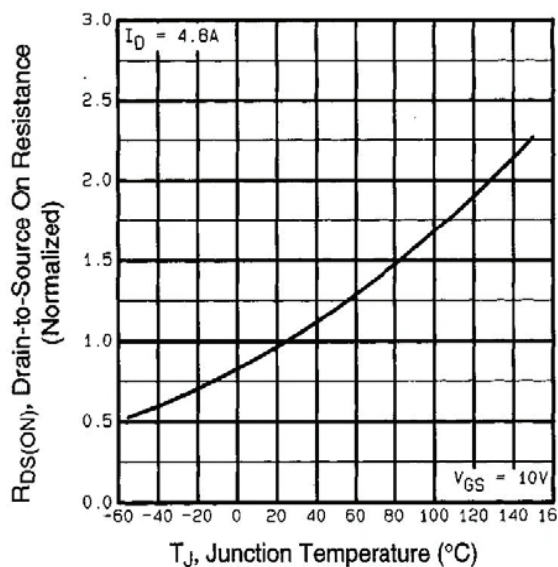
Fig. 2 - Typical Output Characteristics, $T_A = 150\text{ }^{\circ}\text{C}$ 

Fig. 4 - Normalized On-Resistance vs. Temperature

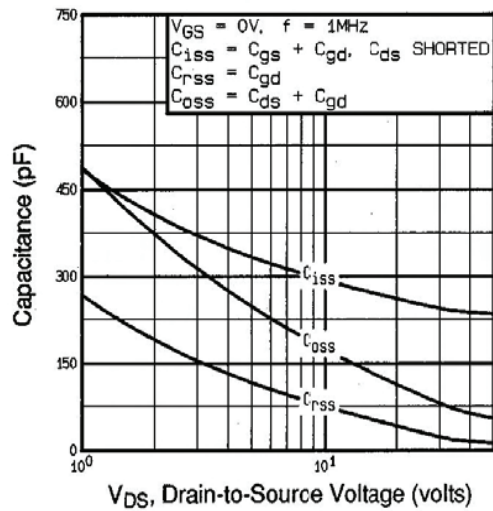


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

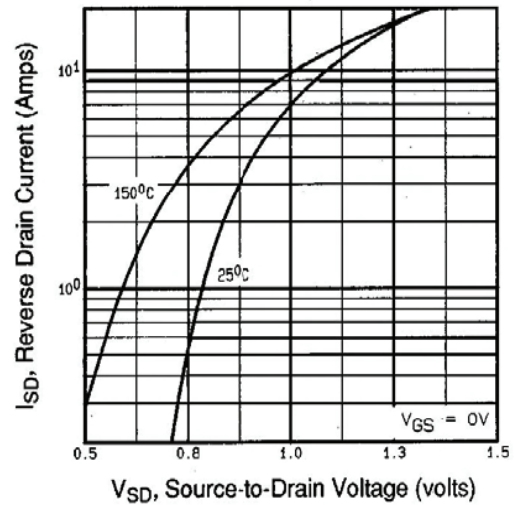


Fig. 7 - Typical Source-Drain Diode Forward Voltage

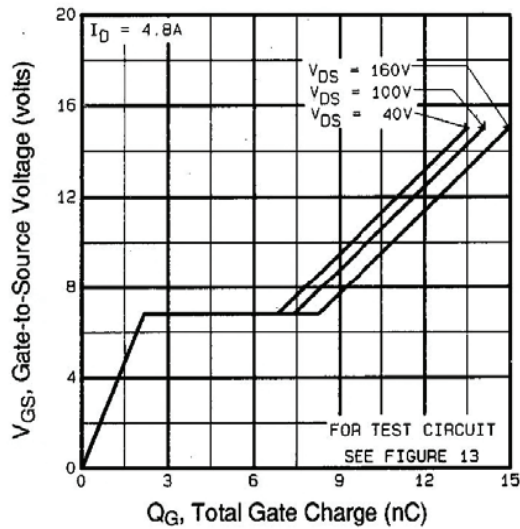


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

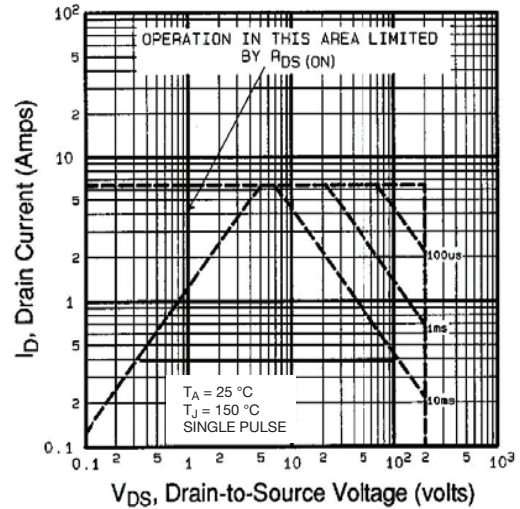


Fig. 8 - Maximum Safe Operating Area

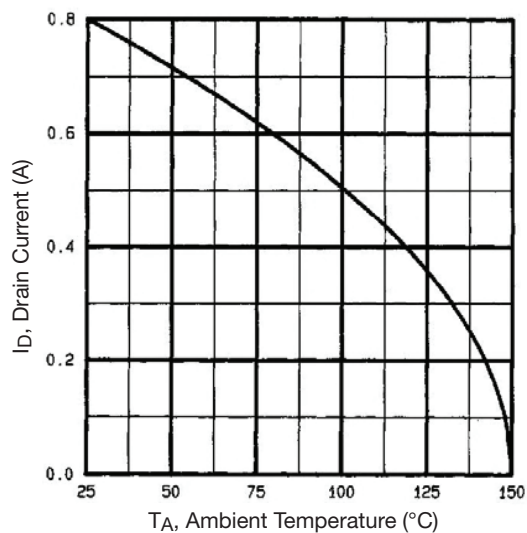


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

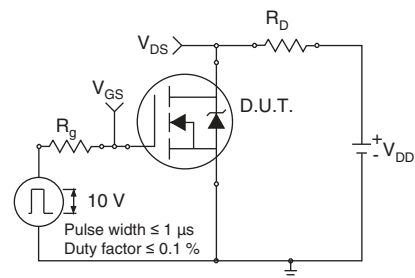


Fig. 10a - Switching Time Test Circuit

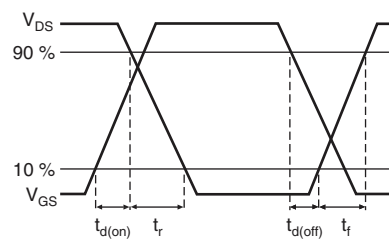


Fig. 10b - Switching Time Waveforms

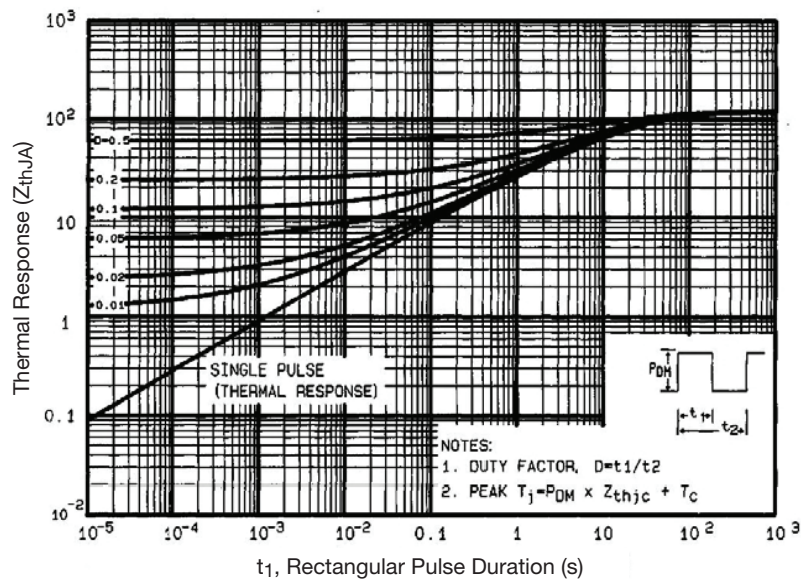


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

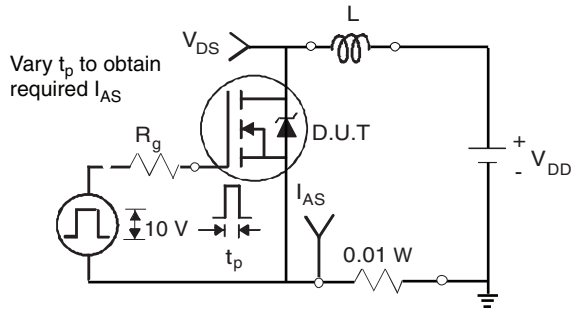


Fig. 12a - Unclamped Inductive Test Circuit

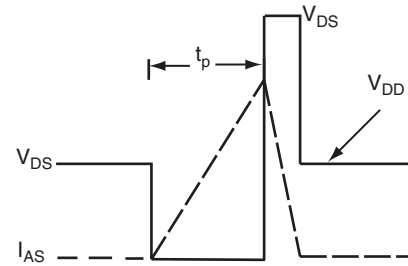


Fig. 12b - Unclamped Inductive Waveforms

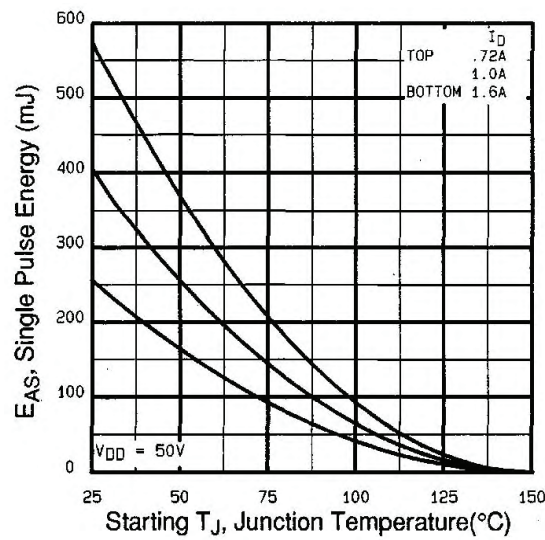


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

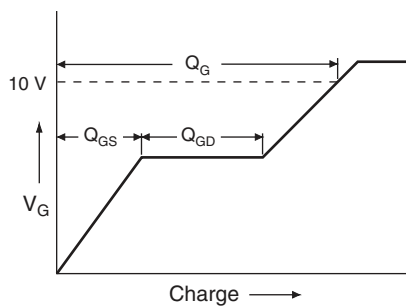


Fig. 13a - Basic Gate Charge Waveform

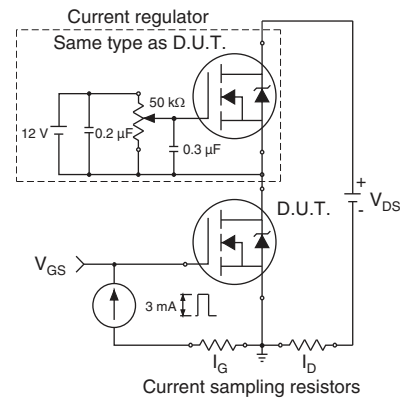
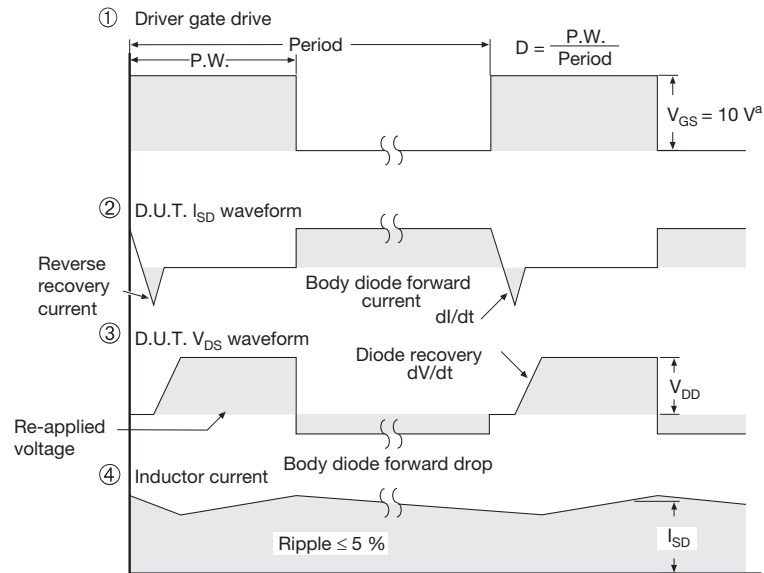
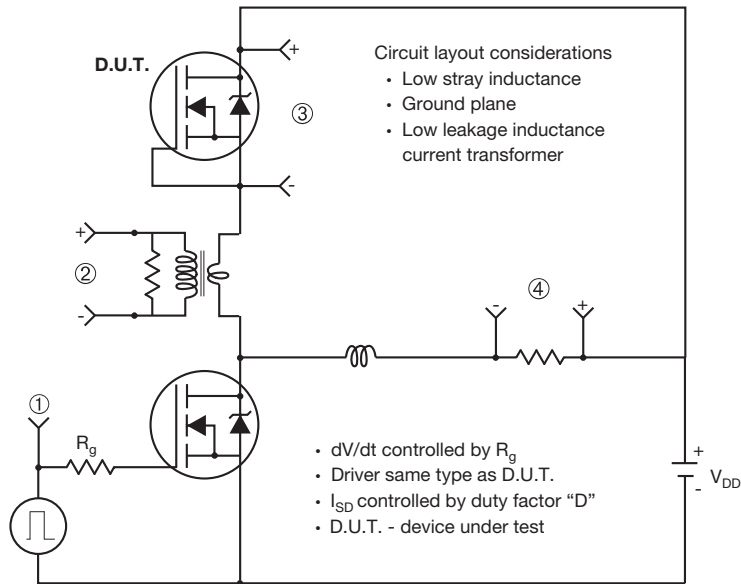


Fig. 13b - Gate Charge Test Circuit

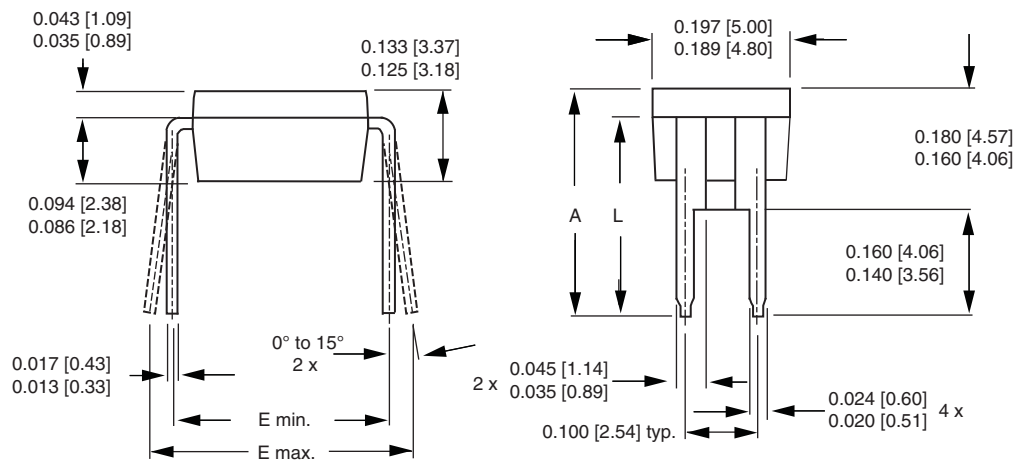
Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel



1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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