

Power MOSFET

PRODUCT SUMMARY

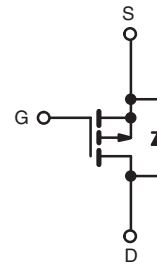
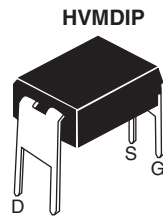
V_{DS} (V)	- 200	
$R_{DS(on)}$ (Ω)	$V_{GS} = -10\text{ V}$	0.50
Q_g (Max.) (nC)	18	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	9.0	
Configuration	Single	

FEATURES

- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- For Automatic Insertion
- End Stackable
- P-Channel
- 175 °C Operating Temperature
- Fast Switching
- Compliant to RoHS Directive 2002/95/EC



Available

RoHS*
 COMPLIANT


P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	- 200	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at - 10 V	$T_A = 25\text{ }^{\circ}\text{C}$	I_D	- 1.5	A
		$T_A = 100\text{ }^{\circ}\text{C}$		- 1.05	
Pulsed Drain Current ^a			I_{DM}	- 8.0	
Linear Derating Factor				0.0083	W/ $^{\circ}\text{C}$
Single Pulse Avalanche Energy ^b			E_{AS}	140	mJ
Repetitive Avalanche Current ^a			I_{AR}	- 1.0	A
Repetitive Avalanche Energy ^a			E_{AR}	0.13	mJ
Maximum Power Dissipation	$T_A = 25\text{ }^{\circ}\text{C}$		P_D	1.3	W
Peak Diode Recovery dV/dt ^c			dV/dt	- 5.5	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 175	$^{\circ}\text{C}$
Soldering Recommendations (Peak Temperature)	for 10 s			300 ^d	

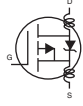
Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = -25\text{ V}$, starting $T_J = 25\text{ }^{\circ}\text{C}$, $L = 52\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = -2.0\text{ A}$ (see fig. 12).
- $I_{SD} \leq -6.8\text{ A}$, $dI/dt \leq 110\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ }^{\circ}\text{C}$.
- 1.6 mm from case.

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	120	°C/W

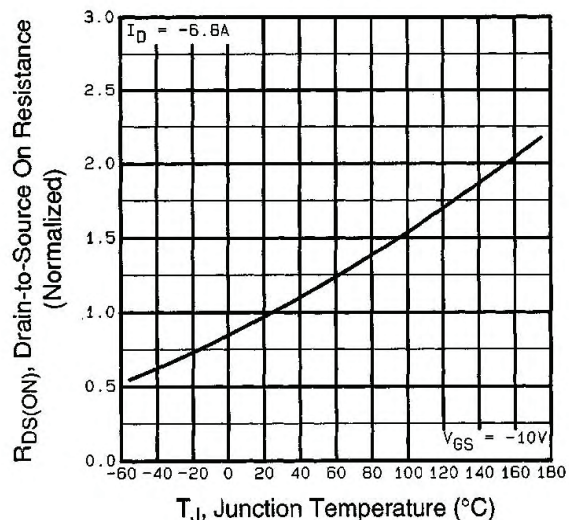
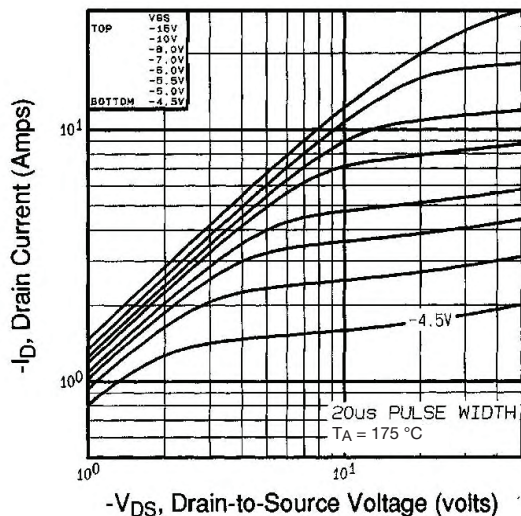
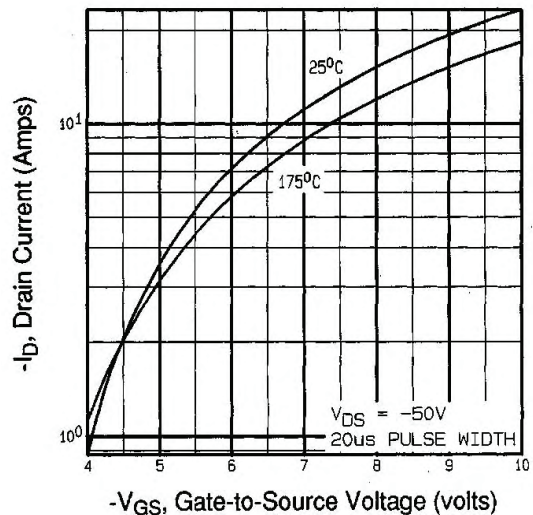
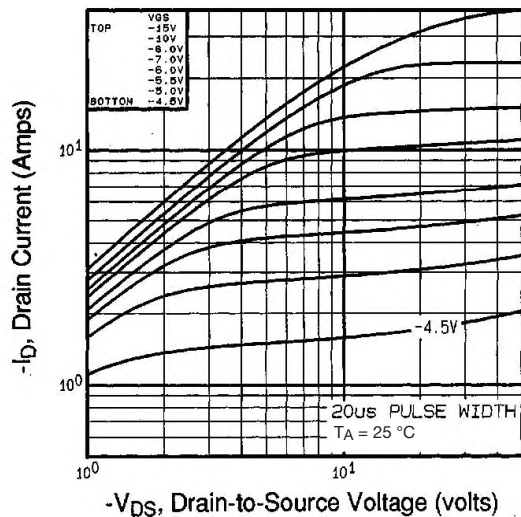
SPECIFICATIONS ($T_J = 25\text{ °C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 200	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = - 1 mA		-	- 0.10	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = - 200 V, V _{GS} = 0 V		-	-	- 100	μA
		V _{DS} = - 160 V, V _{GS} = 0 V, T _J = 150 °C		-	-	- 500	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 0.6 A ^b	-	0.50	-	Ω
Forward Transconductance	g _{fs}	V _{DS} = - 50 V, I _D = - 0.60 A ^b		0.71	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V V _{DS} = - 25 V f = 1.0 MHz, see fig. 5		-	390	-	pF
Output Capacitance	C _{oss}			-	170	-	
Reverse Transfer Capacitance	C _{rss}			-	45	-	
Total Gate Charge	Q _g	V _{GS} = - 10 V	I _D = - 6.8 A, V _{DS} = - 160 V see fig. 6 and 13 ^b	-	-	18	nC
Gate-Source Charge	Q _{gs}			-	-	3.0	
Gate-Drain Charge	Q _{gd}			-	-	9.0	
Turn-On Delay Time	t _{d(on)}	V _{DD} = -100 V, I _D = - 6.8 A R _g = 18 Ω, R _D = 7.1 Ω, see fig. 10 ^b		-	9.6	-	ns
Rise Time	t _r			-	29	-	
Turn-Off Delay Time	t _{d(off)}			-	21	-	
Fall Time	t _f			-	25	-	
Internal Drain Inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.0	-	nH
Internal Source Inductance	L _S			-	6.0	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 1.0	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	- 8.0	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = - 1.0 A, V _{GS} = 0 V ^b		-	-	- 6.3	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = - 6.8 A, dI/dt = 100 A/μs ^b		-	98	200	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	0.33	0.66	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
 b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



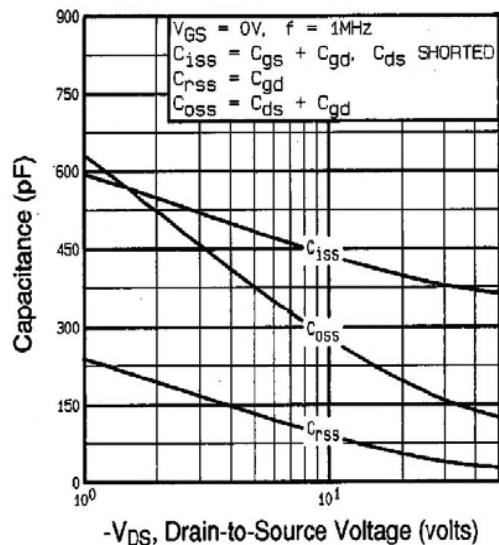


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

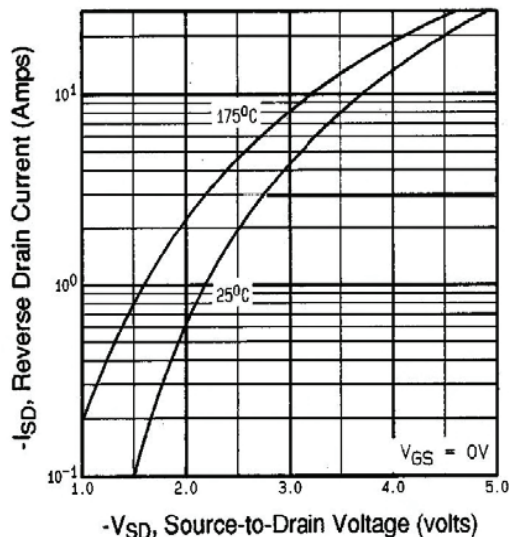


Fig. 7 - Typical Source-Drain Diode Forward Voltage

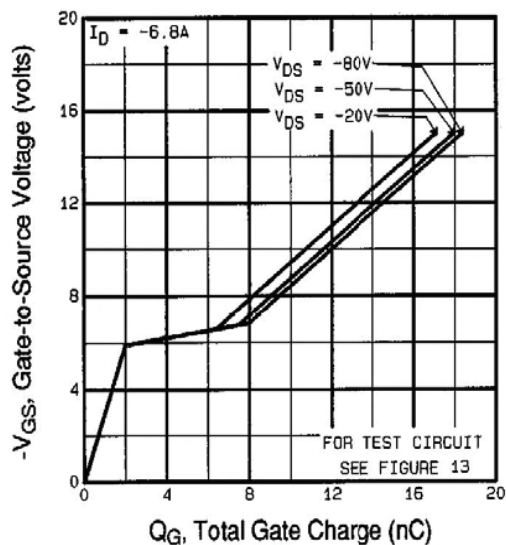


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

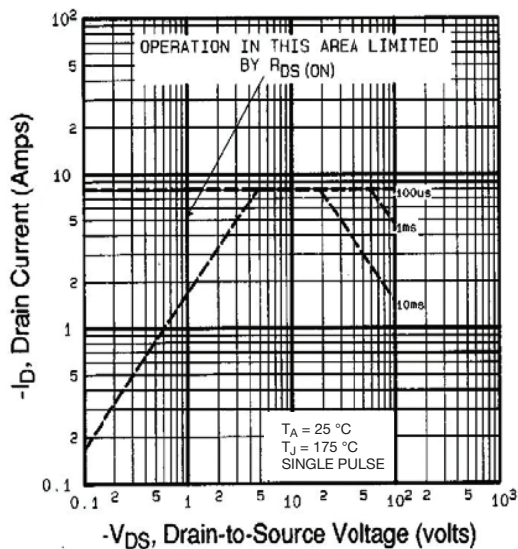


Fig. 8 - Maximum Safe Operating Area

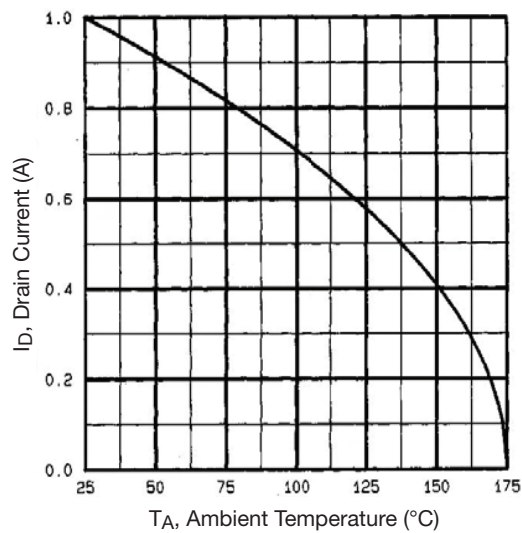


Fig. 9 - Maximum Drain Current vs. Ambient Temperature

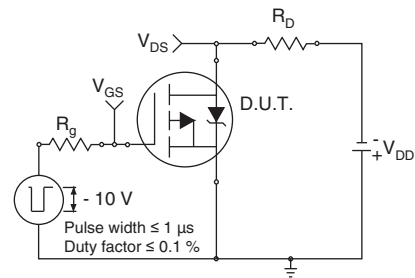


Fig. 10a - Switching Time Test Circuit

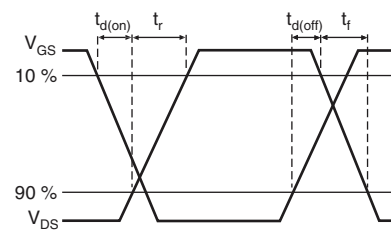


Fig. 10b - Switching Time Waveforms

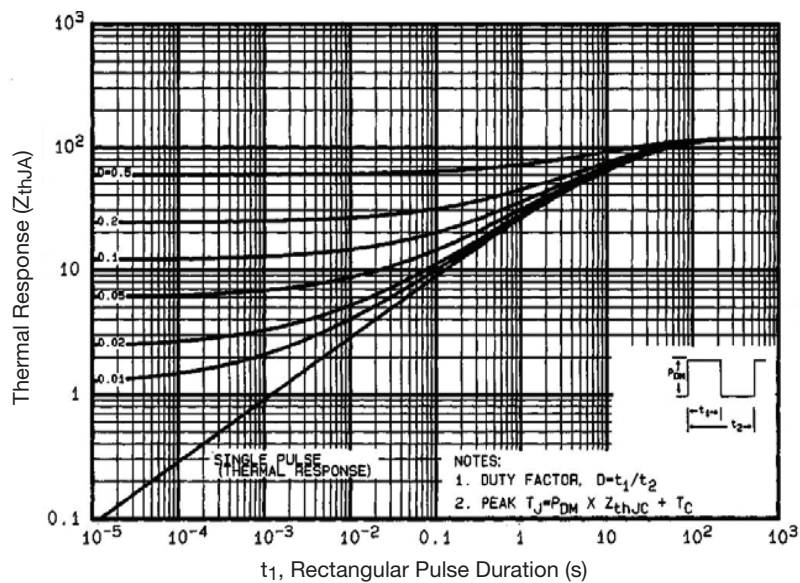


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

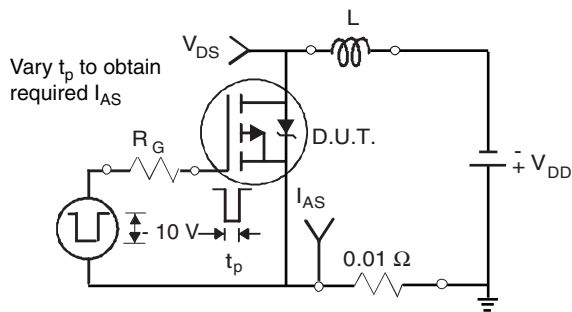


Fig. 12a - Unclamped Inductive Test Circuit

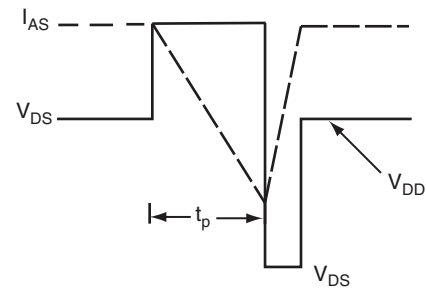


Fig. 12b - Unclamped Inductive Waveforms

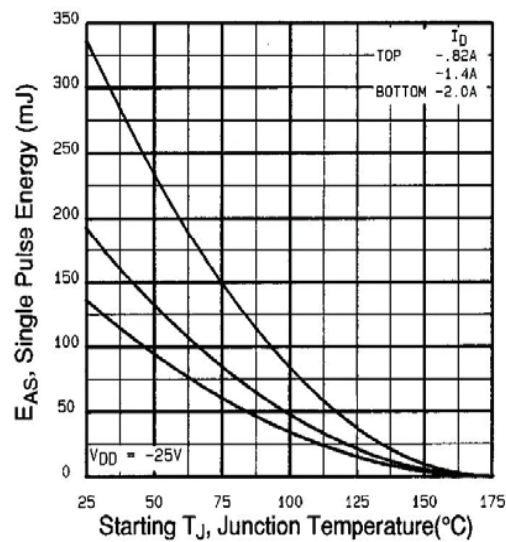


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

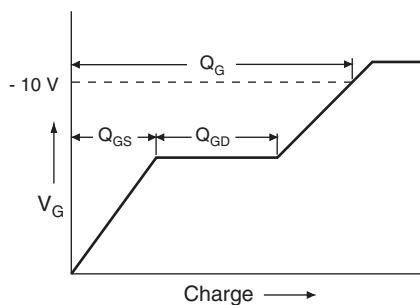


Fig. 13a - Basic Gate Charge Waveform

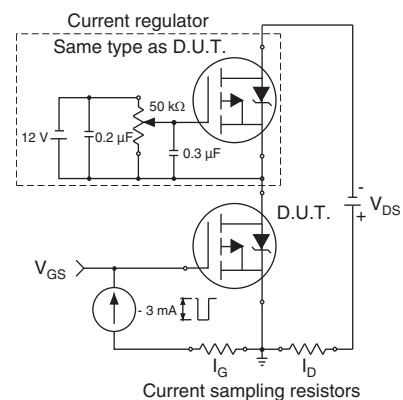
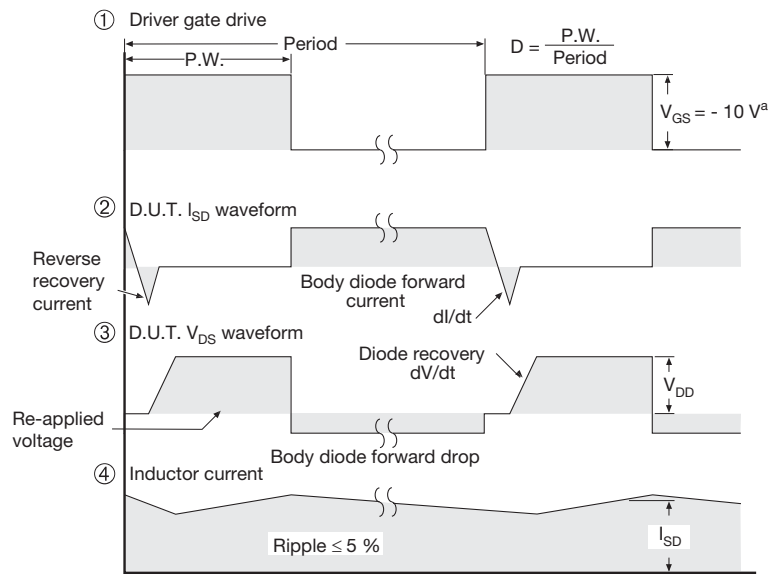
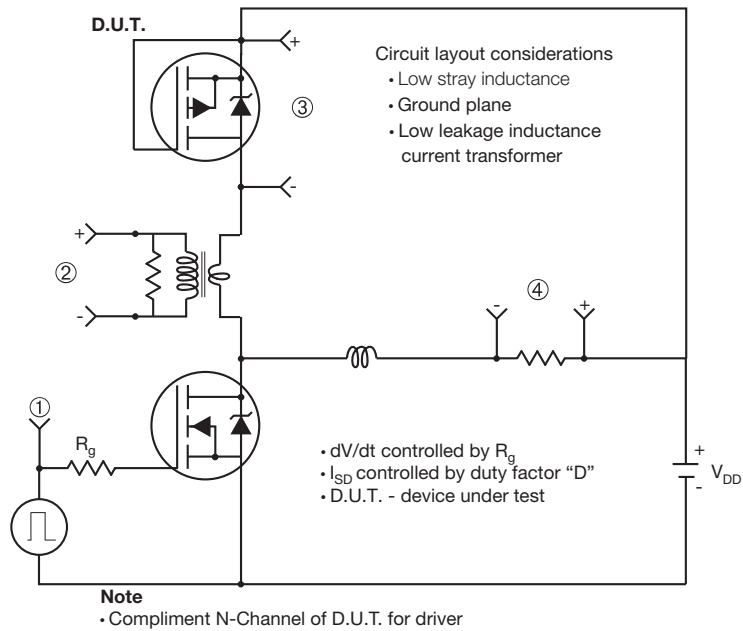


Fig. 13b - Gate Charge Test Circuit

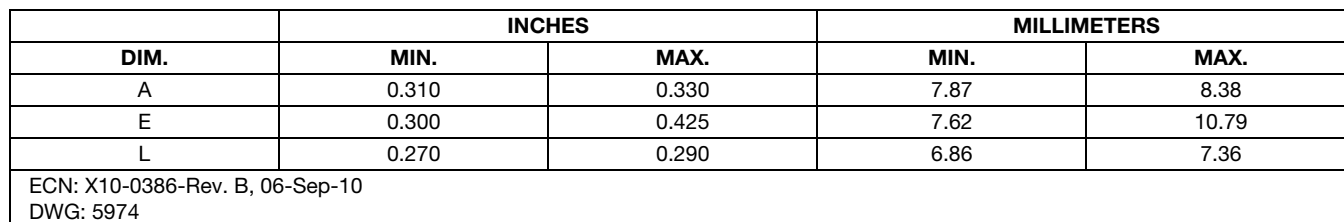
Peak Diode Recovery dV/dt Test Circuit



Note

a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 14 - For P-Channel



1. Package length does not include mold flash, protrusions or gate burrs. Package width does not include interlead flash or protrusions.

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