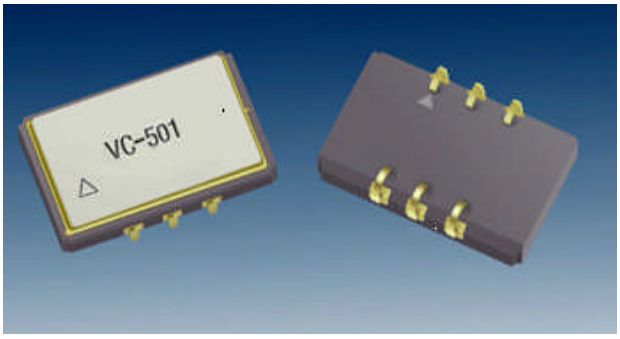
VECTRON INTERNATIONAL
A DOVER COMPANY

VC-501

Voltage Controlled Crystal Oscillator



Features

- Industry Standard Package, 14.0 x 9.0 x 4.5 mm
- Output Frequencies from 100.00 MHz to 200 MHz
- 3.3 V Operation
- HFF/fundamental crystal for ultra low jitter
- Complementary PECL Outputs
- Low phase noise and custom options
- 0/70° C or –40/85° C operating temperature
- Enable /Disable (PECL)

Applications

PLL circuits for Clock Smoothing and Frequency Translation

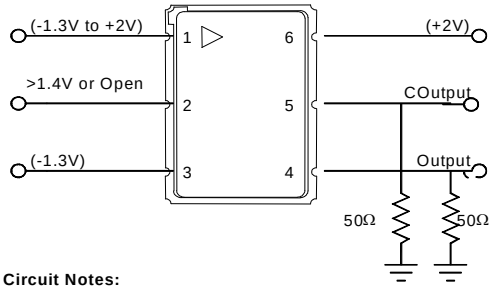
- Fiber Channel
- SONET
- SDH, ITU-T G.709
- SONET, GR-253-CORE Issue3

Description

The VC-501 is a voltage controlled crystal oscillator that operates at the fundamental frequency of the internal HFF crystal. The HFF crystal is a high-Q quartz device that enables the circuit to achieve low phase jitter performance over a wide operating temperature range. The oscillator is housed in an industry standard hermetically sealed leadless surface mount package and is available on tape and reel.

VC-501 Voltage Controlled Crystal Oscillator

Electrical Performance					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	100.000	155.52	200	MHz
Supply Voltage (+3.3 V)	V_{DD}	3.135	3.3	3.465	V
Supply Current	I_{DD}		50	90	mA
Output Logic Levels					
Output Logic High 0/70 ºC	V_{OH}	V_{DD} -1.025		V_{DD} -0.880	V
Output Logic Low 0/70 ºC	V_{OL}	V_{DD} -1.810		V_{DD} -1.620	V
Output Logic High -40/85 ºC	V_{OH}	V_{DD} -1.085		V_{DD} -0.880	V
Output Logic Low -40/85 ºC	V_{OL}	V_{DD} -1.830		V_{DD} -1.555	V
Transition Times					
Rise Time	t_R		0.5	1	ns
Fall Time	t_F		0.5	1	ns
Symmetry or Duty Cycle	SYM	45	50	55	%
Operating temperature (*ordering option*)		0/70 or –40/85			°C
Jitter (12 kHz – 20 MHz BW), 155.52 MHz			0.3	1	ps (rms)
Jitter (50 kHz – 80 MHz BW), 155.52 MHz			0.5		ps (rms)
Phase Noise, f_0 = 155.52 MHz					
10 Hz offset			-64		dBc/Hz
100 Hz offset			-95		dBc/Hz
1kHz offset			-123		dBc/Hz
10 kHz offset			-143		dBc/Hz
100 kHz offset			-146		dBc/Hz
1 MHz offset			-146		dBc/Hz
10 MHz offset			-146		dBc/Hz
Test Conditions for APR (+3.3V)	V_C	0.3		3.0	V
Absolute Pull Range (*APR*)	APR	± 50			ppm
Gain Transfer		Positive			
		100			ppm/V
Control Voltage Bandwidth (-3dB)	BW	20			kHz
Package Size		14.0 x 9.0 x 4.5			mm



Test Circuit Notes:
1) To Permit 50Ω Measurement of Outputs, all DC Inputs are Biased Down 1.3V.
2) All Voltage Sources Contain Bypass Capacitors to Minimize Supply Noise.
3) 50Ω Terminations are Within Test Equipment.

Figure 1. Test Circuit (3.3 V)

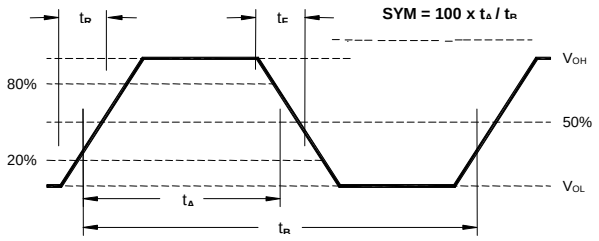
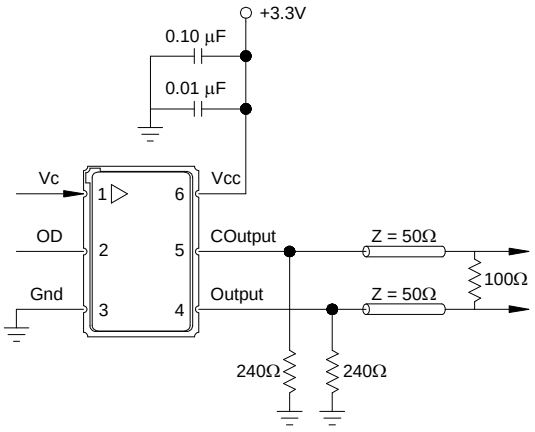
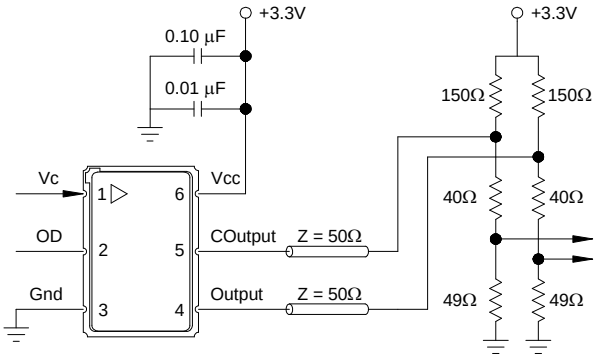


Figure 2. PECL Waveform

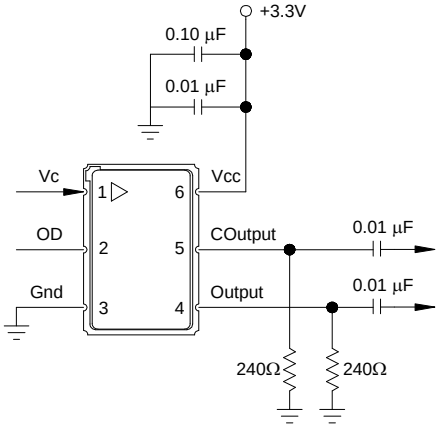
Suggested Output Load Configurations



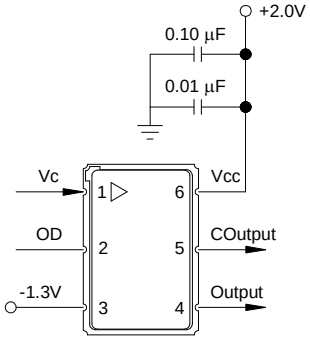
LV-PECL to LV-PECL: For short transmission lengths, the power consumption could be reduced by removing the 100Ω resistor and doubling the value of the pull down resistors.



LV-PECL to LVDS: Restricted for short transmission lengths. Configuration may require modification depending on LVDS receiver.



Functional Test: Allows standard power supply configuration. Since AC coupled, the LV-PECL levels cannot be measured.



Production Test: Allows direct DC coupling into 50Ω measurement equipment. Must bias the power supplys as shown. Similar to Figure 1.

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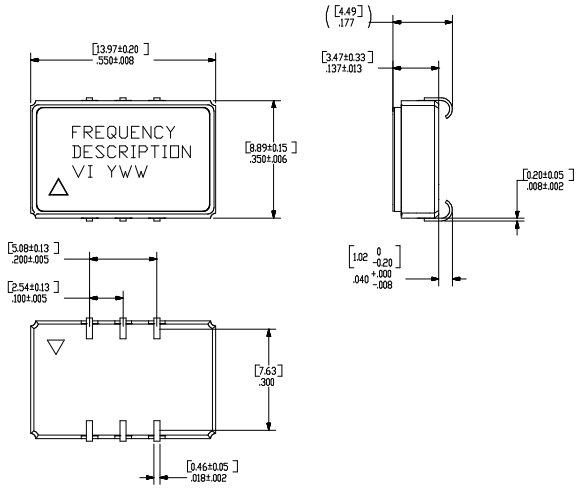
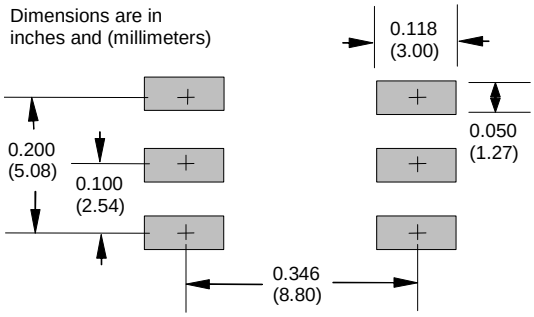
Outline Diagram



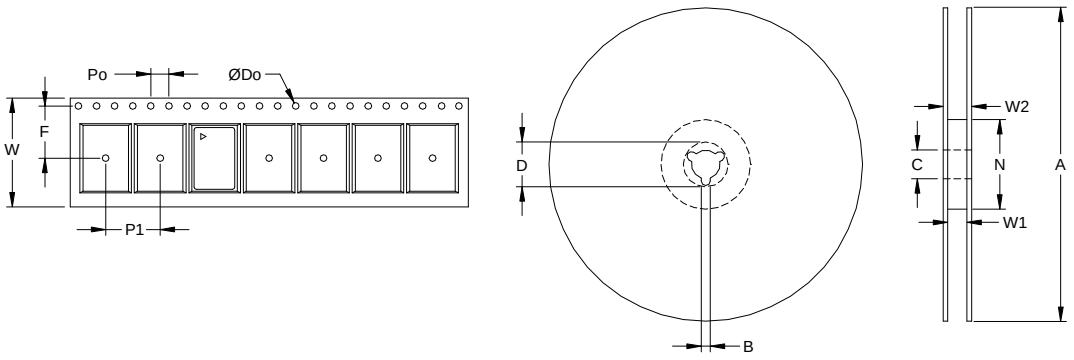
Pad Layout



Pin Out

Pin	Symbol	Function
1	V_C	VCXO Control Voltage
2	OE	Enable / Disable *Ordering option, standard **F** configuration*: Output is Enabled = High or Open Output is Disabled = Low (High impedance output, Oscillator running)
3	GND	Case and Electrical Ground
4	Output	Output
5	COutput	Complementary Output
6	V_{CC}	Power Supply Voltage (3.3 V)

Tape and Reel (EIA-481-2-A)



Tape Dimensions (mm) / Reel Dimensions (mm)

Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# Per
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Min	Typ	Min	Min	Typ	Max	Reel
VC-501	24	11.5	1.5	4	12	330	1.78	13	21	100	25	30	200

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Power Supply	V_{CC}	0 to 6	V
Voltage Control Range	V_C	0 to V_{CC}	V
Storage Temperature	TS	-55 to 125	°C
Soldering Temp/Time	T_{LS}	240/10	°C/sec

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Reliability

The VC-501 family is capable of meeting the following qualification tests:

Environmental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Solderability	MIL-STD-883, Method 2003
Gross and Fine Leak	MIL-STD-883, Method 1014
Resistance to Solvents	MIL-STD-883, Method 2015

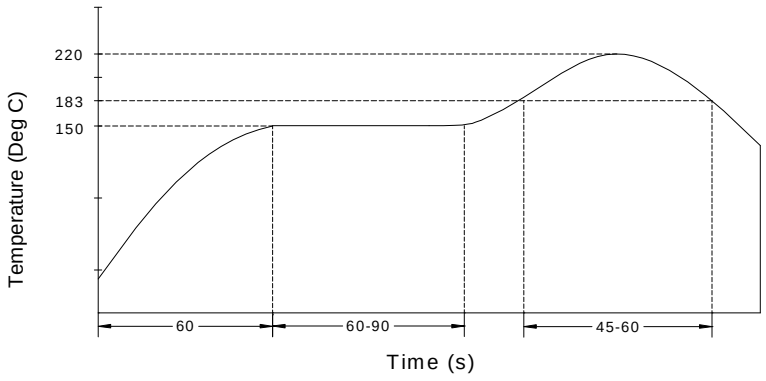
Handling Precautions

Although ESD protection circuitry has been designed into the VC-501 proper precautions should be taken when handling and mounting. VI employs a human body model and a charged-device model (CDM) for ESD susceptibility testing and design protection evaluation.

ESD Ratings

Model	Minimum	Conditions
Human Body Model	500	MIL-STD 883, Method 3015
Charged Device Model	500	JESD 22-C101

Recommended Solder Reflow Profile



VI qualification includes aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The conditions a device can withstand are well understood and devices can be subjected to the profile above. This profile shows a ramp up condition to prevent thermal shock, a preheat period in which the flux is activated, a ramp up to 183°C which is the reflow temperature of Sn/Pb eutectic, and a gradual cool down. The time above 183°C should not exceed 60 seconds and the peak temperature should be no more than 240°C for 10 seconds. The VC-501's are hermetically sealed so an aqueous wash is not an issue.

Standard Frequencies (MHz)

100.00	106.250	125.000	155.520	156.250	161.1328	167.3316	