Complementary Enhancement-Mode Vertical DMOS FET Quad Array

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max) Q1 + Q2 or Q3 + Q4	Order Number / Package	
		14-Pin P-Dip	14-Pin C-Dip*
60V	11Ω	VC0106N6	VC0106N7

* 14-pin Side Brazed Ceramic Dip.

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- 4 independent channels
- 4 electrically isolated die
- Commercial and military versions available
- Free from secondary breakdown
- Low power drive requirement
- Low C_{ISS} and fast switching speeds
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Convertors
- Power supply circuits
- Driver (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)
- Amplifiers
- Switches

Thermal Characteristics

Package		Plastic DIP	Ceramic DIP
I_D continuous & I_{DR} (single die)	N-Channel	0.56A	0.7A
	P-Channel	-0.35A	-0.4A
I_D pulsed† & I_{DRM}†	N-Channel	2.0A	2.0A
	P-Channel	-1.0A	-1.0A
Power Dissipation @ T_C = 25°C‡		2W	3W
θ_{ja} (°C/W)‡		110	83.3
θ_{jc} (°C/W)‡		62.5	41.6

† Pulse test 300 µS pulse, 2% duty cycle.

‡

Advanced DMOS Technology

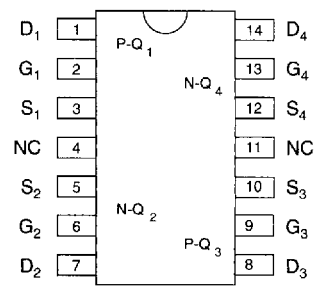
These enhancement-mode (normally-off) DMOS FET arrays utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex quad arrays use four independent DMOS transistors. They are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Electrical Characteristics

Refer to VN0104/VN0106/VN0109 and VP0104/VP0106/VP0109 data sheets for detailed characteristics of N- and P-channel devices.

Pin Configuration



top view

14-pin DIP