



VC0345TLNA

USB2.0 PC Camera Processor

Datasheet

Version 1.0

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1. GENERAL DESCRIPTION

VC0345TLNA is Vimicro's new low cost PC Camera Processor with small footprint design, targeted for attachable PC camera, notebook embedded camera and special LCD camera markets for high-end system configuration. With a programmable sensor master clock output, VC0345TLNA can support any common CMOS image sensors, ranging from VGA to 2 Mega pixel resolutions. Being fully compliant with the increased bandwidth of USB 2.0 High-Speed (HS) protocol, VC0345TLNA can produce uncompressed high quality video stream at 30fps for VGA and is capable of capture still images at up to 3 Mega pixels resolution.

VC0345TLNA will be implemented using the OTP memory to store its internal firmware and it can also support firmware patch function using external EEPROM and internal code RAM. These features will give PC camera makers the ultimate flexibility when trying to customize their own firmware.

VC0345TLNA is a UVC device that will work with Operating Systems that supports the UVC standard, such as Windows XP (with Service Pack 2) and Vista, without the need to install the Vimicro driver. However to provide for additional powerful functions such as better video quality and other special image effects, the Vimicro UVC driver needs to be installed for these functions to work.

The following tables show the main video operation modes that VC0345TLNA supports:

USB2.0 Full Speed (Isochronous) or USB1.1

Maximum Frame Rate	VGA	CIF	QVGA	QCIF	QQVGA
Uncompressed (Bayer raw 8-bit)	-	-	10fps	10fps	30fps
Uncompressed (Bayer raw 10-bit)	-	-	5fps	5fps	15fps
YUY422	-	-	-	-	15fps

USB2.0 High Speed (Isochronous)

Maximum Frame Rate	QXGA	UXGA	SXGA	VGA	CIF	QVGA	QCIF	QQVGA
Uncompressed (Bayer raw 8-bit)	-	10fps	15fps	30fps	30fps	30fps	30fps	30fps
Uncompressed (Bayer raw 10-bit)	4fps	5fps	7.5fps	30fps	30fps	30fps	30fps	30fps
YUY422	-	5fps	7.5fps	30fps	30fps	30fps	30fps	30fps
MJPEG	15fps	15fps	-	-	-	-	-	-

Notes:

- 1) VC0345 can bypass 8-bit and 10-bit Bayer raw data from the sensor to the USB host.
- 2) When MS UVC driver is used, the output format from the chip will only support YUY2 or JPEG.
- 3) VC0345 can bypass sensor's MJPEG data from the sensor to the USB host.

VC0345TLNA's package information is listed below:

PRODUCT NUMBER	PACKAGE
VC0345TLNA	48-pin Tiny QFN at 6.5mm x 5mm

2. FULL FEATURE LIST

- Parallel sensor interface support VGA/SXGA/UXGA CMOS sensors
- Adapting USB2.0 PHY and compatible with USB2.0 HS/FS and USB 1.1
- USB Video Class (UVC) 1.0 standard compliant
- Support HID (require 2 GPIOs: Receiver, Power management) configurable by EEPROM
- Microsoft WHQL Logo compliance
- Support various OS including 64-bit Windows
- Support Win 2000 and Win 98 using a Vimicro UVC driver
- Build-in OTP (One Time Programmable device with 32KB memory) ROM
- Support 3-Mega motion JPEG sensors data bypass mode
- Support I2C for sensor configuration (two sensors) / EEPROM / Auto Focus (AF) control
- Imaging Applications
 - ✧ Video streaming up to 30fps at VGA resolution, 15fps@SXGA, and 10fps@UXGA
 - ✧ Still image capture and preview at up to 3M pixel resolution
- Software ISP
 - ✧ 8-bit wide accuracy in color processing
 - ✧ Auto Exposure (AE)
 - ✧ Auto White Balance (AWB)
 - ✧ Auto Gain Control (AGC)
 - ✧ Auto defect pixel detection (DPD) and advanced defect pixel cancellation (DPC) function
 - ✧ Configurable image noise reduction
 - ✧ Configurable image sharpness enhancement
 - ✧ Configurable gamma, contrast and color correction
 - ✧ Configurable brightness, color saturation, and hue
 - ✧ Anti-flicker detection and cancellation
 - ✧ Indoor/outdoor auto detection
 - ✧ Configurable lens shading compensation (optional)
 - ✧ Edge-adaptive CFA interpolation
 - ✧ Black and white sensor native support
 - ✧ Exposure and backlight correction
- Output Video Format
 - ✧ YUY2 (16 bits/pixel)
 - ✧ MJPEG
 - ✧ Bayer (raw 8 or 10 bits/pixel), requires Vimicro driver
- Software digital scaling support many different resolutions
- Build-in 8-bit MCU

- ◇ High performance MCU core with rich supporting peripherals
- ◇ On-chip ROM and SRAM for high performance
- GPIOs for Typical Camera Control Support
 - ◇ Snapshot button
 - ◇ LED indicator
 - ◇ Flip and Mirror
- Anti-glitch function built into all GPIOs
- 48-pin Tiny QFN package
- Support Watch-Dog function
- Support additional sensors through EEPROM
- 1.8V Core and 3.3V I/O
- 6.5V OTP programming power supply
- Support remote wake up from suspend status by GPIO triggers
- Power Management
 - ◇ Normal mode
 - ◇ Suspend mode

3. CHIP BLOCK DIAGRAM

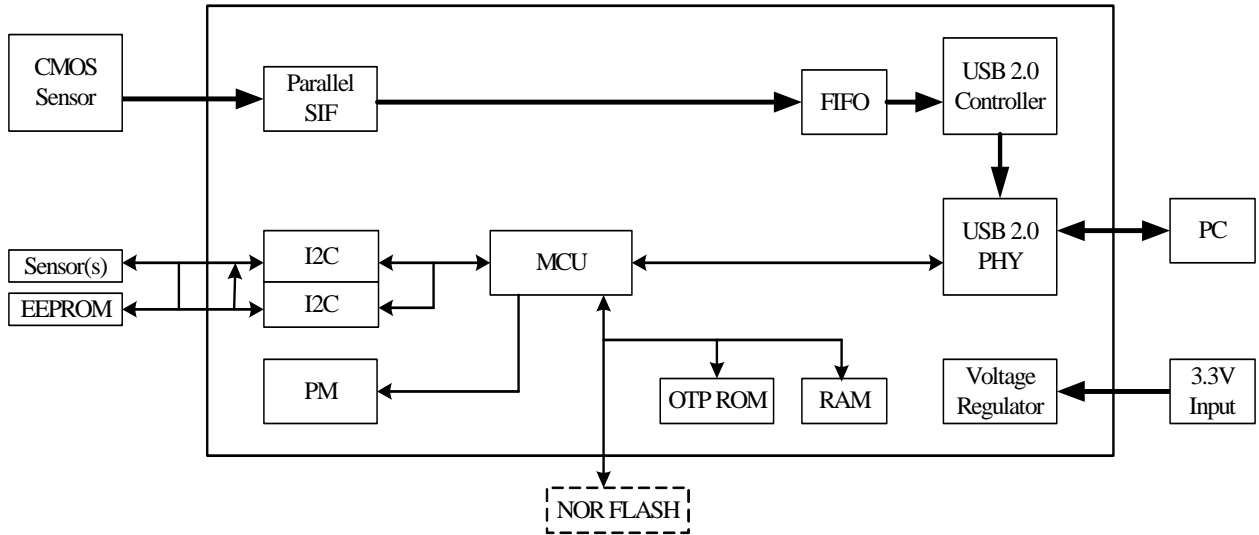


Figure 1: VC0345TLNA Chip Block Diagram

4. KEY BLOCK DESCRIPTIONS

● Sensor Interface (SIF) Unit

The sensor interface (SIF) acts as the bridge between the external sensor and the USB controller (UDC) inside the VC0345TLNA chip. To the sensor side, the SIF receives 10-bit image data and synchronous signals from the sensor and outputs control signals to it. The synchronous signals from different sensors may vary from one to another. The SIF uniforms the synchronous signals and forwards them together with the image data to UDC / JPEG HEADER. Some of the features supported by SIF are:

- ✧ Support 10-bit Bayer pattern and YUV422 data format from sensor
- ✧ Generate sync signals for UDC, whose width and polarity are programmable
- ✧ Image window size adjustable
- ✧ Support parallel JPEG data transfer

● USB2.0 Controller and PHY Unit

This unit transfers the image data at very high speed to the host through an on-chip PHY. This unit provides a USB 2.0 compliant interface. It also contains a controller, which deals with USB transfer protocol, and the video function interface of the device. The USB 2.0 unit supports three kinds of transfer: control transfer, isochronous transfer and interrupt transfer. Suspend and Resume functions are supported by this unit also.

● Micro-Controller Unit

VC0345TLNA contains an embedded 8051 core compatible micro-controller. It is a fully functional 8-bit embedded controller that executes all ASM51 instructions the same as the 80C31. Besides a 256 bytes internal ram to implement register bank and SFR of 8051 MCU core, a 2Kb on-chip RAM is configured as the external data memory. Third party application and image processing firmware can be stored in the on-chip ROM for a cost-effective solution. The available code size includes 32Kb OTPROM and 2Kb SRAM. An external EEPROM will be used to store the customized settings.

● Serial Interface Controller

2-wire serial interface is supported by VC0345TLNA. There are two I2C masters: one is for sensor I2C and the other is for EEPROM. VC0345TLNA can provide two modes:

Mode A – separated, the sensor I2C uses pin33 and pin34, EEPROM uses pin9 and pin10;

Mode B – shared, the sensor I2C and EEPROM I2C are connected to both pin33 and pin34.

● Chip Control and Power Management Unit

This unit takes care of VC0345TLNA's global control, including power management, reset and clock control. When the chip is in suspend mode, the clock oscillator will be shut down and peripheral power is shut down to make suspend current less than 300uA. USB reset, resume signals can make the device exit from this state.

5. PIN ASSIGNMENTS

5.1 VC0345TLNA (Tiny QFN 48-pin) Pin Assignments

PIN No.	NAME	TYPE	DESCRIPTION
1	CS_D0	I/O	Parallel sensor data
2	OVSS2	P	I/O ground
3	OVDD2	P	I/O power
4	CLKXOUT	C	Crystal output
5	CLKXIN	C	Crystal input
6	GPIO4_UART0	I/O, S	UART port
7	GPIO5_UART1	I/O, S	UART port
8	GPIO10	I/O, S	GPIO used for WP_EEPROM
9	GPIO11	I/O, S	GPIO
10	GPIO1_ESCK	I/O, S	GPIO and EEPROM I2C clock port
11	GPIO0_ESDA	I/O, S	GPIO and EEPROM I2C data port
12	DVSS3	P	Core ground
13	DVDD3	P	Core power
14	PWUP_RSTN	I, S	Active low power-on reset
15	GPIO6_SNAPB	I/O, S	GPIO Snap button
16	USB_VRES	A	Connect to external 8.2K resistor (one end of the resistor connects to VRES and the other end connects to PCB ground)
17	USB_VDDA0	PA	USB PHY analog power, 3.3V
18	USB_VSSA0	PA	USB PHY analog ground
19	USB_PADM	A	USB data pin data-
20	USB_PADP	A	USB data pin data+
21	USB_VDDL0	PA	USB PHY digital power, 1.8V
22	USB_VSDL0	PA	USB PHY digital ground
23	GPIO3_FLIP	I/O, S	GPIO Flip and mirror
24	GPIO7_LED1	I/O, S	GPIO for low active to light for LED
25	VPROG_OTP	PA	OTP ROM VPP power 6.5V
26	GPIO12_LED2	I/O	PWM output for controlling LED
27	GPIO8_IRHID	I/O	GPIO and IR HID
28	GPIO9_IRPWR	I/O	GPIO and IR power

PIN No.	NAME	TYPE	DESCRIPTION
29	CS_PWDB	I/O	Power-down pin controlling sensor DC/DC regulator
30	TEST	I	Manufacturing test mode, 0 represents work mode
31	CS_PCLK	I/O	Parallel sensor clock
32	OVDD	P	I/O power
33	OVSS	P	I/O ground
34	CS_CLK	I/O, S	Sensor clock
35	CS_SCK	I/O	IIC SCK & ESCK
36	CS_SDA	I/O, S	IIC SDA & ESDA
37	CS_RSTB	I/O	Sensor reset
38	CS_HSYNC	I/O, PD	Sensor horizontal sync
39	CS_VSYNC	I/O, PD	Sensor vertical sync
40	CS_D9	I/O	Parallel sensor data
41	CS_D8	I/O	Parallel sensor data
42	CS_D7	I/O	Parallel sensor data
43	CS_D6	I/O	Parallel sensor data
44	CS_D5	I/O	Parallel sensor data
45	CS_D4	I/O	Parallel sensor data
46	CS_D3	I/O	Parallel sensor data
47	CS_D2	I/O	Parallel sensor data
48	CS_D1	I/O	Parallel sensor data

Note: I/O – Input/Output
 I – Input
 O – Output
 P – Power
 A – Analog
 PD – Pull-down
 PU – Pull-up

5.2 VC0345TLNA Pin Layout Diagram

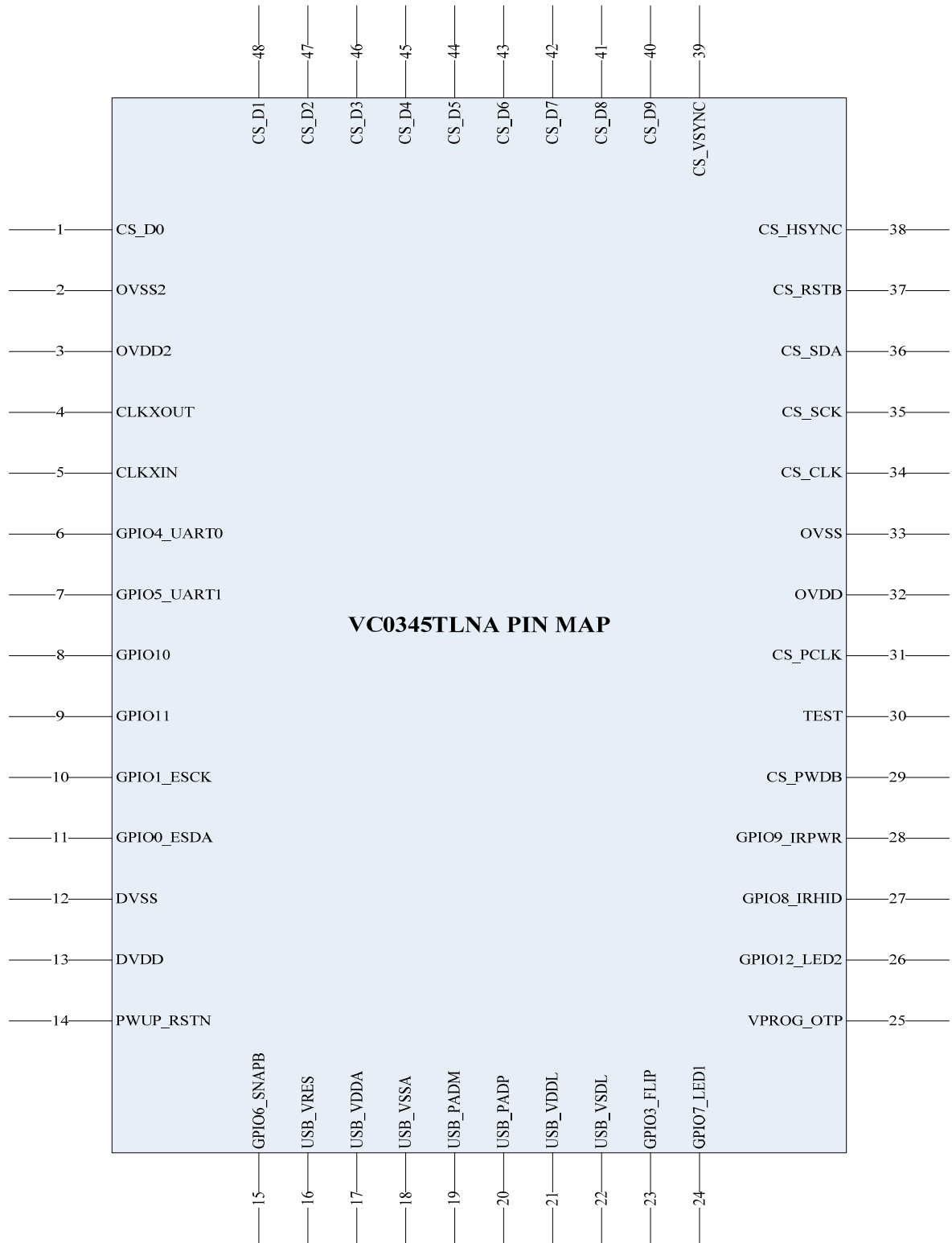


Figure 2: VC0345TLNA Pin Layout Diagram

6. ELECTRICAL CHARACTERISTICS

6.1 Recommended Operating Conditions

The recommended operating conditions are the recommended values to assure normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) described below are assured.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage:					
Core*	DVDD	1.62	1.80	1.98	V
I/O*	OVDD	3.0	3.3	3.6	V
Maximum input voltage	V_{Imax}	-	-	3.6	V
Operating Temperature	T_{OPR}	-20	-	+85	°C
Storage Temperature	T_{STOR}	-40	-	+150	°C

6.2 DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input low voltage	V_{IL}	-0.3	-	0.8	V
Input high voltage	V_{IH}	2	-	3.6	V
Input leakage current	I_{LI}	-	-	±10	μA
Input pull-up resistor	R_{PU}	38	54	83	kΩ
Input pull-down resistor	R_{PD}	25	49	110	kΩ
Output low voltage	V_{OL}	-	-	0.4	V
Output high voltage	V_{OH}	2.4	-	-	V
Low level output current @ $V_{OL}=0.4V$	I_{OL}	4.5	7.4	10.5	mA
High level output current @ $V_{OH}=2.4V$	I_{OH}	6.3	12.8	21.1	mA
Operation supply current*	I_{OP}	-	-	80	mA

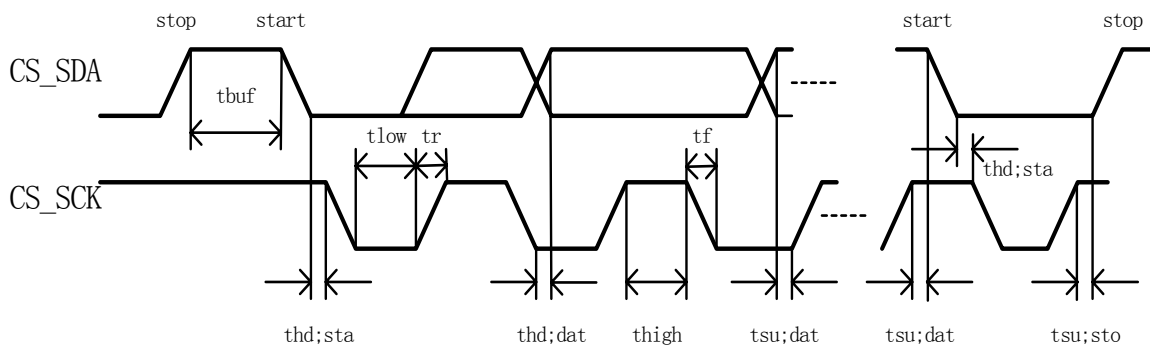
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Suspend supply current	I_{SUSP}	-	-	300	μA

* I_{OP} tested under 30fps@VGA and using 3.3V.

6.3 AC Characteristics

This section describes the AC characteristics of VC0345TLNA, including output delays, input setup, hold times, and all the interface timing.

6.3.1 Sensor Interface



PARAMETER	SYMBOL	MIN	MAX	UNIT
CS_SCK clock frequency	f_{sck}	0	100	KHz
Time that sensor serial bus must be free before a new transmission can start	t_{buf}	4.7	-	μs
Hold time for a start	$t_{hd;sta}$	4.0	-	μs
Low period of CS_SCK	t_{low}	4.7	-	μs
High period of CS_SCK	t_{high}	4.0	-	μs
Setup time for start	$t_{su;sta}$	4.7	-	μs
Data hold time	$t_{hd;dat}$	0	-	μs
Data setup time	$t_{su;dat}$	200	-	ns
Rise time of both CS_SDA and CS_SCK	t_r	-	1	μs
Fall time of both CS_SDA and CS_SCK	t_f	-	300	ns
Setup time for stop	$t_{su;sto}$	4.7	-	μs

7. PACKAGE INFORMATION

7.1 Chip Marking Information

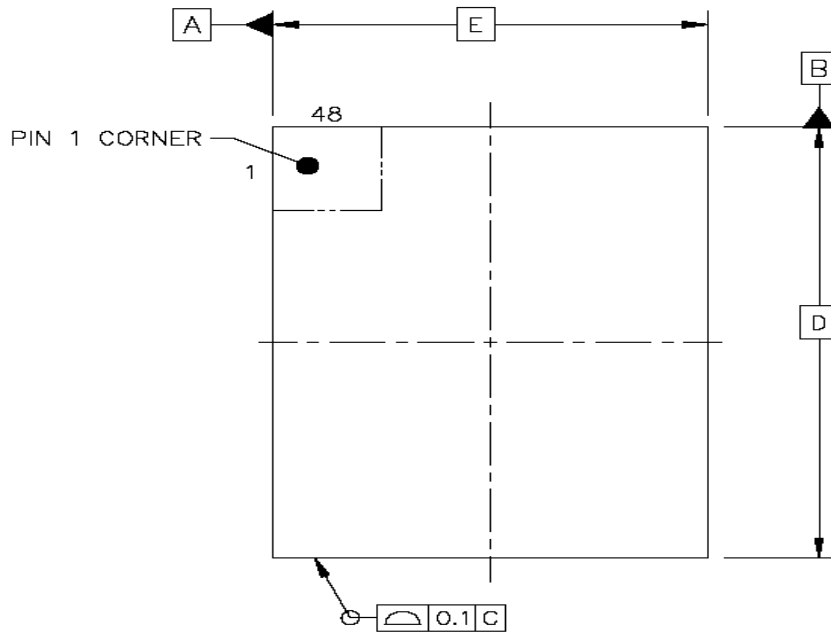
	LEAD-FREE PACKAGE
MARKING INFORMATION	Vimicro VC0345TLNA Tracking No.
Chip Marking for A version	Vimicro VC0345TLNAA Tracking No.

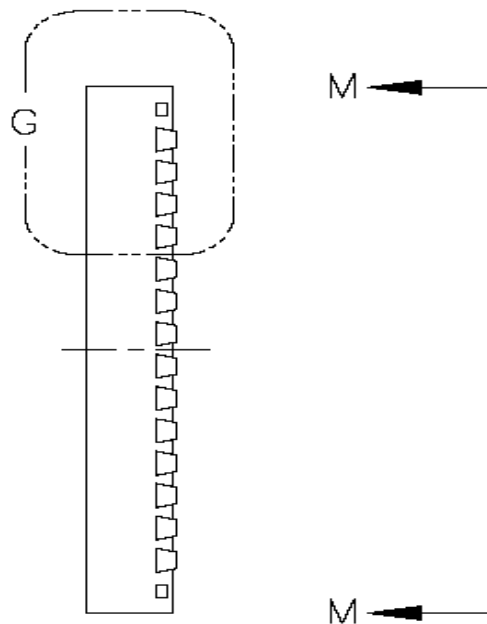
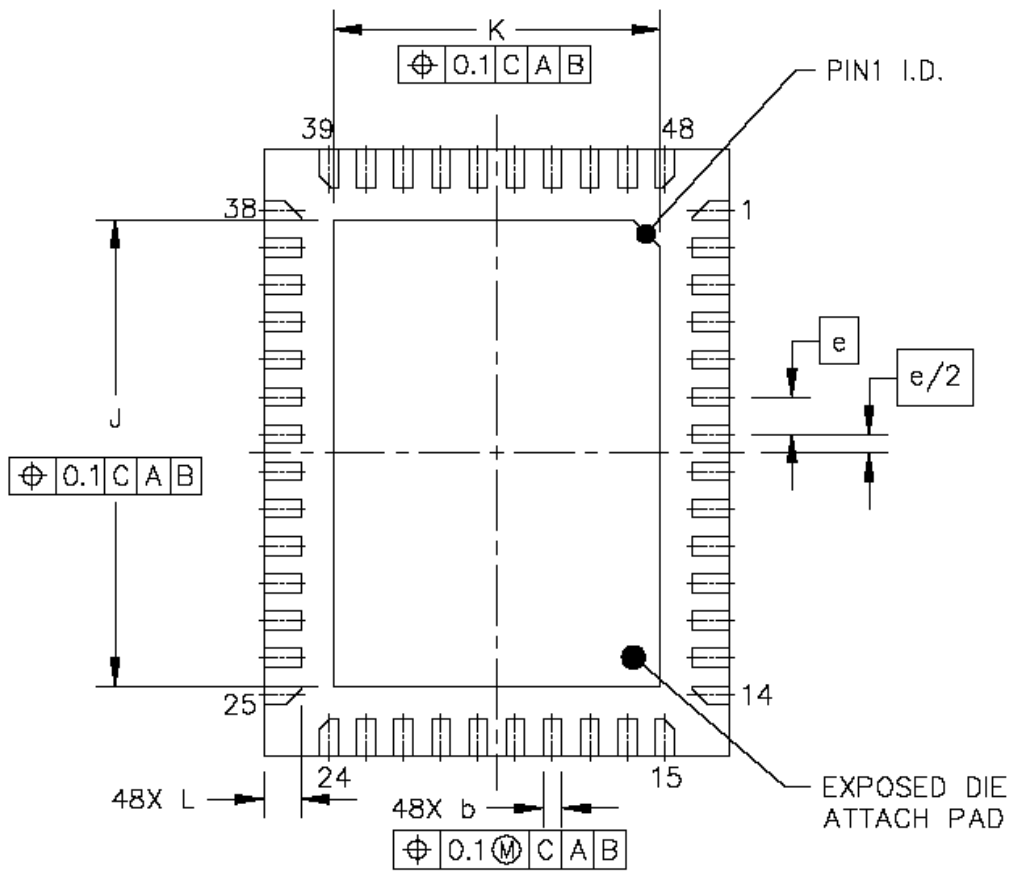
Note:

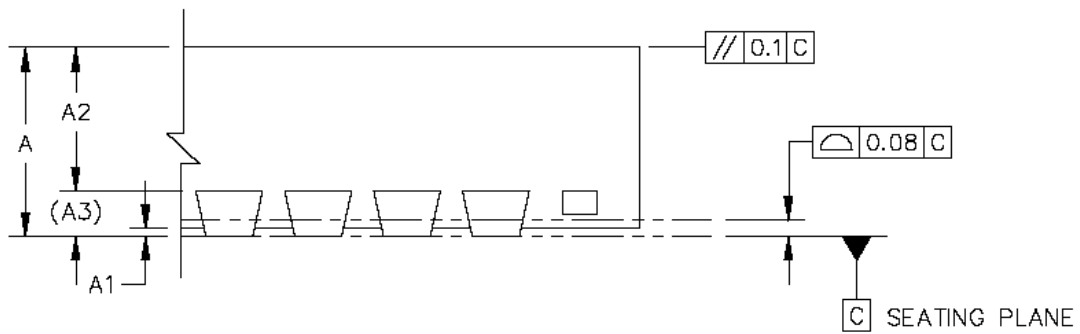
VC0345TLNA will use internal OTP memory to store firmware. So an extra letter (the 5th letter) is added to the package marking. For example:

- 1) VC0345TLNA will be a un-programmed chip with empty firmware in its OTP;
- 2) If the 1st version of the 345TLNA firmware code is authorized into production, we will mark the chip to be VC0345TLNAA;
- 3) If the 2nd version of the 345TLNA firmware code is authorized into production, we will mark the chip to be VC0345TLNAB.

7.2 VC0345TLNA Package Specification (6.5mm x 5mm)







DETAIL G
VIEW ROTATED 90° CLOCKWISE

VC0345TLNA Package Dimension (unit: mm)

DIM	MIN	NOM	MAX	NOTES
A	0.8	0.85	0.9	1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.
A1	0	0.035	0.05	
A2	---	0.65	0.67	
A3	0.203 REF			
b	0.15	0.2	0.25	
D	6.5 BSC			
E	5 BSC			
e	0.4 BSC			
J	4.9	5	5.1	
K	3.4	3.5	3.6	
L	0.35	0.4	0.45	

8. CONTACT INFORMATION

Vimicro Corporation
15/F Shining Tower
No.35 Xueyuan Road
Haidian District, Beijing
P. R. China 100083
Tel: 86-10-68948888
Fax: 86-10-68944075
Web: www.vimicro.com

Vimicro Corporation – USA
1758 N. Shoreline Blvd.,
Mountain View, CA 94043
USA
Tel: 1-650-966-1882
Fax: 1-650-966-1885

9. REVISION HISTORY

Version No.	Remarks	Release Date
0.1	Initial version released for engineering review.	2008-11-17
0.2	Updated version based on the feedbacks from engineering review.	2008-11-24
0.3	Misc. information update after review.	2008-11-27
1.0	Formal datasheet version for release.	2009-2-9