VC0528BRVC

Mobile Phone Video Processor

Datasheet

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1. GENERAL DESCRIPTIONS

VC0528BRVC is the cost down version from the VC0568 solution. It supports the sensor up to 0.3Mega, and uses SRAM technology. It is the most cost efficient mobile camera processor in the market place.

By integrating JPEG codec, sensor interface, LCD controller interface, VC0528BRVC enables mobile phone designers to quickly add camera solutions to their products with performance approaching leading digital still cameras.

VC0528BRVC can capture still images (up to 0.3 Mega resolutions) and video clips, and pass them to mobile phone baseband device, or receive JPEG images, MJPEG video from baseband device for LCD display.

VC0528BRVC can support hardwired image scaler, that supports zoom in and zoom out from 1/16 to 2x, VC0528BRVC also provides special image effects.

The following package is available:

PRODUCT NUMBER	REMARKS
VC0528BRVC PK	fpBGA, 100 pin, 3.3V CPU IF I/O, 3.3V Sensor and LCD IF IO, 16-bit LCD interface.

2. FEATURE LIST

System Architecture

- Provide a transparent, flexible physical bridge between mobile phone baseband processor, image sensor and LCD panel.
- With camera function off, host CPU can refresh LCD directly.
- To add camera function, mobile phone design only need minimal change with the help of VC0528BRVC and a API set provided by Vimicro.

Low Power Design

- 1.2V for core
- 2.6-3.3V for I/O

Host Interface

- Support ARM, 80-type and 68-type bus MCU
- In-direct addressing mode:
  - ✧ 1 bit address bus 16 bits data bus
  - ✧ 1 bit address bus 8 bits data bus

Sensor Interface

- Support up to 0.3M pixel off-shelf CMOS/CCD sensor
- Support CCIR656, CCIR601
- Strobe flash timing control
- Support both master/slave mode

JPEG Codec

- Standard baseline JPEG codec with dynamic bit-rate control
  - ✧ Encoder and decoder (non-simultaneous)
  - ✧ Variable size of image
  - ✧ Support different YUV type when encoding: 422, 420, 411 and gray
  - ✧ Support different YUV type when decoding: 444, 422, 420, 411 and gray
  - ✧ 128 quantization tables for both Y and C in compression
  - ✧ JPEG file header
  - ✧ Real-time video compression and decompression
  - ✧ Single clock Huffman coding and decoding
  - ✧ Up to four programmable quantization tables in decoding
  - ✧ Fully programmable Huffman tables (two AC and two DC) in decoding
  - ✧ Support up to four channels of component color
  - ✧ Support restart marker when decoding

Image Sizer and Digital Zoom

- Programmable image sub-sampling with anti-aliasing filtering
- Programmable image dithering
- Up to 16x digital zoom during preview, display mode
- 16x at 128x160 LCD resolution with 1280x1024 sensor resolution
- Support fully hardwired image scale up to 2x zoom (horizontally 2x and vertically 2x, in comparing to the original image size)
- Scaling up output resolution up to 1280x1024
- Real Zoom
- Continuous Zoom
- Hardware YUV to RGB conversion
- Programmable image dithering

Programmable Image Resolution and Data Format

- Support image resolution up to 1280x1024
- Hardware Thumbnail
    - ✧ Multiple output image formats
    - ✧ JPEG
    - ✧ Thumbnail: YUV422/ RGB565

LCD Controller Interface

- Support through mode, the host CPU will write the graphics data to the LCD panel through graphics SRAM.
- Supports parallel interface
- Supports dual LCD panels
- Supports TFT /UFB/STN/OLED LCD panels
- Supports LCD with following bit-depth: 8/12/16/18/24
- Supports LCD with following size: 160 x 120 ~ 320 x 240
- Supports OSD function
- Separate controls for layer A and layer B
- Backlight white LED control
- Illumination LED control

Video Post-processing

- Alpha-blending between video and host graphics
- Overlay between video and host graphics
- 90/180/270 degree image rotation and mirror function
- Special image effects:

    - ✧ Sepia
    - ✧ Speical Color

- ✧ Monochrome
- ✧ Negative

3. CHIP BLOCK DIAGRAM

3.1. Chip Block Diagram

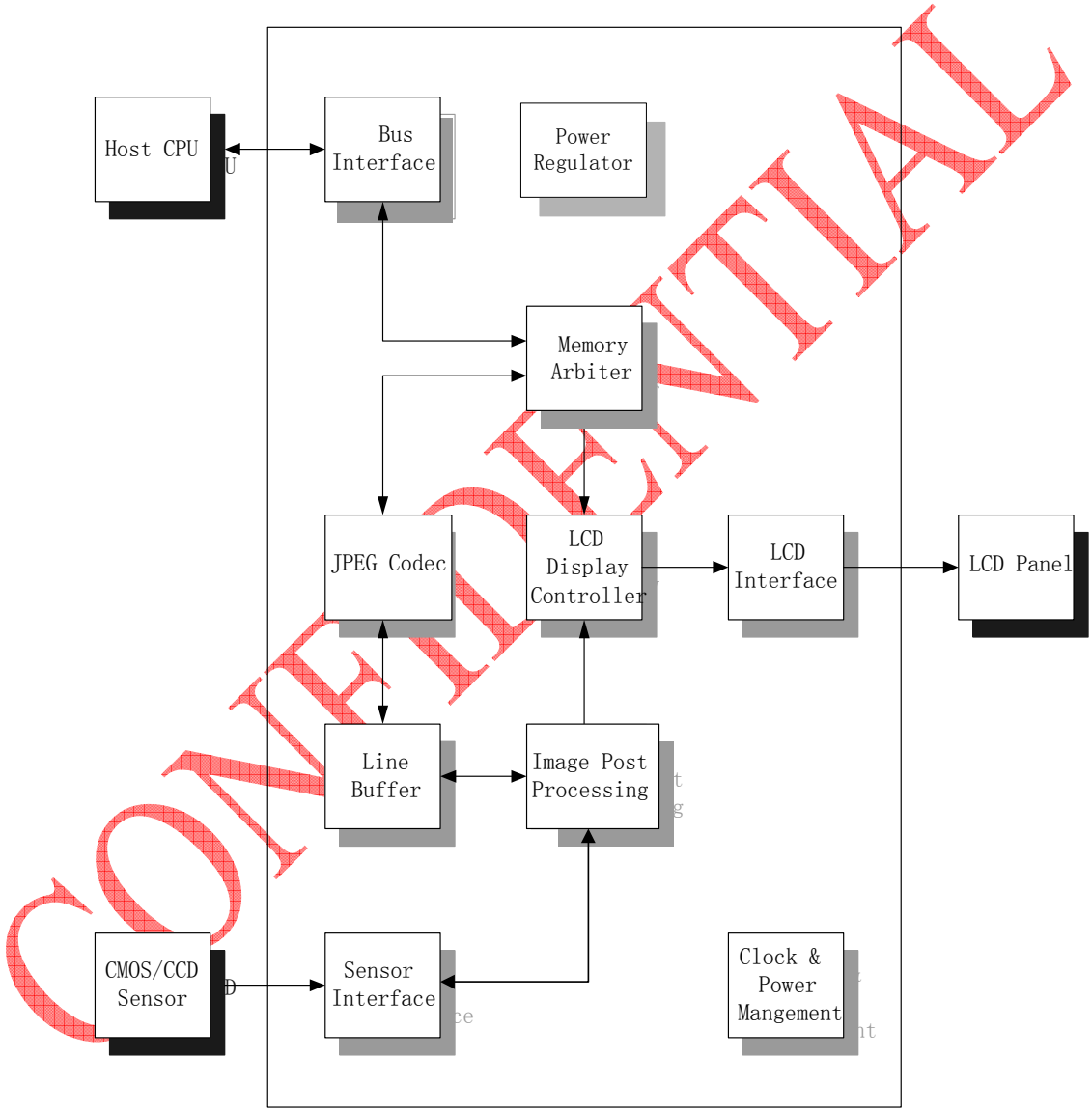


Figure 3-1 VC0528 Block Diagram

3.2. System Block Diagram

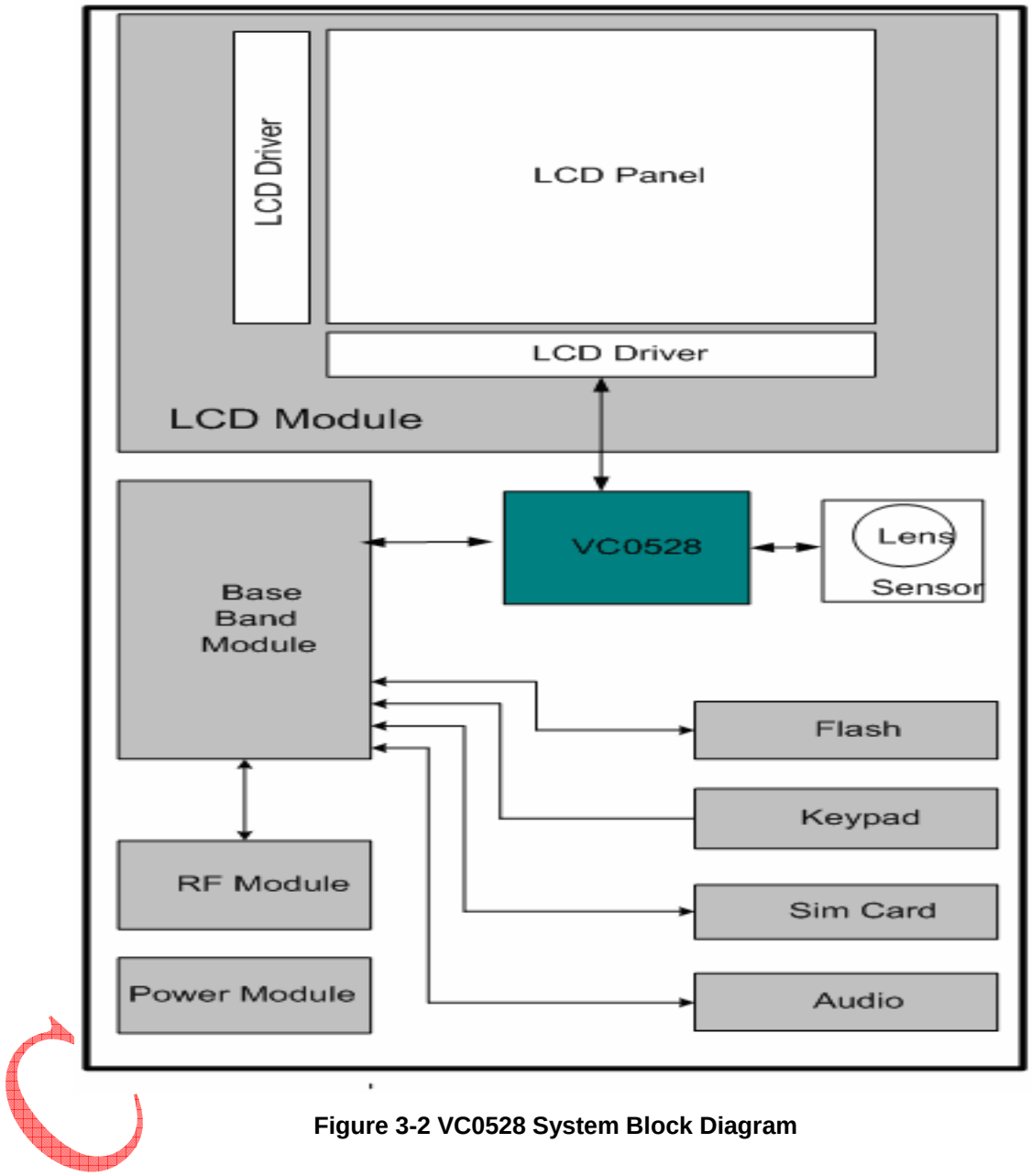


Figure 3-2 VC0528 System Block Diagram

4. KEY BLOCK DESCRIPTIONS

4.1. Overview

The main internal blocks in VC0528 are:

Sensor Interface (SIF)
Image data in YUV422 format is captured synchronously. The sensor clock is generated by VC0528 and it can be adjusted accordingly up to *48MHz*, while the pixel rate can reach *48MHz*. VC0528 supports up to 1280x1024 image resolution from the sensor. Serial bus interface is used for controlling the sensor.

Image Post Processing (IPP)
This module can add special effects to the image during capture and display, such as sepia, color range, negative, etc. Also, when the resolution of the input image from the sensor or host CPU does not match display or capture requirement, IPP can be used to convert these images into appropriate size, i.e., screen display size or the capture resolution set by users.

LCD Display Controller (LCDC)
This module generates the correct data for LCD panel to display. Alpha blending and overlay function between video and graphics from host CPU are supported. Rotation (90, 180 and 270 degree), mirror (horizontal and vertical) and gamma correction on video plane are all supported in this module.

LCD Panel Interface (LCDIF)
VC0528 supports TFT and STN-type LCD panels up to QVGA resolution (320x240). It communicates with the LCD panel through standard asynchronous 8/16 bit data bus with the color depth of 4/8/12/16/18 bit per pixel. Direct interface between host CPU and LCD panel is also supported.

JPEG Codec (JPEG)
VC0528 has an embedded JPEG codec for both image compression and decompression. The input of the encoder comes from either the sensor or the host CPU under different operation modes, and the output of the encoder is saved in on-chip SRAM for host CPU to read. The input of the decoder is from the on-chip SRAM which can be accessed by the host CPU and the decompressed data is sent back either to host CPU or LCD display. The JPEG CODEC supports YUV422, YUV411, YUV420, YUV400 data format.

Memory Arbiter (MARB)

The built-in 128KByte SRAM is used for storing the JPEG image data and graphics data. The size and position of graphics buffer and JPEG buffer can be configured dynamically. Some modules, such as JPEG, BIU, LCDC and IPP will address the on-chip SRAM. The memory arbiter will arrange the request from these modules and then response correctly.

Line Buffer (LBUF)

Two sets of 8-line buffer (1280x8x2 Bytes) are built in VC0528 for converting the data from line sequence to block sequence in capture mode and from block sequence to line sequence in display mode and decoder mode. The line buffer unit controls data read/write access to 8-Line Buffer. The two sets of 8-line buffer is configured as ping-pong architecture in capture and display modes. In decoder mode, one set is used as the FIFO to change block sequence to line sequence and the other is used for data storage after resizing.

Bus interface (BIU)

The host CPU can read/write the control registers and on-chip SRAM of VC0528 via host interface unit. VC0528 supports most popular CPUs such as ARM, XScale, and other 68/80-series CPUs. The data bus is 8bit/16bit (synchronous or asynchronous). The internal control bus is AMBA.

System Controller (CPM, including clock, reset and power management)

VC0528 has a variety of power management mechanisms to reduce power consumption. The internal clock can be stopped or modified by the clock control registers, and the internal PLL oscillation may be stopped under PLL bypass mode (note that the performance depends on the input clock frequency in PLL bypass mode). Also, the gated clock function stops the clock of non-operation block automatically. This unit also controls the action of the on-chip analog Phase-Locked-Loop (PLL).

Figure 3-2 The System Block Diagram shows a typical camera phone. VC0528 is the bridge between the baseband processor and LCD module, enabling mobile phones to capture and display still images and video clips at real-time. Most of the display and camera functions are conducted by VC0528, which will greatly reduce the burden on host CPU for computation-intensive image and graphics processing.

4.2. Detailed Description of Host Interface

4.2.1. 16-bit Multiplex Interface

In the 16-bit multiplex mode, the CPU_A8 pin is used as the address and data select pin. When CPU_A8 is set to '0', DATA[15:0] is the address of the memory or register to be accessed; when A8 is set to '1', DATA[15:0] is the data of the accessed cell. CPU_RS pin is used in directly through mode by mapping CPU_RS to LCD_RS when host CPU directly accesses the LCD panel.

In normal operation mode, the internal register and memory can be accessed according to the following table:

Table 4-1: Operation mode internal register and memory access

VC0528 side	CPU_ CS1N	CPU_ A8	CPU_ RS	CPU_ DATA	CPU_ ADDR	CPU_ WEN	CPU_ RDN	Operation mode
CPU side	H	-	-	-	-	-	-	Inactive mode
	L	L	-	DATA[7:0]	DATA[15:8]	L	H	Index address Write mode
	L	H	-	DATA[7:0]	DATA[15:8]	L	H	data Write mode
	L	H	-	DATA[7:0]	DATA[15:8]	H	L	Data Read mode

In through mode, the following table is the mapping between the LCD panel and host CPU:

Table 4-2: Through mode mapping between LCD panel & host CPU

VC0528 side	CPU_ CS1N	CPU_ A8	CPU_ RS	CPU_ DATA	CPU_ ADDR	CPU_ WEN	CPU_ RDN	Operation mode
CPU side	H	-	-	-	-	-	-	Inactive mode
	L	L	LCD_RS	LCD_DATA [7:0]	LCD_DATA [15:8]	L	H	Index address Write mode
	L	L	LCD_RS	LCD_DATA [7:0]	LCD_DATA [15:8]	L	H	Data Write mode
	L	L	LCD_RS	LCD_DATA [7:0]	LCD_DATA [15:8]	H	L	Data Read mode

There are several methods for writing data into a register or memory cell:

1. When writing data to a register:

- Write index address register (A8=0);
- Write control data (A8=1)

2. When writing data to the memory;

- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_FLG);
- Write control data (A8 = 1);

For the meaning of the above register, please see the register table.

3. Address increment automatic access (memory access)

- Set sel_port and sel_write (SEL_PORT, SEL_WRITE);
- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_FLG);
- Write control data (A8 = 1);
- Write control data (A8 = 1) ….

Normal register read cycle:

1. When reading data from a register

- Write index address of register (A8 = 0);
- Control data is outputted (A8 = 1)

2. When reading data from memory

- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_FLG);
- Read control data (A8 = 1);

3. Address increment automatic access (memory access)

- Set the sel_port and sel_read register (SEL_PORT, SEL_READ);
- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_FLG);
- Write control data (A8 = 1);
- Write control data (A8 = 1) ….

4.2.2. 8-bit Multiplex Interface

In the 8-bit multiplex mode, the A8 pin is used as address and data select pin.

Operation mode for normal register

Table 4-3: Operation mode normal register

CSN	A8	RS	DATA	ADDR	WEN	RDN	OPERATION MODE
H	-	-	-	-	-	-	Inactive mode
L	L	-	DATA[7:0]	-	L	H	Index address Write mode
L	H	-	DATA[7:0]	-	L	H	Data Write mode
L	H	-	DATA[7:0]	-	H	L	Data Read mode

Normal register/memory writing:

1. Data/memory writing:

- Write register high address index (REG_8_HIGH_WORD);
- Write address high 8 bits;
- Write register low address index (REG_8_LOW_WORD);
- Write address low 8 bits;
- Write register flag index (REG_8_FLG);
- Write control data (A8 = 1).

2. Write data to the same index address successively (memory access)

- Write index address of memory register according to above register write method (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port index address (MEM_8_FLG) ;
- Write control data (A8 = 1);

3. Address increment automatic access (memory access)

- Set the increment register according (INCREMENT);
- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_8_FLG);
- Write control data (A8 = 1);
- Write control data (A8 = 1) ….

Note: in the access mode, the address is increased automatically

Normal register read cycle:

1. Data/register read:

- Write register high address index (REG_8_HIGH_WORD);
- Write address high 8 bits;
- Write register low address index (REG_8_LOW_WORD);
- Write address low 8 bits;
- Write register flag index (REG_8_FLG);
- Read control data (A8 = 1);

2. Memory read:

- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_8_FLG);
- Read control data (A8 = 1);
- Read control data (A8 = 1)….

3. Address increment automatic access (memory access)

- Set the increment register (INCREMENT);
- Write index address of register (MEM_LOW_WORD, MEM_HIGH_WORD);
- Write port address (MEM_8_FLG);
- Read control data (A8 = 1);
- Read control data (A8 = 1) ….

4.3. Chip Configuration

The CONF pin is used to configure the chip and should be connected to the VSS or VDD before chip reset.

Table 4-4: CONF Configuration

CONFIGURATION INPUT	DESCRIPTION
CONF [1:0]	Host bus interface type “000”: type 0; “001”: type 1; “010”: type 2; “011”: type 3;

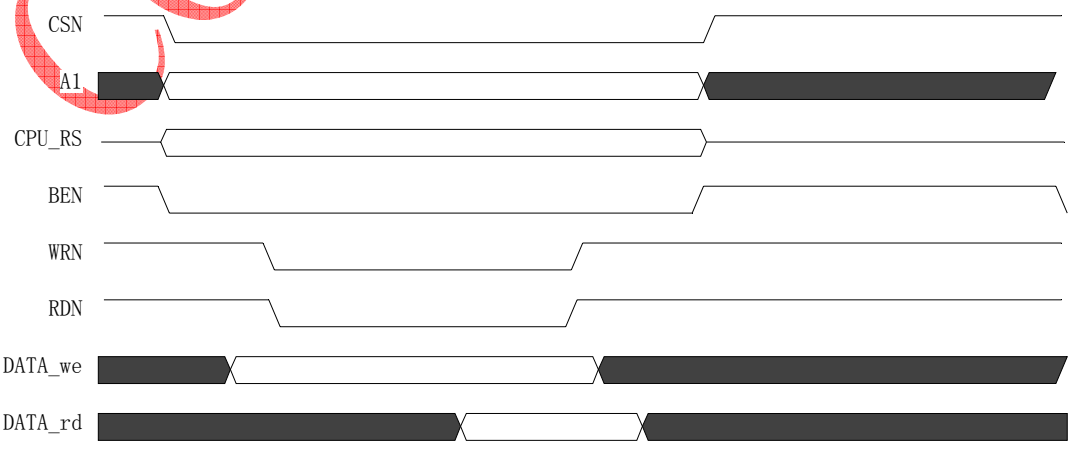
For different bus type, the CPU interface has different configuration, which can be seen in the following table.

Table 4-5: CPU Configuration

PIN NAME	TYPE0	TYPE1	TYPE2	TYPE3
ADDR [7:0]	DATA [15:8]	DATA [15:8]	DATA [15:8]	DATA [15:8]
CPU_A8	A1	A1	A1	A1
CPU_RS	Low	Low	Low	Low
DATA	DATA [7:0]	DATA [7:0]	DATA [7:0]	DATA [7:0]
CSN	CS#	CS#	CS#	CS#
RDN	RD#	RD#	RDL#	High
WEN	WR#	High	WRL#	R/W#
BEN[1]	UBE#	WRU#	RDU#	UDS#
BEN[0]	LBE#	WRL#	WRU#	LDS#

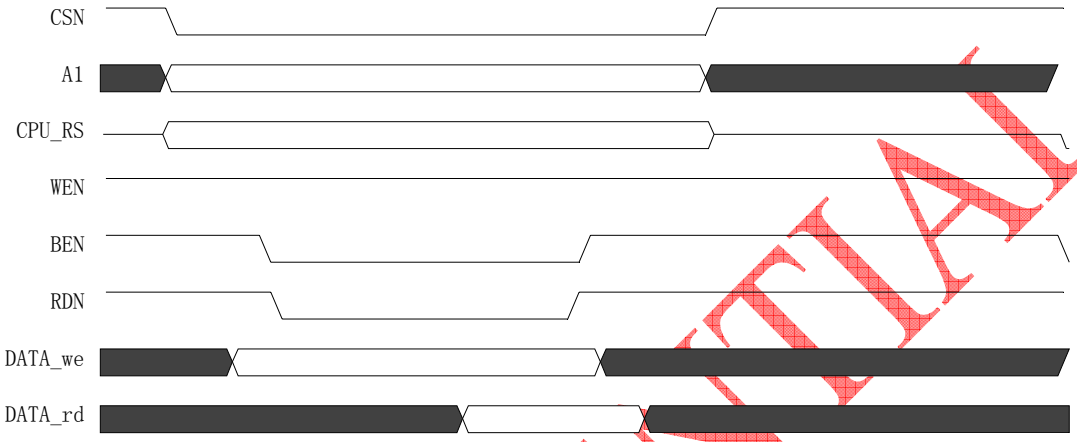
A1: address/data select pin
RDL#: read data low byte enable
RDU#: read data high byte enable
WRL#: write data low byte enable
WRU#: write data high byte enable
R/W#: CPU write/read signal(68 type)
UBE#: upper byte enable
LBE#: low byte enable
LDS#: low data select pin
UDS#: upper data select pin

4.3.1. Multiplex 80 type 0



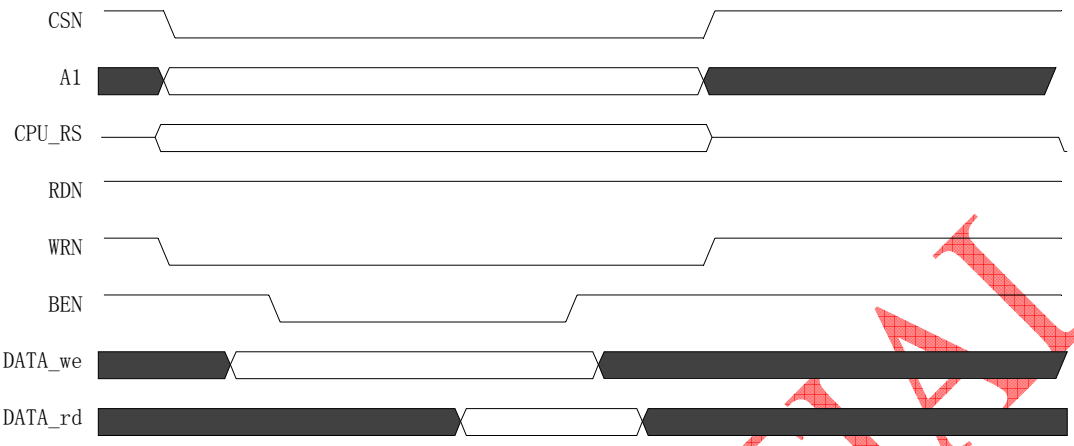
Note: WRN and RDN share using the BEN they do not care about the CPU_RS value.

4.3.2. Multiplex 80 type 1



4.3.3. Multiplex 80 type 2

4.3.4. 68 type 3



4.4. Operating Mode

The following operation modes are supported in VC0528 accompanied with Camera module and LCD panel:

4.4.1. Viewfinder Mode

In viewfinder mode, continuous video stream (up to 30fps) from the sensor is shown on the LCD panel with no frame delay. The user can adjust the zooming factor and images of different resolutions will be displayed on the LCD. When the user is happy with the image frame on display, the user can push a button and capture it. The chip will then go to the capture mode.

In viewfinder mode, the following features are supported:

- Video streaming at high frame rate (up to 30fps)
- No frame delay (What you see is what you capture!)
- Zoom in/out
- Add frame on the video
- Configurable display window

4.4.2. Capture Mode

VC0528 can capture still images, multi-shot and video clip.

When capturing still image, the user first chooses an appropriate frame in the viewfinder mode, then they can press a capture button and the next frame from the image sensor will be captured. The JPEG compression image is stored in the internal SRAM and the host CPU can read the data. The user can choose the image size to be captured and whether there is a 'frame' outside the captured image or not. VC0528 has an on-chip buffer for capturing high-quality still images up to 0.3M pixels in JPEG format. Thumbnail with configurable size can be generated accompanied with the JPEG image data.

When capturing multi-shot, the user first pushes the capture button, and then VC0528 will capture consecutive TBD images at TBD interval from image sensor. The images will be resized to VGA size and compressed as JPEG files along with a thumbnail version, and stored in an on-chip buffer. Each image will be assigned a unique number internally for reference. The thumbnail images will be sent to LCD for display side by side. When the user selects one of the thumbnail images, the corresponding VGA sized image will be sent to LCD for display at the right size and bit depth. 2-D graphics functions (including special image effects) are supported in capture mode.

After the user pushes the capture button, VC0528 will capture the video stream from image sensor, until he/she pushes the stop button. The video stream will be compressed as AVI file, and then sent to baseband processor. At the same time, video frames of the right size and bit-depth will be sent to the LCD for display. 2-D graphics functions (including special image effects) are supported in capture mode. VC0528 will allow the user to capture video up to 320 x 240.

The captured still image, multi-shot and video clip can be sent to the host CPU or the storage card.

In capture mode, the following features are supported:

- Capture still images up to 0.3Mega resolution
- Capture SIF (320x240), QSIF (160x120) and QQSIF (80x60) MJEPG video clip
- Capture still image with various resolution of thumbnail
- Capture still image with overlay
- Capture still image with alpha-blending
- Capture multi-shot with VGA resolution

4.4.3. Display Mode

Under display mode, JPEG image or AVI saved in host memory or the storage card will be sent to VC0528, where it will be prepared (right size and bit depth) for LCD display. 2-D

graphics functions are supported in display mode.

In display mode, the following features are supported:

- Receive JPEG still image or MJPEG video clip from host CPU
- Decode and display on LCD with right size and color depth
- Support various image format: 4:4:4, 4:2:2, 4:1:1, 4:2:0, 4:0:0
- Support JPEG image up to resolution 0.3Mega pixels
- Resize the image with anti-aliasing pre-filtering
- Add frame to the image
- Add special effect to the image

4.4.4. JPEG Decode Mode

It is possible to use VC0528 as a JPEG decoding engine. When it is used as a JPEG decoder, the JPEG data is written to internal 128KB SRAM similar to the display mode and then decompressed by JPEG codec. But the decompressed data is sent back to the host CPU, other than LCD panel. The decoding result (YUV444/YUV422/YUV411/YUV420) is written in 8-line buffer. When data of 8 lines (YUV422/YUV411/YUV444) or 16 lines (YUV420) is decompressed, an interrupt is issued and the host CPU will read the data. Then the host CPU will restart the decompression. Then 'Interruption-read-restart' repeats until decompression of one frame is complete.

In JPEG decoder mode, the following features are supported:

- Receive JPEG image from host CPU
- Decode the JPEG image to YUV image data
- Add optional special effect to the image
- Resize the image data to specific resolution
- Send the YUV image data back to host CPU
- Support 4:4:4, 4:2:2, 4:1:1, 4:2:0
- Support JPEG image up to VGA resolution

4.4.5. JPEG Encode Mode

VC0528 can also be used as a JPEG encoder. At this mode, image data can be encoded into JPEG format by writing the image data in the specific registers one by one. Data of YUV422/YUV411/YUV420/YUV400 is written to the register in block sequence (8x8). The compressed JPEG data is saved in the internal 128KB SRAM and then is read by the host CPU after one frame is completed.

In JPEG encoder mode, the following features are supported:

- Receive YUV image data from host CPU
- Encode the image to JPEG format
- Send the JPEG image back to host CPU
- Support 4:2:2, 4:1:1, 4:2:0
- Support JPEG image up to VGA resolution

4.4.6. Through Mode

In this mode, the camera functions are disabled. The host CPU will read/write the LCD module directly. VC0528 supports two ways for interfacing LCD panel in this mode: i) through registers for forwarding the index and the data to the LCD panel. Conversion from 8bit to 16bit of can be supported; ii) directly mapping the data and address from host CPU to LCD panel and there is no registers between host CPU and LCD panel, just like the host CPU interface LCD panel directly.

In through mode, the following features are supported:

- Video function is disabled
- Host CPU update LCD panel directly
- Directly pin mapping between host CPU and LCD module
- Index register for address and data for host CPU to update LCD
- Low power

5. PIN ASSIGNMENT

5.1. Pin Descriptions

PIN NAME	I/O TYPE	BALL PIN	DESCRIPTIONS	LEVEL DURING		SUPPLY
				BYPASS	ACTIVE	
SYSTEM PINS						
INT	I	B4	Interrupt to the host CPU	CFG	*	OVDD2
XCLK	I	F12	Clock from the host CPU or oscillator	INPUT	INPUT	OVDD3
TEST	B,	M1	Test mode enable	INPUT0	INPUT0	OVDD8
RSTN	I, S	A4	Reset signal, active low	INPUT1	INPUT1	OVDD1
PR_CAP	I	A1	TOCAP pin for LDO, should be connected with a 4.7uF cap.	-	-	-
GLOBAL PURPOSE IO						
GPIO0	I, PD	F2	Global purpose IO pin, bit [0]	CFG	CFG	OVDD3
GPIO1	I, PD	F1	Global purpose IO pin, bit [1]	CFG	CFG	OVDD3
GPIO2	B, PU	L7	Global purpose IO pin, bit [2], shared with sensor pclk input	CFG	CFG,*	OVDD4
GPIO3	B, PU	M7	Global purpose IO pin, bit [3], shared with flash trigger	CFG	CFG,*	OVDD4
GPIO4	B, PU	J7	Global purpose IO pin, bit [4], shared with flash charge	CFG	CFG,*	OVDD4
CPU INTERFACE WITH THE BASEBAND						
CONF0	I	D4	Configuration pin for CPU bus, bit 0	INPUT	INPUT	OVDD1
CONF1	I	B3	Configuration pin for CPU bus, bit 1	INPUT	INPUT	OVDD1
CPU_CS2N	B	L9	Chip select 2, active low	INPUT	INPUT	OVDD2
CPU_CS1N	B	L8	Chip select 1, active low	INPUT	INPUT	OVDD2
CPU_RS	B, PU	B12	Register select	INPUT	INPUT	OVDD1
CPU_A8	B, PU	A12	Address bus / HOST register select	INPUT	INPUT	OVDD1
CPU_WBEN0	I	G1	Write byte enable, bit [0]	INPUT	INPUT	OVDD1
CPU_WBEN1	I	H4	Write byte enable, bit [1]	INPUT	INPUT	OVDD1
CPU_WEN	I	H1	Write signal, active low	INPUT	INPUT	OVDD1
CPU_OEN	I	H2	Output enable, active low	INPUT	INPUT	OVDD1

PIN NAME	I/O TYPE	BALL PIN	DESCRIPTIONS	LEVEL DURING		SUPPLY
				BYPASS	ACTIVE	
CPU_ADDR0	B, PD	L11	Address bus between host CPU and VC0528, bit [0]	INPUT	INPUT	OVDD2
CPU_ADDR1	B, PD	L12	Address bus between host CPU and VC0528, bit [1]	INPUT	INPUT	OVDD2
CPU_ADDR2	B, PD	K11	Address bus between host CPU and VC0528, bit [2]	INPUT	INPUT	OVDD2
CPU_ADDR3	B, PD	K12	Address bus between host CPU and VC0528, bit [3]	INPUT	INPUT	OVDD2
CPU_ADDR4	B	B11	Address bus between host CPU and VC0528, bit [4]	INPUT	INPUT	OVDD1
CPU_ADDR5	B	A11	Address bus between host CPU and VC0528, bit [5]	INPUT	INPUT	OVDD1
CPU_ADDR6	B	B10	Address bus between host CPU and VC0528, bit [6]	INPUT	INPUT	OVDD1
CPU_ADDR7	B	B9	Address bus between host CPU and VC0528, bit [7]	INPUT	INPUT	OVDD1
CPU_D0	B	C2	Data bus between host CPU and VC0528, bit [0]	*	*	OVDD1
CPU_D1	B	C1	Data bus between host CPU and VC0528, bit [1]	*	*	OVDD1
CPU_D2	B	D2	Data bus between host CPU and VC0528, bit [2]	*	*	OVDD1
CPU_D3	B	E2	Data bus between host CPU and VC0528, bit [3]	*	*	OVDD1
CPU_D4	B	L3	Data bus between host CPU and VC0528, bit [4]	*	*	OVDD2
CPU_D5	B	M3	Data bus between host CPU and VC0528, bit [5]	*	*	OVDD2
CPU_D6	B	L4	Data bus between host CPU and VC0528, bit [6]	*	*	OVDD2
CPU_D7	B,	L5	Data bus between host CPU and VC0528, bit [7]	*	*	OVDD2
LCD INTERFACE						
LCD_D0	B	A2	Data bus to the LCD panel, bit [0]	*	*	OVDD3
LCD_D1	B	B1	Data bus to the LCD panel, bit [1]	*	*	OVDD3
LCD_D2	B	E1	Data bus to the LCD panel, bit [2]	*	*	OVDD3
LCD_D3	B	F4	Data bus to the LCD panel, bit [3]	*	*	OVDD3

PIN NAME	I/O TYPE	BALL PIN	DESCRIPTIONS	LEVEL DURING		SUPPLY
				BYPASS	ACTIVE	
LCD_D4	I	L1	Data bus to the LCD panel, bit [4]	*	*	OVDD6
LCD_D5	I	M2	Data bus to the LCD panel, bit [5]	*	*	OVDD6
LCD_D6	B	M5	Data bus to the LCD panel, bit [6]	*	*	OVDD4
LCD_D7	B	J6	Data bus to the LCD panel, bit [7]	*	*	OVDD4
LCD_D8	B	J11	Data bus to the LCD panel, bit [8]	*	*	OVDD6
LCD_D9	B	H11	Data bus to the LCD panel, bit [9]	*	*	OVDD6
LCD_D10	B	H12	Data bus to the LCD panel, bit [10]	*	*	OVDD6
LCD_D11	B	G9	Data bus to the LCD panel, bit [11]	*	*	OVDD6
LCD_D12	B	A9	Data bus to the LCD panel, bit [12]	*	*	OVDD8
LCD_D13	B	B8	Data bus to the LCD panel, bit [13]	*	*	OVDD8
LCD_D14	B	A8	Data bus to the LCD panel, bit [14]	*	*	OVDD8
LCD_D15	B	D7	Data bus to the LCD panel, bit [15]	*	*	OVDD8
LCD_WRN	B	D6	LCD Write strobe to be asserted in write operation	*	*	OVDD8
LCD_RDN	B	A7	LCD Read strobe to be asserted in read operation	*	*	OVDD8
LCD_RST	B	E9	LCD panel reset	*	*	OVDD3
LCD_RS	B	D11	LCD Register Select index and command register	*	*	OVDD3
LCD_CS1N	B	J8	LCD Chip Select for main panel	*	*	OVDD4
LCD_CS2N	B	M8	LCD Chip Select for sub panel	*	*	OVDD4
SENSOR INTERFACE						
CS_D0	B, PD	M12	Video data input from camera module, bit [0]	INPUT	INPUT	OVDD6
CS_D1	B, PD	M11	Video data input from camera module, bit [1]	INPUT	INPUT	OVDD6
CS_D2	B, PD	L10	Video data input from camera module, bit [2]	INPUT	INPUT	OVDD6
CS_D3	B, PD	M10	Video data input from camera module, bit [3]	INPUT	INPUT	OVDD6
CS_D4	B	K2	Video data input from camera module, bit [4]	INPUT	INPUT	OVDD6
CS_D5	B	J4	Video data input from camera module, bit [5]	INPUT	INPUT	OVDD6
CS_D6	B	J1	Video data input from camera module, bit [6]	INPUT	INPUT	OVDD6

PIN NAME	I/O TYPE	BALL PIN	DESCRIPTIONS	LEVEL DURING		SUPPLY
				BYPASS	ACTIVE	
CS_D7	B	J2	Video data input from camera module, bit [7]	INPUT	INPUT	OVDD6
CS_SCK	B	E11	Serial clock for camera module control	INPUT	*	OVDD6
CS_SDA	B	E12	Serial data for camera module control	INPUT	*	OVDD4
CS_PWDN	B	D12	Power down signal of camera module	CFG	*	OVDD4
CS_ENB	B	C11	Camera module enable signal	CFG	*	OVDD4
CS_VSYNC	B, PD	A6	Vertical synchronous signal to/from camera module	CFG	*	OVDD8
CS_HSYNC	B, PD	D5	Horizontal synchronous signal to/from camera module	CFG	*	OVDD8
CS_CLK	B,	A5	Synchronous clock of camera data transfer (max.27MHz)	CFG	*	OVDD8
CS_RSTN	B,	B5	Camera module reset signal	CFG	*	OVDD8
POWER AND GROUD						
OVDD1	P	D1	IO power for CPU interface, 1.8v	-	-	-
OVDD2	P	K1				
OVSS1	G	E4	IO ground for CPU interface	-	-	-
OVSS2	G	L2				
OVDD3	P	M4	IO power for sensor and LCD interface, whose voltage should be the same with the sensor module and LCD panel. It's 3.3v	-	-	-
OVDD4	P	M9				
OVDD5	P	J12				
OVDD6	P	C12				
OVDD7	P	A10				
OVDD8	P	A3				
OVSS3	G	J5	IO ground for sensor and LCD interface	-	-	-
OVSS4	G	J9				
OVSS5	G	H9				
OVSS6	G	D9				
OVSS7	G	D8				
OVSS8	G	B2				
DVDD1	P	G2	Core power for internal PMU module	-	-	-
DVSS1	G	G4	Core ground for internal PMU module	-	-	-

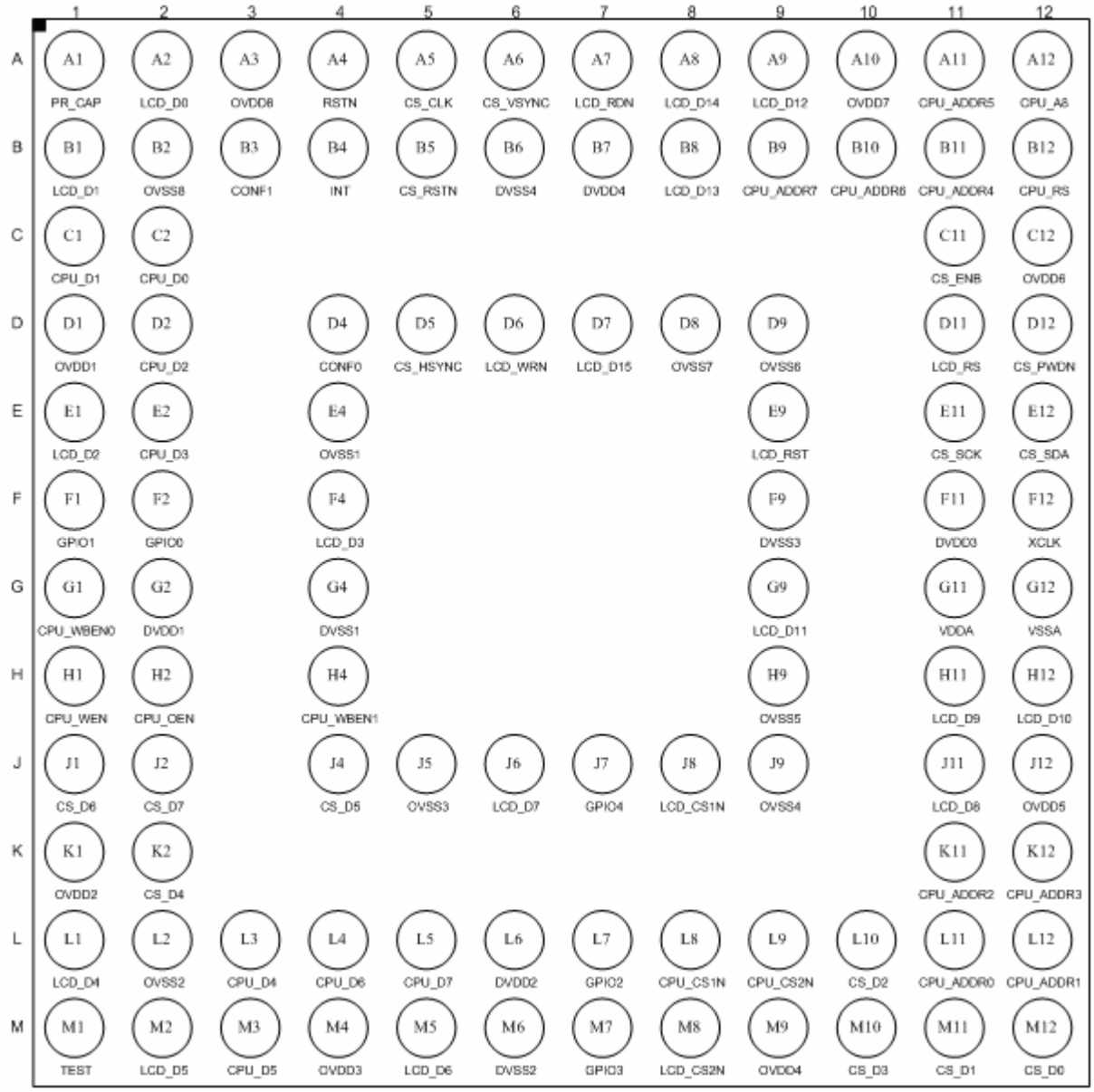
PIN NAME	I/O TYPE	BALL PIN	DESCRIPTIONS	LEVEL DURING		SUPPLY
				BYPASS	ACTIVE	
DVDD2	P	L6	Internal LDO's output which provides the power of the other digital core logic	-	-	-
DVDD3	P	F11	power of the other digital core logic	-	-	-
DVDD4	P	B7				
DVSS2	G	M6	Ground for the other digital core logic	-	-	-
DVSS3	G	F9				
DVSS4	G	B6				
VDDA	P	G11	PLL power	-	-	-
VSSA	G	G12	PLL ground	-	-	-

I = Input
O = Output
B = Bi-directional
P = Power
G = Ground
PD = Pull down
PU = Pull up

S = Schmitt trigger
CFG= Can be configured by baseband
INPUT = The IO is under input mode, IO's voltage is decided by the outside
* = Can output High or Low
INPUT0 = Must keep the Low voltage
INPUT1 = Must keep the High voltage

6. PIN LAYOUTS

6.1. VC0528 Pin-out Diagram



VC0528 fpBGA-100 Pin-out Diagram – Top View

7. ELECTRICAL CHARACTERISTICS

7.1. Absolute Maximum Ratings

Permanent device damage may occur if absolute maximum ratings are exceeded, hence the maximum ratings must never be exceeded. Functional operation should be restricted to the conditions as detailed in recommended operating conditions. Exposure to the absolute maximum conditions for extended periods may affect device reliability.

PARAMETER	SYMBOL	MIN	MAX	UNIT
Input voltage	V_I	-0.5	4.6	V
Output voltage	V_O	-0.5	4.6	V
Pre-driver power supply voltage	-	-0.5	1.8	V
Post-driver power supply voltage	-	-0.5	4.6	V
Operation temperature	T_{OPT}	-40	125	℃
Storage temperature	T_{STG}	-65	150	℃

7.2. Recommended Operating Conditions for 3.3V IO Application

The recommended operating conditions are the recommended values for assuring normal logic operation. As long as the device is used within the recommended operating conditions, the electrical characteristics (DC and AC characteristics) described below are assured.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Pre-driver supply voltage	VDD	1.08	1.2	1.32	V
I/O supply voltage	VDD33	2.6	3.3	3.63	V
Input high voltage	V_{IH}	2.0	-	VDD33+0.3	V
Input low voltage	V_{IL}	-0.3	-	0.8	V
Threshold point	V_T	1.31	1.42	1.54	V
Schmitt trig low to high threshold point	V_{T+}	1.57	1.65	1.72	V
Schmitt trig high to low threshold point	V_{T-}	0.94	1.01	1.07	V
Junction temperature	T_J	0	25	125	°C
Input leakage current	I_L	-	-	±1	uA
Tri-state output leakage current	I_{OZ}	-	-	±1	uA
Pull-up resistor	R_{PU}	56	73	113	Kohm
Pull-down resistor	R_{PD}	55	79	155	Kohm
Output low voltage @I_{OL}=4mA	V_{OL}	-	-	0.4	V
Output high voltage @I_{OH}=4mA	V_{OH}	2.4	-	-	V
Low level output current @V_{OL}=0.4V	I_{OL}	4.5	7.4	9.3	mA
HIGH LEVEL OUTPUT CURRENT @VOH=2.4V	I_{OH}	4.5	9.4	14.7	mA

*The value of the supply voltage is the typical case.

7.3. Working Current

Table 7-1: Working Current

CURRENT MODE STYLE	3.3V(MA)	
	IO & CORE	PLL
Viewfinder Mode	*17.62*	*0.490*
Capture Mode	*22.68*	*0.490*
Display Mode	*20.31*	*0.490*
Through Mode	*0.065*	*0.003*

7.4. AC Characteristics

This section describes the VC0528 AC characteristics, which consist of output delays, input setup and hold times and all the interface timing.

7.4.1. Host Interface

Multiplex Interface Characteristics

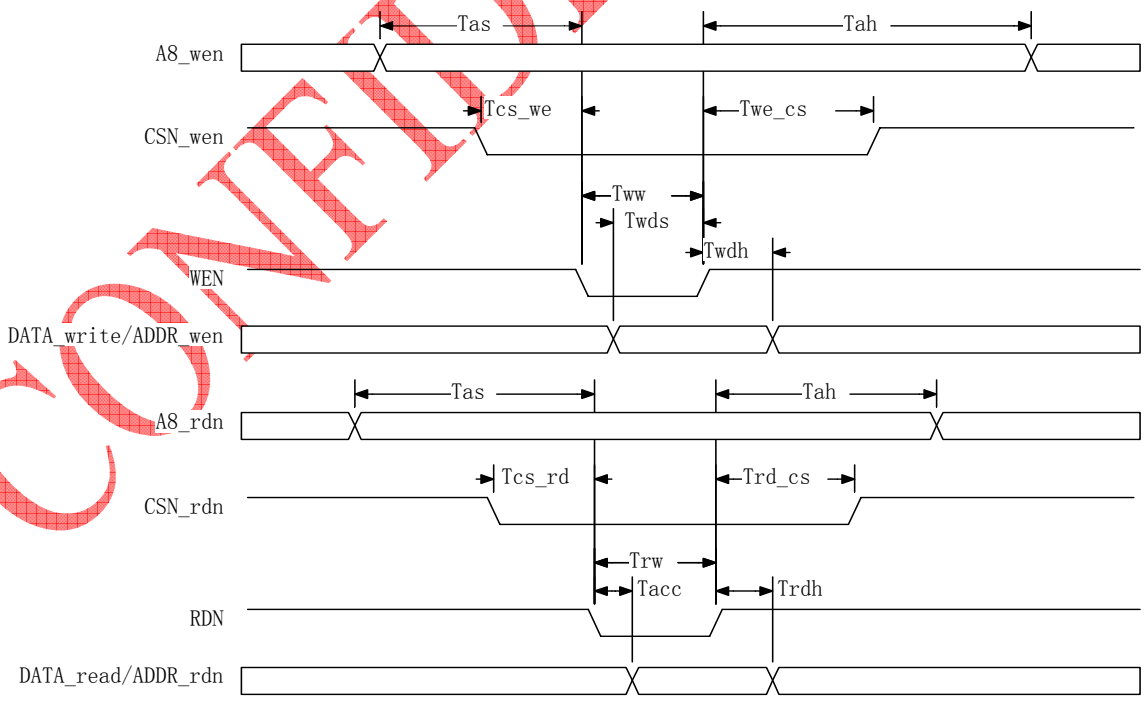


Table 7-2: Host Interface

ITEM	SYMBOL	MIN	TYPICAL	MAX	UNIT
Address setup time	Tas	0	-	-	ns
Address hold time	Tah	13.8	20	-	ns
Cs setup time at write status	Tcs_we	0	-	-	ns
Cs hold time at write status	Twe_cs	0	-	-	ns
Data setup time	Twds	12.2	24	-	ns
Data hold time	Twdh	8.8	10	-	ns
Write width	Tww	120	-	-	ns
Cs setup time at read status	Tcs_rd	0	-	-	ns
Cs hold time at read status	Trd_cs	0	-	-	ns
Read data access time	Tacc	120	-	-	ns
Read width	Trw	120	-	-	ns
Data hold time	Trdh	2.5	-	-	ns

7.4.2. LCD Panel Interface

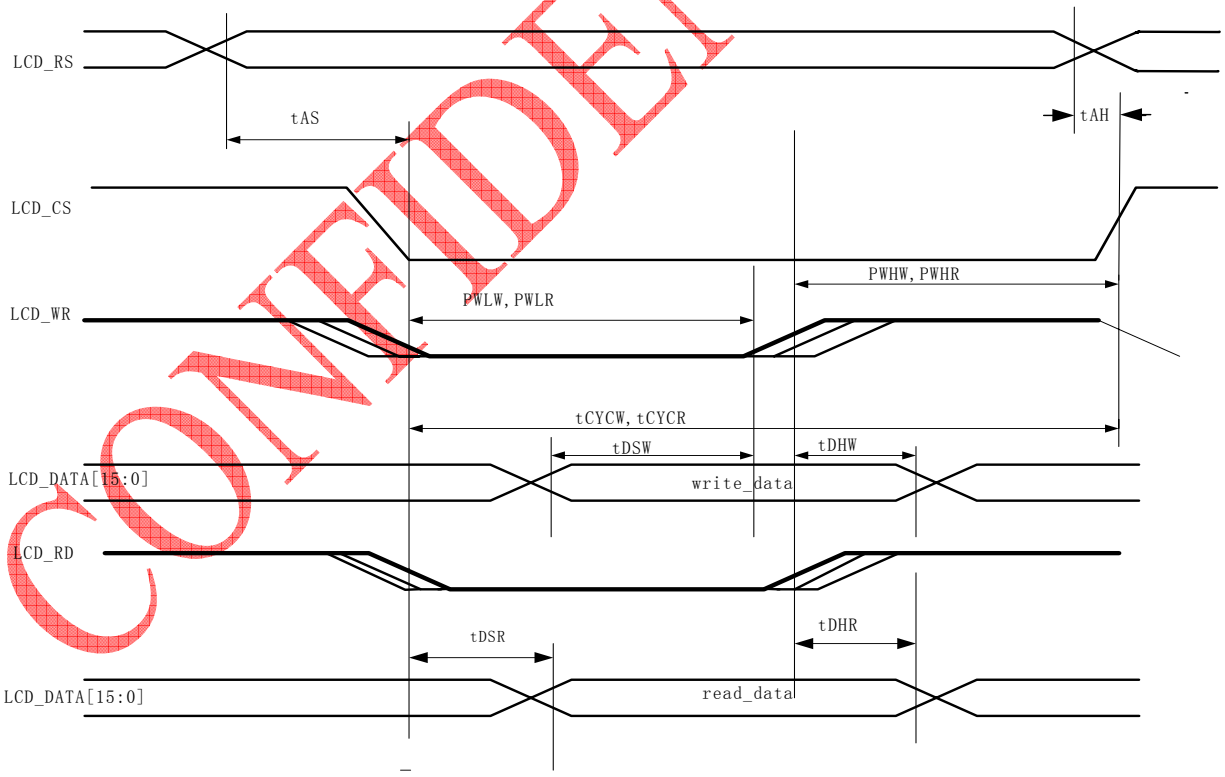


Table 7-3: LCD Panel Interface

PARAMETER		SYMBOL	MIN	MAX	UNIT
Bus cycle time	Write	t_{CYCW}	2	-	cycle *
	Read	t_{CYCR}	2	-	cycle
Write low-level pulse width		PW_{LW}	1	-	cycle
Read low-level pulse width		PW_{LR}	1	-	cycle
Write high-level pulse width		PW_{HW}	1	-	cycle
Read high-level pulse width		PW_{HR}	1	-	cycle
Setup time (LCD_RS to LCD_CS, LCD_WRN, LCD_RDN)		t_{AS}	0	-	ns
Hold time (LCD_RS to LCD_CS)		t_{AH}	0	-	ns
Write data setup time		t_{DSW}	1	-	cycle
Write data hold time		t_{DHW}	1	-	cycle
Read data setup time		t_{DSR}	0	-	ns
Read data hold time		t_{DHR}	0	-	ns

* The cycle width is according to the VC0528 system clock period

7.4.3. Sensor Interface

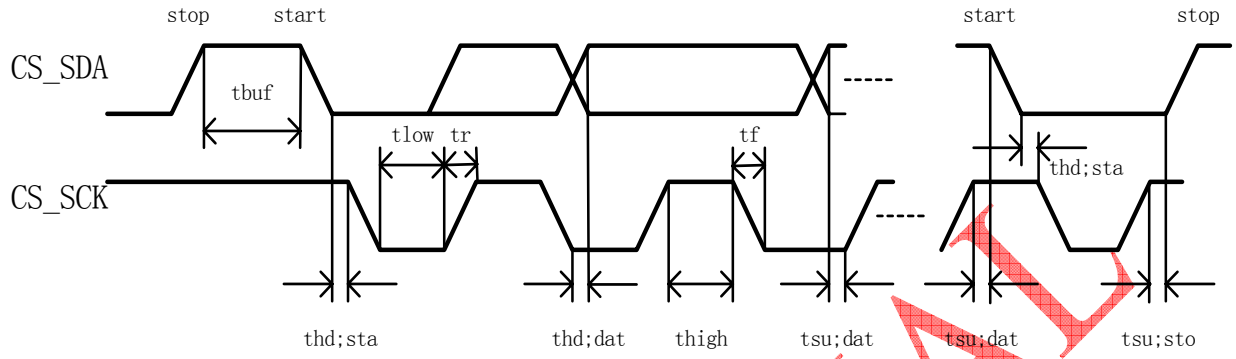
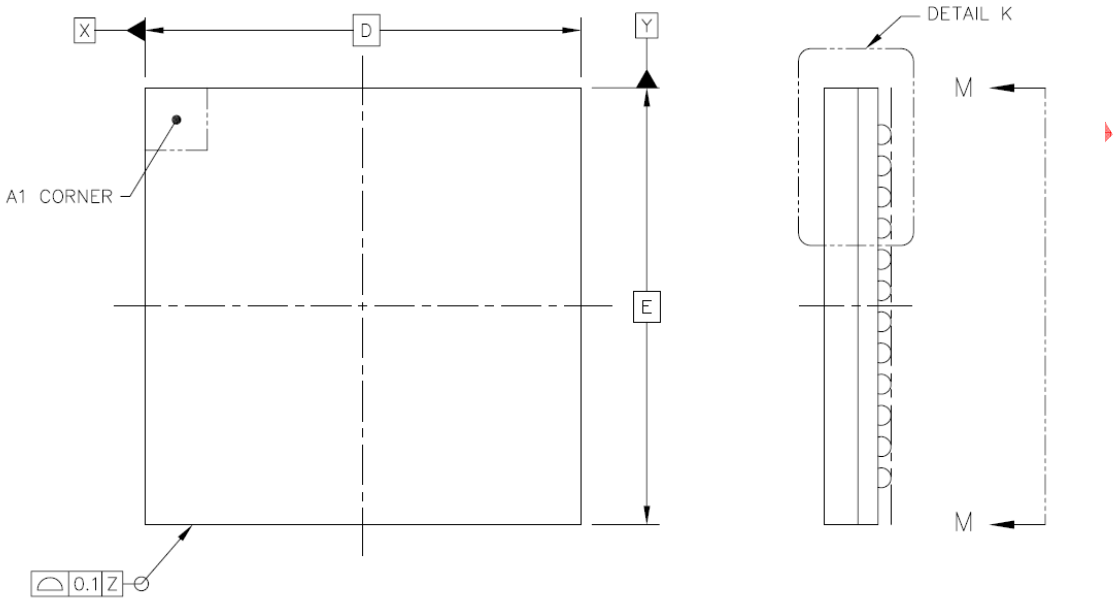


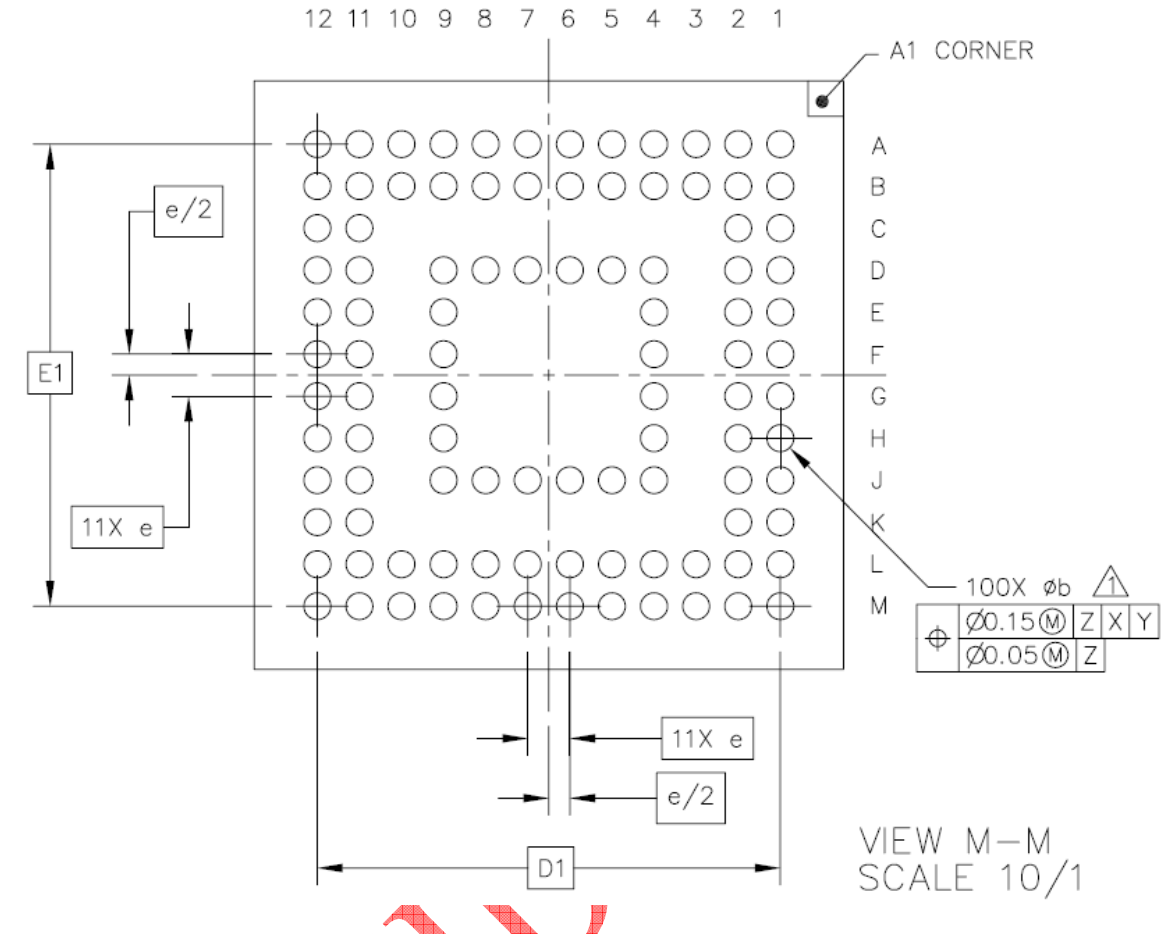
Table 7-4: Sensor Interface

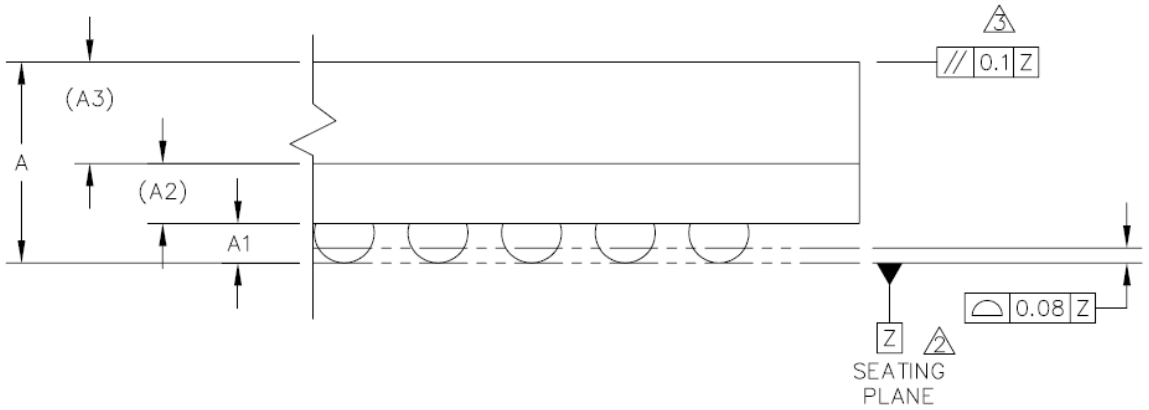
PARAMETER	SYMBOL	MIN	MAX	UNIT
CS_SCK clock frequency	f_{sck}	0	375	kHz
Time that sensor serial bus must be free before a new transmission can start	t_{buf}	1.3	-	us
Hold time for a start	$t_{hd;sta}$	0.6	-	us
Low period of CS_SCK	t_{low}	1.3	-	us
High period of CS_SCK	t_{high}	1.3	-	us
Setup time for start	$t_{su;sta}$	0.6	-	us
Data hold time	$t_{hd;dat}$	0	-	us
Data setup time	$t_{su;dat}$	100	-	ns
Rise time of both CS_SDA and CS_SCK	t_r	-	1	us
Fall time of both CS_SDA and CS_SCK	t_f	-	300	ns
Setup time for stop	$t_{su;sto}$	0.6	-	us

8. PACKAGE INFORMATION

8.1. Package Mechanical Dimensions




12 11 10 9 8 7 6 5 4 3 2 1
A1 CORNER
A
B
C
D
E
F
G
H
J
K
L
M
e/2
E1
11X e
100X øb
Ø0.15 M Z X Y
Ø0.05 M Z
11X e
e/2
D1
VIEW M–M
SCALE 10/1


(A3)
A
(A2)
A1
3
// 0.1 Z
0.08 Z
Z
2
SEATING
PLANE

8.2. Dimensional Reference

Table 8-1: Dimensional Reference

DIM	MIN	NOM	MAX	NOTES
A			1.15	1. dimensional and tolerancing per asme y14.5-1994. 2. all dimensions are in millimeters. 3. the "b" represents the Max. solder ball diameter, parallel to datum plane Z. . 4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
A1	0.16	0.22	0.26	
A2		0.32REF		
A3		0.54REF		
D		7 BSC		
b	0.27	0.32	0.37	
E		7BSC		
e		0.5BSC		
D1		5.5BSC		
E1		5.5BSC		

8.3. Marking information

Marking Information	Vimicro VC0528BRVC …… ……

9. CONTACT INFORMATION

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10. REVISION HISTORY

REVISION NO.	REMARKS	DATE
0.9	Preliminary version	2006-12-07
0.95	Updated based on review feedbacks.	2007-06-21
1.05	Modify Pin Assignment and Pin Layout map	2007-07-2