# DATA SHEET

# 74LVC162374A; 74LVCH162374A

16-bit edge triggered D-type flip-flop with 30 Ω series termination resistors; 5 V input/output tolerant; 3-state

Product specification
File under Integrated Circuits, IC24

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Philips Semiconductors

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# 74LVC162374A; 74LVCH162374A

## FEATURES

- ESD protection:
  HBM EIA/JESD22-A114-A exceeds 2000 V
  MM EIA/JESD22-A115-A exceeds 200 V
- 5 V tolerant input/output for interfacing with 5 V logic
- Wide supply voltage range of 1.2 to 3.6 V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple power and ground pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold (74LVCH162374A only)
- High impedance when $V_{CC}$ = 0
- Power off disables outputs, permitting live insertion.

## DESCRIPTION

The 74LVC(H)162374A is a 16-bit edge triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. The 74LVC162374A consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided for each octal. Inputs can be driven from either 3.3 or 5 V devices. In 3-state operation, outputs can handle 5 V. These features allow the use of these devices in a mixed 3.3 and 5 V environment.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

The 74LVCH162374A bus hold data inputs eliminates the need for external pull up resistors to hold unused inputs.

The 74LVC(H)162374A is designed with 30 Ω series termination resistors in both HIGH and LOW output stages to reduce line noise.

## FUNCTION TABLE

See note 1.

| OPERATION MODES | INPUTS | | | INTERNAL FLIP-FLOPS | OUTPUTS |
|---|---|---|---|---|---|
| | $n\overline{OE}$ | nCP | $nD_n$ | | $Q_0$ to $Q_7$ |
| Load and read register | L | ↑ | l | L | L |
| | L | ↑ | h | H | H |
| Latch register and disable outputs | H | ↑ | l | L | Z |
| | H | ↑ | h | H | Z |

**Note**

1. H = HIGH voltage level;
   h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   L = LOW voltage level;
   l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
   Z = high-impedance OFF-state;
   ↑ = LOW-to-HIGH CP transition.

## QUICK REFERENCE DATA

GND = 0 V; $T_{amb}$ = 25 °C; $t_r = t_f \leq 2.5$ ns.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | propagation delay CP to $Q_n$ | $C_L$ = 50 pF; $V_{CC}$ = 3.3 V | 3.8 | ns |
| $f_{max}$ | maximum clock frequency | | 150 | MHz |
| $C_I$ | input capacitance | | 5.0 | pF |
| $C_{PD}$ | power dissipation capacitance per flip-flop | $V_{CC}$ = 3.3 V; note 1 | 30 | pF |

**Note**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in μW).

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   $f_i$ = input frequency in MHz;

   $f_o$ = output frequency in MHz;

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

   $C_L$ = output load capacitance in pF;

   $V_{CC}$ = supply voltage in Volts.

## ORDERING INFORMATION

| OUTSIDE NORTH AMERICA | NORTH AMERICA | PACKAGE | | | | |
|---|---|---|---|---|---|---|
| | | TEMPERATURE RANGE | PINS | PACKAGE | MATERIAL | CODE |
| 74LVC162374ADL | VC162374A DL | −40 to +85 °C | 48 | SSOP | plastic | SOT370-1 |
| 74LVC162374ADGG | VC162374A DGG | | 48 | TSSOP | plastic | SOT362-1 |
| 74LVCH162374ADL | VCH162374A DL | | 48 | SSOP | plastic | SOT370-1 |
| 74LVCH162374ADGG | VCH162374A DGG | | 48 | TSSOP | plastic | SOT362-1 |

## PINNING

| PIN | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | $1\overline{OE}$ | output enable input (active LOW) |
| 2, 3, 5, 6, 8, 9, 11, 12 | $1Q_0$ to $1Q_7$ | 3-state flip-flop outputs |
| 4, 10, 15, 21, 28, 34, 39, 45 | GND | ground (0 V) |
| 7, 18, 31, 42 | $V_{CC}$ | DC supply voltage |
| 13, 14, 16, 17, 19, 20, 22, 23 | $2Q_0$ to $2Q_7$ | 3-state flip-flop outputs |
| 24 | $2\overline{OE}$ | output enable input (active LOW) |
| 25 | 2CP | clock input |
| 36, 35, 33, 32, 30, 29, 27, 26 | $2D_0$ to $2D_7$ | data inputs |
| 47, 46, 44, 43, 41, 40, 38, 37 | $1D_0$ to $1D_7$ | data inputs |
| 48 | 1CP | clock input |

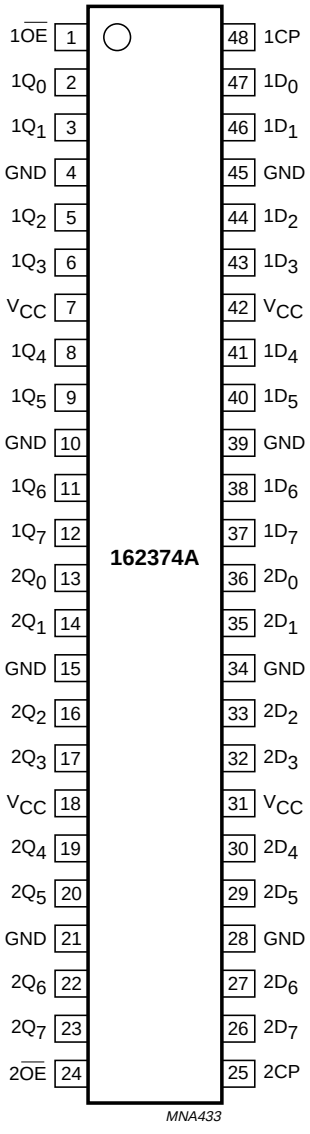



Fig.1 Pin configuration.

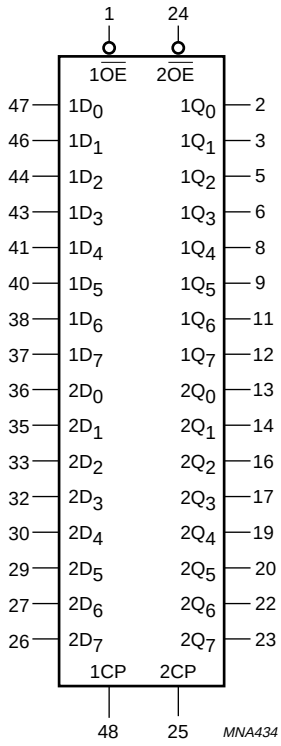



Fig.2 Logic symbol.

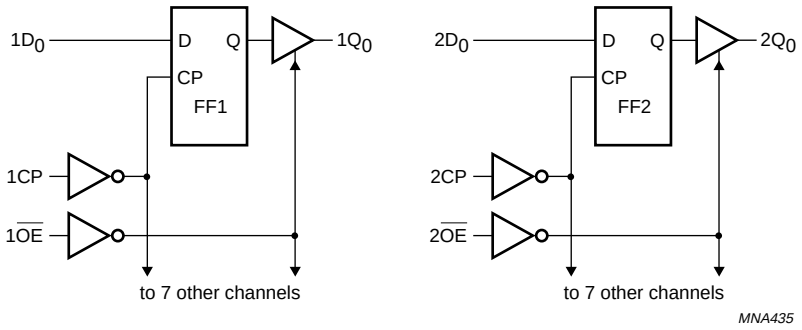



Fig.3 Logic diagram.

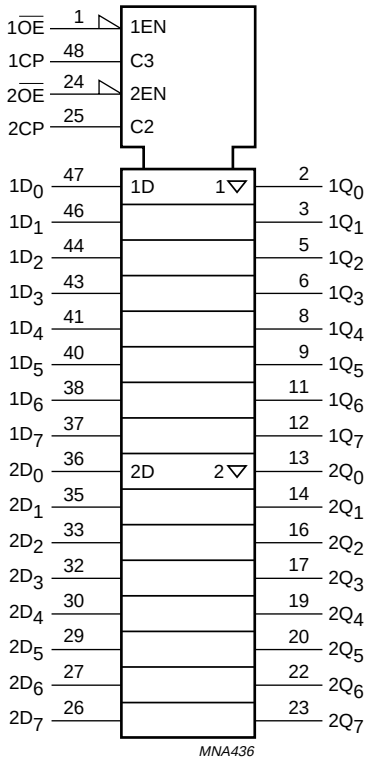



Fig.4 IEC logic symbol.

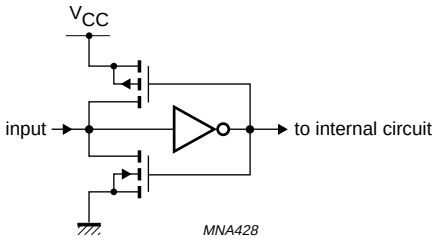



Fig.5 Bus hold circuit.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---|---|---|---|---|---|
| | | | MIN. | MAX. | |
| $V_{CC}$ | DC supply voltage | | | | |
| | for max. speed performance | | 2.7 | 3.6 | V |
| | for low-voltage applications | | 1.2 | 3.6 | V |
| $V_I$ | DC input voltage range | | 0 | 5.5 | V |
| $V_O$ | DC output voltage range | | | | |
| | output HIGH or LOW state | | 0 | $V_{CC}$ | V |
| | 3-state | | 0 | 5.5 | V |
| $T_{amb}$ | operating ambient temperature | see DC and AC characteristics per device | –40 | +85 | °C |
| $t_r$, $t_f$ | input rise and fall times | $V_{CC}$ = 1.2 to 2.7 V | 0 | 20 | ns/V |
| | | $V_{CC}$ = 2.7 to 3.6 V | 0 | 10 | ns/V |

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134). Voltages are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 | +6.5 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | – | –50 | mA |
| $V_I$ | DC input voltage | note 1 | –0.5 | +5.5 | V |
| $I_{OK}$ | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | – | ±50 | mA |
| $V_O$ | DC output voltage | | | | |
| | output HIGH or LOW | note 1 | –0.5 | $V_{CC}$ + 0.5 | V |
| | output 3-state | note 1 | –0.5 | +6.5 | V |
| $I_O$ | DC output diode current | $V_O$ = 0 to $V_{CC}$ | – | ±50 | mA |
| $I_{GND}$, $I_{CC}$ | DC $V_{CC}$ or GND current | | – | ±100 | mA |
| $T_{stg}$ | storage temperature | | –65 | +150 | °C |
| $P_{tot}$ | power dissipation plastic shrink mini-pack (SSOP and TSSOP) | above 60 °C derate linearly with 5.5 mW/K | – | 500 | mW |

**Note**

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC CHARACTERISTICS**

Over recommended operating conditions; voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | | $T_{amb}$ (°C) | | | UNIT |
|---|---|---|---|---|---|---|---|
| | | OTHER | $V_{CC}$ (V) | –40 to +85 | | | |
| | | | | MIN. | TYP.(1) | MAX. | |
| $V_{IH}$ | HIGH-level input voltage | | 1.2 | $V_{CC}$ | – | – | V |
| | | | 2.7 to 3.6 | 2.0 | – | – | |
| $V_{IL}$ | LOW-level input voltage | | 1.2 | – | – | GND | V |
| | | | 2.7 to 3.6 | – | – | 0.8 | |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –6 mA | 2.7 | $V_{CC}$ – 0.5 | – | – | V |
| | | $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –100 µA | 3.0 | $V_{CC}$ – 0.2 | $V_{CC}$ | – | |
| | | $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –12 mA | 3.0 | $V_{CC}$ – 0.8 | – | – | |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 6 mA | 2.7 | – | – | 0.40 | V |
| | | $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100 µA | 3.0 | – | – | 0.20 | |
| | | $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 12 mA | 3.0 | – | – | 0.55 | |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; note 2 | 3.6 | – | ±0.1 | ±5 | µA |
| $I_{OZ}$ | 3-state output OFF-state current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = 5.5 V or GND | 3.6 | – | 0.1 | ±5 | µA |
| $I_{off}$ | power off leakage supply | $V_I$ or $V_O$ = 5.5 V | 0.0 | – | 0.1 | ±10 | µA |
| $I_{CC}$ | quiescent supply current | $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | 3.6 | – | 0.1 | 20 | µA |
| $\Delta I_{CC}$ | additional quiescent supply current per control pin | $V_I$ = $V_{CC}$ – 0.6 V; $I_O$ = 0 | 2.7 to 3.6 | – | 5 | 500 | µA |
| $I_{BHL}$ | bus hold LOW sustaining current | $V_I$ = 0.8 V; notes 3, 4 and 5 | 3.0 | 75 | – | – | µA |
| $I_{BHH}$ | bus hold HIGH sustaining current | $V_I$ = 2.0 V; notes 3, 4 and 5 | 3.0 | –75 | – | – | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | $V_I$ = 0.8 V; notes 3, 4 and 6 | 3.6 | 500 | – | – | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | $V_I$ = 0.8 V; notes 3, 4 and 6 | 3.6 | –500 | – | – | µA |

**Notes**

1. All typical values are at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.
2. For bus hold parts, the bus hold circuit is switched off when $V_I$ exceeds $V_{CC}$ allowing 5.5 V on the input terminal.
3. Valid for data inputs of bus hold parts (LVCH162374A) only.
4. For data inputs only, control inputs do not have a bus hold circuit.
5. The specified sustaining current at the data input holds the input below the specified $V_I$ level.
6. The specified overdrive current at the data input forces the data input to the opposite logic input state.

**AC CHARACTERISTICS**

GND = 0 V; $t_r = t_f \leq 2.5$ ns; $T_{amb} = -40$ to +85 °C.

| SYMBOL | PARAMETER | WAVEFORMS | LIMITS | | | | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 3.3 V ±0.3 V | | | $V_{CC}$ = 2.7 V | | |
| | | | MIN. | TYP.(1) | MAX. | MIN. | MAX. | |
| $t_{PHL}/t_{PLH}$ | propagation delay nCP to $nQ_n$ | see Figs 6 and 9 | 1.5 | 3.8 | 6.2 | 1.5 | 7.2 | ns |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time $n\overline{OE}$ to $nQ_n$ | see Figs 8 and 9 | 1.5 | 4.1 | 7.1 | 1.5 | 8.1 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time $n\overline{OE}$ to $nQ_n$ | see Figs 8 and 9 | 1.5 | 3.7 | 5.2 | 1.5 | 6.2 | ns |
| $t_W$ | nCP pulse width HIGH or LOW | see Fig.6 | 3 | 1.5 | – | 3.0 | – | ns |
| $t_{su}$ | set-up time $nD_n$ to nCP | see Fig.7 | 2.0 | 0.3 | – | 2.0 | – | ns |
| $t_h$ | hold time $nD_n$ to nCP | see Fig.7 | +1.5 | –0.3 | – | 1.5 | – | ns |
| $f_{max}$ | maximum clock pulse frequency | see Fig.6 | 100 | – | – | 80 | – | MHz |

**Note**

1. Typical values at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

**AC WAVEFORMS**

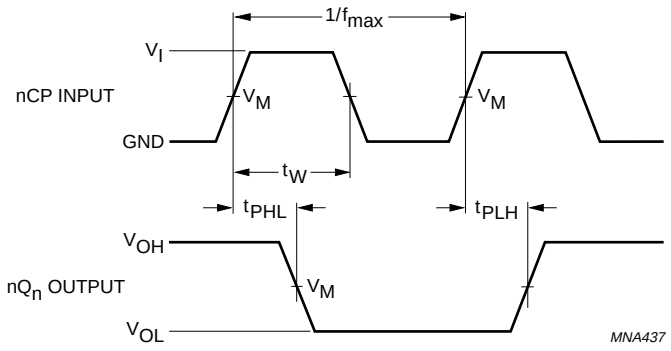
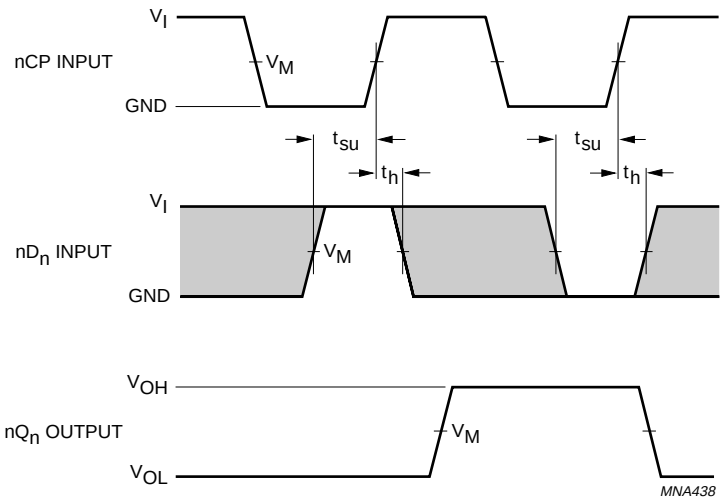



Fig.6 Clock input (nCP) to output ($nQ_n$) propagation delay, the clock pulse width and the maximum clock pulse frequency.




The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig.7 Data set-up and hold times for the $nD_n$ input to the nCP input.

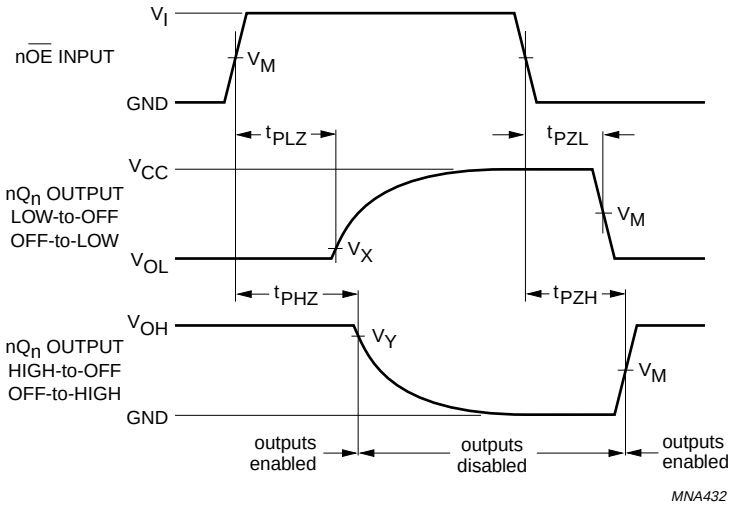
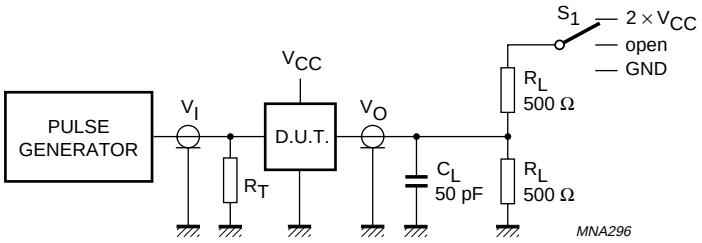



Fig.8 3-state enable and disable times.




| TEST | $S_1$ |
|---|---|
| $t_{PLH}/t_{PHL}$ | open |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $V_I$ |
|---|---|
| <2.7 V | $V_{CC}$ |
| 2.7 - 3.6 V | 2.7 V |

Definitions for test circuit:

$R_L$ = Load resistor; see Chapter “AC Characteristics”.

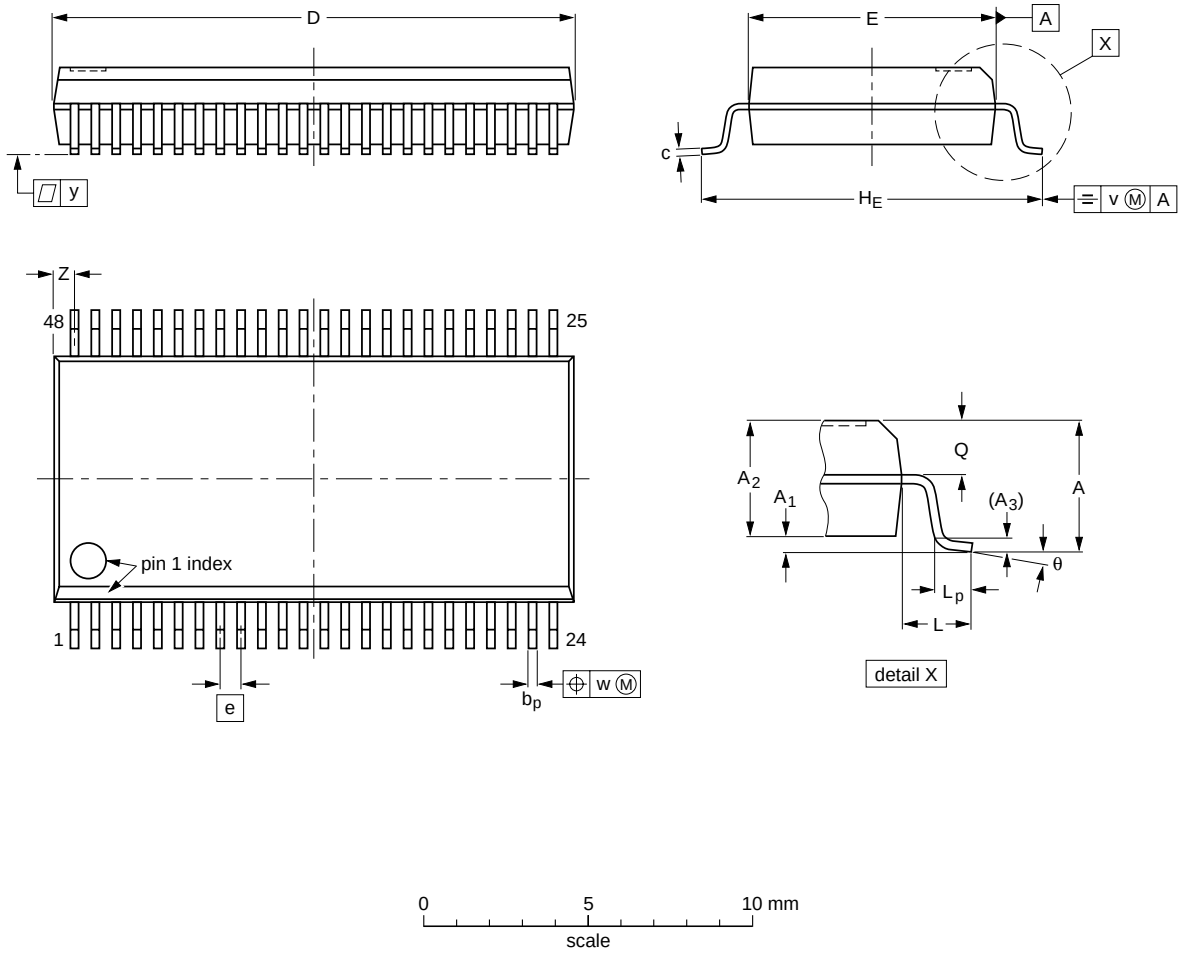
$C_L$ = Load capacitance including jig and probe capacitance (see Chapter “AC Characteristics”).

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

Fig.9 Load circuitry for switching times.

## PACKAGE OUTLINES

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm** **SOT370-1**




**DIMENSIONS (mm are the original dimensions)**

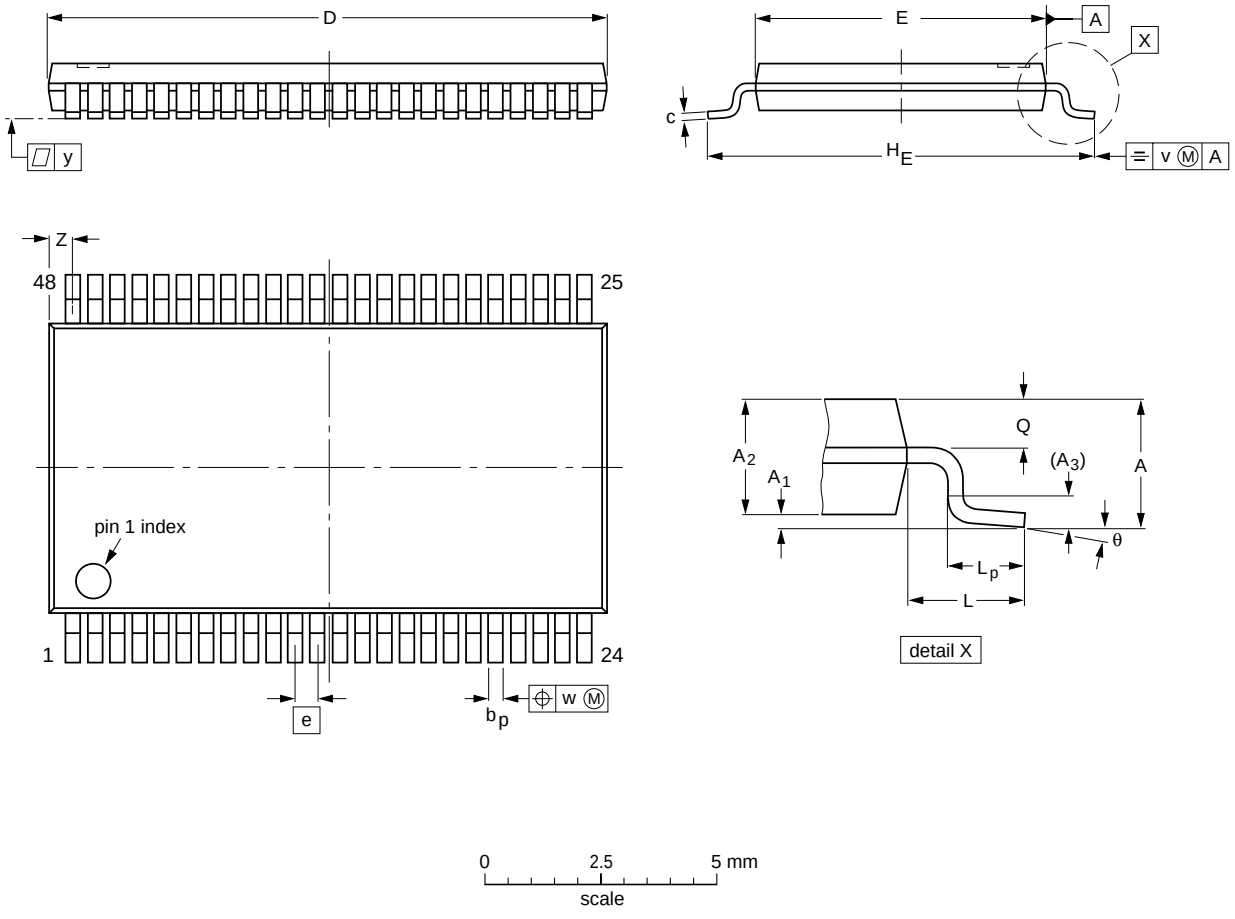
| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | |
| SOT370-1 | | MO-118AA | | | | ~~93-11-02~~<br>95-02-04 |

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 12.6<br>12.4 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT362-1 | | MO-153ED | | | | | ~~93-02-03~~<br>95-02-10 |

## SOLDERING

### Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

### Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

### Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

**Suitability of surface mount IC packages for wave and reflow soldering methods**

| PACKAGE | SOLDERING METHOD | |
|---|---|---|
| | WAVE | REFLOW(1) |
| BGA, SQFP | not suitable | suitable |
| HLQFP, HSQFP, HSOP, SMS | not suitable(2) | suitable |
| PLCC(3), SO, SOJ | suitable | suitable |
| LQFP, QFP, TQFP | not recommended(3)(4) | suitable |
| SSOP, TSSOP, VSO | not recommended(5) | suitable |

**Notes**

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

**DEFINITIONS**

| **Data sheet status** | |
|---|---|
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| **Limiting values** | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| **Application information** | |
| Where application information is given, it is advisory and does not form part of the specification. | |

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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