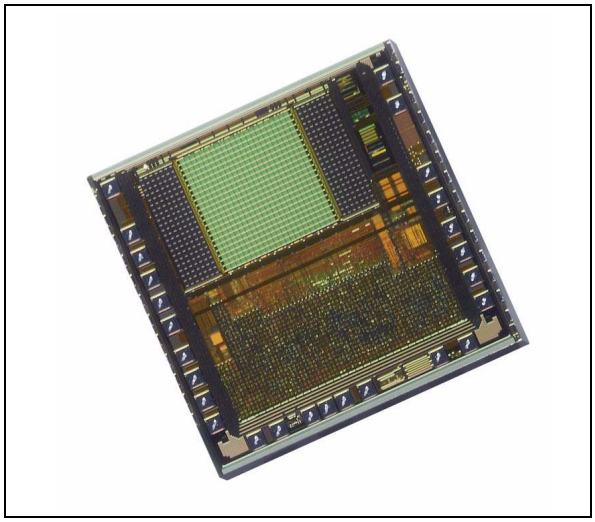
VD5377

Ultra-low power motion sensor for optical finger navigation (OFN)

Datasheet - preliminary data

Features

- Ultra-low power performance and high speed/high accuracy motion detection (up to 28 in/s @ 4000 f/s)
- Manual or automatic power management options
- Very low quiescent and operating current modes for battery life saving
- Fully integrated solution: internal oscillator and LED driver
- I^2C interface with fast polling rates for high-end applications (report rate up to 1 per ms).
- User-selectable I^2C address (default I^2C address is 0xA6)
- CPI programmable up to 3,200 CPI
- Fully automatic exposure control (AEC)



Applications

- Smart phones
- Laptop/Netbook PCs
- Media players
- GPS devices
- Remote controls for home entertainment equipment

Description

The VD5377 is an ultra-low power, single-chip controller IC containing all the functions necessary for optical joysticks/optical finger navigation modules enabling improved mobile experience and longer battery life. This device is cost and performance optimized for Optical Finger Navigation applications and includes special features to ensure optimum performance even in bright sunlight.

Contents

List of tables

List of figures

1 Overview

The VD5377 is an ultra-low power, single-chip controller IC containing all the functions necessary for optical joysticks/optical finger navigation modules. It incorporates a 20 x 20, 30.4 µm pixel imaging array supporting frame rates up to 4 k frames/s capable of detecting and tracking motion at up to 28 inches/s with high accuracy and low drift. Maximum velocity is calculated as follows:

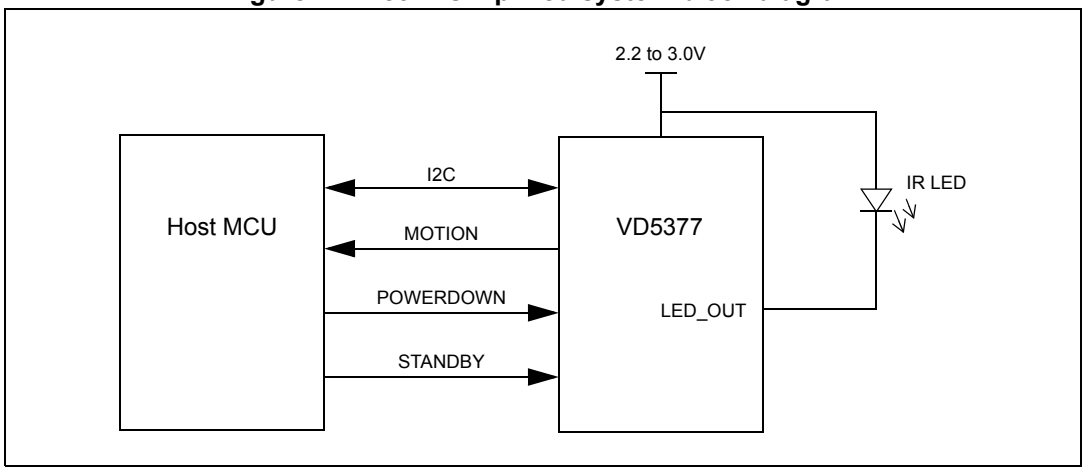
```
maximum velocity = (pixel size/lens magnification) x max frame rate x
max.displacement per frame
```

For example:

```
0.5 magnification = (30 µm/0.5) x 4000 f/s x 3 pixels = 0.72 m/s (28
inches/s)
```

Figure 1 shows a simplified block diagram of a typical optical navigation system. Communication with the device is over a 400 kHz I^2C serial link (I^2C address is user-selectable). The MOTION signal is asserted when the VD5377 senses motion and motion X/Y data is accessed over the I^2C link. The user can choose between Automatic power management mode, where the device will automatically go into low power hibernation if no motion is detected or Manual power management mode where there is a choice of two low power states: Standby or Powerdown. The external navigation LED driver is fully integrated in the device, supporting drive currents up to 14 mA. Where higher power is required, an external driver can be used.

Figure 1. VD5377 simplified system block diagram



1.1 Technical specification

Table 1. Technical specification

Feature	Detail
Resolution	Programmable up to 3200 cpi
Pixel size	30.4 µm
Array size	20 x 20 pixels
Frame rate	Up to 4 kf/s (auto or manual)
Tracking performance	Up to 720 mm/s (28 in/s) low drift, high accuracy
Supply voltage	2.2 V to 3.0 V using internal regulator or 1.8 V direct drive
Operating temperature	-20°C to 70°C

1.2 VD5377 enhancements

The VD5377 has been optimized for optical finger navigation (OFN) applications. For applications migrating from the previous VD5376 device, the following list highlights the key differences:

- optimized floor plan for improved module design
- enhanced automatic power management mode: fully programmable sleep and wake-up intervals
- ultra-low powerdown mode (<1 µA)
- user-selectable I^2C addresses with the option to create custom start-up configurations
- programmable polarity on external MOTION signal
- power-on reset (POR) function gated on MOTION signal
- unique Backlight controller: three PWM controlled LED drive outputs (10 mA)
- enhanced performance in high ambient light conditions
- new filter added to aid navigation in low contrast images
- increased LED on-time for greater dynamic range
- simplified support circuit: Rbin and Cosc components now integrated
- smaller external capacitor on VREG (220 nF)
- improved I^2C frame capture

1.3 Floor plan changes

Table 2. Die size and optical center comparison

	Conditions	VD5377		VD5376	
		X (µm)	Y (µm)	X (µm)	Y (µm)
Die size	Including seal	1794	1758	1800	1832
	Including scribe (step & repeat)	1894	1858	1900	1932
Optical center	Relative to die center	-83	+447	-91	+319

2 Silicon specification

This chapter contains physical die information.

2.1 Silicon thickness

Standard silicon thickness is 180 µm (see *Table 40: Delivery formats on page 86*).

2.2 Die size and optical center

All dimensions and all coordinates are referenced to the origin at die center.

Table 3. Die size

Conditions	X size (µm)	Y size (µm)
Including seal	1794	1758
Including scribe (step and repeat)	1894	1858

Table 4. Optical center

Parameter	X (µm)	Y (µm)
Die center	0	0
Array center	-83	+447

2.3 Pad opening sizes

Table 5. Pad openings

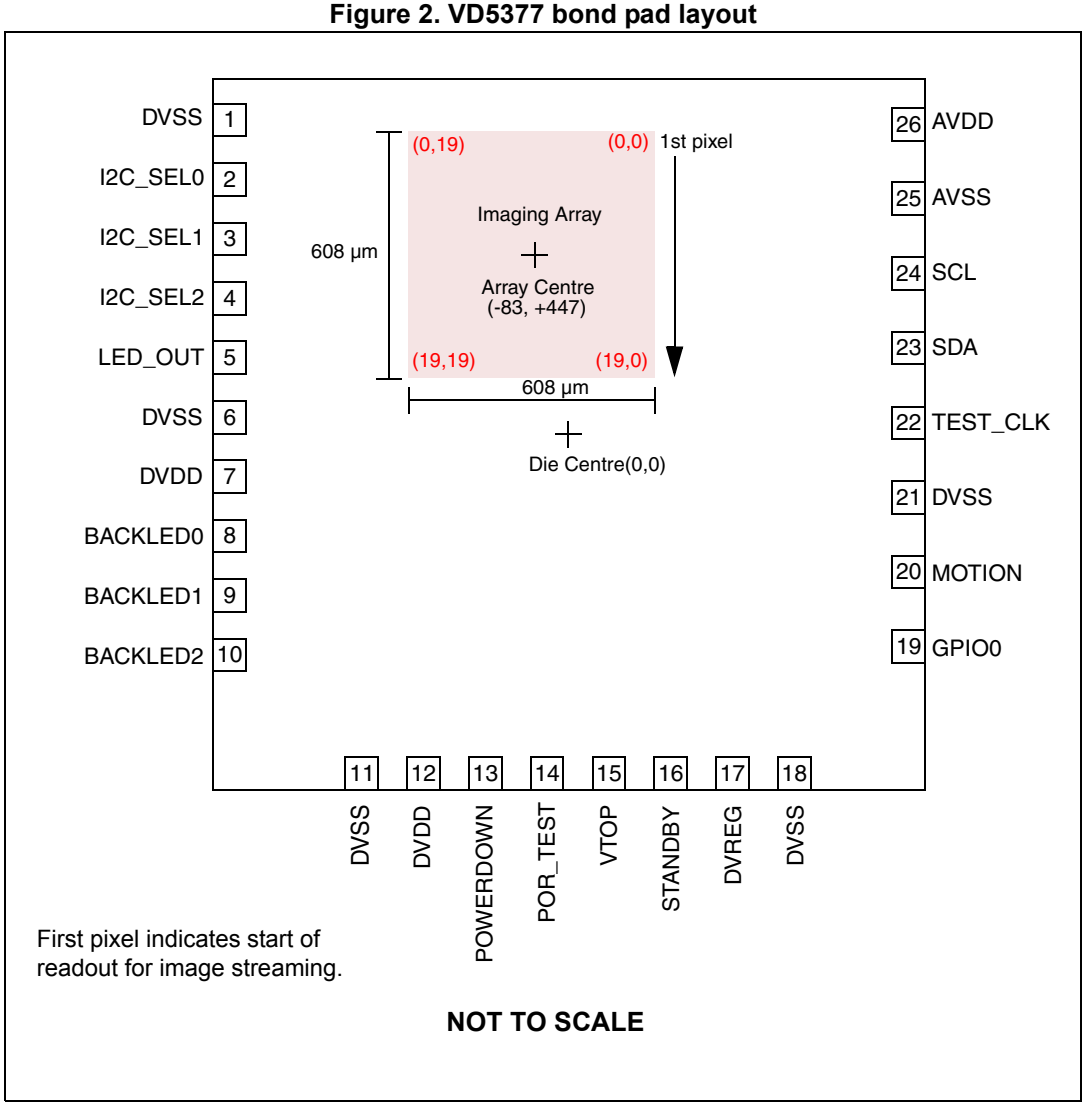
	X (µm)	Y (µm)
Size	86.4	86.4

Minimum bond pad pitch: 138 µm.

2.4 Device pinout

Figure 2 shows the bond pad layout and *Table 6* provides the bond pad coordinates. All dimensions are in microns.

Figure 2. VD5377 bond pad layout



2.5 Bond pad coordinates

All dimensions are in microns. Bond pad coordinates correspond to the bond pad centers referenced to the die center.

Table 6. Bond pad coordinates

Pad #	Pad name	X co-ordinate	Y co-ordinate
1	DVSS	-827.6	792.7
2	I2C_SEL0	-827.6	515.6
3	I2C_SEL1	-827.6	378.0
4	I2C_SEL2	-827.6	240.3
5	LED_OUT	-827.6	102.6
6	DVSS	-827.6	-35.0
7	DVDD	-827.6	-218.8
8	BACKLED0	-827.6	-356.4
9	BACKLED1	-827.6	-494.1
10	BACKLED2	-827.6	-631.8
11	DVSS	-649.8	-810.1
12	DVDD	-511.4	-810.1
13	POWERDOWN	-317.5	-810.1
14	POR_TEST	-213.8	-810.1
15	VTOP	-110.1	-810.1
16	STANDBY	28.3	-810.1
17	DVREG	470.1	-810.1
18	DVSS	649.6	-810.1
19	GPIO0	827.6	-632.3
20	MOTION	827.6	-484.3
21	DVSS	827.6	-336.1
22	TEST_CLK	827.6	-187.5
23	SDA	827.6	-10.3
24	SCL	827.6	145.4
25	AVSS	827.6	556.0
26	AVDD	827.6	733.4

3 Application schematics

There are two power configurations for the VD5377: a 2.2 V to 3.0 V external supply utilizing the device's internal 1.8 V regulator or direct drive using an externally regulated 1.8 V supply. Typical application schematics are shown for both configurations in *Figure 3* and *Figure 4*.

The internal 1.8 V core regulator requires a minimum 220 nF decoupling capacitor. Larger values may increase the minimum power down time which is required to guarantee a proper reset of the device.

Figure 3. VTOP supply (using internal regulator)

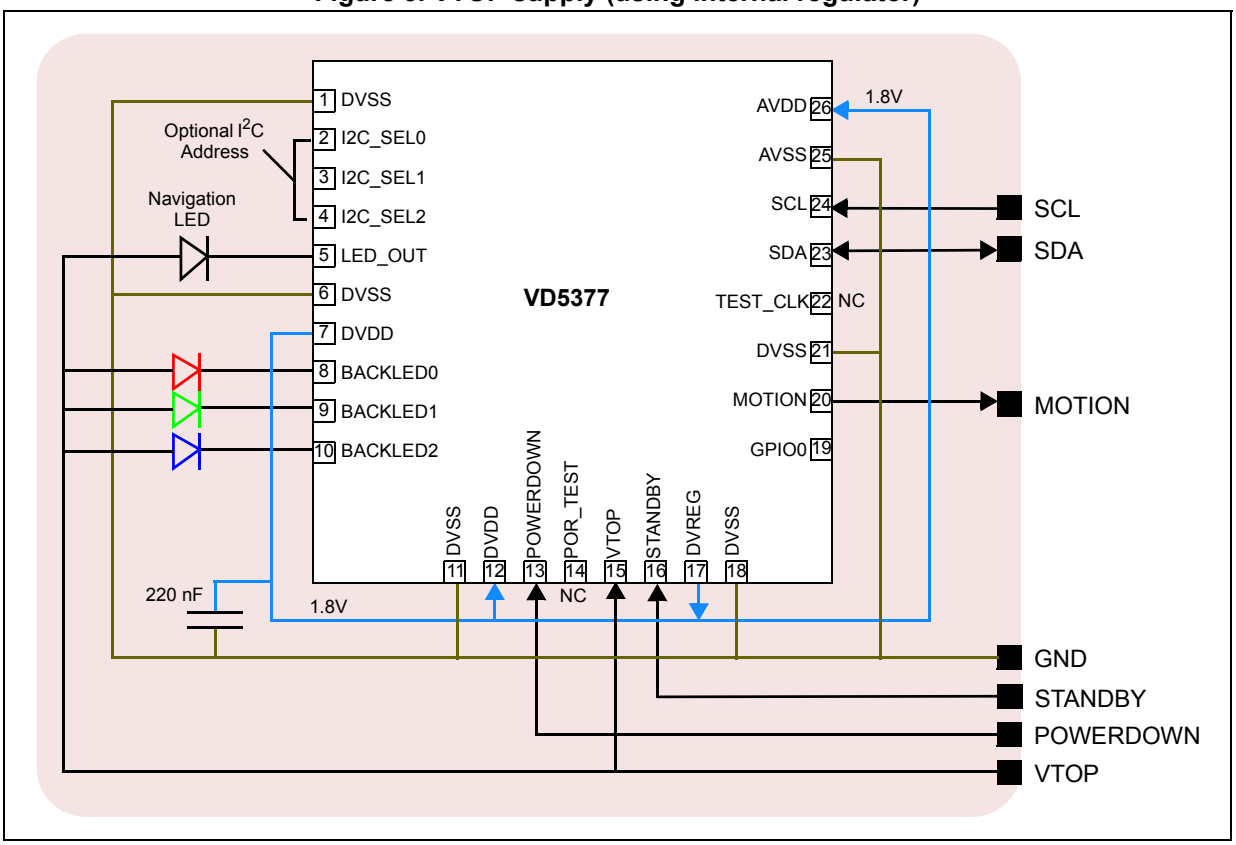
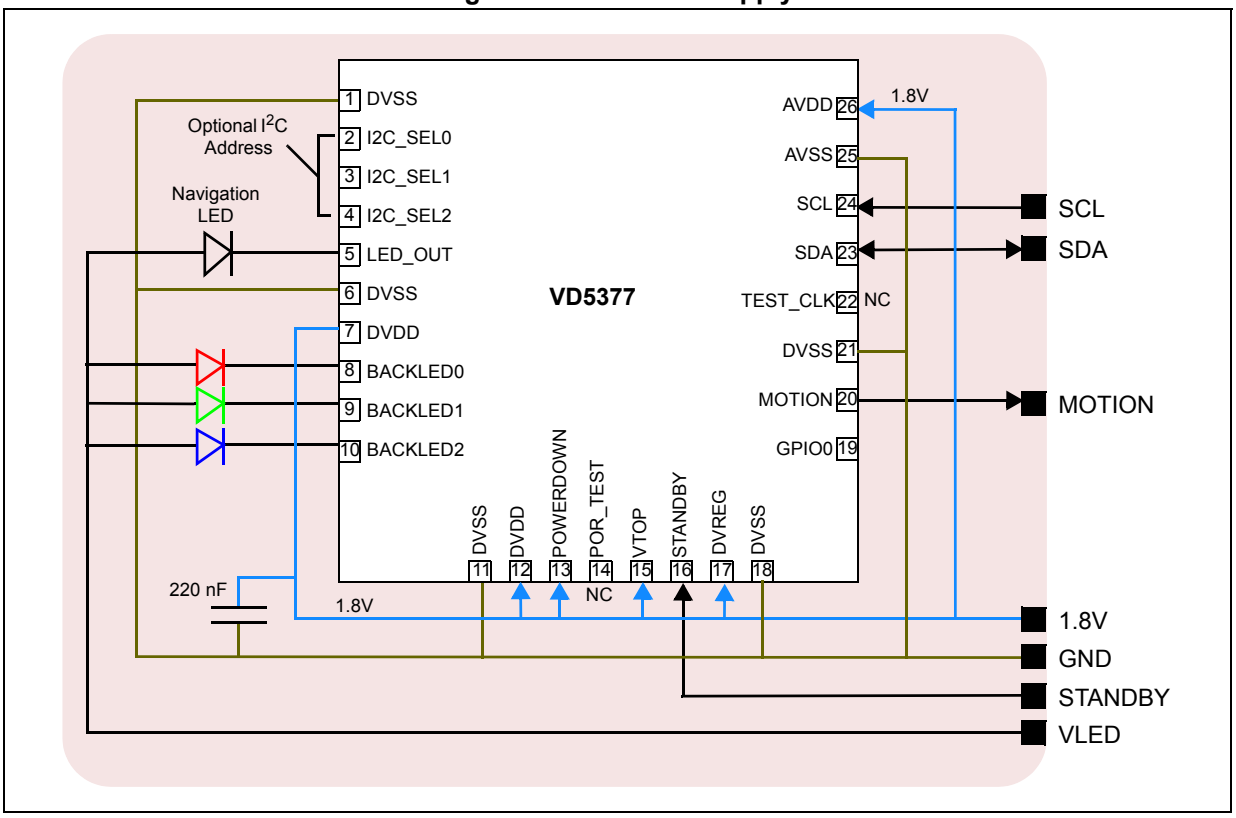


Figure 4. 1.8 V direct supply



Note: In a 1.8 V direct drive configuration, the POWERDOWN pin should be connected to 1.8 V to ensure the internal regulator is switched off to minimize power consumption.

3.1 Signal descriptions

Table 7. Signal descriptions

Pad #	Signal name	Type	Description
1	DVSS	Supply	Digital ground
2	I2C_SEL0	1.8V digital input	I^2C address select input. 5 V tolerant inputs with integrated pull-down resistor. If unconnected default address is 0xA6. (Pads have internal 35 kOhm pull-down resistors. If connected to VDD, the pull-down resistor is disconnected after the internal microcontroller boot sequence is completed to reduce power consumption).
3	I2C_SEL1	1.8V digital input	
4	I2C_SEL2	1.8V digital input	
5	LED_OUT	Current DAC output	Navigation LED drive pad. Constant current sink set by internal DAC. Maximum setting 14 mA. For external LED driver use GPIO0.
6	DVSS	Supply	Digital ground
7	DVDD	Supply	1.8 V digital supply

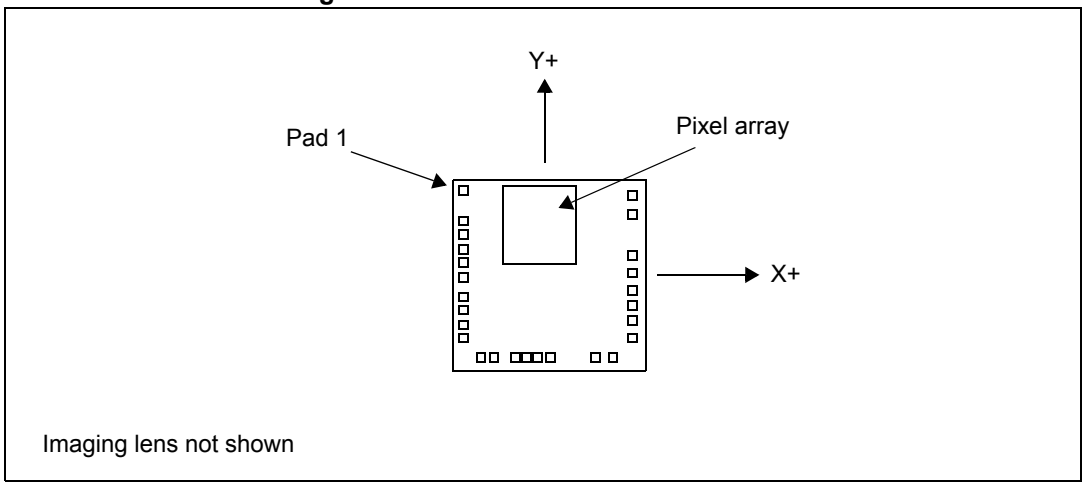
Table 7. Signal descriptions (continued)

Pad #	Signal name	Type	Description
8	BACKLED0	1.8V digital I/O	Backlight LED Driver (4 mA, open-drain). 5 V tolerant. If unused, connect to DVSS.
9	BACKLED1	1.8V digital I/O	Backlight LED Driver (4 mA, open-drain). 5 V tolerant. If unused, connect to DVSS.
10	BACKLED2	1.8V digital I/O	Backlight LED Driver (4 mA, open-drain). 5 V tolerant. If unused, connect to DVSS.
11	DVSS	Supply	Digital ground
12	DVDD	Supply	1.8 V digital supply
13	POWERDOWN	Analog input	Active high. This disables the internal 1.8 V core regulator. Input switching level is 0.8 V to be compatible with 1.8 V or 2.8 V signal.
14	POR_TEST	-	No connect
15	VTOP	Supply	Internal 1.8 V regulator supply input: – 2.2 to 3.0 V for internal regulator configuration – 1.8 V in direct drive mode.
16	STANDBY	1.8V digital input	If use_standby_pin register is selected (register 0x5 bit 4): – In manual mode STANDBY = 1 puts the device in low power mode – In auto mode STANDBY = 1 disables I^2C Otherwise, connect to DVSS if not used. This pad is 5 V tolerant.
17	DVREG	Supply	1.8V internal regulator output. Connect to DVDD and AVDD supplies. Requires a 220 nF capacitor to DVSS.
18	DVSS	Supply	Digital ground
19	GPIO0	3.0V digital I/O	External LED drive control signal or general purpose I/O. Referenced to Vtop. This pad is 5 V tolerant.
20	MOTION	3.0V digital output	Motion detection flag. Configurable as Push/Pull or open-drain. Active high or low (programmable polarity). Referenced to Vtop. This pad is 5 V tolerant.
21	DVSS	Supply	Digital ground
22	TEST_CLK	-	No connect
23	SDA	1.8V digital I/O	I^2C bidirectional data (open-drain). This pad is 5 V tolerant.
24	SCL	1.8V digital input	I^2C clock. This pad is 5 V tolerant.
25	AVSS	Supply	Analog ground
26	AVDD	Supply	1.8 V analog supply

3.2 Cursor orientation

Figure 5 shows the direction of positive motion vectors relative to silicon orientation with the default power-up register settings: parameters_2 (0x27) = 0x08 that is, invert_x = 0, invert_y = 0 and swap_xy = 1. An imaging lens is assumed but not shown. The direction of X/Y motion can be reversed or swapped by writing to register 0x27 allowing preferred cursor movement from any die orientation.

Figure 5. VD5377 default XY orientation

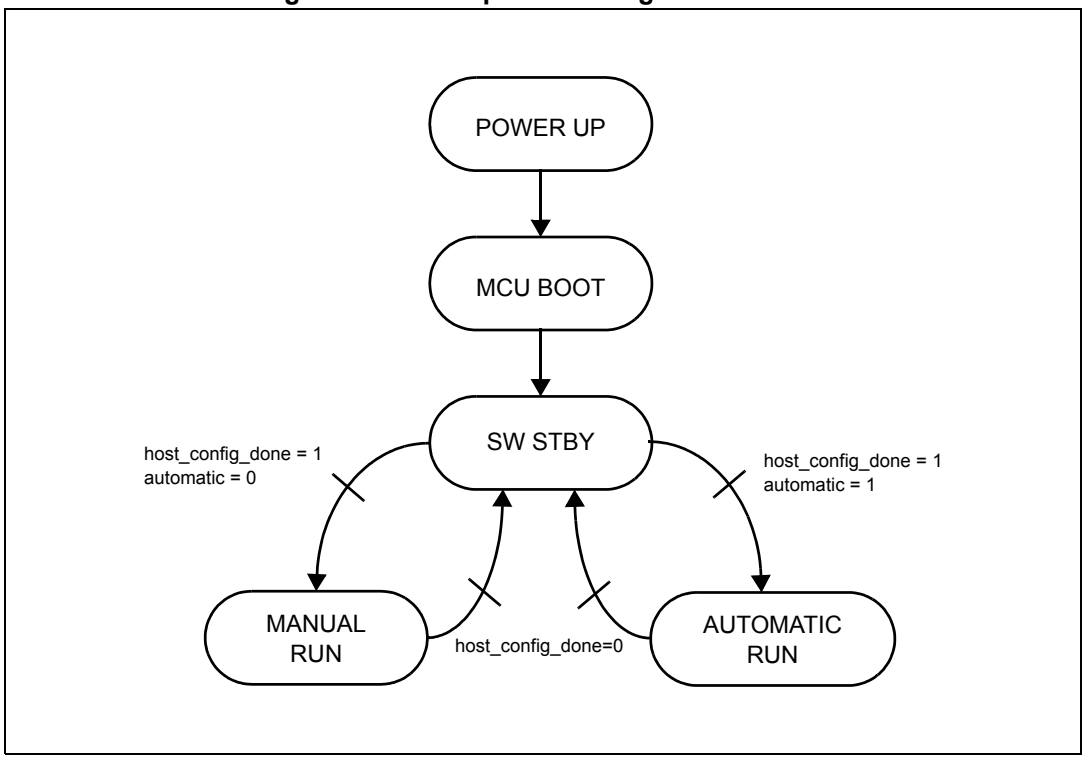


4 System overview

The VD5377 operates in one of two power management modes: MANUAL or AUTOMATIC (see *Figure 6*). After initial MCU BOOT the device enters the SW STBY state and waits for configuration from the host. When configured, the device enters MANUAL RUN or AUTOMATIC RUN mode.

- MANUAL power management mode is the simplest mode where the host initializes the device which then remains in MANUAL RUN mode until it receives a command to change mode (either an I^2C command to return to the SW STBY state or a low power state using the POWERDOWN or STANDBY pin).
- AUTOMATIC power management mode is an intelligent, power efficient mode where the device automatically switches to low power mode depending on motion activity. When initialized, the device will continue to operate autonomously minimizing power consumption and host CPU overhead.

Figure 6. VD5377 power management modes

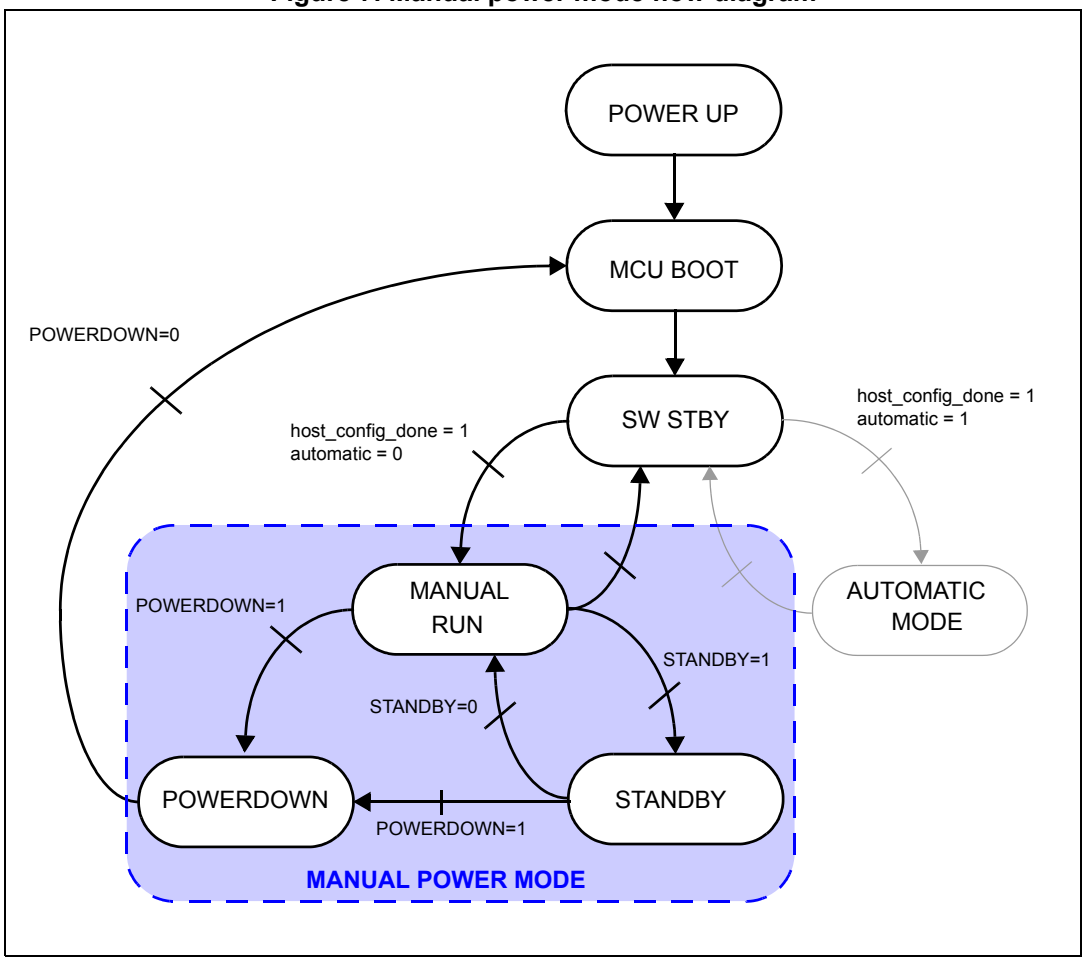


4.1 MANUAL power management

Manual power mode is the basic mode of the VD5377. After initialization, the sensor remains in MANUAL RUN mode even when no motion activity is detected. The host can use the external POWERDOWN or STANDBY signals to achieve lower current consumption.

- STANDBY pin[a] (active high): if set, the system goes into low power STANDBY mode **at the end of the current frame.** Typical power consumption in STANDBY mode is shown in *Table 8 on page 19*. The internal clock and motion engine are switched off and so the VD5377 does not respond to any I^2C communication and no motion activity is detected. All register settings are maintained in this state, so when STANDBY is de-asserted the system immediately resumes in RUN mode.
- POWERDOWN pin: if set, this signal immediately disables the internal 1.8 V core regulator. After power down, the system needs to be re-initialized. Power consumption is typically <1 µA in this state.

Figure 7. Manual power mode flow diagram



a. During initialization, the user must set the use_standby_pin register bit (system_config 0x05 bit 4) to 1 to enable the STANDBY pin function otherwise it is ignored.

Table 8 summarizes the typical operating current in Manual mode.

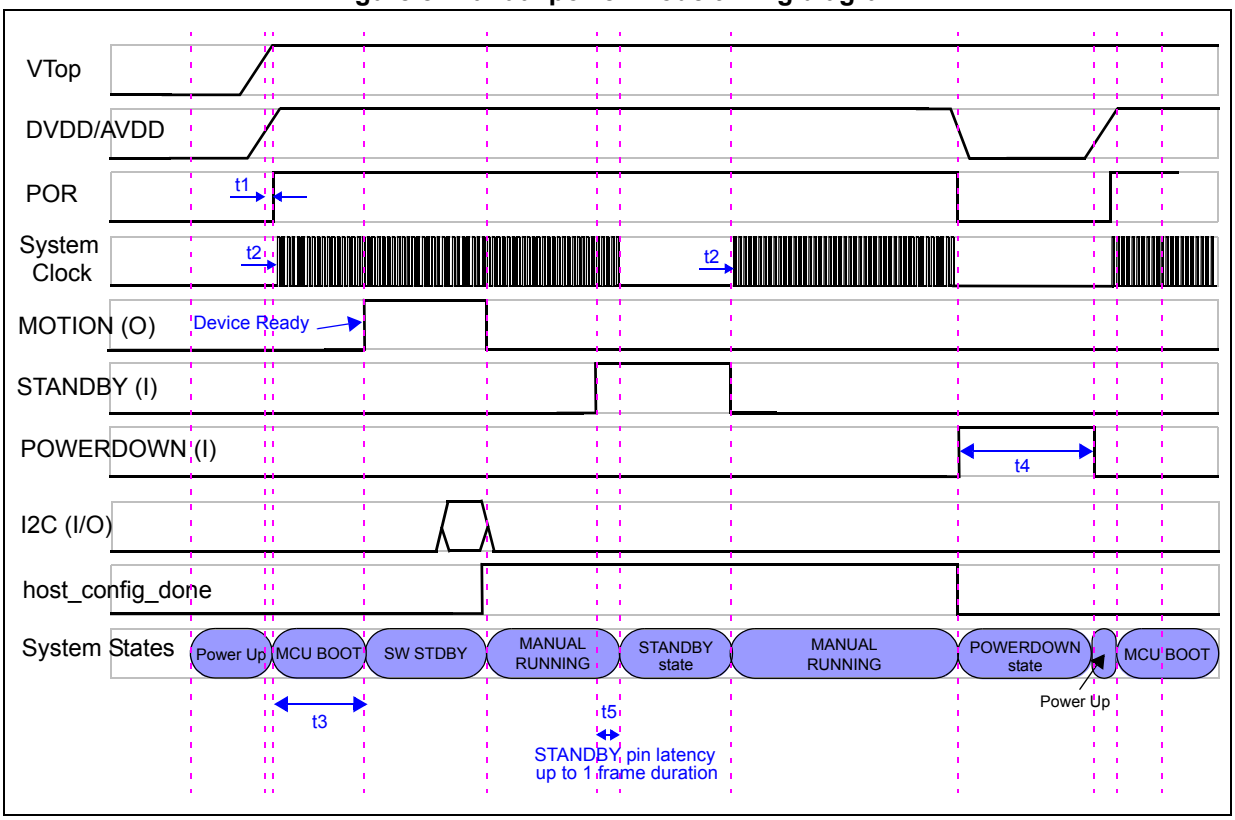
Table 8. Typical power consumption(1) - Manual mode

Run(2)			Standby	Power down
3k3 kf/s	2 kf/s	1 kf/s		
10.2 mA	6.9 mA	4.5 mA	25 µA	<1 µA

1. Includes LED (maximum exposure)
2. Internal clock = 44 MHz; led_dac 14 mA; Maximum exposure

Figure 8 describes the power-up sequence of the VD5377.

Figure 8. Manual power mode timing diagram



After the MCU boot sequence is completed, the system enters SW STDBY state and the MOTION pin is set to 1 indicating that the device is ready to receive commands from the host. After initialization by the host over I^2C, the device enters the MANUAL RUN state and the MOTION pin goes low.

Note: The MOTION pin polarity is programmable. If active low polarity is selected during initialization, the MOTION pin will remain high.

If the STANDBY pin is asserted, the system completes the current frame operation before entering the STANDBY state and stopping the internal system clock. When the STANDBY pin is deasserted, the system clock is restarted and the device resumes in the RUN state (no re-initialization required). If the POWERDOWN pin is asserted (active high), the internal 1.8 V regulator is disabled and the 1.8 V core supply is switched off. When the

POWERDOWN pin is deasserted, the internal 1.8 V regulator is re-enabled triggering a POR (Power-On Reset) and the MCU re-initializes as at power-up before entering the SW STBY state. The device must be re-configured after POWERDOWN.

Key timing parameters are shown in *Table 9*.

Table 9. Manual mode timing constraints

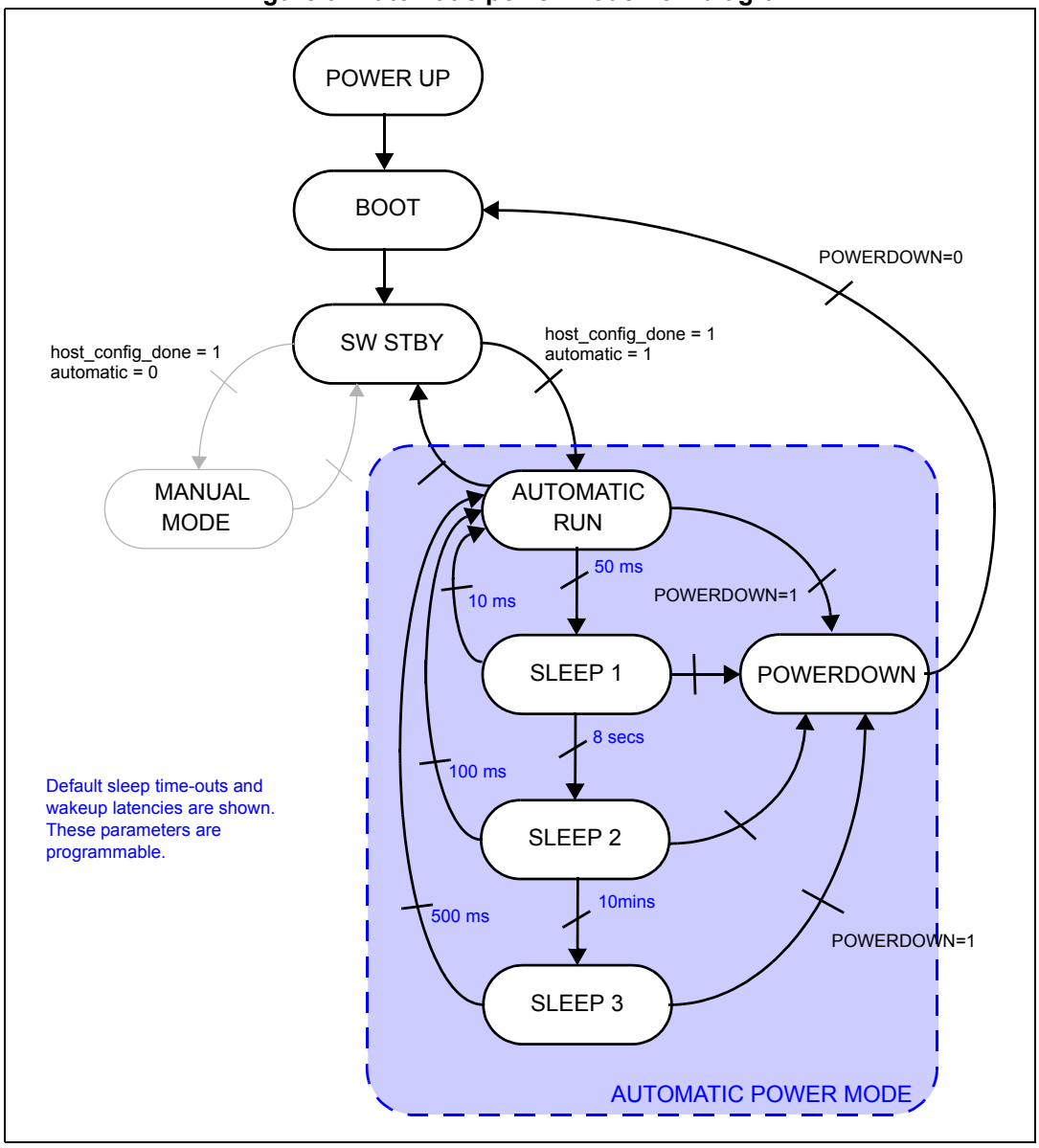
Symbol	Parameter	Typical
t1	POR Delay (POR threshold = 1.4 V typ)	20 µs
t2	Clock Startup	1 µs
t3	MCU boot time	450 µs
t4	Minimum Powerdown time (220 nF regulator capacitor)	10 ms
t5(1)	Standby pin latency (up to 1 frame at 1 kf/s)	up to 1 ms

1. No I^2C comms permitted to VD5377 after Standby pin asserted

4.2 AUTOMATIC power management

AUTOMATIC power mode is the advanced power saving mode of the VD5377. When this mode is activated, the sensor automatically enters low power modes (called SLEEP states) after a given time if the sensor does not detect any motion.

Figure 9. Automatic power mode flow diagram



A SLEEP state is a low power state where the internal system clock is disabled, the analog block is powered down and only the internal 50 kHz oscillator is running to wake the sensor up periodically. Each time the sensor wakes up, a single frame is captured and the motion versus previous frame is estimated. If motion is detected the system resumes in RUN mode; otherwise if no motion is detected the sensor goes back to SLEEP. Up to three SLEEP states (default) can be selected. The sleep time-out and wake-up latency periods are programmable.

In AUTOMATIC power mode, if the use_standby_pin register is set, the STANDBY pin is configured as a chip select (active low) to perform I^2C communications. This allows the host to perform I^2C communications to the VD5377 at anytime even during SLEEP modes. If the use_standby_pin register is not set, the host can only perform I^2C communications when motion data is pending.

Low power states:

- SLEEP states: Typical power consumption in the various sleep states is shown in *Table 10*.
- POWERDOWN pin: if set, this signal immediately disables the internal 1.8 V core regulator. After power down, the system needs to be re-initialized. Power consumption is typically <1 µA in this state.

Table 10. Typical power consumption(1) - automatic mode

Run(2)			Sleep1	Sleep2	Sleep3	Power down
3.3 kf/s	2 kf/s	1 kf/s				
10.2 mA	6.9 mA	4.5 mA	350 µA	60 µA	20 µA	<1 µA

1. Includes LED (maximum exposure)
2. Internal clock = 44 MHz; led_dac 14 mA; Maximum exposure

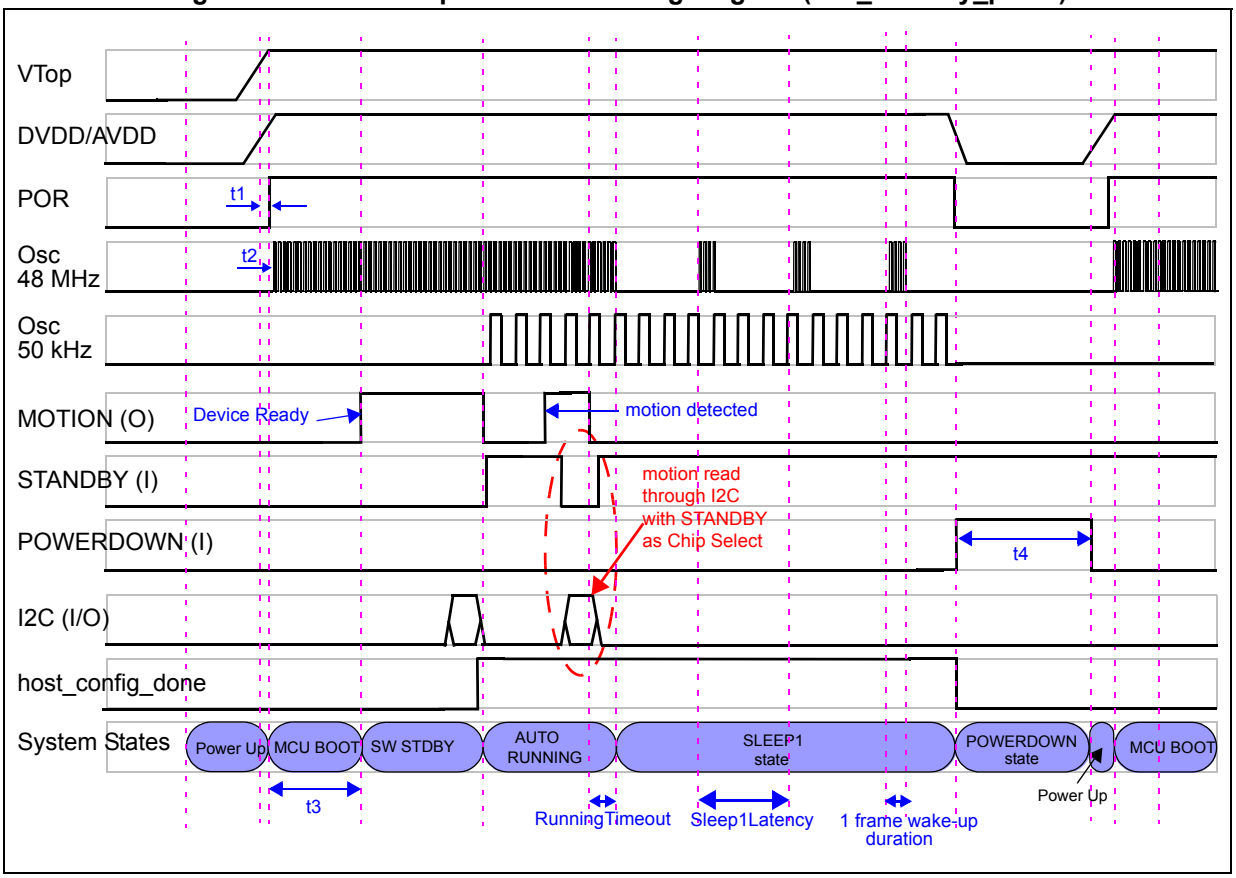
Figure 10 describes the power-up sequence of the VD5377 in AUTOMATIC power management mode. After the MCU boot sequence is completed, the system enters SW STDBY state and the MOTION pin is set to 1 indicating that the device is ready to receive commands from the host. After initialization by the host over I^2C, the device enters the AUTO RUN state and the MOTION pin will go low.

Note: The MOTION pin polarity is programmable. If active low polarity is selected during initialization, the MOTION pin will remain high.

After a time, motion is detected and the MOTION PIN goes high. Once motion is detected the device can no longer enter SLEEP until all pending motion data has been read. The host deasserts the STANDBY pin to enable I^2C comms (if use_standby_pin register was set in initialization routine); motion data is read and the STANDBY pin is re-asserted. After the RunningTimeout period, if no further motion is detected, the device enters the SLEEP1 state. After the Sleep1Latency period, the device wakes up for 1 frame to detect any movement. No motion is detected so the device remains in the SLEEP1 state.

If the POWERDOWN pin is asserted, the internal 1.8 V regulator is disabled and the 1.8 V core supply is switched off. When the POWERDOWN pin is deasserted, the internal 1.8 V regulator is re-enabled and the MCU re-initializes as at power-up before entering the SW STBY state. The device must be re-configured after POWERDOWN.

Figure 10. Automatic power mode timing diagram (use_standby_pin=1)



Key timing parameters are shown in *Table 11*.

Table 11. Automatic mode timing constraints

Symbol	Parameter	Typical
t1	POR Delay (POR threshold = 1.4 V typ)	20 µs
t2	Clock Startup	1 µs
t3	MCU boot time	450 µs
t4	Minimum Powerdown time	10 ms

5 I/O description

5.1 I2C_SEL[2:0]

The default I^{2}C address is 0xA6. However, in some applications the default address may conflict with other I^{2}C devices sharing the bus or it may be necessary to chain multiple OFN devices on the same bus. For that reason, the user can select from one of seven I^{2}C addresses as shown in *Table 12*.

Table 12. User-selectable I^{2}C addresses

I2CSEL[2:0]	8-bit I^{2}C address
000	0xA6
001	Reserved
010	0xC6
011	0xD6
100	0xE6
101	0x36
110	0x46
111	0x20

The I2C_SEL pads have internal pull-down resistors and can be left unconnected for the default address. For any other address, connect pads that require a logic “1” to DVDD (the internal pull-down resistor is automatically disconnected after the internal microcontroller boot sequence is completed to conserve power).

If required, custom configurations can be stored in ROM on the device corresponding to a particular I^{2}C address to reduce the number of required register writes by the host. If interested in this feature, please contact STMicroelectronics.

The device I^{2}C address can also be configured dynamically by writing to register DEVADDR (0x7c) bits [7:1] (see *Table 13*). This sets the 7-bit base I^{2}C address of the device and allows multiple devices with the same default address to be re-mapped dynamically. This operation must be done in 2 steps:

- program register 0x7c using the current device address to program the new one
- access registers with the new device address

Each device must be powered in turn to reconfigure its address and this operation must be repeated each time the system is initialized.

Table 13. Control register to dynamically configure device I^{2}C address

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
7c	DEVADDR	i2cs_index_auto_inc_en	0	PRW	01	Auto increment function
		i2cs_dev_addr	7:1	PRW	53	I^{2}C device address

5.2 LED_OUT (tracking LED) and GPIO0

LED_OUT is controlled by a 3-bit current DAC (0x3 ANALOG_CTRL2 bits [6:4]) capable of driving up to 14 mA (current sink). Where higher power output is required, an external LED driver can be used controlled by GPIO0 (0x3 ANALOG_CTRL2 bit7 and 0xd GPIO_GPIO0 bit 4). *Figure 11* shows the two LED drive options. LED pulse timing is controlled automatically (see *Figure 12*). GPIO0 can also be used as a general purpose I/O and is configured using register 0xd GPIO_GPIO0 bit 4. A typical configuration of a GPIO is shown in *Figure 13 on page 27*.

Figure 11. LED drive options

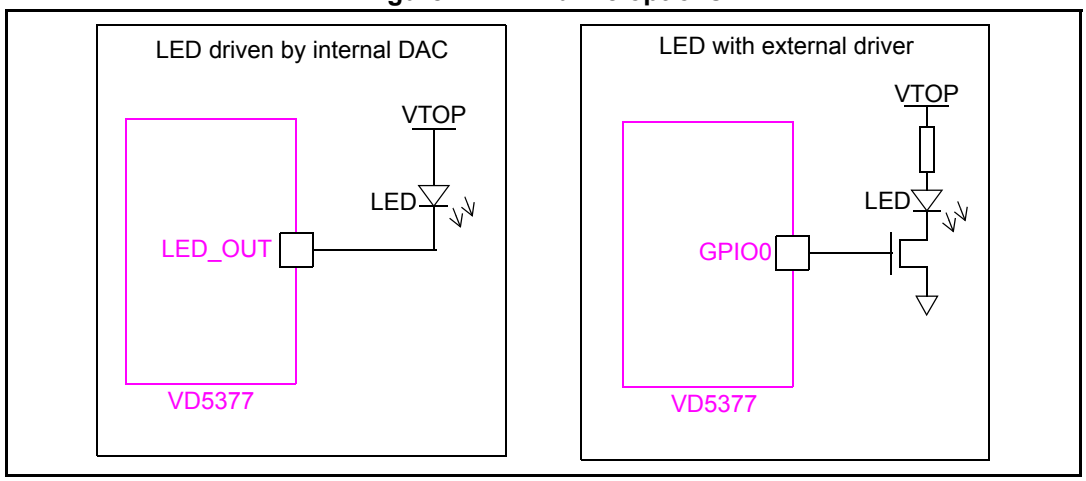


Figure 12. LED control

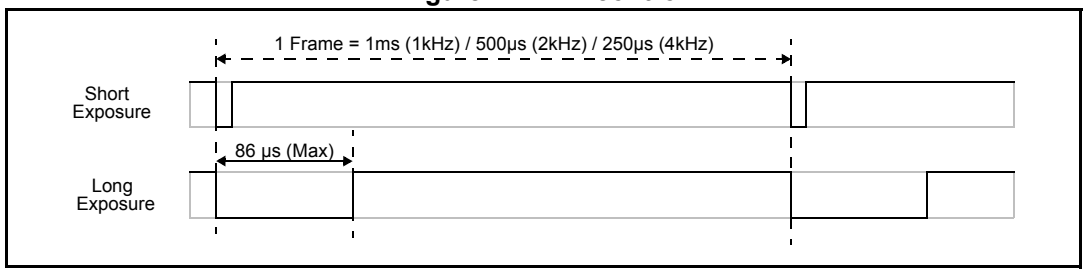


Table 14. Control register for LED_OUT and GPIO0

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
3	ANALOG_CTRL2	led_dac_control	6:4	PRW	07	Adjust Led Drive DAC drive output current. 0 = Iout = 0 mA 1 = Iout = 2.0 mA 2 = Iout = 4.0 mA 3 = Iout = 6.0 mA 4 = Iout = 8.0 mA 5 = Iout = 10.0 mA 6 = Iout = 12.0 mA 7 = Iout = 14.0 mA (default)
		led_out_polarity	7	PRW	01	LED_OUT_EN polarity 0 = High when LED must be ON 1 = Low when LED must be ON
d	GPIO_GPIO0	gpio_gpio0_en	0	PRW	00	GPIO0 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_gpio0_a	1	PRW	00	GPIO0 data output (when _en = 0)
		gpio_gpio0_zi	2	PR	00	GPIO0 IO value
		gpio_gpio0_a_ctrl	4	PRW	00	GPIO0 data output select, either as LED_OUT_EN or from register bank. 0 = Output value from HW register 1 = LED_OUT_EN (polarity set in register 0x3 analog_ctrl2 bit 7)
		gpio_gpio0_opendrain	7	PRW	00	GPIO0 pad open drain control 0 = GPIO0 pad normal config 1 = GPIO0 pad in open drain (A=EN)

Figure 13. Typical configuration of GPIO

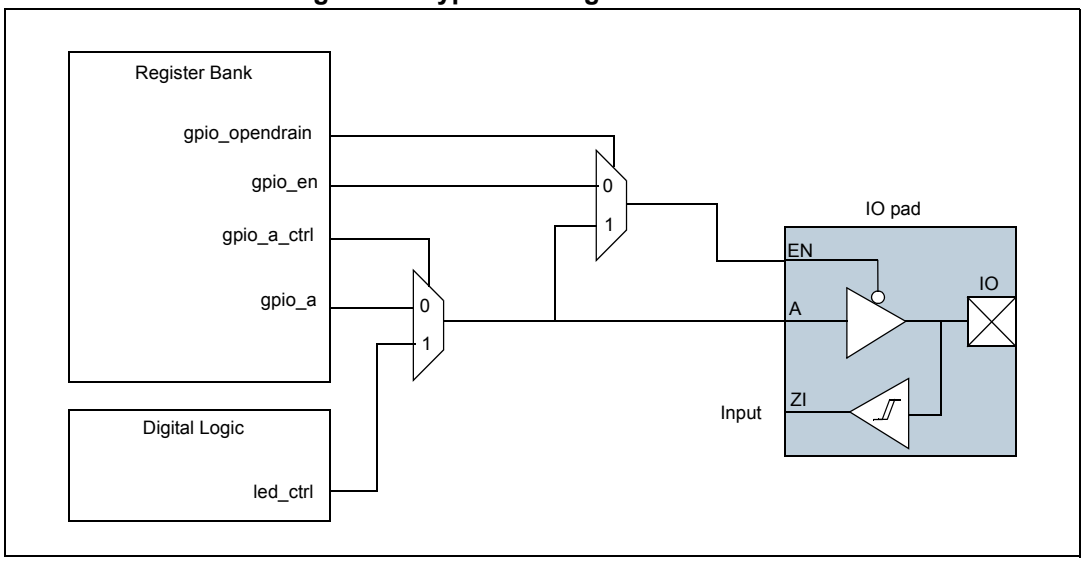


Table 15. Truth-table

gpio_opendrain	gpio_en	gpio_a or led_ctrl	Condition	Output
0	0	0	Output	0
0	0	1	Output	1
0	1	X	Input	-
1	X	0	Open-drain	0
1	X	1	Open-drain	Tri-state

5.3 MOTION

The MOTION pad is a 3.0 V digital I/O pad referenced to VTOP and can be configured either as a push/pull output or open-drain. It combines the functions of motion pending flag and power-on reset indicator (see *Figure 14*). The MOTION signal is driven low at power-up and stays low until the internal MCU boot sequence is completed. Once the boot sequence is completed the MOTION signal goes high and remains high until the device is configured and enters the AUTOMATIC or MANUAL RUN state. Thereafter the level on the MOTION pad depends on the MOTION pin polarity setting (register 0x5 SYSTEM_CONFIG bit 2).

Note: In Powerdown, a 35 kOhm pull-down resistor is activated in the Motion pad. This may result in leakage current in the external circuit. Also, in open-drain configuration, careful choice of pull-up resistor is required to ensure the resultant intermediate voltage on the Motion pad does not induce leakage current in the Motion input gate.

Figure 14. MOTION behavior at power-up

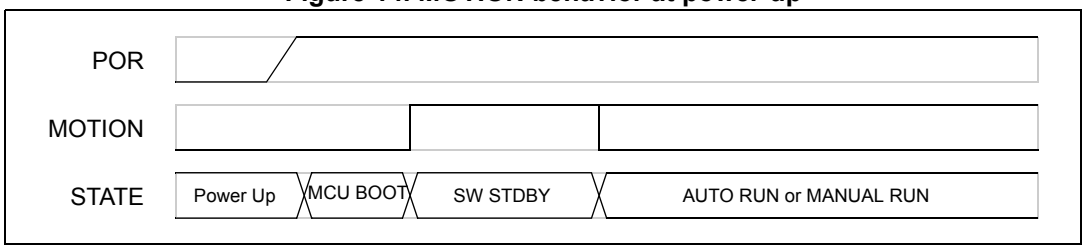


Table 16. Control register for motion pin polarity

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
5	SYSTEM_CONFIG	automatic_power_mode	0	PRW	01	Power mode scheme 0 = Manual 1 = Automatic
		motion_pin_polarity	2	PRW	00	MOTION pin polarity (in non IDLE system state) 0 = MOTION pin LOW when motion detected 1 = MOTION pin HIGH when motion detected
		host_config_done	3	PRW	00	Bit needs to be set by host when configured after power up.
		use_standby_pin	4	PRW	01	STANDBY pin is used as chip select to enable I^2C in AUTO power mode and STANDBY pin is used to wake up the OSC/DVREG (in sleep states in auto power mode). 0 = STANDBY pin not used 1 = STANDBY pin is used
		system_state	7:5	RW	01	Legacy register - please use system_state (0x91) instead.

Table 16. Control register for motion pin polarity (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
c	GPIO_MOTION	gpio_motion_en	0	PRW	00	MOTION output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_motion_a	1	PRW	01	MOTION data output (when _en = 0)
		gpio_motion_zi	2	PR	01	MOTION IO value
		gpio_motion_pd	3	PRW	01	MOTION pull-down control (internal 35 kOhms pull-down resistor) - active LOW 0 = IO is pulled down 1 = IO not pulled down
		gpio_motion_a_ctrl	4	PRW	00	MOTION data output origin 0 = Output value from HW register 1 = Output value from motion detect IP
		Reserved	6:5	PRW	02	Reserved
		gpio_motion_opendrain	7	PRW	00	MOTION pad open drain control 0 = MOTION pad normal config 1 = MOTION pad in open drain (A = EN)

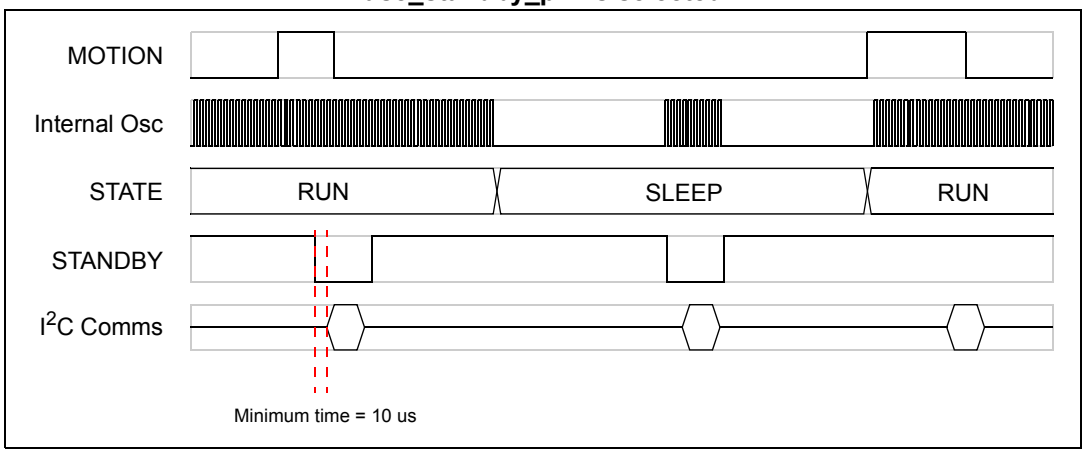
5.4 STANDBY

The STANDBY pad is a 1.8 V digital input (active high/ 5 V tolerant). In MANUAL RUN mode, if STANDBY is asserted the device enters a low power STANDBY state **at the end of the current frame** (see *Figure 7: Manual power mode flow diagram on page 18*). When STANDBY is de-asserted the device resumes in RUN mode without requiring re-initialization.

In AUTOMATIC RUN mode, the STANDBY pin acts as a I^2C enable (see *Figure 15*). When STANDBY = 0, I^2C is enabled and the VD5377 will respond to I^2C communication from the host in either RUN or any of the SLEEP states. When STANDBY = 1 the VD5377 consumes less power but will not respond to I^2C communication. In order to use the STANDBY pin in AUTOMATIC mode the use_standby_pin (register 0x5 SYSTEM_CONFIG bit 4 in *Table 17: Features and scaling on page 32*) must be set during system initialization. If this function is not required, the use_standby_pin register should be set to 0 and the STANDBY pad should be connected to either VDD or VSS.

Note: If use_standby_pin = 1, the STANDBY pin must be set to 0 before each I^2C transaction even if motion data is pending.

Figure 15. In AUTOMATIC mode the STANDBY pin functions as I²C enable if use_standby_pin is selected



5.5 POWERDOWN

POWERDOWN is a 3.0 V capable analog input pad referenced to Vtop. The input switching level is 0.8 V and is compatible with 1.8 V and 2.8 V systems. When POWERDOWN is set to 1 the core 1.8 V digital supply is switched off. The device typically consumes <1 µA in this state[(a)]. When POWERDOWN is set to 0, the internal 1.8 V core regulator is enabled and the power-up sequence is initiated (see *Figure 8: Manual power mode timing diagram on page 19*). The device requires full re-initialization after POWERDOWN.

Note: In a 1.8 V direct drive configuration where the internal regulator is not used, the POWERDOWN pin should be connected to VDD to ensure the regulator is disabled (see Figure 4: 1.8 V direct supply on page 14).

a. See the note in *Section 5.3: MOTION on page 28*.

6 Key features

This chapter gives an overview of some of the most important registers and functions.

6.1 Feature count

Feature count is a measure of the useful detail in an image which is used to match successive frames. Generally, the higher the feature count the better the tracking. The FEATURES register (0x31) in *Figure 17* is an 8-bit value representing the 8 MSBs of a 12-bit internal register. A maximum value of 255 represents a feature count of 16 x 255 = 4080. A reasonable average target feature count is around 2000. Feature counts averaging less than 1000 are likely to result in missing counts and sluggish navigation. This is usually as a result of low contrast in the image or significant vignetting due to the lens.

Note: On some textured surfaces the feature count may exceed 4080. When this occurs the FEATURES register clips at 255. This is normal and does not affect tracking.

6.2 Minimum features threshold

Without any object on the sensor the feature count will be non-zero, typically around 200. This residual value is usually due to the characteristics of the lens and/or pixel noise but may also be caused by internal or external light reflection which can sometimes result in unintentional cursor movement (or jitter). To prevent this unwanted movement, the motion engine is inhibited until the feature count register exceeds the value in the MIN_FEATURES register (0x29). Multiply the register value by 16 to get the actual feature count threshold. Default value is 16d x 16 = 256.

6.3 X/Y scaling

The VD5377 outputs a single count for each one pixel displacement of the object. The physical dimension of one pixel is 30 µm. The actual displacement depends on the magnification of the lens used. For a lens of magnification M = 0.5 one pixel displacement equates to 60 µm physical displacement of the object.

Cursor movement is typically expressed in Counts or Dots per Inch (CPI or DPI). In this case (M = 0.5):

```
Counts per Inch = 25.4mm/60µm = 423 CPI
```

The X/Y scaling registers (*Table 17: Features and scaling on page 32*) can be used to increase or decrease the native CPI according to the following equation:

```
Counts per Inch = register_value x M x 100
```

Scale factors can be applied to X and Y independently to compensate for any lens distortion.

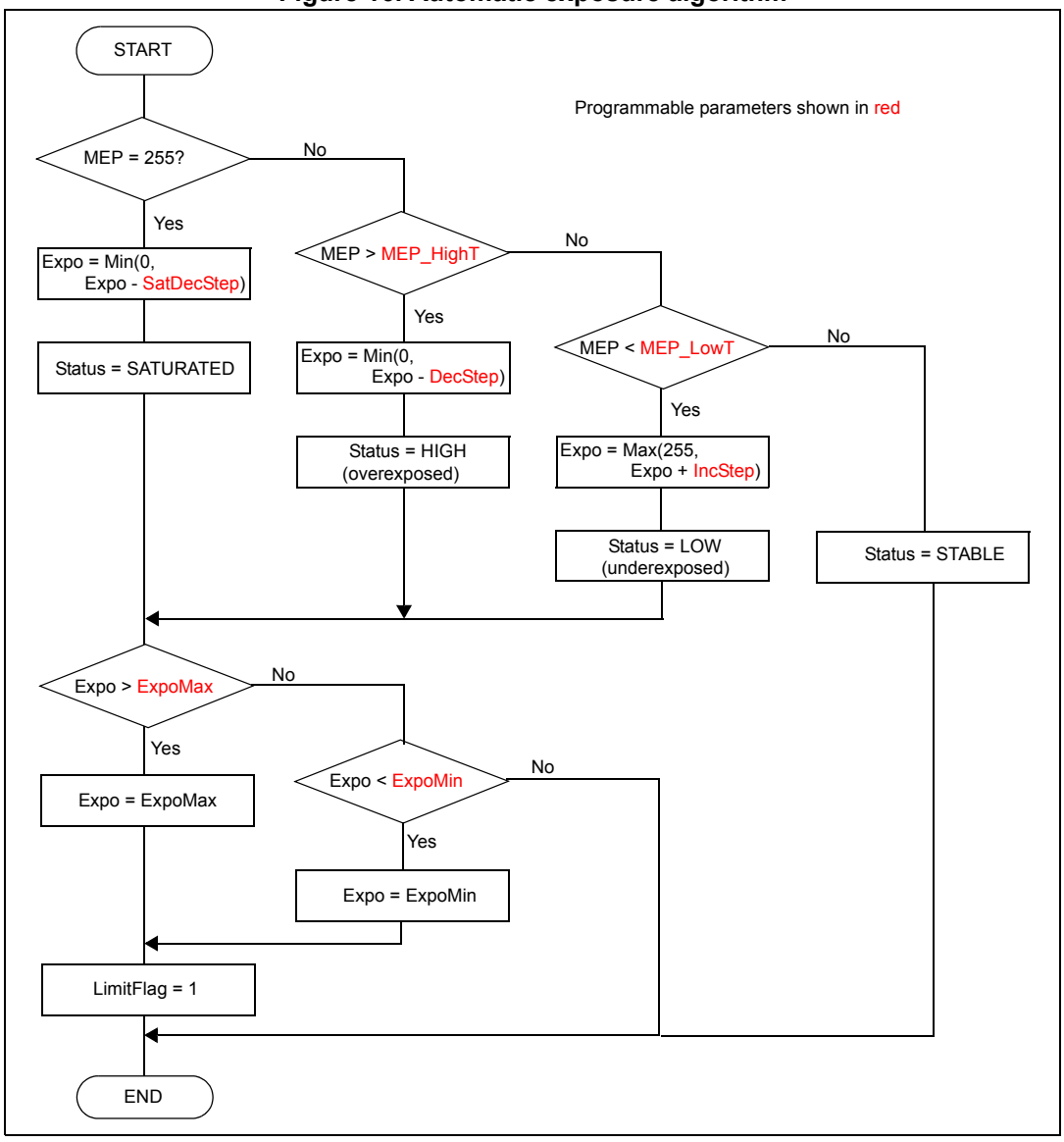
Table 17. Features and scaling

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
29	MIN_FEATURES	min_features	7:0	PRW	10	This register represents the minimum feature count below which motion is inhibited. Multiply by 16 to get the actual feature count threshold. Default is 16d x 16 = 256.
2a	X_SCALING	motion_x_scaling	7:0	PRW	10	Scaling for X motion vectors. Resolution is calculated as register value x 100 x M, where M is the lens magnification. So, for M = 0.5: 0x08 = 400 CPI that is 8 x 100 x 0.5 0x0c = 600 CPI that is 12 x 100 x 0.5
2b	Y_SCALING	motion_y_scaling	7:0	PRW	10	Scaling for Y motion vectors. Resolution is calculated as register value x 100 x M, where M is the lens magnification. So, for M = 0.5: 0x08 = 400 CPI that is 8 x 100 x 0.5 0x0c = 600 CPI that is 12 x 100 x 0.5
31	FEATURES	features_report	7:0	PR	00	Feature count report, as the SUM of absolute differences between pixels and the field average. Bits [11:4] are represented here so x16 to calculate the actual feature count. Maximum value is 4080 = 255 x 16.

6.4 Automatic exposure control

Figure 16 describes the automatic exposure control function. This routine is performed every EXPO_FRAME_UPDATE (register 0x4B).The auto-exposure control algorithm works by adjusting exposure until the brightest (max exposed[a]) pixel in the frame lies within a specified target range. This is to ensure that no part of the frame is saturated.

Figure 16. Automatic exposure algorithm



Manual or automatic exposure control can be selected. This is controlled using register EXPOSURE_CONTROL 0x43 bit 0 (see *Table 18*). Bits [6:4] give the exposure status and bit 7 is the exposure limit flag. In automatic exposure control mode, register EXPOTIME

a. In fact the second brightest pixel is used. Note that AEC operates on the exposed frame, that is, before noise cancellation. Processing is done on the CDS frame which is derived from the exposed frame as follows: CDS frame = Exposed frame - Black frame + 8

0x47 gives the current exposure time. This register is also used to enter the required exposure time in manual exposure mode. Register 0x44 is the MAX_EXPO_PIX (read-only).

Registers 0x45/0x46 are the upper and lower exposure targets (180 to 240 by default). When the MEP is within this range the exposure is judged to have “converged” and no further exposure updates are required until the MEP moves outside the target range. It is not normally required to adjust the exposure targets.

The default exposure range is 1 to 255. These limits are programmable with registers 0x49/0x4a.

By default, exposure update rate is every two frames. This can be adjusted using register 0x4b. Exposure convergence can be modified by changing the exposure increment/decrement step sizes with registers 0x4e/0x4f/0x50.

Table 18. Exposure control

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
43	EXPOSURE_CONTROL	autoexpo_en	0	RW	01	Auto exposure control 0 = Disable 1 = Enable
		autoexpo_status	6:4	R	00	Auto exposure status 0 = UNDEF (no AEC performed yet) 1 = LOW (exposure increasing) 2 = STABLE (max exposed pixel within range) 3 = HIGH (exposure decreasing) 4 = SATURATED (exposure saturation decreasing)
		autoexpo_limit_flag	7	R	00	Exposure limit reached flag 0 = Exposure time within range 1 = Exposure time limit reached
44	MAX_EXPO_PIX	max_exposed_pixel_value	7:0	PR	00	Second maximum pixel value of the current frame (before CDS)
45	MAX_EXPO_PIX_THRESH_HIGH	max_exposed_pixel_thresh_high	7:0	RW	f0	High threshold value of max exposed pixel where the AEC is stable.
46	MAX_EXPO_PIX_THRESH_LOW	max_exposed_pixel_thresh_low	7:0	RW	b4	Low threshold value of max exposed pixel where the AEC is stable.
47	EXPOTIME	exposure_time	7:0	PRW	40	Exposure time value in 3 MHz clk period step (333ns)

Table 18. Exposure control (continued)

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
49	EXPOTIME_MAX	exposure_time_max	7:0	RW	ff	Maximum exposure time applied by the AEC.
4a	EXPOTIME_MIN	exposure_time_min	7:0	RW	01	Minimum exposure time applied by the AEC.
4b	EXPO_FRAME_UPDATE	autoexpo_frame_update	7:0	RW	01	Exposure update frequency (every N+1 frames). Default is every two frames.
4e	EXPOTIME_INC_STEP	expo_inc_step	7:0	RW	04	Exposure increment step (used when below max_expo_pix_thresh_low).
4f	EXPOTIME_DEC_STEP	expo_dec_step	7:0	RW	04	Exposure decrement step (used when above max_expo_pix_thresh_high).
50	EXPOTIME_SAT_DEC_STEP	expo_sat_dec_step	7:0	RW	10	Exposure decrement step (used when above max_expo_pix is saturated = 255).

6.5 5 x 5 high pass filter

Before each frame is processed the image data is passed through a high-pass filter to extract edge information. The PARAMETERS_3 register 0x28 bit 5 (*Table 19*) permits selection between two high pass filter options. 3 x 3 is the default high-pass filter. The alternative 5 x 5 high-pass filter has a lower cut-off frequency and so preserves more information in lower contrast images. This may help improve tracking performance in some situations, although a possible effect is an increase in hover (this can be overcome by increasing min_features threshold, register 0x29).

Table 19. 5x5 high-pass filter register

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
28	PARAMETERS_3	Reserved	3:0	PRW	04	Reserved
		Reserved	4	PRW	01	Reserved
		hpf_5x5_sel	5	PRW	00	Select between 3 x 3 and 5 x 5 high pass filter. 0 = 3 x 3 high pass filter 1 = 5 x 5 high pass filter
		Reserved	6	PRW	01	Reserved

6.6 Sunlight timing

In applications where strong external ambient lighting could interfere with tracking such as direct sunlight, "*Sunlight DMIB timing*" mode is recommended (0x51 bit 1 = 1). This can either be set to always on, that is 0x51 = 0x2 or set to change automatically when the sensor detects high ambient light conditions (that is, 0x51 = 0x1). See *Table 20*. The default is "Normal DMIB timing" mode.

Note: The maximum permitted frame rate in Sunlight timing mode is 3.3 kf/s (see Section 6.7: Automatic/manual frame rate).

Table 20. Sunlight DMIB timing mode

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
51	CONTROL	dmib_ctrl_mode	0	RW	00	DMIB controller timing switch mode 0 = Manual (chosen by dmib_timing register) 1 = Automatic (system auto sets the dmib_timing mode, status reported in dmib_timing register)
		dmib_timing	1	PRW	00	DMIB controller timing mode 0 = Normal DMIB timing (same as 376 with double expo time possible) 1 = Sunlight DMIB timing
		Reserved	7	PRW	00	Reserved

6.7 Automatic/manual frame rate

The VD5377 can operate in either automatic or manual frame rate control mode. The default frame rate control mode is automatic (*see Table 21,* register 0x1c bit 4). This means that the device adjusts frame rate automatically depending on the tracking velocity. By default, frame rate is adjusted in the range 1 k to 2 k to Max. Because power consumption increases as frame rate increases, automatic frame rate control is the most efficient in terms of power consumption and requires no additional overhead from the host CPU. The maximum frame rate to be applied in auto frame rate mode is set with register 0x1c bits 7:5. The default maximum frame rate is 3.3 kf/s. Manual frame rate is selected with register 0x1c bits [2:0].

Table 21. Adaptive frame rate control

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
1c	FRAME_RATE_CONTROL	frame_rate_sel	2:0	PRW	02	Frame rate selection (value for internal osc running @48 MHz) 0 = 0.5kf/s (2 ms period) 1 = 1 kf/s (1 ms period) 2 = 2 kf/s (500 us period) 3 = 2.5kf/s (400 us period) 4 = 2.9kf/s (350 us period) 5 = 3.3kf/s (300 us period) 6 = 3.6kf/s (275 us period) 7 = 4 kf/s (250 us period)
		frame_rate_ctrl	4	RW	00	Frame rate management control 0 = Automatic (1 k / 2 k / Max f/s auto frame rate) 1 = Manual (set with frame_rate_sel reg)
		max_auto_frame_rate	7:5	RW	05	Maximum frame rate to be applied in auto frame rate mode. 0 = not allowed 1 = not allowed 2 = 2 kf/s (500 us period) 3 = 2.5 kf/s (400 us period) 4 = 2.9 kf/s (350 us period) 5 = 3.3 kf/s (300 us period) 6 = 3.6 kf/s (275 us period) 7 = 4 kf/s (250 us period)

Due to CPU bandwidth limitations of the on-board MCU, maximum frame rate is limited to 3.3 kf/s in sunlight timing mode. In Normal DMIB timing mode only (default mode - register 0x51 = 0), the maximum frame rate may be increased up to 4 kf/s but in order to meet internal timing constraints, the maximum exposure time (EXPOTIME_MAX 0x49) needs to be reduced according to *Table 22*. The motion_threshold_low_comp (SPARE 0x32) should also be updated.

Table 22. Modified exposure limits

	Frame rate control mode					
	Automatic			Manual		
Maximum frame rate	3.3 kf/s	3.6 kf/s	4 kf/s	3.3 kf/s	3.6 kf/s	4 kf/s
Maximum exposure	255	232	157	255	249	174

Table 23. Motion threshold

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
32	SPARE	Reserved	0	RW	00	Reserved
		Reserved	1	RW	00	Reserved
		motion_threshold_low_comp	7:4	RW	03	Update motion_threshold_low register for adaptive frame rate: 0 = 4 kf/s 2 = 3.6 kf/s 3 = 3.3 kf/s

7 Additional features

7.1 Auto-movement filter

An auto-movement filter has been added in VD5377 rev 2.0 to enhance the navigation performance in high ambient light conditions.

The filter can only be enabled in automatic power mode[(b)]. On initial wakeup, after sleep, the filter will hold the sensor in the lowest run state until motion is seen is X times in Y period. Both X and Y are programmable.

With the default settings, the AMF will look for motion in three separate 7 ms periods. Once motion is seen in one 7 ms period, the filter will immediately move onto the next 7 ms period.

Table 24. Auto-movement filter

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
8d	AUTO_MOVEMENT_CTRL1	bAutoMoveFilterEnable	0	RW	00	Auto movement filter enable 0 = Disable 1 = Enable
		ucAutoMoveFilterFrameNb	6:1	RW	07	Number of frames on which the auto movement filter is applied (must be greater than 1).
		bAutoMoveSaturatedExpo	7	RW	00	When image in high light and exposure (reg 0x47) is set to 1, flag used by engine to discard motion in this condition. 0 = Disable 1 = Enable

b. Automatic power mode without standby (SYSTEM_CONFIG 0x5 = 0x09) does not function correctly when the auto-movement filter is enabled. Suggested workaround is to use automatic power mode with use_standby_pin enabled. Alternatively, there is a firmware patch available which can be requested from STMicroelectronics.

Table 24. Auto-movement filter (continued)

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
8e	AUTO_MOVEMENT_CTRL2	ucAutoMoveFilterLatency	3:0	RW	01	Latency between frames on which the auto movement filter is applied. 0 = 400 us 1 = 1 ms 2 = 1.4 ms 3 = 2 ms 4 = 4 ms 5 = 10 ms 6 = 20 ms 7 = 50 ms 8 = 100 ms 9 = 150 ms 10 = 200 ms 11 = 500 ms 12 = 1 s 13 = 1.5 s 14 = 2 s 15 = 2.6 s
		ucAutoMoveFilterLoop	7:4	RW	03	Set the number of sequences to detect motion to grant motion in sleep mode.

7.2 Adaptive CPI

To be able to cope with large screen resolution an adaptive CPI functionality has been implemented in VD5377, where the motion scaling can be adjusted depending on the speed of the detected motion.

The algorithm is shown in *Figure 17* where maximum motion is max_abs_motion (register 0x2f).

Figure 17. Adaptive CPI algorithm

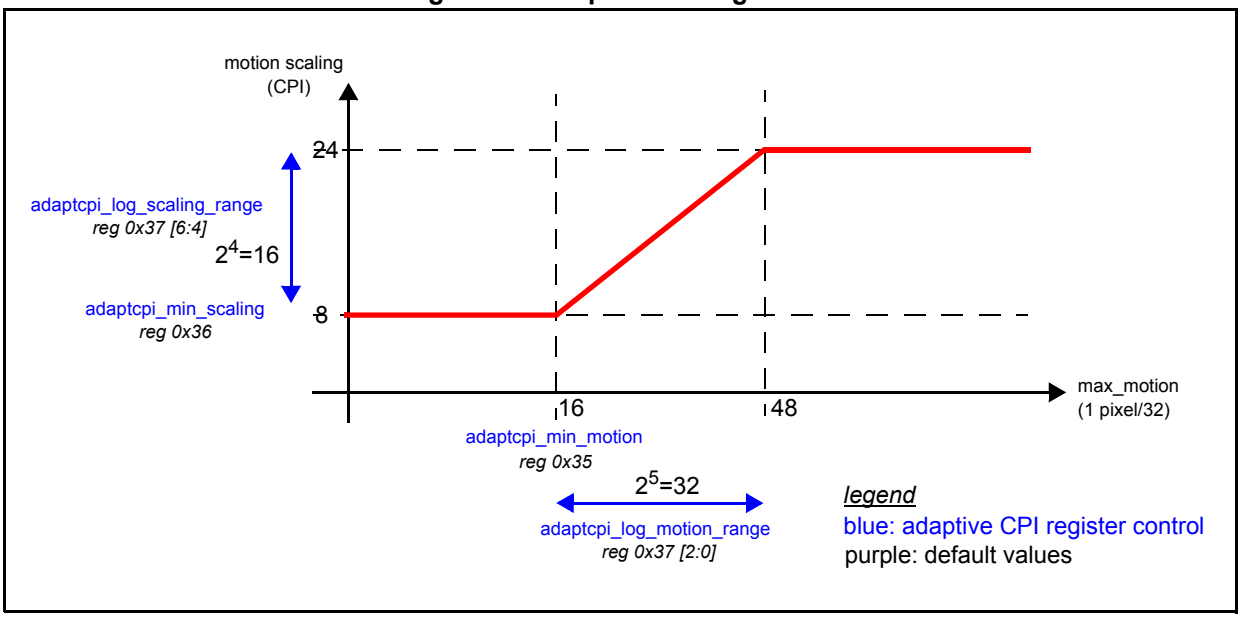


Table 25. Adaptive CPI

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
23	OVERFLOW	adapt_cpi_en	6	PRW	00	If set, the CPI is function of the detected motion. 0 = No adaptive CPI 1 = Enable adaptive CPI
2f	MAX_ABS_MOTION	max_abs_motion	6:0	PR	00	Max(ABS(X motion), ABS(Y motion)) either from integrated or instant motion
35	ADAPTCPI_MIN_ MOTION	adaptcpi_min_ motion	7:0	PRW	10	Minimum value of max(|X frame motion|, |Y frame motion|) from which the CPI is adaptive (if feature enabled) - multiply by 1/32
36	ADAPTCPI_MIN_ SCALING	adaptcpi_min_ scaling	7:0	PRW	08	Minimum motion scaling value when adaptive CPI feature is enabled.

Table 25. Adaptive CPI (continued)

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
37	ADAPTCPI_RANGES	adaptcpi_log_ motion_range	2:0	PRW	05	Log value of motion range from which the CPI is adaptive (that is max motion = min + 2^adaptcpi_log_motion_range) 0 = motion range = 1 1 = motion range = 2 2 = motion range = 4 3 = motion range = 8 4 = motion range = 16 5 = motion range = 32 6 = motion range = 64 7 = motion range = 128
		adaptcpi_log_ scaling_range	6:4	PRW	04	Log value of motion scaling range from which the CPI is adaptive (that is max scaling = min + 2^adaptcpi_log_scaling_range) 0 = scaling range = 1 1 = scaling range = 2 2 = scaling range = 4 3 = scaling range = 8 4 = scaling range = 16 5 = scaling range = 32 6 = scaling range = 64 7 = scaling range = 128

7.3 BACKLED[2:0]

Three pads are provided to optionally drive up to three backlight LEDs. Each pad is a 4 mA (current limited), digital I/O with open-drain capability which can drive up to three LEDs independently or can be combined to drive a single LED up to 12 mA (see *Figure 18.*). Each output can be controlled by an independent PWM controller to provide a versatile dimming function. When combined, all three pads are driven by PWM0. The PWM signals are automatically gated during pixel integration to ensure there is no light pollution of the tracking function. BACKLED control registers are shown in *Table 26*. These pads can also be used as GPIO.

Note: The BACKLED[2:0] pads are tri-state by default and should be connected to ground if not used.

Figure 18. BACKLED configuration

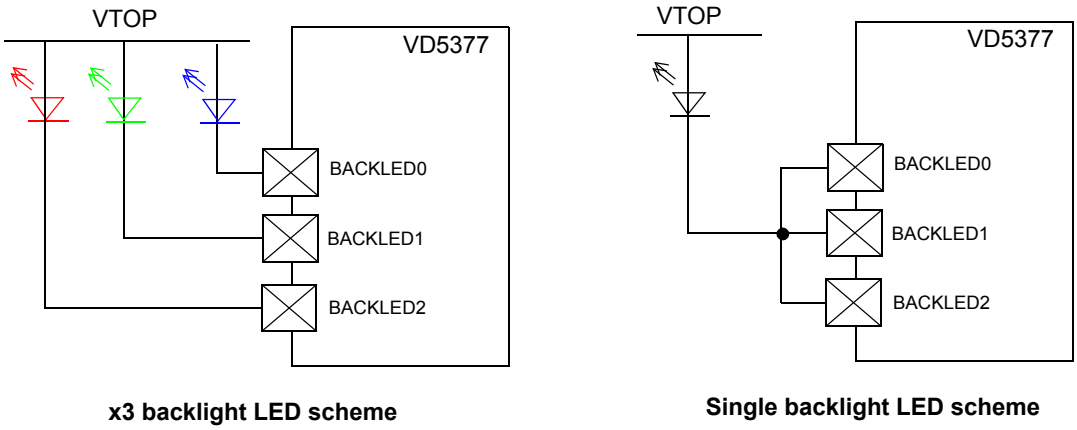


Table 26. BACKLED control registers

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
9	GPIO_BACKLED0	gpio_backled0_en	0	PRW	00	BACKLED0 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_backled0_a	1	PRW	01	BACKLED0 data output (when _en = 0)
		gpio_backled0_zi	2	PR	01	BACKLED0 IO value
		gpio_backled0_tm	3	PRW	00	Reserved. Do not modify this bit.
		gpio_backled0_a_ ctrl	4	PRW	00	BACKLED0 data output origin 0 = Output value from HW register 1 = Output value from PWM 0
		gpio_backled0_ opendrain	7	PRW	01	BACKLED0 pad open drain control 0 = BACKLED0 pad normal config 1 = BACKLED0 pad in open drain (A=EN)

Table 26. BACKLED control registers (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
a	GPIO_BACKLED1	gpio_backled1_en	0	PRW	00	BACKLED1 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_backled1_a	1	PRW	01	BACKLED1 data output (when _en = 0)
		gpio_backled1_zi	2	PR	01	BACKLED1 IO value
		gpio_backled1_tm	3	PRW	00	Reserved. Do not modify this bit.
		gpio_backled1_a_ ctrl	4	PRW	00	BACKLED1 data output origin 0 = Output value from HW register 1 = Output value from PWM 1
		gpio_backled1_ opendrain	7	PRW	01	BACKLED1 pad open drain control 0 = BACKLED1 pad normal config 1 = BACKLED1 pad in open drain (A = EN)
b	GPIO_BACKLED2	gpio_backled2_en	0	PRW	00	BACKLED2 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_backled2_a	1	PRW	01	BACKLED2 data output (when _en = 0)
		gpio_backled2_zi	2	PR	01	BACKLED2 IO value
		gpio_backled2_tm	3	PRW	00	Reserved. Do not modify this bit.
		gpio_backled2_a_ ctrl	4	PRW	00	BACKLED2 data output origin 0 = Output value from HW register 1 = Output value from PWM 2
		gpio_backled2_ opendrain	7	PRW	01	BACKLED2 pad open drain control 0 = BACKLED2 pad normal config 1 = BACKLED2 pad in open drain (A = EN)
f	PWM_PERIOD	pwm_period	7:0	PRW	ff	PWM period duration (20 us tick period)
10	PWM_PULSEHIGH0	pwm_pulse_high0	7:0	PRW	00	PWM 0 pulse high duration (20 us tick period) - 0 = disable
11	PWM_PULSEHIGH1	pwm_pulse_high1	7:0	PRW	00	PWM 1 pulse high duration (20 us tick period) - 0 = disable
12	PWM_PULSEHIGH2	pwm_pulse_high2	7:0	PRW	00	PWM 2 pulse high duration (20 us tick period) - 0 = disable

Table 26. BACKLED control registers (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
83	BACKLIGHT_ CONTROL	bBackLightEnable	0	RW	00	BACKLED PWM enable 0 = Disable 1 = Enable
		bSingleBackled	1	RW	00	Single BACKLED scheme control par PWM0 only 0 = 3 independent BackLEDs 1 = BackLED controlled by PWM 0
		bPwmPolarity	2	RW	00	BACKLED PWM signal polarity 0 = High when LED must be ON (=pwm0) 1 = Low when LED must be ON (=!pwm0)
		bBackledGaterEnable	3	RW	00	Enable the gating of BACKLED PWM signal with DMIB gater signal 0 = Disable 1 = Enable
		bPwmHoldEnable	4	RW	00	Enable the hold mechanism when DMIB gater signal is ON 0 = Disable 1 = Enable
		bBackLightReset	7	RWC	00	In SW STBY, reset the control of backlight control (self cleared) 0 = Disable 1 = Enable

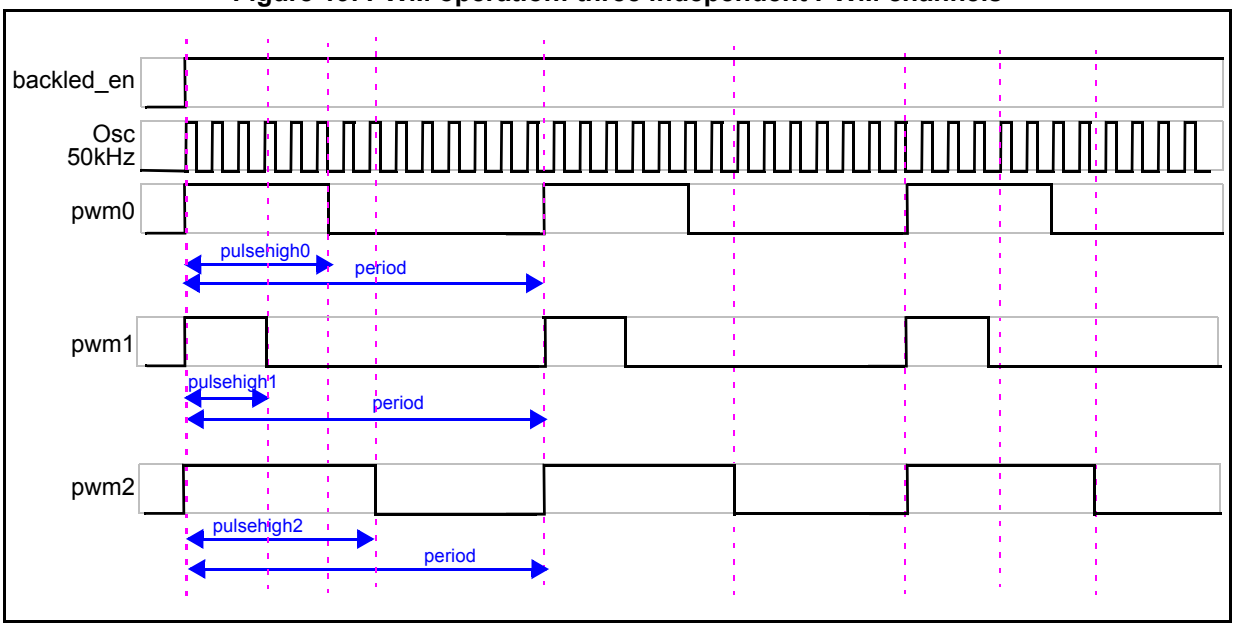
7.3.1 PWM operation

The following list is a summary of PWM operation (*Figure 19*).

- The PWM block is clocked by the internal 50 kHz oscillator which means in STANDBY state in MANUAL power mode and in SLEEP states in AUTOMATIC power mode the backlight LEDs are still running.
- Maximum LED period is 5.12 ms (256 x OSC50K clock period).
- Programmable pulse width (from 0 to 5.12 ms).
- BACKLED pulses can be “gated” or “delayed” during the tracking LED “on” time to avoid interference with the tracking function. This should not be required if the BACKLED are shielded.

Note: No test is performed on pulsehigh value versus period value so the host must ensure that pulsehigh < period.

Figure 19. PWM operation: three independent PWM channels



8 Basic start-up information

8.1 Register override

To ensure correct operation over the device operating temperature range (see *Table 34: Operating conditions on page 61*) it is recommended to make the single register override specified in *Table 27* as part of the user initialization of the device in sw_standby.

Table 27. Analog_ctrl2 recommended setting

Addr (Hex)	Register name	Default setting (Hex)	Recommended setting	Description
3	ANALOG_CTRL2	0xf4	0xfc	Bits [3:2] DMIB DAC Vref setting = 1.6V

8.2 Recommended start-up settings

The VD5377 needs to be initialized after power-up. The only required register write is host_config_done = 1 (SYSTEM_CONFIG 0x5 bit 3). The rest of the start up settings vary depending on application type.

The registers in *Table 28* are the most commonly used on power on. (See *Table 38: I2C register map on page 67* for more details about the registers.)

Table 28. Start-up settings

Register address	Description
0x3	Set LED DAC current (max is default) and register override
0xc	Set motion pin pin to open drain or push/pull (default)
0x27	Set X/Y direction
0x29	Set min features (default = 256 [16 x 16d])
0x2a / 0x2b	Set X/Y scaling
0x51	Set sun mode on (off is default)
0x5(1)	Set Auto/Manual power mode, motion pin polarity, use_standby_pin and host_config_done

1. Customers are advised to set up the sensor (that is, CPI, XY direction and so on) before setting host_config_done.

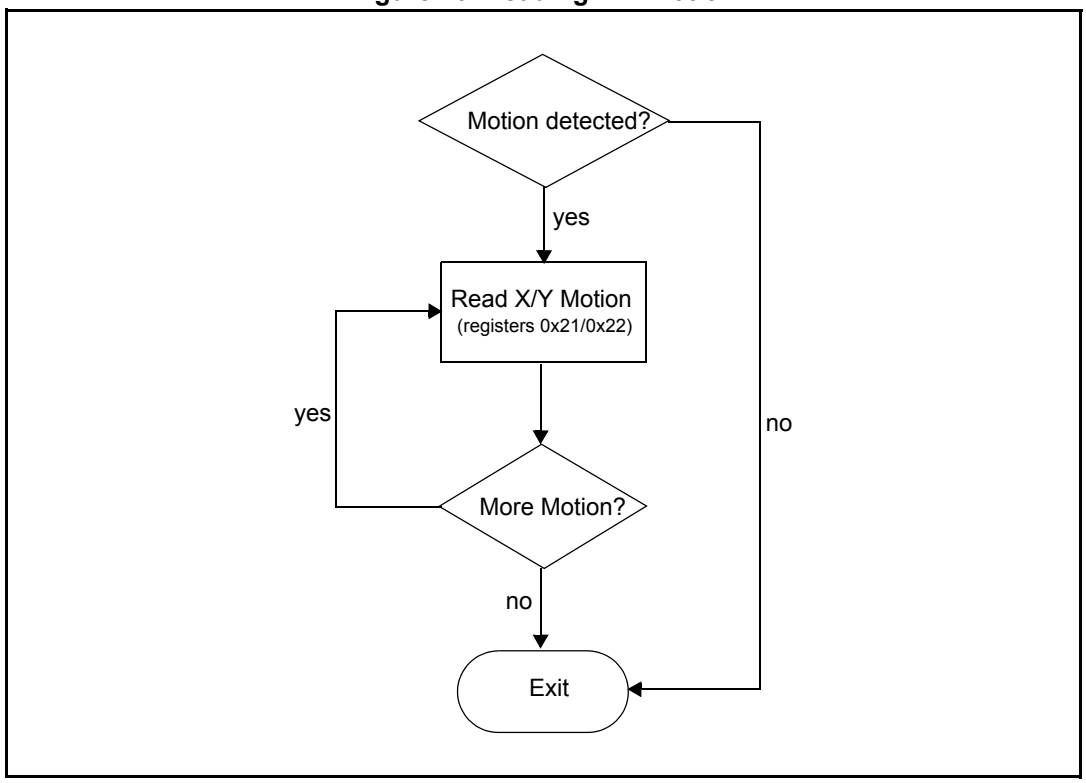
As an example, the initialization routines could use the following sequence.

1. Sensor in automatic power mode without “use standby pin”, int LED_DAC set at max current, 800CPI (M = 0.5), motion pin polarity high (push-pull).
   - Register 0x5 = 0xd
     ([0] - automatic power mode, [2] - motion pin high, [3] - host config done)
2. Sensor in automatic power mode with “use standby pin”, int LED_DAC set to 10 mA, register override, 800 CPI (M = 1), motion pin polarity high (open drain).
   - Register 0x3 = 0x5c
     ([3:2] - register override and [6:4] - LED DAC current)
   - Register 0xc = 0xce
     ([7:0] - motion open drain)
   - Register 0x2a/0x2b = 0x8
     ([7:0] - 800 CPI for 1 x magnification)
   - Register 0x5 = 0x1d
     ([0] - automatic power mode, [2] - motion pin high, [3] - host config done and [4] - use standby pin)
3. Sensor in manual power mode with “use standby pin”, int LED_DAC set at max current, 1000 CPI (M = 0.5), motion pin polarity low (push-pull), sunlight mode on, min features set to 1024.
   - Register 0x29 = 0x40
     ([7:0] - min features)
   - Register 0x2a/0x2b = 0x14
     ([7:0] - 1000 CPI for 0.5 x magnification)
   - Register 0x51 = 0x2
     ([1:0] - sunlight mode on)
   - Register 0x5 = 0x18
     ([0] - manual power mode, [2] - motion pin low, [3] - host config done and [4] - use standby pin)

8.3 Reading X/Y motion data

The host can service motion data either by polling the motion signal on a regular basis or by using the motion signal to generate a host interrupt. The procedure for reading X/Y motion vectors is shown in *Figure 20*.

Figure 20. Reading X/Y motion



Note: X/Y motion registers 0x21 and 0x22 must be read consecutively using a multiple location I^2C read sequence. See Section 11.4.4: Multiple location read on page 66.

X/Y motion data is stored internally in a 17-bit accumulator ensuring that no data is lost even if the host CPU is delayed responding to motion. X/Y motion data is read from the accumulator using register 0x21 and 0x22 (see *Table 29*). 0x21/0x22 are 8-bit registers comprising 7 bits of data plus 1 sign bit. The X/Y_overflow bits (register 0x23 bits 0 and 1) indicate when the X/Y motion registers are full and there is more than 1 byte of data to be read. There is no overflow indicator for the accumulator but it is unlikely that an overflow will ever happen in practice.

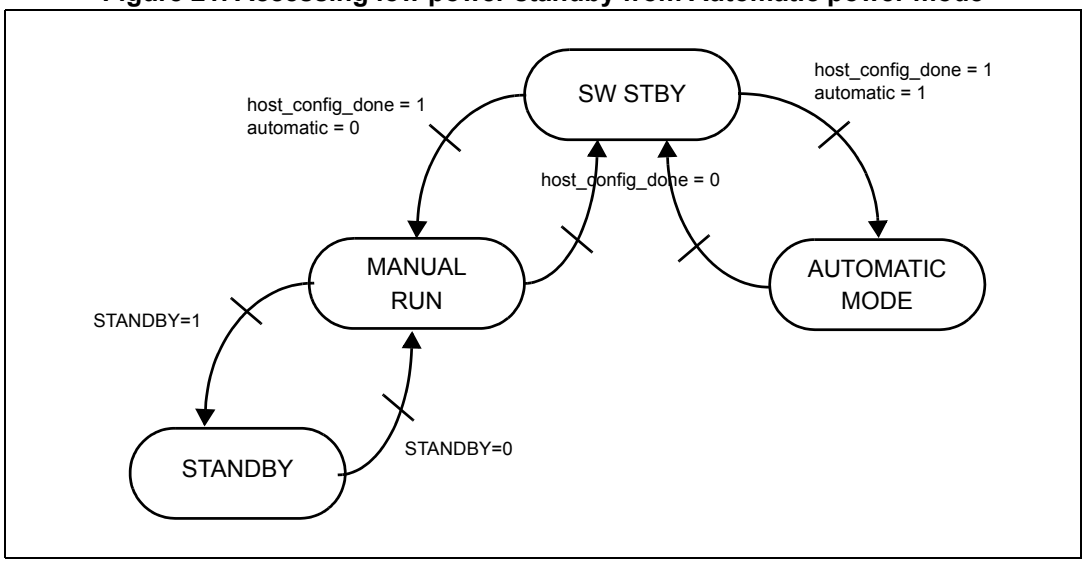
Table 29. X/Y motion data

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
21	X_MOTION	x_motion	7:0	PR	00	X motion data since last polling was done. Note that the internal accumulator is reduced from this value every time it is read.
22	Y_MOTION	y_motion	7:0	PR	00	Y motion data since last polling was done. Note that the internal accumulator is reduced from this value every time it is read.
23	OVERFLOW	x_overflow	0	PR	00	This register records if the X-motion integrator has reached its limit. 0 = No overflow 1 = Overflow
		y_overflow	1	PR	00	This register records if the Y-motion integrator has reached its limit. 0 = No overflow 1 = Overflow
		Reserved	2	PR	00	Reserved
		no_motion	3	PR	01	This bit is asserted as long as both X/Y integrators are empty (logical or between motion_w and motion_y). 0 = Motion 1 = No motion
		motion_acc_flush_en	5	PRWC	00	If set this bit flushes the motion accumulators (self cleared).
		adapt_cpi_en	6	RW	00	If set the CPI is function of the detected motion 0 = No adaptive CPI 1 = Enable adaptive CPI
		Reserved	7	PRW	00	Reserved

8.4 Switching between Automatic mode and Manual mode

This section describes how to use low power standby mode in conjunction with automatic power management mode. Low power standby has to be accessed from MANUAL RUN as shown in *Figure 21*. MANUAL RUN mode is accessed from AUTOMATIC MODE through SW STBY.

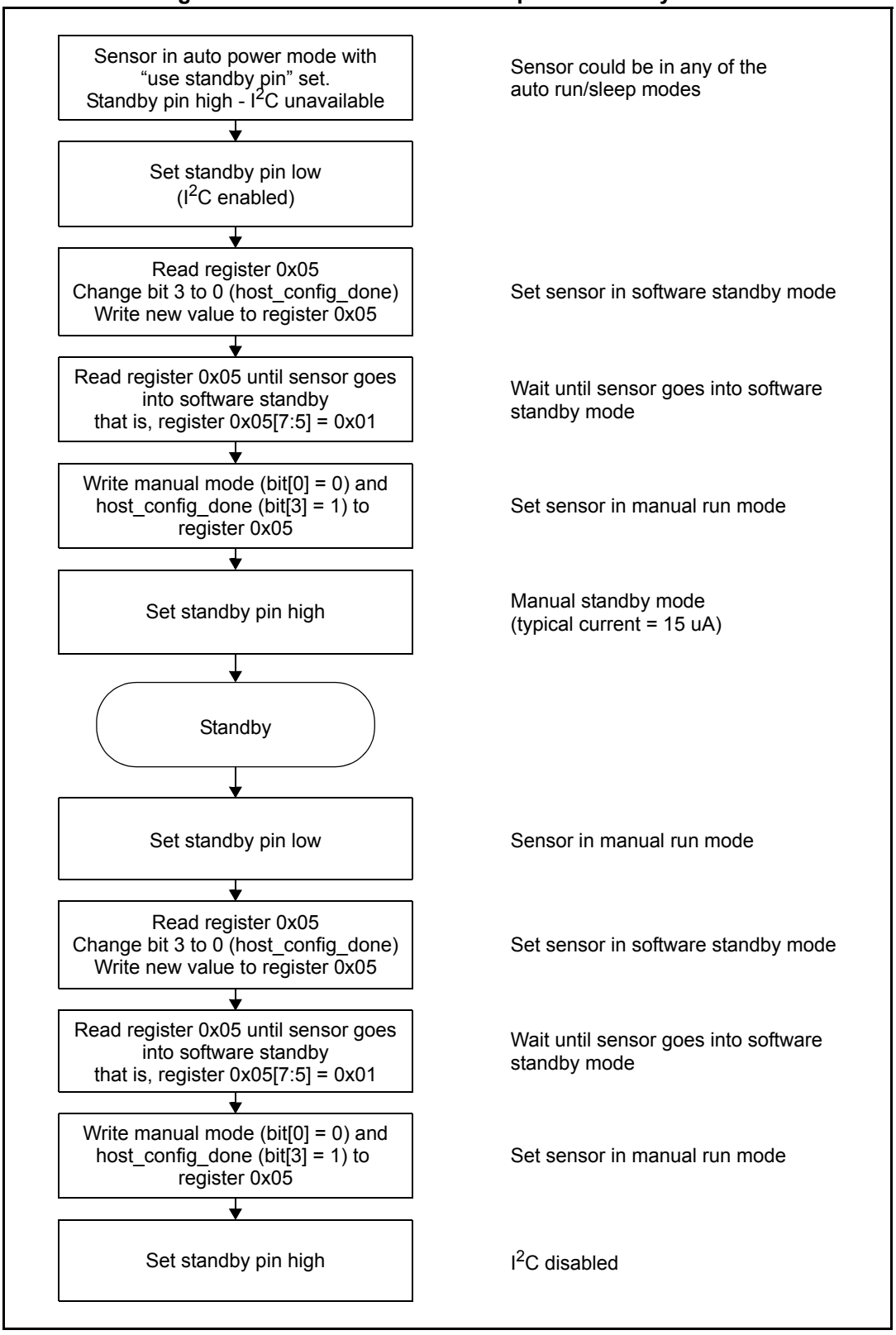
Figure 21. Accessing low power standby from Automatic power mode



The flowchart in *Figure 22* shows the procedure for going into low power standby mode from automatic power mode.

Note: Automatic power mode with "use standby pin" must be used to enable switching between power management modes.

Figure 22. Automatic mode to low power standby mode



8.5 Revision ID

The major and minor revision registers can be used to identify different revisions of the VD5377 silicon as shown in *Table 30*. Currently, only two revisions exist: rev 1.0 (0.0) and rev 2.0 (1.0). Register 0x90 is the device ID and returns 0x4d (77 dec) when read.

Table 30. Major/minor revision registers

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
0	MAJOR_REVISION	major_revision	7:0	PR	01	Major hardware revision number. Updated in case of full mask regeneration. 0 = rev 1.x 1 = rev 2.x 2 = rev 3.x x = minor revision
1	MINOR_REVISION	minor_revision	7:0	RW	00	Minor hardware revision number. Updated in case of metal fix and or ROM changes. 0 = rev 0 1 = rev 1 2 = rev 2
90	DEVICE_ID	ucDeviceID	7:0	RW	4d	Device ID 0 = VD5376 (and previous) 77 = VD5377

8.6 Soft reset

In *Table 31* clearing register 0x16 bit 0 (software_reset_n) initiates an internal reset. All registers are initialized and the MCU performs a reboot. This is equivalent to a power-on reset.

Table 31. Soft reset

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
16	RESETS	software_reset_n	0	PRWC	01	Software reset result in full system reboot (active low - auto cleared)
		reserved	7:1	PRW	0f	Do not modify these bits.

9 Image capture

9.1 I²C image capture

The chip can acquire a single frame coming from the image array (either CDS, exposed or black frame), store it internally (in RAM), and deliver its 400 pixels through I²C registers. A maximum of 105 frames per second can be achieved in this mode.

The timing diagram (*Figure 23*) describes the sequence of steps carried out within a complete frame in I²C frame dump mode.

Figure 23. I²C frame dump timing diagram

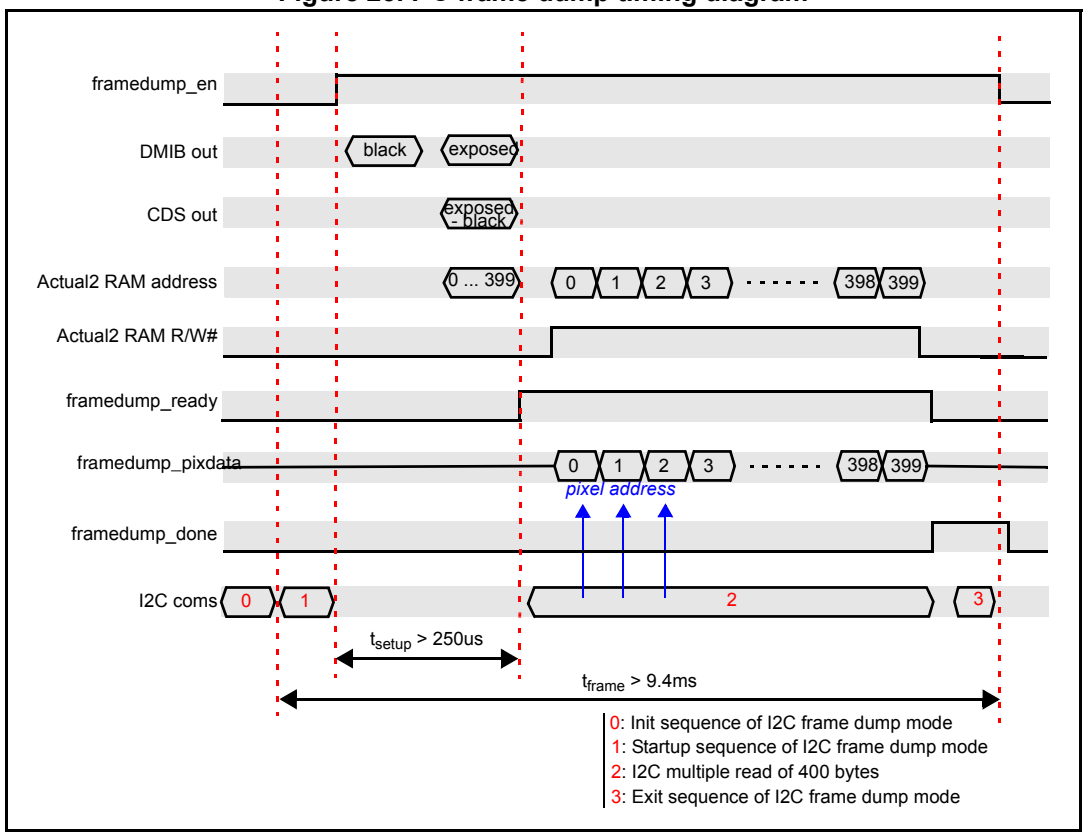


Table 32 lists the registers related to the control of the I²C frame dump mode.

Table 32. I²C frame dump registers

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
3	ANALOG_CTRL2	led_out_dmib_ctrl	0	PRW	00	Select the source of LED out. 0 = Automatic (by DMIB controller) 1 = Direct ctrl (by led_out_manual)
		led_out_manual	1	PRW	00	If led_out_dmib_ctrl is low, LED driver enable control. 0 = LED driver disable (direct ctrl) 1 = LED driver enable (direct ctrl)
		dmib_dac_avdd_sel	3:2	PRW	01	AVDD select for DMIB DAC 0 = AVDD1V5 = 1v45 1 = AVDD1V5 = 1v5 2 = AVDD1V5 = 1v55 3 = AVDD1V5 = 1v6
		led_dac_control	6:4	PRW	07	Adjust LED Drive DAC drive output current. 0 = Iout = 0 mA 1 = Iout = 2 mA 2 = Iout = 4 mA 3 = Iout = 6 mA 4 = Iout = 8 mA 5 = Iout = 10 mA 6 = Iout = 12 mA 7 = Iout = 14 mA
		led_out_polarity	7	PRW	01	LED_OUT_EN polarity 0 = High when LED must be ON (= dmib_led_on) 1 = Low when LED must be ON (= !dmib_led_on)
15	CLOCKS_LO	clk_motion_timer	1	PRW	00	Timer clock enabled (forced always on).
		clk_framedump_en	5	PRW	00	Framedump clock enabled (forced always on).
16	RESETS	framedump_reset_n	5	PRW	00	Framedump reset signal (active low)
19	CONTROL	motion_engine_start	7	PRW	00	Timer interrupt enable. This enables the motion timer to operate. Motion timer generates pulses that trigger frame capture and motion processing.

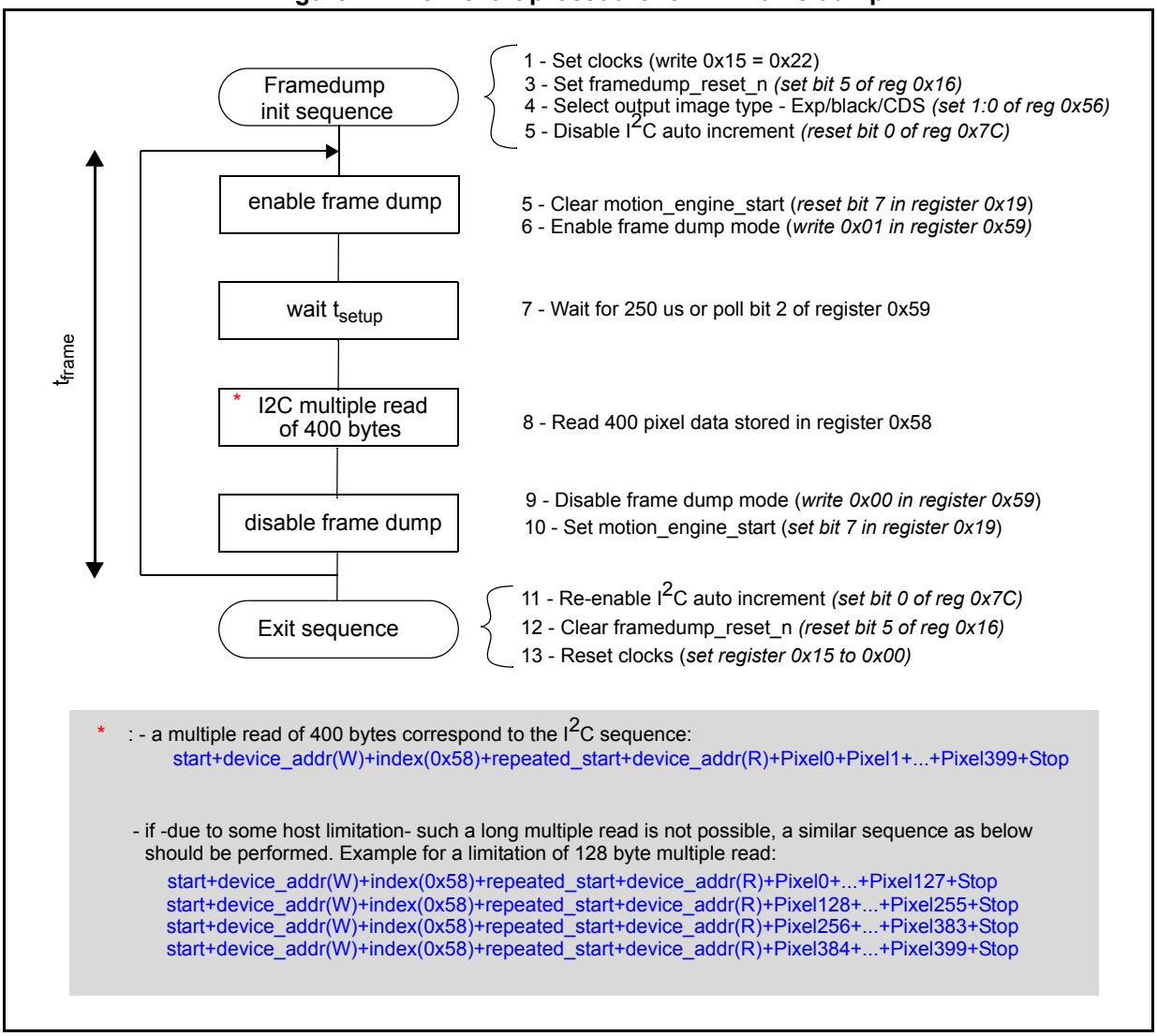
Table 32. I²C frame dump registers (continued)

Addr (Hex)	Register name	Signal name	Bit	Type	Default (Hex)	Comment
56	CDSOUT_SEL	cds_out_sel	1:0	PRW	0	Selects the output from the DMIB controller (going to motion engine and or video output data). 0 = CDS frame 2 = exposed frame 3 = black frame
58	FRAMEDUMP_ PIXDATA	framedump_pixdata	7:0	PR	00	Pixel data in frame dump mode. Automatically increments to next pixel after a read of this register.
59	FRAMEDUMP_CTRL	framedump_en	0	PRW	00	Frame dump mode enable 0 = Disable 1 = Enable
		framedump_start	1	PR	00	Frame dump started
		framedump_ready	2	PR	00	Flag set when a frame is ready to be read by host, Pixel[0] is ready in register FRAMEDUMP_PIXDATA.
		framedump_done	3	PR	00	Flag set when a complete frame (400 pixels) has been read.
		pci_test_enable	4	PRW	00	Muxed PCI data onto pads (2 bits nibble + FST + Qclk) 0 = Disable 1 = Enable
		framedump_mire	7	PRW	00	In frame dump mode outputs a grey scale image (pixel_counter)
7C	DEVADDR	i2cs_index_auto_ inc_en	0	PRW	01	Auto increment function

9.1.1 Step-by-step procedure

The flow chart in *Figure 24* represents the implementation of the I²C frame dump mode from the host's point of view.

Figure 24. Flow chart procedure for I²C frame dump



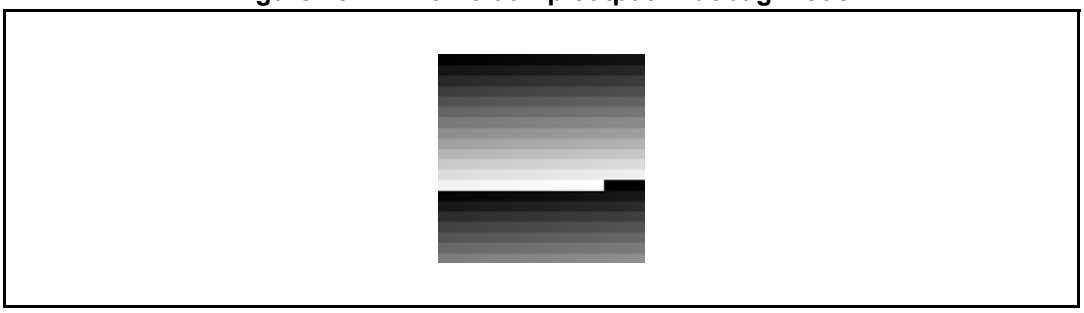
For I²C multiple read see *Section 11.4.4: Multiple location read on page 66*.

9.1.2 Debug mode

The VD5377 implements a debug mode where a grey scale image can be output instead of the image data.

To enter this mode, bit 7 of register 0x59 (“framedump_mire”) must be set. The output frame should resemble the picture in *Figure 25*.

Figure 25. I²C frame dump output in debug mode



9.2 Fast capture

To enter this test mode:

1. Set register 0x5 = 0x18 - sensor in manual power mode and host_config_done set.
2. Set bit 4 of registry 0x15 to 1 (clk_pci_en).
3. Set bit 4 of registry 0x59 to 1 (pci_test_enable).

Table 33. Fast capture

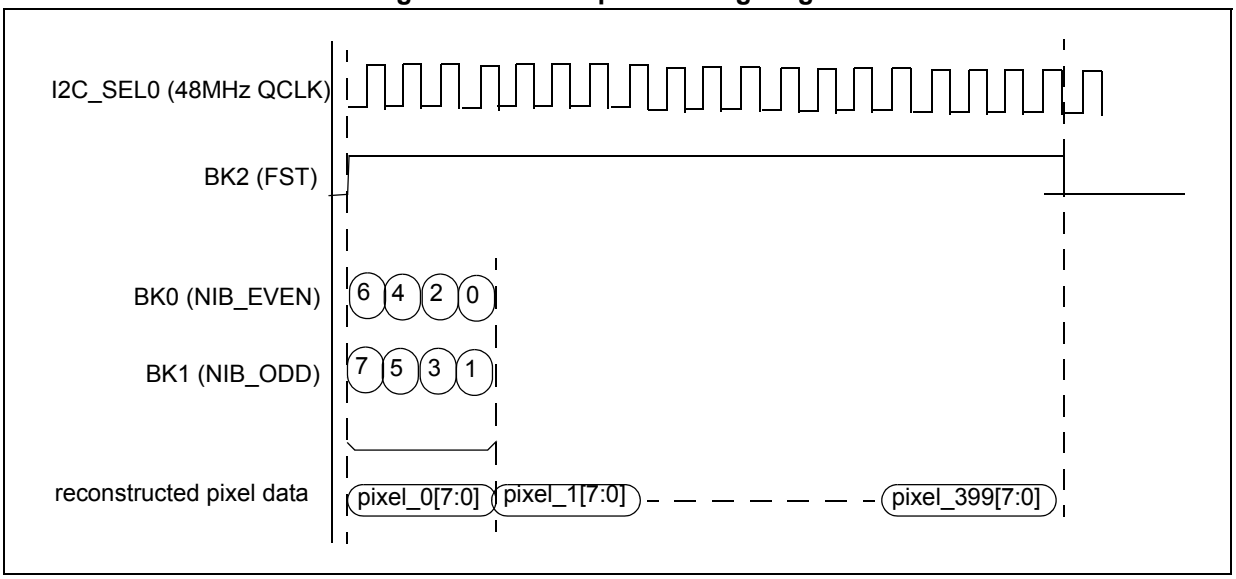
Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
5	SYSTEM_CONFIG	automatic_power_mode	0	PRW	01	Power mode scheme 0 = Manual 1 = Automatic
		motion_pin_polarity	2	PRW	00	MOTION pin polarity (in non IDLE system state) 0 = MOTION pin LOW when motion detected 1 = MOTION pin HIGH when motion detected
		host_config_done	3	PRW	00	Bit needs to be set by host when configured after power up.
		use_standby_pin	4	PRW	01	STANDBY pin is used as chip select to enable I^2C in AUTO power mode and STANDBY pin is used to wake up the OSC/DVREG (in sleep states in auto power mode). 0 = STANDBY pin not used 1 = STANDBY pin is used
		system_state	7:5	RW	01	Legacy register - please use system_state (0x91) instead.
15	CLOCKS_LO	clk_motion_timer	1	PRW	00	Timer clock enabled (forced always on)
		clk_pci_en	4	PRW	00	PCI clock enable (forced always on)
59	FRAMEDUMP_CTRL	pci_test_enable	4	PRW	00	Muxed PCI data onto pads (2 bits nibble + FST + Qclk) 0 = Disable 1 = Enable

In this mode, the pins BK0, BK1, BK2 and I2C_SEL0 are used for serial output of video data in the form of 2 bits nibble + FST and QCLK.

Upon receipt of an FST (BK2) rising edge, NIB_EVEN (BK0) and NIB_ODD (BK1) output data every 48 MHz clock cycle. The signals should be sampled the first rising CLK (I2C_SEL0) edge after the FST rising edge, and then every rising CLK edge after that during the 1600 cycles (400 x 4).

Groups of four consecutive NIB_EVEN and NIB_ODD must then be repackaged together to form a single 8-bit pixel data. This format enables the pixels to be output at the same frame rate as normal operation, and keeps I^2C available to access the usual register settings.

Figure 26. Fast capture timing diagram



10 Electrical characteristics

Typical values are quoted for nominal voltage, process and temperature. Maximum values are quoted for worst case conditions (process, voltage and functional temperature) unless otherwise specified. Current measurements include LED at maximum exposure.

10.1 Operating conditions

Table 34. Operating conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Supply voltage					
VTOP	External supply (using internal regulator)	2.2	-	3.0	V
DVREG	Internal 1.8 V regulator	TBD	1.8	TBD	V
DVDD	External 1.8 V supply (direct drive configuration)	1.7	1.8	1.9	V
Internal system clock frequency					
Fosc	Center frequency = 48 MHz Center frequency = 44 MHz Center frequency = 39 MHz Center frequency = 34 MHz	TBD	45.5 41.5 37.0 32.5	TBD	MHz
Operating current (Automatic mode)					
I_{VTOP}	Auto run (3.3 kf/s)	-	10.2	TBD	mA
I_{VTOP}	Auto run (1 kf/s)	-	4.5	TBD	mA
I_{VTOP}	Sleep 1	-	350	TBD	µA
I_{VTOP}	Sleep 2	-	60	TBD	µA
I_{VTOP}	Sleep 3	-	20	TBD	µA
I_{VTOP}	Powerdown	-	1	TBD	µA
Operating current (Manual mode)					
I_{VTOP}	Manual run (3.3 kf/s)	-	10.2	TBD	mA
I_{VTOP}	Manual run (1 kf/s)	-	4.5	TBD	mA
I_{VTOP}	Standby	-	25	TBD	µA
I_{VTOP}	Powerdown	-	1	TBD	µA
LED drive current					
LED_OUT	Internal LED driver: led_dac_setting = 7 (Max) led_dac_setting = 4 (Mid)) led_dac_setting = 1 (Min)		 14.0 8.0 2.0	 TBD TBD TBD	mA

Table 34. Operating conditions (continued)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
Storage and normal operating temperature					
T_{AS}	Storage temperature	-40	-	+85	°C
T_{AN}	Normal operating temperature	-20	-	+70	°C

10.2 Digital I/O

Table 35. Digital IO electrical characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
CMOS digital inputs					
V_{IL}	Low level input voltage	0		0.3 VDD	V
V_{IH}	High level input voltage	0.7 VDD		VDD	V
I_{IL}	Low level input current			-1	µA
I_{IH}	High level input current			1	µA
CMOS digital outputs					
V_{OL}	Low level output voltage (4 mA load)			0.15	V
V_{OH}	High level output voltage (4 mA load)	VDD to 0.15			V

Note: In Table 35, VDD = 1.8 V for all digital I/O except for MOTION, GPIO0 and POWERDOWN which are referenced to VTOP.

Note: POWERDOWN input switching level is 0.8 V.

10.3 I^2C timing

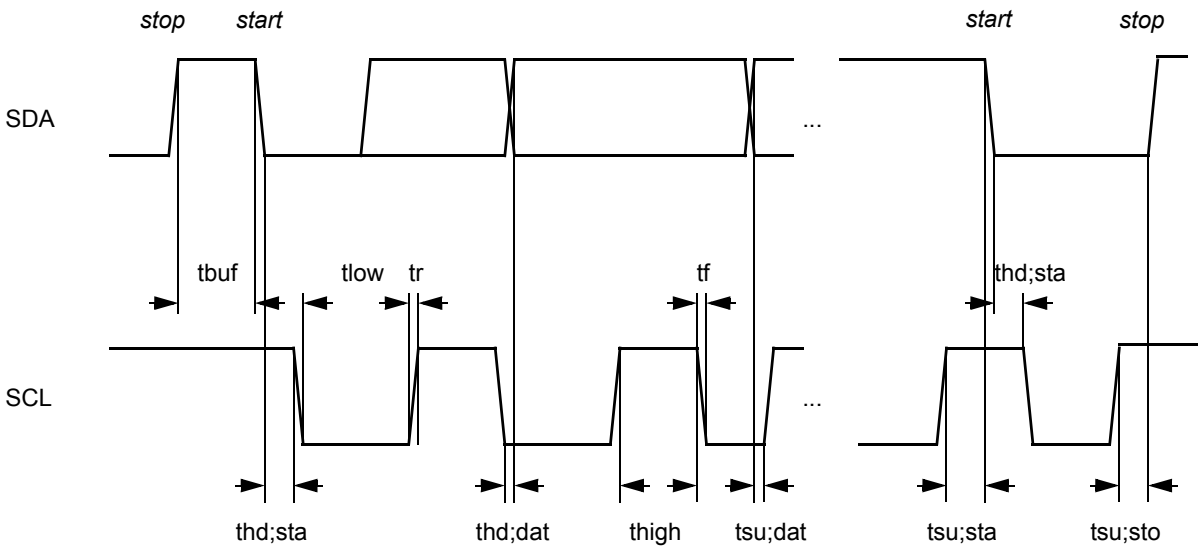
Table 36. I^2C timing characteristics

Symbol	Parameter	Minimum	Maximum	Unit
f_{SCL}	SCL clock frequency	100	400	kHz
tbuf	Bus free time between a ***stop*** and a ***start***	1.3		ns
thd;sta	Hold time for a repeated ***start***	0.6		µs
tlow	LOW period of SCL	1.3		µs
thigh	HIGH period of SCL	0.6		µs
tsu;sta	Set-up time for a repeated ***start***	0.6		µs
thd;dat	Data hold time	300		ns
tsu;dat	Data Set-up time	100		ns
tr	Rise time of SCL, SDA	20+0.1 Cb	300	ns

Table 36. I²C timing characteristics (continued)

Symbol	Parameter	Minimum	Maximum	Unit
tf	Fall time of SCL, SDA	20+0.1 Cb	300	ns
tsu;sto	Set-up time for a ***stop***	0.6		µs
Cb	Capacitive load of each bus line (SCL, SDA)	-	400	pF

Figure 27. I²C timing characteristics



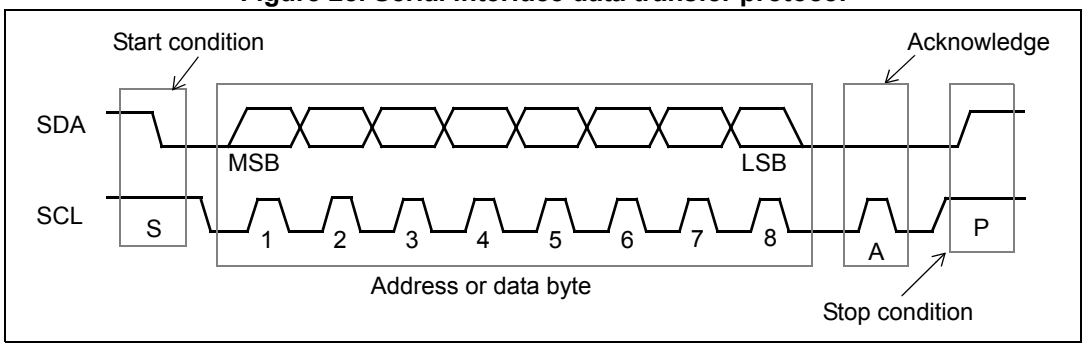
All values referred to the minimum input level (high) = 0.7 VDD, and maximum input level (low) = 0.3 VDD

11 I²C interface

The interface is 400 kHz I²C, with very fast polling rate for high CPI applications (down to 1 ms period).

11.1 Protocol

Figure 28. Serial interface data transfer protocol

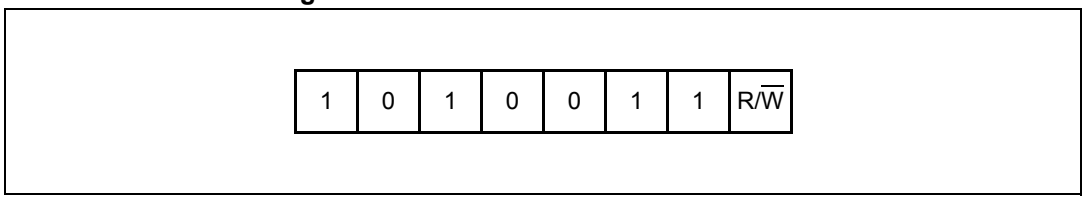


11.2 Data format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

The first byte contains the device address byte which includes the data direction read (R), ~write ($\overline{W}$), bit.

Figure 29. VD5377 serial interface address



The byte following the address byte contains the address of the first data byte (also referred to as the index).

11.3 Message interpretation

All serial interface communications with the sensor must begin with a start condition. If the start condition is followed by a valid address byte then further communications can take place. The sensor acknowledges the receipt of a valid address by driving the SDA wire low. The state of the read/~write bit (LSB of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted.

During a write sequence the second byte received is an address index and is used to point to one of the internal registers. The serial interface automatically increments the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition or sends a repeated start, (Sr).

As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the content of the addressed register is then parallel loaded into the serial/parallel register and clocked out of the device by SCL.

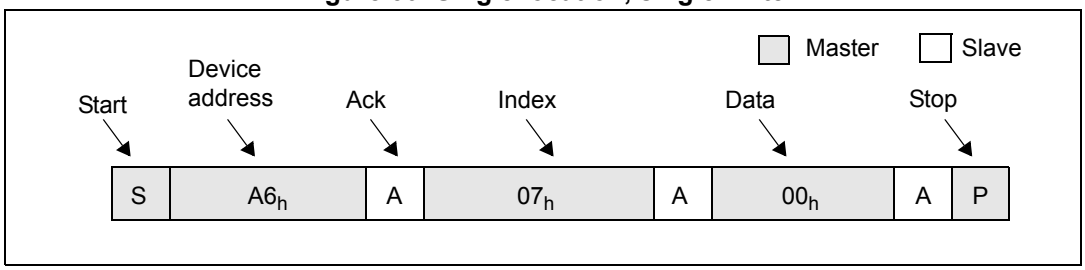
At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge (NAck) after reading a complete byte during a read operation.

11.4 Type of messages

11.4.1 Single location, single data write

When a random value is written to the sensor, the message appears as shown in *Figure 30*.

Figure 30. Single location, single write

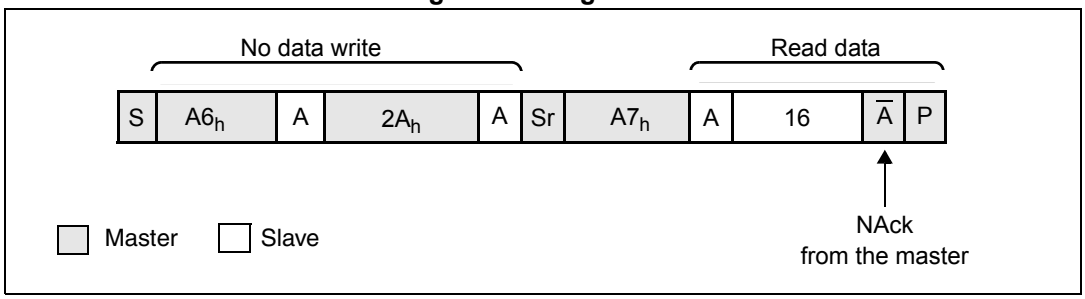


The R/W bit is set to zero for writing. The write message is terminated with a stop condition from the master.

11.4.2 Single location read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial bus to another master a repeated start condition is set between the write and read messages. In the example in *Figure 31*, the X motion vector scaling value (index 0x2A) is read.

Figure 31. Single read



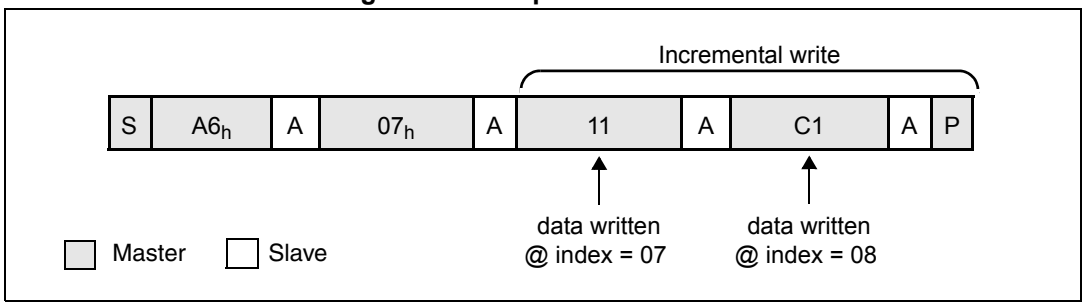
As mentioned in the previous example, the read message is terminated with a negative acknowledge ($\overline{A}$) from the master.

11.4.3 Multiple location write

It is possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte.

Note: An auto-increment write is assumed if no stop condition occurs.

Figure 32. Multiple location write

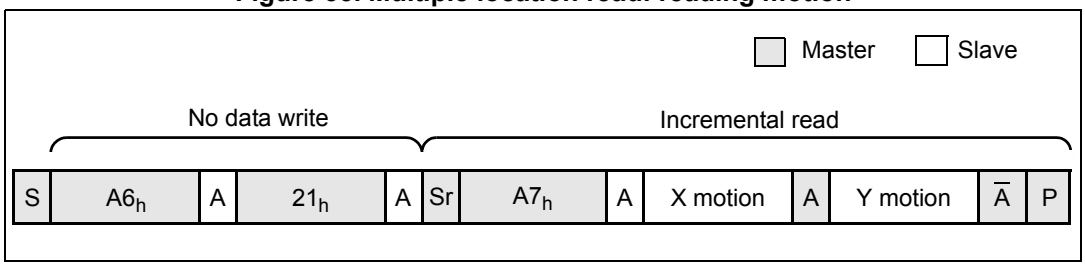


11.4.4 Multiple location read

Multiple locations can be read within a single read message. An auto-increment write is assumed.

Note: Registers are read until the master NAcks the data.

Figure 33. Multiple location read: reading motion



Note: When reading X/Y motion data a multiple read must be performed.

12 I²C register map

Table 38 contains a subset of device registers which may be required by the end user.

Note: Register addresses and default values are in hexadecimal.

The “default” column refers to the power-on register values in software standby before user initialization. The register type definitions are summarized in *Table 37*.

Table 37. Register types

Type	Description
PR	Hardware Read only register
PRW	Hardware Read/Write register
PRWC	Hardware Read/Write register with auto set/clear
R	Firmware Read register
RW	Firmware Read/Write register

Table 38. I²C register map

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
0	MAJOR_REVISION	major_revision	7:0	PR	01	Major hardware revision number. Updated in case of full mask regeneration. 0 = rev 1.x 1 = rev 2.x 2 = rev 3.x x = minor revision
1	MINOR_REVISION	minor_revision	7:0	RW	00	Minor hardware revision number. Updated in case of metal fix and or ROM changes. 0 = rev 0 1 = rev 1 2 = rev 2
2	ANALOG_CTRL1	Reserved	0	PRW	01	Reserved
		osc_48MHz_sel	2:1	PRW	02	Oscillator 48 MHz center frequency select. 0 = Center freq = 34 MHz 1 = Center freq = 39 MHz 2 = Center freq = 44 MHz 3 = Center freq = 48 MHz
		Reserved	3	PRW	00	Reserved
		Reserved	4	PRW	01	Reserved
		Reserved	7:5	PRW	00	Reserved

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
3	ANALOG_CTRL2	led_out_dmib_ctrl	0	PRW	00	Select the source of LED out. 0 = Auto (by DMIB controller) 1 = Manual (by led_out_manual) - FOR LED TEST PURPOSES ONLY.
		led_out_manual	1	PRW	00	If led_out_dmib_ctrl is high, defines the state of led_out. 0 = LED driver disable (in manual mode) 1 = LED driver enable (in manual mode) (FOR LED TEST PURPOSES ONLY)
		dmib_dac_vref	3:2	PRW	01	Vref select for DMIB DAC 0 = 1v45 1 = 1v5 (default) 2 = 1v55 3 = 1v6 (recommended)
		led_dac_control	6:4	PRW	07	Adjust Led Drive DAC drive output current. 0 = Iout = 0 mA 1 = Iout = 2.0 mA 2 = Iout = 4.0 mA 3 = Iout = 6.0 mA 4 = Iout = 8.0 mA 5 = Iout = 10.0 mA 6 = Iout = 12.0 mA 7 = Iout = 14.0 mA (default)
		led_out_polarity	7	PRW	01	LED_OUT_EN polarity 0 = High when LED must be ON 1 = Low when LED must be ON

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
5	SYSTEM_CONFIG	automatic_power_mode	0	PRW	01	Power mode scheme 0 = Manual 1 = Automatic
		motion_pin_polarity	2	PRW	00	MOTION pin polarity (in non IDLE system state) 0 = MOTION pin LOW when motion detected 1 = MOTION pin HIGH when motion detected
		host_config_done	3	PRW	00	Bit needs to be set by host when configured after power up.
		use_standby_pin	4	PRW	01	STANDBY pin is used as chip select to enable I²C in AUTO power mode and STANDBY pin is used to wake up the OSC/DVREG (in sleep states in auto power mode). 0 = STANDBY pin not used 1 = STANDBY pin is used
		system_state	7:5	RW	01	Legacy register - please use system_state (0x91) instead.
6	GPIO_I2CSEL0	gpio_i2csel0_en	0	PRW	01	I2CSEL0 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_i2csel0_a	1	PRW	00	I2CSEL0 data output (when _en = 0)
		gpio_i2csel0_zi	2	PR	00	I2CSEL0 IO value
		gpio_i2csel0_pd	3	PRW	00	I2CSEL0 pull-down control (internal 35 kOhms pull-down resistor) - active LOW 0 = IO is pulled down 1 = IO not pulled down

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
7	GPIO_I2CSEL1	gpio_i2csel1_en	0	PRW	01	I2CSEL1 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_i2csel1_a	1	PRW	00	I2CSEL1 data output (when _en = 0)
		gpio_i2csel1_zi	2	PR	00	I2CSEL1 IO value
		gpio_i2csel1_pd	3	PRW	00	I2CSEL1 pull-down control (internal 35 kOhms pull-down resistor) - active LOW 0 = IO is pulled down 1 = IO not pulled down
8	GPIO_I2CSEL2	gpio_i2csel2_en	0	PRW	01	I2CSEL2 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_i2csel2_a	1	PRW	00	I2CSEL2 data output (when _en = 0)
		gpio_i2csel2_zi	2	PR	00	I2CSEL2 IO value
		gpio_i2csel2_pd	3	PRW	00	I2CSEL2 pull-down control (internal 35 kOhms pull-down resistor) - active LOW 0 = IO is pulled down 1 = IO not pulled down
9	GPIO_BACKLED0	gpio_backled0_en	0	PRW	00	BACKLED0 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_backled0_a	1	PRW	01	BACKLED0 data output (when _en = 0)
		gpio_backled0_zi	2	PR	01	BACKLED0 IO value
		gpio_backled0_tm	3	PRW	00	Reserved. Do not modify this bit.
		gpio_backled0_a_ctrl	4	PRW	00	BACKLED0 data output origin 0 = Output value from HW register 1 = Output value from PWM 0
		gpio_backled0_ opendrain	7	PRW	01	BACKLED0 pad open drain control 0 = BACKLED0 pad normal config 1 = BACKLED0 pad in open drain (A=EN)

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
a	GPIO_BACKLED1	gpio_backled1_en	0	PRW	00	BACKLED1 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_backled1_a	1	PRW	01	BACKLED1 data output (when _en = 0)
		gpio_backled1_zi	2	PR	01	BACKLED1 IO value
		gpio_backled1_tm	3	PRW	00	Reserved. Do not modify this bit.
		gpio_backled1_a_ctrl	4	PRW	00	BACKLED1 data output origin 0 = Output value from HW register 1 = Output value from PWM 1
		gpio_backled1_ opendrain	7	PRW	01	BACKLED1 pad open drain control 0 = BACKLED1 pad normal config 1 = BACKLED1 pad in open drain (A=EN)
b	GPIO_BACKLED2	gpio_backled2_en	0	PRW	00	BACKLED2 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_backled2_a	1	PRW	01	BACKLED2 data output (when _en = 0)
		gpio_backled2_zi	2	PR	01	BACKLED2 IO value
		gpio_backled2_tm	3	PRW	00	Reserved. Do not modify this bit.
		gpio_backled2_a_ctrl	4	PRW	00	BACKLED2 data output origin 0 = Output value from HW register 1 = Output value from PWM 2
		gpio_backled2_ opendrain	7	PRW	01	BACKLED2 pad open drain control 0 = BACKLED2 pad normal config 1 = BACKLED2 pad in open drain (A=EN)

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
c	GPIO_MOTION	gpio_motion_en	0	PRW	00	MOTION output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_motion_a	1	PRW	01	MOTION data output (when _en = 0)
		gpio_motion_zi	2	PR	01	MOTION IO value
		gpio_motion_pd	3	PRW	01	MOTION pull-down control (internal 35 kOhms pull-down resistor) - active LOW 0 = IO is pulled down 1 = IO not pulled down
		gpio_motion_a_ctrl	4	PRW	00	MOTION data output origin 0 = Output value from HW register 1 = Output value from motion detect IP
		Reserved	6:5	PRW	02	Reserved
		gpio_motion_ opendrain	7	PRW	00	MOTION pad open drain control 0 = MOTION pad normal config 1 = MOTION pad in open drain (A=EN)
d	GPIO_GPIO0	gpio_gpio0_en	0	PRW	00	GPIO0 output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_gpio0_a	1	PRW	00	GPIO0 data output (when _en = 0)
		gpio_gpio0_zi	2	PR	00	GPIO0 IO value
		gpio_gpio0_a_ctrl	4	PRW	00	GPIO0 data output select, either as LED_OUT_EN or from register bank. 0 = Output value from HW register 1 = LED_OUT_EN (polarity set in register 0x3 analog_ctrl2 bit 7)
		gpio_gpio0_ opendrain	7	PRW	00	GPIO0 pad open drain control 0 = GPIO0 pad normal config 1 = GPIO0 pad in open drain (A=EN)

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
e	GPIO_STANDBY	gpio_standby_en	0	PRW	01	STANDBY output enable (active low) 0 = PAD configured as OUTPUT 1 = PAD configured as INPUT
		gpio_standby_a	1	PRW	00	STANDBY data output (when _en = 0)
		gpio_standby_zi	2	PR	00	STANDBY IO value
f	PWM_PERIOD	pwm_period	7:0	PRW	ff	PWM period duration (20us tick period)
10	PWM_PULSEHIGH0	pwm_pulse_high0	7:0	PRW	00	PWM0 pulse high duration (20 us tick period) - 0 = disable
11	PWM_PULSEHIGH1	pwm_pulse_high1	7:0	PRW	00	PWM1 pulse high duration (20 us tick period) - 0 = disable
12	PWM_PULSEHIGH2	pwm_pulse_high2	7:0	PRW	00	PWM2 pulse high duration (20 us tick period) - 0 = disable
15	CLOCKS_LO	clk_motion_timer	1	PRW	00	Timer clock enabled (forced always on)
		clk_pci_en	4	PRW	00	PCI clock enable (forced always on)
		clk_framedump_en	5	PRW	00	Framedump clock enable (forced always on)
16	RESETS	software_reset_n	0	PRWC	01	Software reset result in full system reboot (active low - auto cleared)
		Reserved	4:1	PRW	0f	Do not modify these bits.
		framedump_reset_n	5	PRW	00	Framedump reset signal (active low)
		Reserved	7:6	PRW	00	Do not modify these bits.
19	CONTROL	motion_engine_start	7	PRW	00	Timer interrupt enable. This enables the Motion timer to operate. Motion timer generates pulses that trigger frame capture and motion processing.

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
1c	FRAME_RATE_ CONTROL	frame_rate_sel	2:0	PRW	02	Frame rate selection (value for internal osc running @48MHz) 0 = 0.5 kf/s (2 ms period) 1 = 1 kf/s (1 ms period) 2 = 2 kf/s (500 us period) 3 = 2.5 kf/s (400 us period) 4 = 2.9 kf/s (350 us period) 5 = 3.3 kf/s (300 us period) 6 = 3.6 kf/s (275 us period) 7 = 4 kf/s (250 us period)
		frame_rate_ctrl	4	RW	00	Frame rate management control 0 = Automatic (1k/2 k/Max f/s auto frame rate) 1 = Manual (set with frame_rate_sel reg)
		max_auto_frame_ rate	7:5	RW	05	Maximum frame rate to be applied in auto frame rate mode 0 = not allowed 1 = not allowed 2 = 2 kf/s (500 us period) 3 = 2.5 kf/s (400 us period) 4 = 2.9 kf/s (350 us period) 5 = 3.3 kf/s (300 us period) 6 = 3.6 kf/s (275 us period) 7 = 4 kf/s (250 us period)
21	X_MOTION	x_motion	7:0	PR	00	X motion data since last polling was done. Note that the internal accumulator is reduced from this value every time it is read.
22	Y_MOTION	y_motion	7:0	PR	00	Y motion data since last polling was done. Note that the internal accumulator is reduced from this value every time it is read.

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
23	OVERFLOW	x_overflow	0	PR	00	This register records if the X-motion integrator has reached its limit. 0 = No overflow 1 = Overflow
		y_overflow	1	PR	00	This register records if the Y-motion integrator has reached its limit. 0 = No overflow 1 = Overflow
		Reserved	2	PR	00	Reserved
		no_motion	3	PR	01	This bit is asserted as long as both X/Y integrators are empty (logical or between motion_w and motion_y). 0 = Motion 1 = No motion
		motion_acc_flush_en	5	PRWC	00	If set this bit flushes the motion accumulators (self cleared).
		adapt_cpi_en	6	RW	00	If set the CPI is function of the detected motion 0 = No adaptive CPI 1 = Enable adaptive CPI
		Reserved	7	PRW	00	Reserved
27	PARAMETERS_2	invert_x	0	PRW	00	Allows X to be inverted
		invert_y	1	PRW	00	Allows Y to be inverted
		Reserved	2	PRW	00	Reserved
		swap_xy	3	PRW	01	Replaces X with Y and Y with X.
		test_pattern_en	5	PRW	00	Test pattern enable 0 = normal vector from motion detector 1 = diamond shape vector test pattern
		test_pattern_speed	7:6	PRW	00	Test pattern enable 0 = |motion| = 127 maximum speed 1 = |motion| = 64 2 = |motion| = 32 3 = |motion| = 16

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
28	PARAMETERS_3	Reserved	3:0	PRW	04	Reserved
		Reserved	4	PRW	01	Reserved
		hpf_5x5_sel	5	PRW	00	Select between 3 x 3 and 5 x 5 high pass filter 0 = 3 x 3 high pass filter 1 = 5 x 5 high pass filter
		Reserved	6	PRW	01	Reserved
29	MIN_FEATURES	min_features	7:0	PRW	10	This register represents the minimum feature count below which motion is inhibited. Multiply by 16 to get the actual feature count threshold. Default is 16d = 256.
2a	X_SCALING	motion_x_scaling	7:0	PRW	10	Scaling for X motion vectors. Resolution is calculated as register value x 100 x M, where M is the lens magnification. So, for M = 0.5: 0x08 = 400 CPI that is 8 x 100 x 0.5 0x0c = 600 CPI that is 12 x 100 x 0.5
2b	Y_SCALING	motion_y_scaling	7:0	PRW	10	Scaling for Y motion vectors. Resolution is calculated as register value x 100 x M, where M is the lens magnification. So, for M = 0.5: 0x08 = 400 CPI that is 8 x 100 x 0.5 0x0c = 600 CPI that is 12 x 100 x 0.5
2c	FRAME_AVERAGE	frame_avg	7:0	PR	00	Frame average calculated over a 16 x 16 centered window. Possibly useful for production test.
2f	MAX_ABS_MOTION	max_abs_motion	6:0	PR	00	Max(ABS(X motion), ABS(Y motion)) either from integrated or instant motion.
31	FEATURES	features_report	7:0	PR	00	Feature count report, as the SUM of absolute differences between pixels and the field average. Bits [11:4] are represented here so x16 to calculate the actual feature count. Maximum value is 4080 = 255 x 16.

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
35	ADAPTCPI_MIN_ MOTION	adaptcpi_min_motion	7:0	PRW	10	Minimum value of max(|X frame motion|, |Y frame motion|) from which the CPI is adaptive (if feature enabled).
36	ADAPTCPI_MIN_ SCALING	adaptcpi_min_scaling	7:0	PRW	08	Minimum motion scaling value when adaptive CPI feature is enabled.
37	ADAPTCPI_RANGES	adaptcpi_log_ motion_range	2:0	PRW	05	Log value of motion range from which the CPI is adaptive (that is max motion = min + 2^adaptcpi_log_motion_range). 0 = motion range = 1 1 = motion range = 2 2 = motion range = 4 3 = motion range = 8 4 = motion range = 16 5 = motion range = 32 6 = motion range = 64 7 = motion range = 128
		adaptcpi_log_ scaling_range	6:4	PRW	04	Log value of motion scaling range from which the CPI is adaptive (that is max scaling = min + 2^adaptcpi_log_scaling_range). 0 = scaling range = 1 1 = scaling range = 2 2 = scaling range = 4 3 = scaling range = 8 4 = scaling range = 16 5 = scaling range = 32 6 = scaling range = 64 7 = scaling range = 128
		Reserved	7	PR	01	Reserved

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
43	EXPOSURE_ CONTROL	autoexpo_en	0	RW	01	Auto exposure control 0 = Disable 1 = Enable
		autoexpo_status	6:4	R	00	Auto exposure status 0 = UNDEF (no AEC performed yet) 1 = LOW (exposure increasing) 2 = STABLE (max exp pix within range) 3 = HIGH (exposure decreasing) 4 = SATURATED (exposure saturation decreasing)
		autoexpo_limit_flag	7	R	00	Exposure limit reached flag 0 = Exposure time within range 1 = Exposure time limit reached
44	MAX_EXPO_PIX	max_exposed_pixel_ value	7:0	PR	00	Second maximum pixel value of the current frame (before CDS)
45	MAX_EXPO_PIX_ THRESH_HIGH	max_exposed_pixel_ thresh_high	7:0	RW	f0	High threshold value of max exposed pixel where the AEC is stable.
46	MAX_EXPO_PIX_ THRESH_LOW	max_exposed_pixel_ thresh_low	7:0	RW	b4	Low threshold value of max exposed pixel where the AEC is stable.
47	EXPOTIME	exposure_time	7:0	PRW	40	Exposure time value in 3MHz clk period step (333ns)
49	EXPOTIME_MAX	exposure_time_max	7:0	RW	ff	Maximum exposure time applied by the AEC.
4a	EXPOTIME_MIN	exposure_time_min	7:0	RW	01	Minimum exposure time applied by the AEC.
4b	EXPO_FRAME_ UPDATE	autoexpo_frame_ update	7:0	RW	01	Exposure update frequency (every N + 1 frames). Default is every two frames.
4e	EXPOTIME_INC_ STEP	expo_inc_step	7:0	RW	04	Exposure increment step (used when below max_expo_pix_thresh_low)
4f	EXPOTIME_DEC_ STEP	expo_dec_step	7:0	RW	04	Exposure decrement step (used when above max_expo_pix_thresh_high)
50	EXPOTIME_SAT_ DEC_STEP	expo_sat_dec_step	7:0	RW	10	Exposure decrement step (used when above max_expo_pix is saturated = 255)

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
51	CONTROL	dmib_ctrl_mode	0	RW	00	DMIB controller timing switch mode 0 = Manual (chosen by dmib_timing reg) 1 = Automatic (system auto sets the dmib_timing mode, status reported in dmib_timing reg)
		dmib_timing	1	PRW	00	DMIB controller timing mode 0 = Normal DMIB timing (same as 376 with double expo time possible) 1 = Sunlight DMIB timing
		Reserved	7	PRW	00	Reserved
56	CDSOUT_SEL	cds_out_sel	1:0	PRW	00	Selects what is output from the DMIB controller (going to motion engine and or video output data). 0 = CDS frame 2 = exposed frame 3 = black frame
		Reserved	4	PRW	00	Reserved
58	FRAMEDUMP_ PIXDATA	framedump_pixdata	7:0	PR	00	Pixel data in frame dump mode, automatically incremented to next pixel after a read of this register.
59	FRAMEDUMP_CTRL	framedump_en	0	PRW	00	Frame dump mode enable 0 = Disable 1 = Enable
		framedump_start	1	PR	00	Frame dump started
		framedump_ready	2	PR	00	Flag set when a frame is ready to be read by host, Pixel[0] is ready in register FRAMEDUMP_PIXDATA.
		framedump_done	3	PR	00	Flag set when a complete frame (400 pixels) has been read.
		pci_test_enable	4	PRW	00	Muxed PCI data onto pads (2 bits nibble + FST + Qclk) 0 = Disable 1 = Enable
		framedump_mire	7	PRW	00	In frame dump mode outputs a grey scale image (pixel_counter).

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
7c	DEVADDR	i2cs_index_auto_inc_en	0	PRW	01	Auto Increment function
		i2cs_dev_addr	7:1	PRW	53	I²C device address
80	FW_TOP_REVISION	ucFwTopRevision	7:0	RW	20	System level firmware revision
81	PERSONAL_ CONFIG	ucPersonalConfig	7:0	RW	00	Result of the I2C_SEL[20] pad decoding done at start-up. 0 = I2C device address = 0xA6 + config 0 1 = I2C device address = 0xA6 (reserved) 2 = I2C device address = 0xC6 + config 2 3 = I2C device address = 0xD6 + config 3 4 = I2C device address = 0xE6 + config 4 5 = I2C device address = 0x36 + config 5 6 = I2C device address = 0x46 + config 6 7 = I2C device address = 0x20 + config 7
82	POWER_MODE_ CONTROL	reserved	1:0		00	Do not modify these bits.
		ucNbSleepState	5:4	RW	03	In AUTOMATIC power mode, number of sleep states.

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
83	BACKLIGHT_ CONTROL	bBackLightEnable	0	RW	00	BACKLED PWM enable 0 = Disable 1 = Enable
		bSingleBackled	1	RW	00	Single BACKLED scheme control par PWM0 only 0 = three independent BackLEDs 1 = BackLED controlled by PWM 0
		bPwmPolarity	2	RW	00	BACKLED PWM signal polarity 0 = High when LED must be ON (= pwm0) 1 = Low when LED must be ON (= !pwm0)
		bBackledGaterEnable	3	RW	00	Enable the gating of BACKLED PWM signal with DMIB gater signal. 0 = Disable 1 = Enable
		bPwmHoldEnable	4	RW	00	Enable the hold mechanism when DMIB gater signal is ON. 0 = Disable 1 = Enable
		bBackLightReset	7	RWC	00	In SW STBY reset the control of Backlight control (self cleared). 0 = Disable 1 = Enable
84	AUTO_RUNNING_ TIMEOUT_HI	uwRunningTimeout	15:0	RW	00	In RUNNING state, time to enter SLEEP1 state when no motion is detected. Expressed in number of frames, for example, in automatic frame rate = step of 1 ms (1 kf/s), for fixed frame rate depending on the chosen frame rate.
85	AUTO_RUNNING_ TIMEOUT_LO				32	
86	AUTO_SLEEP1_ TIMEOUT_HI	uwSleep1Timeout	15:0	RW	03	In SLEEP1 state, time to enter SLEEP2 state when no motion is detected. Expressed in number of frames, for example, step of SLEEP1 latency.
87	AUTO_SLEEP1_ TIMEOUT_LO				20	
88	AUTO_SLEEP2_ TIMEOUT_HI	uwSleep2Timeout	15:0	RW	17	In SLEEP2 state, time to enter SLEEP3 state when no motion is detected. Expressed in number of frames, for example, step of SLEEP2 latency.
89	AUTO_SLEEP2_ TIMEOUT_LO				70	

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
8a	AUTO_SLEEP1_ LATENCY	ucSleep1Latency	7:0	RW	05	Maximum latency to wake up the system in SLEEP1 state. Corresponds to the time between two wake-up periods (a wake-up period corresponds to a single frame motion detection processing). 0 = 400 us 1 = 1 ms 2 = 1.4 ms 3 = 2 ms 4 = 4 ms 5 = 10 ms 6 = 20 ms 7 = 50 ms 8 = 100 ms 9 = 150 ms 10 = 200 ms 11 = 500 ms 12 = 1 s 13 = 1.5 s 14 = 2 s 15 = 2.6 s
8b	AUTO_SLEEP2_ LATENCY	ucSleep2Latency	7:0	RW	08	Maximum latency to wake up the system in SLEEP2 state. Corresponds to the time between two wake-up periods (a wake-up period corresponds to a single frame motion detection processing). 0 = 400 us 1 = 1 ms 2 = 1.4 ms 3 = 2 ms 4 = 4 ms 5 = 10 ms 6 = 20 ms 7 = 50 ms 8 = 100 ms 9 = 150 ms 10 = 200 ms 11 = 500 ms 12 = 1 s 13 = 1.5 s 14 = 2 s 15 = 2.6 s

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
8c	AUTO_SLEEP3_ LATENCY	ucSleep3Latency	7:0	RW	0b	Maximum latency to wake up the system in SLEEP3 state. Corresponds to the time between two wake-up periods (a wake-up period corresponds to a single frame motion detection processing). 0 = 400 us 1 = 1 ms 2 = 1.4 ms 3 = 2 ms 4 = 4 ms 5 = 10 ms 6 = 20 ms 7 = 50 ms 8 = 100 ms 9 = 150 ms 10 = 200 ms 11 = 500 ms 12 = 1 s 13 = 1.5 s 14 = 2 s 15 = 2.6 s
8d	AUTO_MOVEMENT_ CTRL1	bAutoMoveFilterEnab le	0	RW	00	Auto movement filter enable 0 = Disable 1 = Enable
		ucAutoMoveFilterFra meNb	6:1	RW	07	Number of frames on which the auto movement filter is applied (must be greater than 1).
		bAutoMoveSaturated Expo	7	RW	00	When image in high light and exposure (reg 0x47) is set to 1, flag used by engine to discard motion in this condition. 0 = Disable 1 = Enable

Table 38. I²C register map (continued)

Addr (Hex)	Register name	SIgnal name	Bit	Type	Default (Hex)	Comment
8e	AUTO_MOVEMENT_CTRL2	ucAutoMoveFilterLatency	3:0	RW	01	Latency between frames on which the auto movement filter is applied. 0 = 400 us 1 = 1 ms 2 = 1.4 ms 3 = 2 ms 4 = 4 ms 5 = 10 ms 6 = 20 ms 7 = 50 ms 8 = 100 ms 9 = 150 ms 10 = 200 ms 11 = 500 ms 12 = 1 s 13 = 1.5 s 14 = 2 s 15 = 2.6 s
		ucAutoMoveFilterLoop	7:4	RW	03	Set the number of sequences to detect motion to grant motion in sleep mode.
90	DEVICE_ID	ucDeviceID	7:0	RW	4d	Device ID 0 = VD5376 (and previous) 77 = VD5377
91	SYSTEM_STATE	ucSystemState	2:0	RW	01	S377 system state 0 = Boot 1 = Software Standby 2 = AutoRunning 3 = Sleep_1 4 = Sleep_2 5 = Sleep_3 6 = ManualRunning

13 Acronyms and abbreviations

Table 39. Acronyms and abbreviations

Acronym/abbreviation	Definition
ABS	Absolute (value)
ACC	Accumulator
ACK	Acknowledge
AEC	Automatic exposure control
AMF	Auto-movement filter
OFN	Optical finger navigation
CDS	Correlated double sampling
CPI	Counts per inch
CPU	Central processing unit
DAC	Digital-to-analog converter
DMIB	Digital mouse imaging block
DPI	Dots per inch
DSL	Direct sunlight
f/s	Frames per second
GPIO	General purpose input/output
IC	Integrated circuit
I^2C	Inter integrated circuit
LED	Light emitting diode
M	Magnification
MCU	Micro controller unit
MEP	Maximum exposed pixel
MSB	Most significant bit
NACK	Negative acknowledge
OSC	Oscillator
POR	Power-on reset
PWM	Pulse width modulation
RI	Relative illumination
ROM	Read only memory
SAD	Sum of absolute differences
SCL	I^2C serial clock
SDA	I^2C serial data

14 Ordering information

VD5377 silicon is currently available in the formats listed in *Table 40*. More detailed information is available on request.

Table 40. Delivery formats

Order code	Description	Thickness
VD5377/UW	Unsawn wafer	725 µm
VD5377CB/UW	Unsawn wafer	180 µm
VD5377CB/SW	Sawn wafer	180 µm
VD5377CB/GP	Gel pack (evaluation samples only, maximum quantity 500)	180 µm

15 Revision history

Table 41. Document revision history

Date	Revision	Changes
23-Mar-2012	1	Initial release
07-Feb-2013	2	Minor updates throughout.

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