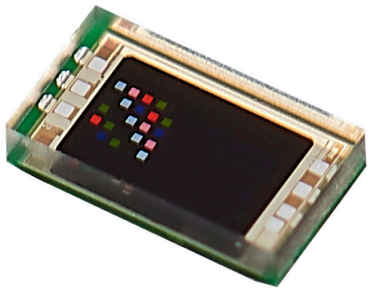
VD6283TX

Datasheet

Hybrid filter multispectral sensor with light flicker engine



Order code	Product version
VD6283TX45/1	Red, green, blue, visible, IR, and clear

Features

- Miniature optical module
  - 1.83 x 1.0 x 0.55 mm
  - Optical BGA, 6-balls, reflowable package
  - Operates with phone cover glass on top
- ALS operation with 6 independent channels
  - Advanced hybrid filters with high photo count response
  - Parallel sensing of all channels: red, green, blue, IR, clear, and visible
  - High dynamic range from 7 mLux to 30 klx (green channel)
  - High sensitivity and low noise in low light conditions
- Light flicker extraction
  - Innovative readout architecture to extract AC light flicker signal
  - From 100 Hz to 2 kHz frequency detection, sine or square wave
  - Several extraction modes are available (analog or digital)
- Software driver provided by STMicroelectronics
- I²C interface up to 1 Mbit/s (fast mode plus)
- Perfectly suited for mobile applications
  - 1.8 V power supply
  - Low-power consumption
  - Operating temperature -30 to 85°C

Applications

- True tone color-sensing IC for smartphone and smartwatch screen adjustments, camera white balance color assistance
- Lux and CCT measurement
- Light frequency extraction for flicker correction assistance

Description

The VD6283TX (1.83 x 1.0 x 0.55 mm) is the third version of ST's ambient light sensors with advanced light flicker extraction. Light measurement is fast and accurate thanks to an individual ADC and a readout for each color channel. The VD6283TX uses hybrid color filters with precise responses which enhance the accuracy of the correlated color temperature (CCT) and Lux performance. The VD6283TX can be used to assist camera white-balance in less than 30 ms.

With a patented architecture and a high-performance photodiode design, the VD6283TX can extract light flickering frequencies to enhance camera experience, and avoid “banding effects” on videos or viewfinder modes. Additionally, the VD6283TX is the only sensor able to extract different light flicker waveforms, including LED square signals that can run flicker operations simultaneously with ALS operations.

1 Product overview

Table 1. Technical specifications

Parameter	Value
Package type	Optical module with thin glass – 6 ball BGA
Product size	1.83 x 1.0 x 0.55 mm
Operating voltage	1.8 V typical (1.65 V to 1.95 V)
Operating temperature	-30 to 85 °C
6 ALS channels	Red, visible, blue, green, IR, and clear
1 flicker channel	Flicker channel using any single channel from above (user selectable)
I²C	1 MHz fast mode plus compatible, default address = 0x40h (write)

Figure 1. System block diagram (full options)

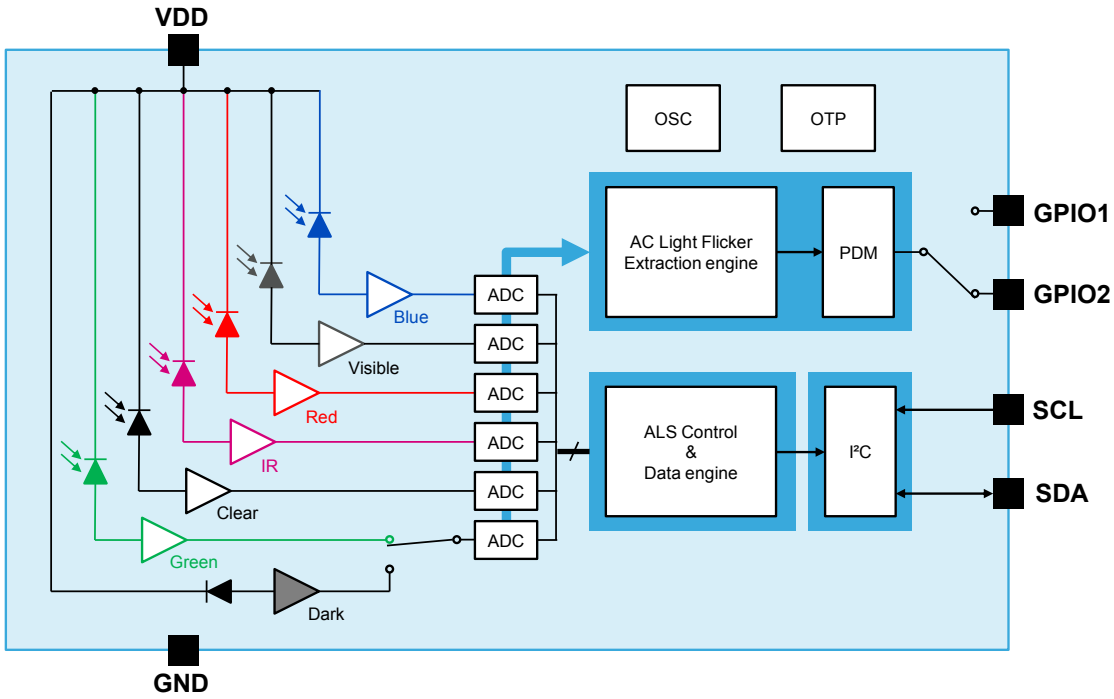


Table 2. VD6283TX45/1 channel affectation

Channel number	Filter color
Channel 1	Red
Channel 2	Visible
Channel 3	Blue
Channel 4	Green
Channel 5	IR
Channel 6	Clear

Table 3. Key functional parameters

Parameter	Value
I²C	Fast mode (400 kHz) and fast mode plus (1 MHz) Programmable I²C address (see Section 3.4.2: I²C new device address)
Channels	6 color channels with independent, parallel reading for ALS or flicker operations: red, visible, blue, green, IR, and clear. 1 dedicated fast channel for light flicker measurement 1 internal dark channel
ADC type	24 bit (16 bit + 8 bit, for high accuracy under low light)
Exposure time (EXTIME)	Integration time step size: 1.6 ms typical Number of integration steps: 1 to 1024 (1.6 ms to 1.6 s)
Readout time	ALS readout: 6 ms typical (fixed) for all channels together. This must be added to EXTIME for overall sensing operations. For example, EXTIME 24 ms and readout 6 ms -> 30 ms overall operation (33 Hz). AC flicker frequency: raw signal (PDM) is output continuously through GPIO1 or GPIO2.
Analog gain	15 programmable gains for high-dynamic range: 66x, 50x, 33x, 25x, 16x, 10x, 7.1x, 5x, 3.33x, 2.5x, 1.67x, 1.25x, 1x, 0.83x, 0.71x. Independent and selectable per channel
Intermeasurement period	256 steps of 20 ms (from 0 ms to 5.12 s)
Light flicker detection	Minimum frequency detection: 100 Hz
	Maximum frequency detection: 2 kHz
	Output modes: Mode 1 = digital PDM (pulse density modulation): in this mode, the host must input a master clock into GPIO2 to synchronize the data stream (Figure 4. Application schematic, ALS, and flicker in digital PDM format (mode 1)). Mode 2 = analog format: in this mode, the PDM signal is routed out of GPIO2 and filtered by an external RC filter to get a continuous analog signal (Figure 5. Application schematic, ALS, and flicker in analog format (mode 2)).
	FFT (Fast Fourier Transform) computation is required at host level for highest frequency detection accuracy. This is recommended for better screening of the light fundamental and harmonic extraction, especially with respect to multitone frequencies (combined light sources).

2 Ballout and application information

The figure below shows the ballout of the VD6283TX (top view with balls down and silicon/glass up).
The table below provides the ball description and voltages.

Figure 2. Ballout (top view)

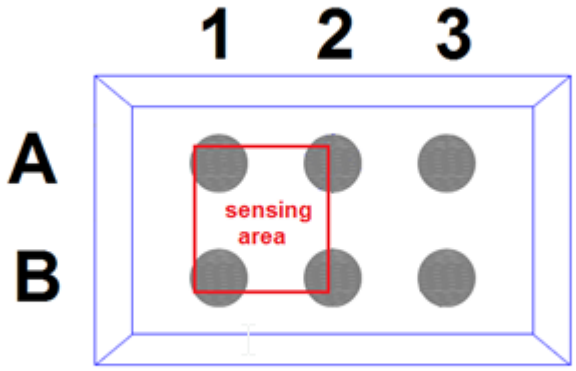


Table 4. Ball description

Ball number	Signal name	Signal type	Typ. voltage	Description
A1	VDD	Supply	VDD	Supply, to be connected to the main supply
A2	SDA	Digital input/output		I²C serial data
A3	VSS	Ground	GND	To be connected to the main ground
B1	GPIO2	Digital input/output	VDD	Pulse-density modulation (PDM) input clock or AC flicker signal output (PDM data)
B2	GPIO1	Digital input/output		Interrupt output or AC flicker signal output (PDM data)
B3	SCL	Digital input		I²C serial clock

Figure 3. **Application schematic, ALS operation only with interrupt handshake**

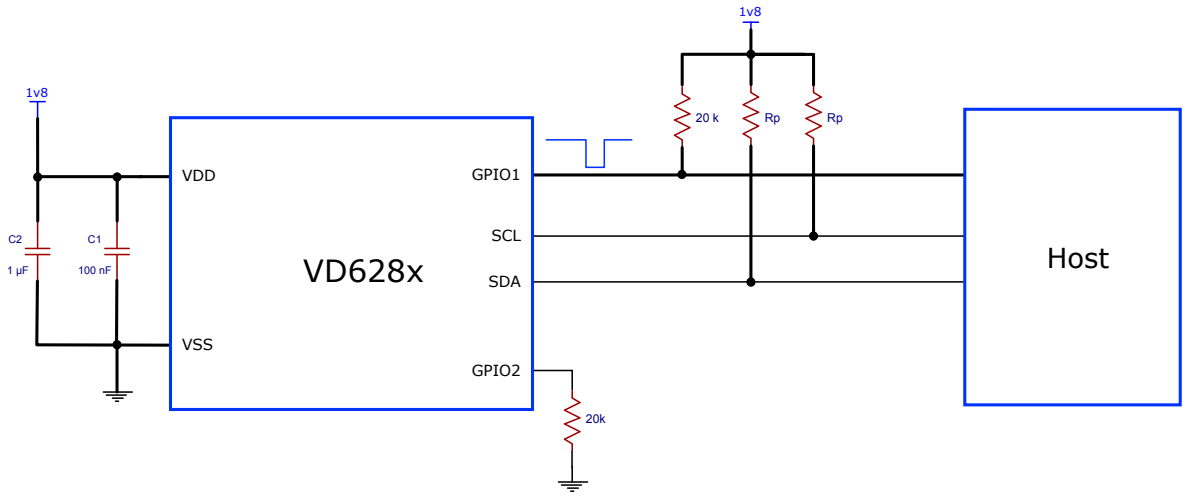


Figure 4. **Application schematic, ALS, and flicker in digital PDM format (mode 1)**

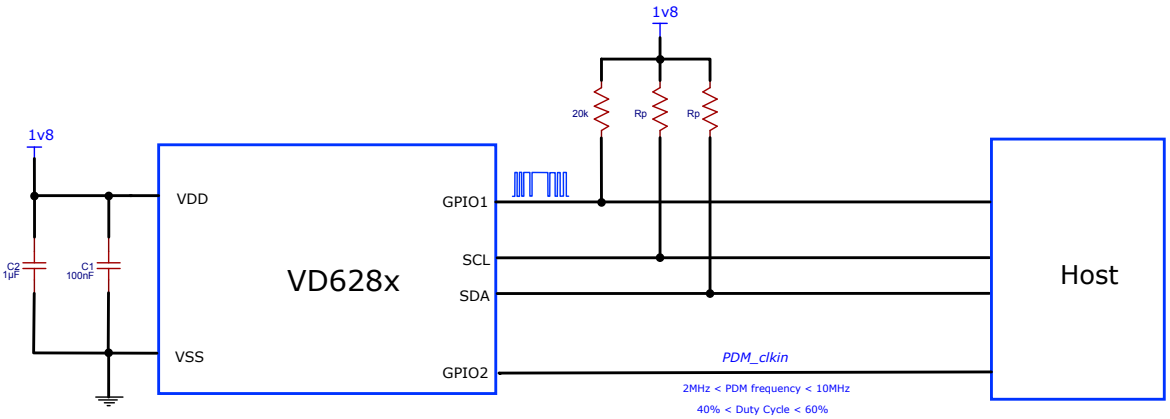


Figure 5. **Application schematic, ALS, and flicker in analog format (mode 2)**

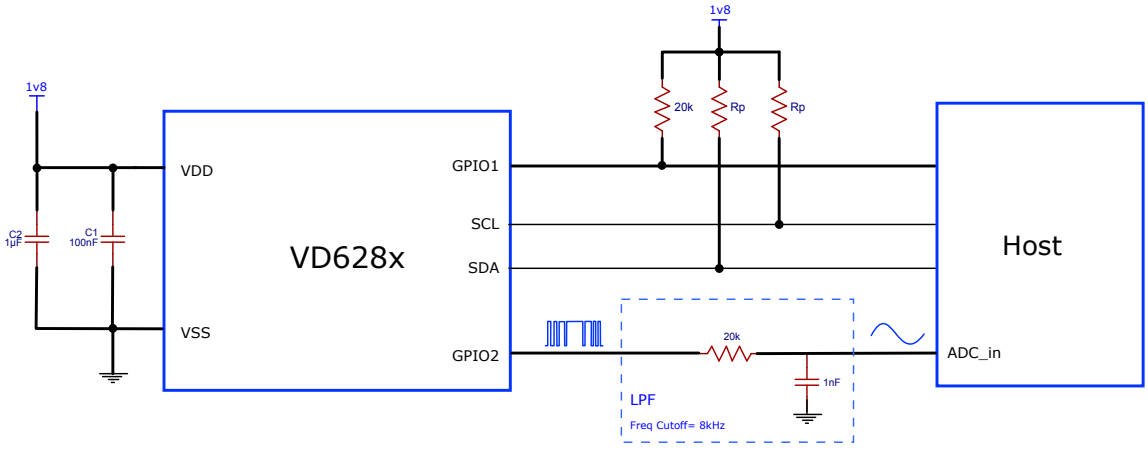


Table 5. Recommended pull up resistors and SDA driver settings for I²C modes

I²C mode	I²C bus capacitive load range (pF)	Pull up resistor Rp (Ω)	SDA driver configuration (mA)
Standard and fast mode	10 - 115	1.65 k	SDA_DRV_CFG = '000' (4 mA) or SDA_DRV_CFG = '001' (8 mA) or SDA_DRV_CFG = '010' (12 mA) or SDA_DRV_CFG = '011' (16 mA)
	115 - 225	909	
	225 - 400	562	
Fast mode plus	13 - 35	1.62 k	SDA_DRV_CFG = '100' (20 mA)
	35 - 95	750	
	95 - 150	453	
	150 - 550	154	

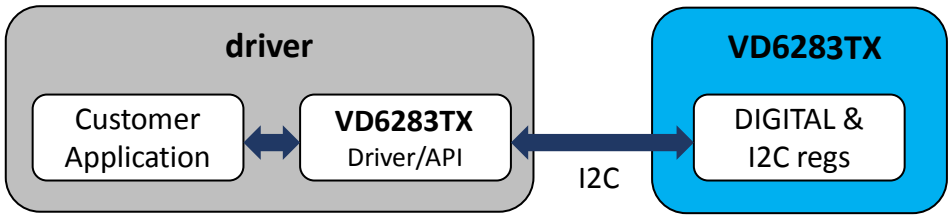
3 System description

3.1 Functional description

The figure below shows the system level functional description. The host customer application controls the VD6283TX device using a software (SW) driver API (application programming interface).

This software driver provides a set of high-level functions that allow the user to control the VD6283TX without worrying about I²C register control. Such control includes: start/stop ALS sensing, color channel selection, activate AC flicker sensing and/or ALS sensing, set the exposure time or set the analog gain. This helps customer evaluation, software development, and prototype building.

Figure 6. System functional description



3.2 Sensing operation

The color channels can be individually enabled to optimize power consumption through the I²C (or software API):

- Up to 6 ALS channels can be read in parallel (ALS mode): red, visible, blue, green, IR, and clear channels can be enabled individually.
- Up to 5 ALS channels can be read in parallel, together with 1 flicker channel (ALS and flicker mode). The RGB - IR-visible channels can be sensed in ALS mode while AC flicker mode is configured with the clear channel. Note that in this configuration, the selected channel routed to the AC light flicker module (that is, clear) cannot provide an ALS value at the same time.

Exposure time (EXTIME) is defined by the user and is identical for all channels in ALS operation. EXTIME can be set from 1.6 ms up to 1.6 s. After each EXTIME duration, a fixed period of time of ~6 ms takes place to allow counts to be converted into digital information. This housekeeping time must be considered in the overall ALS speed framerate.

Individual analog gain (AGAIN) can be applied by the user for each channel, including the channel routed to the AC light flicker module.

3.3 Operating modes

The VD6283TX can stream the following data continuously: ALS color data over the I²C and raw flicker data over the GPIO1 or GPIO2 ball. Streaming starts when the host microcontroller sends a “start/stop” command. Then, the N-1 data measurements are automatically overwritten in the I²C registers with the latest N measurement batch.

The user can set an intermeasurement period through the software driver. This goes from 0 to 5.1 seconds, in steps of 20 ms (256 steps). This can be useful to reduce sensing frame rate and power consumption, without having the master microcontroller host awake during the intermeasurement period.

ALS and flicker sensing are totally independent and can be activated/stopped individually.

The VD6283TX can also work in a "continuous gated” way. Once measurement N is finished, the VD6283TX waits for the microcontroller handshake to carry on to measurement N+1. I²C data are not refreshed until the next acknowledgment, whilst the PDM data are still streaming over the GPIO1 or GPIO2 ball. The handshake mechanism is performed via I²C polling.

3.3.1 Raw and calibration data

The VD6283TX features an OTP memory bank to store calibration data. ST performs a light calibration of each individual channel in production. A calibration factor per channel is then stored in the VD6283TX OTP memory. The user can retrieve both raw data and calibration data through the software driver.

3.3.2 Power up/Power down sequence

Following power up (t_{PU} = 0.03 ms) of the VD6283TX, some internal registers must be initialized before any mode (for example, ALS or Flicker) can operate. To ensure proper initialization of the sensor, one dedicated API function (STALS_Init) is available in the VD6283TX software driver and should be called right after power up.

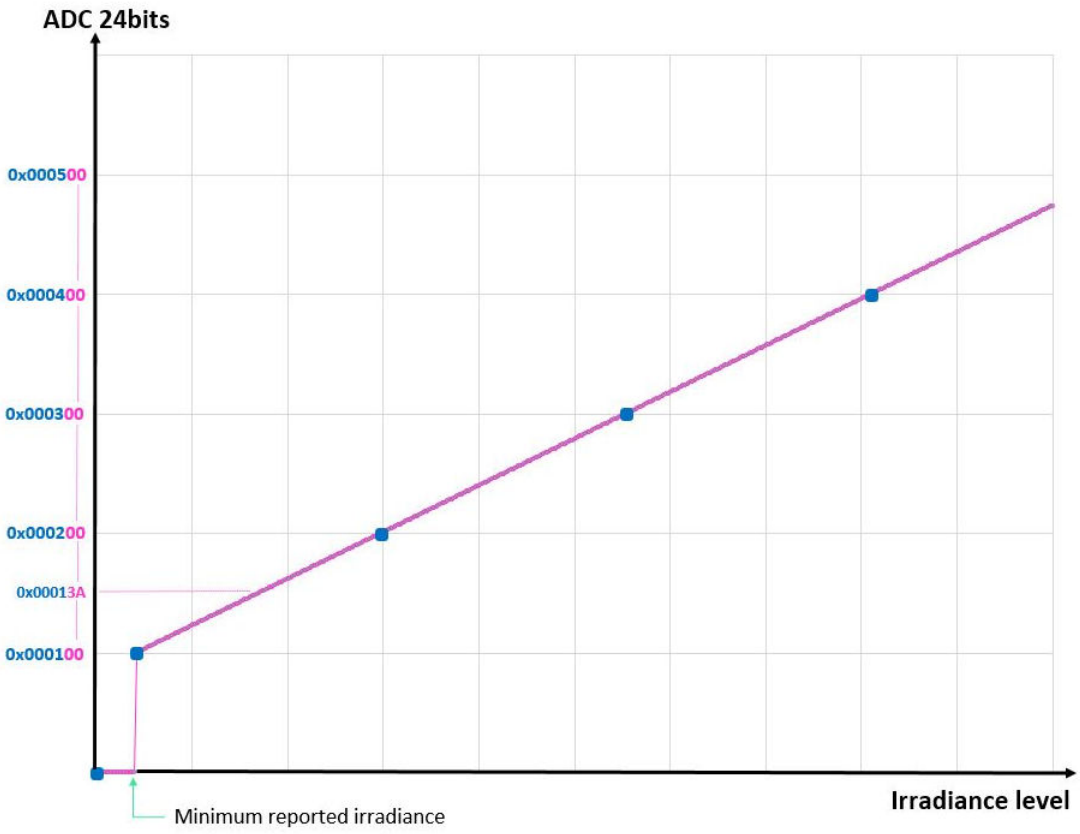
Before power down of the VD6283TX, one dedicated API function (STALS_Term) must be called.

Note that the API function STALS_Term should be called only before power down of the actual sensor.

3.3.3 24-bit/16-bit ADC readout

The VD6283TX features a 24-bit ADC, which converts light information into digital format (counts). Each channel count data is proportional to channel irradiance. Note that the minimum reported irradiance level (guaranteed by design) is 0x000100.

Figure 7. 24-bit ADC readout vs. light level



At low light levels, the ADC data low byte (ALS_CHx_DATA_L) is useful for improving sensing resolution. During nominal light conditions, the ALS_CHx_DATA_L byte can be discarded and the application can read the 16 most significant bits of the ADC (ALS_CHx_DATA_H and ALS_CHx_DATA_M) using the software driver (16-bit ADC format).

3.3.4 Saturation

If an excessive light level is sensed by the VD6283TX, a saturation condition may occur. Digital saturation defines the maximum channel count value software can read. This value is dependent on the exposure time programmed before the ALS operation started.

- If EXTIME is ≤ 113 ms, the saturation level is 910 counts/step
- If EXTIME is > 113 ms, the saturation level is 65535 counts

Note: Values based on a 16-bit ADC format

Note: Step = 1.6 ms (see Table 16. ALS operating characteristics)

Note: To ensure correct functioning of user applications, it is recommended that the application software first checks that the VD6283TX channels are not saturated. This should be done before the calibration data are used further (for example, for setting the AWB and CCT). In addition, it should be performed on VD6283TX raw data.

3.3.5 AC light flicker extraction

The VD6283TX features a digital module that extracts AC light signals (i.e. flicker) based on analog readouts over time. The AC signal produced is then coded in PDM format. The clock selected for this modulation can be either the internal clock or an external clock fed over GPIO2.

This PDM signal can be output either on the GPIO1 or GPIO2 pins. This digital signal can be filtered externally to produce a baseband analog signal of the AC flicker (mode 2).

If an external clock is applied, the PDM output is available on GPIO1 only (mode 1). It is recommended to execute the AC flicker operation on a clear channel for better performance.

3.3.6 Flicker mapping configuration

Two configurations are available to output the PDM signal as described below

Table 6. Flicker mapping configurations

Configuration	GPIO1	GPIO2	PDM clock	External hardware	Host I/F
Mode 1	PDM	PDM_CLKin	External	None	SPI, PDM
Mode 2	Interrupt	PDM	Internal	RC filter	ADC

Mode 1 connects the VD6283TX flicker signal to an external synchronous serial interface (i.e SPI, PDM). The host sends a master clock signal for synchronization into GPIO2 and retrieves a PDM signal out of GPIO1 (Figure 4. Application schematic, ALS, and flicker in digital PDM format (mode 1)).

Mode 2 connects the VD6283TX flicker signal to an ADC module (host or other). External RC filtering is required before connecting the ADC input (Figure 5. Application schematic, ALS, and flicker in analog format (mode 2)).

3.4 I²C interface

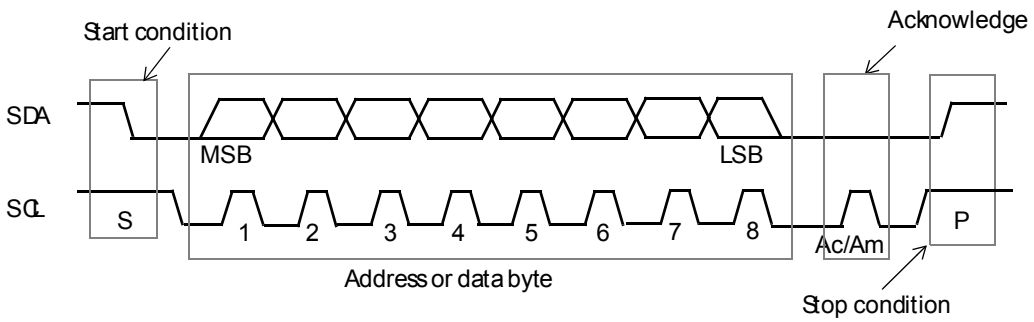
3.4.1 I²C protocol description

Device control and data transfer are performed through an I²C serial communication interface. The I²C interface uses two signals: the serial data line (SDA) and serial clock line (SCL). Each device connected to the bus uses a unique address and a simple master/slave relationship exists.

Both SDA and SCL lines are connected to a positive supply voltage using pull-up resistors located on the host. Lines are only active when driven low. When no data is transmitted both lines are high.

Clock signal (SCL) generation is performed by the master device. The master device initiates data transfer. The I²C bus on the VD6283TX has a maximum speed of 1 Mbit/s and the device supports a slave address of 0x40 (or 0x20 in 7 bits).

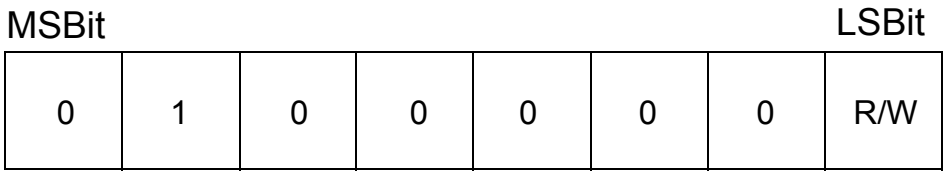
Figure 8. Data transfer protocol



Information is exchanged in 8-bit packets (bytes) always followed by an acknowledge bit, Ac for VD6283TX acknowledge and Am for master acknowledge (host bus master). The internal data are produced by sampling SDA at a rising edge of SCL. The external data must be stable during the high period of SCL. The exceptions to this are start (S) or stop (P) conditions when SDA falls or rises respectively, while SCL is high.

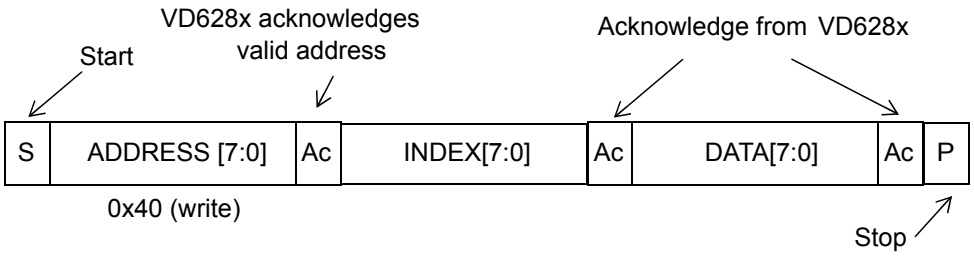
An I²C message contains a series of bytes preceded by a start condition and followed by either a stop or repeated start (another start condition but without a preceding stop condition) followed by another message. The first byte contains the device address and also specifies the data direction. If the least significant bit is low (that is, 0x40) the message is a master write command to the slave. If the LSB is set (that is, 0x41) then the message is a master read command from the slave.

Figure 9. I²C device address



All serial interface communications with the ambient light sensor must begin with a start condition. The sensor acknowledges reception of a valid address by driving the SDA line low. The state of the read/write bit (LSB of the address byte) is stored and the next byte of data, sampled from SDA, can be interpreted. During a write sequence, the second byte received provides an 8-bit index, which points to one of the internal 8-bit registers.

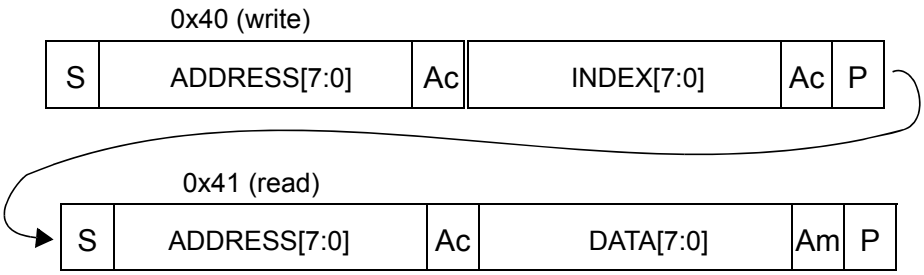
Figure 10. **Data format (write)**



As data are received by the slave, they are written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data are then stored in the internal register addressed by the current index.

During a read message, the contents of the register addressed by the current index are read out in the byte following the device address byte. The contents of this register are parallel loaded into the serial/parallel register and clocked out of the device by the falling edge of SCL.

Figure 11. **Data format (read)**



At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device (that is, the VD6283TX for a write and the host for a read).

A message can only be terminated by the bus master, either by issuing a stop condition or by a negative acknowledge (that is, not pulling the SDA line low) after reading a complete byte during a read operation.

The interface also supports auto-increment indexing. After the first data byte has been transferred, the index is automatically incremented by 1. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a stop condition. If the auto-increment feature is employed, the master does not have to send address indexes between each data byte.

Figure 12. **Data format (sequential write)**

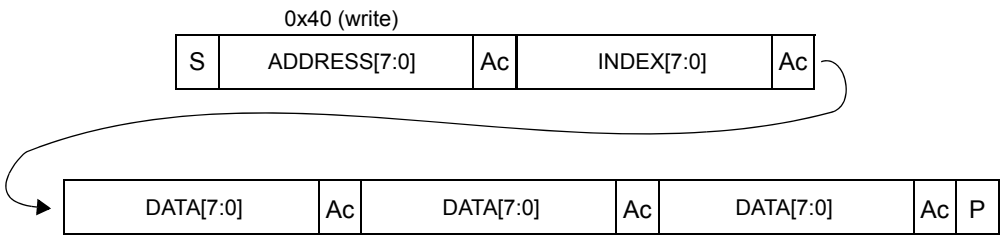
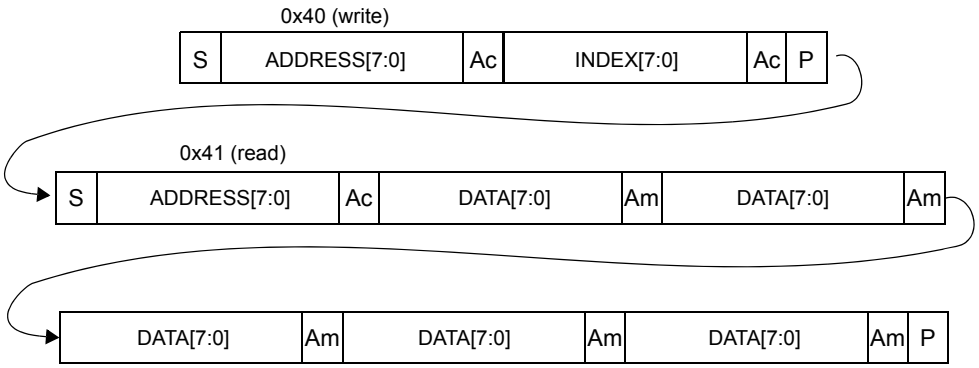


Figure 13. **Data format (sequential read)**



3.4.2 I²C new device address

The VD6283TX provides a feature to assign a new I²C device address, which should be used by the system implementer. The dedicated procedure below needs to be followed to reprogram the device address.

1. The device should be in the OFF state (that is, powered off) for more than 1 ms.
2. The host drives the GPIO1 signal to low state (that is, GND level).
3. Then, the system powers up the VD6283TX.
4. After power-up time has elapsed (tpu = 0.03 ms), the host can send a valid I²C command with the desired new device address.
5. Finally, wait until the host can release the GPIO1 signal (that is, the host output should be set in high impedance).

The VD6283TX I²C address is now changed and should be used as a reference address to communicate with the VD6283TX.

Note: Once the VD6283TX address is changed, any incoming I²C transactions with the default address (0x40) are ignored by the VD6283TX.

Note: If the host attempts to change the VD6283TX I²C address after the first I²C transaction is received, the device ignores such a request.

Note: The new I²C device address procedure should be repeated at each VD6283TX power-up.

Note: During the VD6283TX power-up phase, it is recommended to suspend any I²C transactions to avoid unwanted I²C device address assignment.

Note: The external pull-up resistor on GPIO1 is required to avoid unintended I²C device address assignment. Please refer to the recommended application schematics.

3.4.3 I²C interface timing characteristics

Timing characteristics are shown in the tables below. Refer to the figure below for parameters details.

Table 7. I²C interface - timing characteristics for fast mode plus (1 MHz)

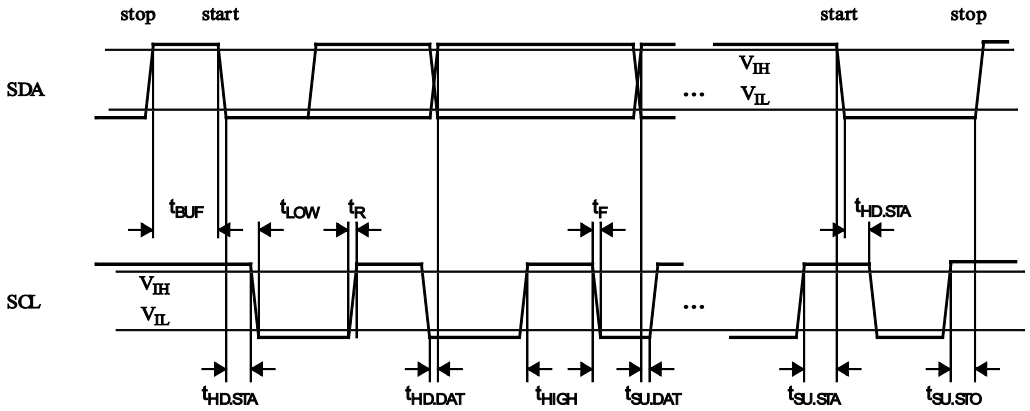
Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I^2C}	Operating frequency	0	—	1000	kHz
t_{LOW}	Clock pulse width low	0.5	—	—	µs
t_{HIGH}	Clock pulse width high	0.26	—	—	
t_{SP}	Pulse width of spikes, which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	0.5	—	—	µs
$t_{HD.STA}$	Start hold time	0.26	—	—	
$t_{SU.STA}$	Start set-up time	0.26	—	—	
$t_{HD.DAT}$	Data in hold time	0	—	0.9	
$t_{SU.DAT}$	Data in set-up time	50	—	—	ns
t_R	SCL/SDA rise time	—	—	120	
t_F	SCL/SDA fall time	—	—	120	
$t_{SU.STO}$	Stop set-up time	0.26	—	—	µs
$t_{VD.DAT}$	Data valid time	—	—	0.4	
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	
C_L	Load capacitance	—	140	550	

Table 8. I²C interface - timing characteristics for fast mode (400 kHz)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
F_{I^2C}	Operating frequency	0	—	400	kHz
t_{LOW}	Clock pulse width low	1.3	—	—	µs
t_{HIGH}	Clock pulse width high	0.6	—	—	
t_{SP}	Pulse width of spikes, which are suppressed by the input filter	—	—	50	ns
t_{BUF}	Bus free time between transmissions	1.3	—	—	µs
$t_{HD.STA}$	Start hold time	0.6	—	—	
$t_{SU.STA}$	Start set-up time	0.6	—	—	
$t_{HD.DAT}$	Data in hold time	0	—	0.9	
$t_{SU.DAT}$	Data in set-up time	100	—	—	ns
t_R	SCL/SDA rise time	—	—	250	
t_F	SCL/SDA fall time	—	—	250	
$t_{SU.STO}$	Stop set-up time	0.6	—	—	µs
$t_{VD.DAT}$	Data valid time	—	—	0.8	
Ci/o	Input/output capacitance (SDA)	—	—	10	pF
Cin	Input capacitance (SCL)	—	—	4	

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_L	Load capacitance	—	125	400	pF

Figure 14. I²C timing characteristics



All timings are measured from either V_{IL} or V_{IH}.

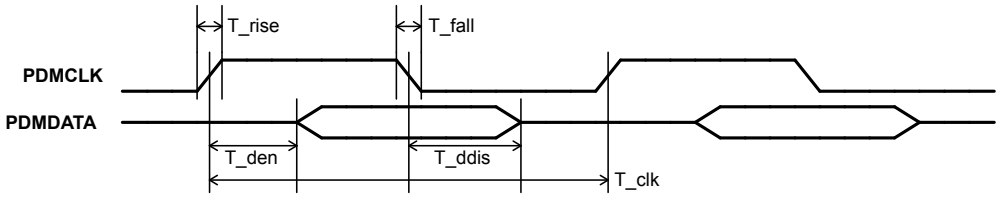
3.5 Pulse density modulation (PDM) interface

Table 9. PDM timing characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_clk	PDM input clock period	95	—	—	ns
T_rise	PDM input clock rise time	—	—	5	
T_fall	PDM input clock fall time	—	—	5	
Duty cycle	PMD input clock duty cycle	40	50	60	%
T_den	Data enabled on PDMDATA line	—	—	20	ns
T_ddis (1)	Data disabled on PDMDATA line	20	—	—	

1. *Guaranteed by design*

Figure 15. PDM timing waveforms



4 VD6283TX registers

4.1 Disclaimer

The VD6283TX register descriptions are for information only. Unless otherwise stated, the VD6283TX registers should be accessed only through the VD6283TX software driver provided by STMicroelectronics.

4.2 I²C interface register map

This section describes in detail all the user-accessible device registers.

Table 10. Register summary

Address	Register name
0x00	DEVICE_ID
0x01	REVISION_ID
0x02	INTERRUPT_CTRL
0x03	ALS_CTRL
0x04	ALS_PERIOD
0x06	ALS_CH1_DATA_H
0x07	ALS_CH1_DATA_M
0x08	ALS_CH1_DATA_L
0x0A	ALS_CH2_DATA_H
0x0B	ALS_CH2_DATA_M
0x0C	ALS_CH2_DATA_L
0x0E	ALS_CH3_DATA_H
0x0F	ALS_CH3_DATA_M
0x10	ALS_CH3_DATA_L
0x12	ALS_CH4_DATA_H
0x13	ALS_CH4_DATA_M
0x14	ALS_CH4_DATA_L
0x16	ALS_CH5_DATA_H
0x17	ALS_CH5_DATA_M
0x18	ALS_CH5_DATA_L
0x1A	ALS_CH6_DATA_H
0x1B	ALS_CH6_DATA_M
0x1C	ALS_CH6_DATA_L
0x1D	ALS_EXPOSURE_M
0x1E	ALS_EXPOSURE_L
0x25	ALS_GAIN_CH1
0x26	ALS_GAIN_CH2
0x27	ALS_GAIN_CH3
0x28	ALS_GAIN_CH4
0x29	ALS_GAIN_CH5
0x2A	ALS_GAIN_CH6
0x2D	CHANNEL6_ENABLE

Address	Register name
0x2E	ALS_CHANNEL_ENABLE
0x31	AC_MODE_CTRL
0x32	PEDESTAL_VALUE
0x3C	SDA_DRV_CFG
0x41	GPIO1_DRV_CFG

4.3 I²C interface register description

4.3.1 Device identification register

7	6	5	4	3	2	1	0
DEV_ID[7:0]							
R							

Address: 0x00

Type: R

Reset: 0x70

Description: DEVICE_ID

[7:0]	DEV_ID: VD6283TX device identification

4.3.2 Silicon revision identification register

7	6	5	4	3	2	1	0
REV_ID[7:0]							
R							

Address: 0x01

Type: R

Reset: 0xBD

Description: REVISION_ID

[7:0]	REV_ID: VD6283TX silicon revision identification

4.3.3 Interrupt control register

7	6	5	4	3	2	1	0
RESERVED						INTR_ST	CLR_INTR
R/W						R	R/W

Address: 0x02

Type: R/W

Reset: 0x00

Description: INTERRUPT_CTRL

[1]	INTR_ST: interrupt status 1: no interrupt has been triggered or the last interrupt has not cleared
[0]	CLR_INTR: clear interrupt flag (handshake mechanism) INTR_ST interrupt flag is cleared by CLR_INTR = '1' followed by CLR_INTR = '0'

4.3.4 ALS control register

7	6	5	4	3	2	1	0
RESERVED					ALS_CONT[1:0]		ALS_EN
R/W					R/W		R/W

Address: 0x03

Type: R/W

Reset: 0x00

Description: ALS_CTRL

[2:1]	ALS_CONT: ALS continuous mode selection 00: ALS mode 1: single ALS measurement request 01: reserved 11: ALS mode 3: continuous ALS measurement request defined by ALS_PERIOD with handshake mechanism from host.
[0]	ALS_EN: enable ALS operation 0: ALS operation is stopped (i.e. idle) 1: ALS operation started with ALS_CONT mode

4.3.5 ALS period register

7	6	5	4	3	2	1	0
ALS_IM_PER[7:0]							
R/W							

Address: 0x04

Type: R/W

Reset: 0x00

Description: ALS_PERIOD

[7:0]	ALS_IM_PER: inter-measurement period LSB = 20.5 ms Min = 0 ms and Max = 5.22 s

4.3.6 ALS channel 1 data register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALS_CH1_DATA_H[7:0]								ALS_CH1_DATA_M[7:0]								ALS_CH1_DATA_L[7:0]							
R																							

Address: 0x06 to 0x08

Type: R

Reset: 0x00

Description: ALS_CH1_DATA

[23:16]	ALS_CH1_DATA_H: ALS channel 1 data high byte
[15:18]	ALS_CH1_DATA_M: ALS channel 1 data medium byte
[7:0]	ALS_CH1_DATA_L: ALS channel 1 data low byte

4.3.7 ALS channel 2 data register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALS_CH2_DATA_H[7:0]								ALS_CH2_DATA_M[7:0]								ALS_CH2_DATA_L[7:0]							
R																							

Address: 0x0A to 0x0C

Type: R

Reset: 0x00

Description: ALS_CH2_DATA

[23:16]	ALS_CH2_DATA_H: ALS channel 2 data high byte
[15:18]	ALS_CH2_DATA_M: ALS channel 2 data medium byte
[7:0]	ALS_CH2_DATA_L: ALS channel 2 data low byte

4.3.8 ALS channel 3 data register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALS_CH3_DATA_H[7:0]								ALS_CH3_DATA_M[7:0]								ALS_CH3_DATA_L[7:0]							
R																							

Address: 0x0E to 0x10

Type: R

Reset: 0x00

Description: ALS_CH3_DATA

[23:16]	ALS_CH3_DATA_H: ALS channel 3 data high byte
[15:18]	ALS_CH3_DATA_M: ALS channel 3 data medium byte
[7:0]	ALS_CH3_DATA_L: ALS channel 3 data low byte

4.3.9 ALS channel 4 data register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALS_CH4_DATA_H[7:0]								ALS_CH4_DATA_M[7:0]								ALS_CH4_DATA_L[7:0]							
R																							

Address: 0x12 to 0x14

Type: R

Reset: 0x00

Description: ALS_CH4_DATA

[23:16]	ALS_CH4_DATA_H: ALS channel 4 data high byte
[15:18]	ALS_CH4_DATA_M: ALS channel 4 data medium byte
[7:0]	ALS_CH4_DATA_L: ALS channel 4 data low byte

4.3.10 ALS channel 5 data register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALS_CH5_DATA_H[7:0]								ALS_CH5_DATA_M[7:0]								ALS_CH5_DATA_L[7:0]							
R																							

Address: 0x16 to 0x18

Type: R

Reset: 0x00

Description: ALS_CH5_DATA

[23:16]	ALS_CH5_DATA_H: ALS channel 5 data high byte
[15:18]	ALS_CH5_DATA_M: ALS channel 5 data medium byte
[7:0]	ALS_CH5_DATA_L: ALS channel 5 data low byte

4.3.11 ALS channel 6 data register

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ALS_CH6_DATA_H[7:0]								ALS_CH6_DATA_M[7:0]								ALS_CH6_DATA_L[7:0]							
R																							

Address: 0x1A to 0x1C

Type: R

Reset: 0x00

Description: ALS_CH6_DATA

[23:16]	ALS_CH6_DATA_H: ALS channel 6 data high byte
[15:18]	ALS_CH6_DATA_M: ALS channel 6 data medium byte
[7:0]	ALS_CH6_DATA_L: ALS channel 6 data low byte

4.3.12 ALS exposure register

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RESERVED						EXTIME[9:0]									
R/W															

Address: 0x1D to 0x1E

Type: R/W

Reset: 0x0032

Description: ALS_EXPOSURE

[9:0]	EXTIME: exposure time = (EXTIME[9:0] + 1) x 16384/Fosc Fosc = 10.24 MHz Default value = 80 ms (min. = 1.6 ms and max. = 1.6 s)

4.3.13 ALS gain channel 1 register

7	6	5	4	3	2	1	0
RESERVED			AGAIN[3:0]				
R/W							

Address: 0x25

Type: R/W

Reset: 0x00

Description: ALS_GAIN_CH1

[3:0]	AGAIN: channel1 analog gain 0000: reserved 0001: AGAIN = 66.6x 0010: AGAIN = 50x 0011: AGAIN = 33x 0100: AGAIN = 25x 0101: AGAIN = 16x 0110: AGAIN = 10x 0111: AGAIN = 7.1x 1000: AGAIN = 5x 1001: AGAIN = 3.33x 1010: AGAIN = 2.5x 1011: AGAIN = 1.67x 1100: AGAIN = 1.25x 1101: AGAIN = 1x 1110: AGAIN = 0.83x 1111: AGAIN = 0.71x

4.3.14 ALS gain channel 2 register

7	6	5	4	3	2	1	0
RESERVED			AGAIN[3:0]				
R/W							

Address: 0x26

Type: R/W

Reset: 0x00

Description: ALS_GAIN_CH2

[3:0]	AGAIN: channel2 analog gain 0000: reserved 0001: AGAIN = 66.6x 0010: AGAIN = 50x 0011: AGAIN = 33x 0100: AGAIN = 25x 0101: AGAIN = 16x 0110: AGAIN = 10x 0111: AGAIN = 7.1x 1000: AGAIN = 5x 1001: AGAIN = 3.33x 1010: AGAIN = 2.5x 1011: AGAIN = 1.67x 1100: AGAIN = 1.25x 1101: AGAIN = 1x 1110: AGAIN = 0.83x 1111: AGAIN = 0.71x

4.3.15 ALS gain channel 3 register

7	6	5	4	3	2	1	0
RESERVED			AGAIN[3:0]				
R/W							

Address: 0x27

Type: R/W

Reset: 0x00

Description: ALS_GAIN_CH3

[3:0]	AGAIN: channel3 analog gain 0000: reserved 0001: AGAIN = 66.6x 0010: AGAIN = 50x 0011: AGAIN = 33x 0100: AGAIN = 25x 0101: AGAIN = 16x 0110: AGAIN = 10x 0111: AGAIN = 7.1x 1000: AGAIN = 5x 1001: AGAIN = 3.33x 1010: AGAIN = 2.5x 1011: AGAIN = 1.67x 1100: AGAIN = 1.25x 1101: AGAIN = 1x 1110: AGAIN = 0.83x 1111: AGAIN = 0.71x

4.3.16 ALS gain channel 4 register

7	6	5	4	3	2	1	0
RESERVED			AGAIN[3:0]				
R/W							

Address: 0x28

Type: R/W

Reset: 0x00

Description: ALS_GAIN_CH4

[3:0]	AGAIN: channel4 analog gain 0000: reserved 0001: AGAIN = 66.6x 0010: AGAIN = 50x 0011: AGAIN = 33x 0100: AGAIN = 25x 0101: AGAIN = 16x 0110: AGAIN = 10x 0111: AGAIN = 7.1x 1000: AGAIN = 5x 1001: AGAIN = 3.33x 1010: AGAIN = 2.5x 1011: AGAIN = 1.67x 1100: AGAIN = 1.25x 1101: AGAIN = 1x 1110: AGAIN = 0.83x 1111: AGAIN = 0.71x

4.3.17 ALS gain channel 5 register

7	6	5	4	3	2	1	0
RESERVED			AGAIN[3:0]				
R/W							

Address: 0x29

Type: R/W

Reset: 0x00

Description: ALS_GAIN_CH5

[3:0]	AGAIN: channel5 analog gain 0000: reserved 0001: AGAIN = 66.6x 0010: AGAIN = 50x 0011: AGAIN = 33x 0100: AGAIN = 25x 0101: AGAIN = 16x 0110: AGAIN = 10x 0111: AGAIN = 7.1x 1000: AGAIN = 5x 1001: AGAIN = 3.33x 1010: AGAIN = 2.5x 1011: AGAIN = 1.67x 1100: AGAIN = 1.25x 1101: AGAIN = 1x 1110: AGAIN = 0.83x 1111: AGAIN = 0.71x

4.3.18 ALS gain channel 6 register

7	6	5	4	3	2	1	0
RESERVED			AGAIN[3:0]				
R/W							

Address: 0x2A

Type: R/W

Reset: 0x00

Description: ALS_GAIN_CH6

[3:0]	AGAIN: channel6 analog gain 0000: reserved 0001: AGAIN = 66.6x 0010: AGAIN = 50x 0011: AGAIN = 33x 0100: AGAIN = 25x 0101: AGAIN = 16x 0110: AGAIN = 10x 0111: AGAIN = 7.1x 1000: AGAIN = 5x 1001: AGAIN = 3.33x 1010: AGAIN = 2.5x 1011: AGAIN = 1.67x 1100: AGAIN = 1.25x 1101: AGAIN = 1x 1110: AGAIN = 0.83x 1111: AGAIN = 0.71x

4.3.19 Channel 6 enable register

7	6	5	4	3	2	1	0
RESERVED							CH6_EN
R/W							

Address: 0x2D

Type: R/W

Reset: 0x00

Description: CHANNEL6_ENABLE

[0]	CH6_EN: channel6 operation activation 0: Channel6 is disabled 1: Channel6 is enabled

4.3.20 ALS channel enable register

7	6	5	4	3	2	1	0
RESERVED			ALS_CH_EN[4:0]				
R/W							

Address: 0x2E

Type: R/W

Reset: 0x00

Description: ALS_CHANNEL_ENABLE

[4:0]	ALS_CH_EN: ALS channel [1..5] operation 00000: no channel enabled 00001: enables channel 1 00010: enables channel 2 00100: enables channel 3 01000: enables channel 4 10000: enables channel 5 11111: all channels [1..5] enabled

4.3.21 AC mode control register

7	6	5	4	3	2	1	0
0	PEDESTAL_DIS	PDM_CLK_SEL	AC_OUT_SEL	AC_CH_SEL[2:0]			AC_FREQEXT_EN
R/W							

Address: 0x31

Type: R/W

Reset: 0x00

Description: AC_MODE_CTRL

[6]	Pedestal feature enable/disable: 0: pedestal feature enabled (default) 1: pedestal feature disabled
[5]	PDM clock input selection: 0: VD6283TX internal clock used to sync the PDM signal (default) 1: external clock connected to GPIO2: used to synchronize the PDM signal (host)
[4]	AC_OUT_SEL: AC flicker signal output selection 0: PDM data output on GPIO1 MUX (default) 1: PDM data output on GPIO2
[3:1]	Flicker operation channel selection: 000: no channel selected (default) 001: ALS channel 6 selected 010: ALS channel 1 selected 011: ALS channel 2 selected 100: ALS channel 3 selected 101: ALS channel 4 selected 110: ALS channel 5 selected
[0]	Flicker frequency extractor: 0: flicker frequency extractor feature disabled (default) 1: flicker frequency extractor feature enabled

4.3.22 Pedestal value register

7	6	5	4	3	2	1	0
RESERVED					PDST_VAL[2:0]		
R/W							

Address: 0x32

Type: R/W

Reset: 0x05

Description: PEDESTAL_VALUE

[2:0]	Read/write of the pedestal value (applies for flicker operation only) Recommended pedestal value = 3

4.3.23 SDA driver configuration register

7	6	5	4	3	2	1	0
RESERVED				SDA_LOAD	SDA_DRV[2:0]		
R/W							

Address: 0x3C

Type: R/W

Reset: 0x09

Description: SDA_DRV_CFG

[3]	SDA capacitive load line: 0: <95 pF 1: >95 pF (default)
[2:0]	SDA_DRV configures the SDA driver output current capability: 000: output driver 1 value (lowest) 001: output driver 2 value (default) 010: output driver 3 value 011: output driver 4 value 100: output driver 5 value (recommended for I²C fast mode plus)

4.3.24 GPIO1 driver configuration register

7	6	5	4	3	2	1	0
RESERVED						GPIO1_CFG[1:0]	
R/W							

Address: 0x41

Type: R/W

Reset: 0x00

Description: GPIO1_DRV_CFG

[1:0]	GPIO1_CFG: GPIO1 driver configuration 00: open drain output (default value) 01: push-pull output 10: output analog via series resistor (200 Ohms) 11: reserved

5 Absolute maximum ratings, operating conditions and electrostatic discharge (ESD) values

5.1 Absolute maximum ratings

Table 11. Absolute maximum ratings

Parameters	Min.	Typ.	Max.	Unit
VDD	-0.5	—	2.5	V
SDA, SCL, GPIO1, GPIO2	-0.5		2.5	

Stresses above those listed in the table above may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended operating conditions

Table 12. Recommended operating conditions

Parameter	Min.	Typ.	Max.	Unit
Voltage (VDD)	1.65	1.8	1.95	V
IO	1.65	1.8	1.95	
Temperature (normal operating)	-30	25	85	°C
Storage temperature	-40	—	125	

5.3 Electrostatic discharge (ESD)

The VD6283TX is compliant with the ESD values presented in the table below.

Table 13. ESD values

Parameter	Specification	Conditions	Max. value	Unit
Human body model	JS001 2017	25 °C, 1500 Ω, 100 pF	±2000	V
Charge device model (1)	JS002 2018	25 °C	±500	

1. *For information only. The final package contributes to CDM performance. Consequently, STMicroelectronics cannot guarantee CDM performances in final packages.*

6 Electrical characteristics

The table gives an overview of the VD6283TX current consumption in different operating states.

Table 14. Current consumption in different operating states

Parameter	Min.	Typ.	Max.	Unit
Idle (no I²C activity)	—	3	5	µA
Intermeasurement		5	10	
ALS only 1 channel		350	400	
ALS only 5 channels		450	500	
Flicker only 1 channel		640	800	
ALS + flicker 5 channels + 1 channel simultaneously		760	850	

Note: All current consumption values include silicon process variations.

Note: In ambient light, temperature and voltage are at nominal conditions (25°C and 1.8 V).

Note: The flicker operation is performed as shown in Figure 5. Application schematic, ALS, and flicker in analog format (mode 2).

One possible application use is given in the figure below.

Figure 16. ALS only, single shot mode

Table 15. Digital I/O electrical characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
GPIO1/GPIO2					
V_{IL}	Low level input voltage	—	—	0.3 * VDD	V
V_{IH}	High level input voltage	0.7 * VDD		—	
V_{OL}	Low level output voltage (IOUT = 4 mA)	—		0.4	
V_{OH}	High level output voltage (IOUT = 4 mA)	VDD – 0.4		—	
I²C interface (SDA/SCL)					
V_{IL}	Low level input voltage	-0.5	—	0.3 * VDD	V
V_{IH}	High level input voltage	0.7 * VDD		VDD + 0.5	
V_{OL}	Low level output voltage (IOUT = 2 mA in standard and fast modes)	—		0.2 * VDD	
I_{OL1}	Low level output current 1, SDA_DRV_CFG = ’000’, V_{OL} = 0.4 V	4		—	mA
I_{OL2}	Low level output current 2, SDA_DRV_CFG = ’001’, V_{OL} = 0.4 V	8			
I_{OL3}	Low level output current 3, SDA_DRV_CFG = ’010’, VOL = 0.4 V	12			
I_{OL4}	Low level output current 4, SDA_DRV_CFG = ’011’, VOL = 0.4 V	16			
I_{OL5}[(1)]	Low level output current 5, SDA_DRV_CFG = ’100’, VOL = 0.4 V	20			
$I_{IL/IH}$	Leakage current, VDD = 0 V, 0.1*VDD < VIL <0.9*VDD	-10		10	µA

1. *Recommended value for I²C fast mode plus. Refer to Table 5. Recommended pull up resistors and SDA driver settings for I²C modes*

7 ALS and flicker performances

Table 16. ALS operating characteristics

Parameter	Conditions		Min.	Typ.	Max.	Unit
Exposure time	EXTIME step size		1.52	1.6	1.68	ms
	Number of EXTIME steps overall, 1.6 ms to 1.6 s		1		1024	Steps
Inter measurement period	IM step size			20		ms
	Number of IM steps overall, 20 ms to 5.12 s		1		256	Steps
ADC count value	Minimum reported irradiance level	24-bit ADC readout	—	256	—	Counts
		16-bit ADC readout (w/o low byte)	—	1	—	
	EXTIME = 0x001 to 0x047 (1.6 ms to 113.6 ms)	24-bit ADC readout	0		233045	Counts/ steps
		16-bit ADC readout (w/o low byte)	0		910	
	EXTIME = 0x048 to 0x3FF (115.2 ms to 1.6 s)	24-bit ADC readout	0		16777215	Counts
		16-bit ADC readout (w/o low byte)	0		65535	
Gain scaling (relative to 1x)	AGAIN = 0.7x		0.7	0.71	0.74	—
	AGAIN = 0.8x		0.82	0.83	0.85	
	AGAIN = 1x		0.99	1.00	1.01	
	AGAIN = 1.25x		1.25	1.25	1.27	
	AGAIN = 1.7x		1.66	1.68	1.69	
	AGAIN = 2.5x		2.49	2.52	2.54	
	AGAIN = 3.3x		3.31	3.36	3.38	
	AGAIN = 5x		4.97	5.04	5.08	
	AGAIN = 7.1x		7	7.17	7.27	
	AGAIN = 10x		9.73	10.07	10.23	
	AGAIN = 16x		16.04	16.76	17.18	
	AGAIN = 25x		23.83	25.1	26.2	
	AGAIN = 33.3x		31.35	33.3	35.07	
	AGAIN = 50x		45.67	50.12	54.39	
	AGAIN = 66.6x		59.2	66.78	73.01	
ALS readout RMS noise	16-bit ADC readout AGAIN = 16x, EXTIME = 24 ms Clear channel Tamb = 25 °C, VDD = 1.8 V Irradiance = 40 µW/cm^2				0.25	Counts
Minimum detectable light level (1)	AGAIN = 66x, EXTIME = 113.6 ms Clear channel (2)				0.0015	Lux
	AGAIN = 66x, EXTIME = 113.6 ms Green channel (2)				0.007	

Parameter	Conditions	Min.	Typ.	Max.	Unit
Maximum light level (1)	AGAIN = 0.7x, EXTIME = 1.6 ms Clear channel (2)	6609			Lux
	AGAIN = 0.7x, EXTIME = 1.6 ms, Green channel (2)	30369			
Dark count noise	Irradiance = 0 µW/m2 (i.e. total dark) AGAIN = 66x, EXTIME = 100 ms Tamb = 25 °C		0	1.484	Counts

1. *Guaranteed by characterization (process and temperature variation included)*
2. *D65 vs visible light source*

Table 17. Flicker operating characteristics

Unless otherwise stated, the flicker characteristics below are valid under the following host conditions: Flicker channel = Clear, Configuration mode 1 (SPI) or mode 2 (ADC), FFT method, 300 ms data capture time.

Parameter	Conditions	Min.	Typ.	Max.	Unit
PDM input clock	External PDM clock frequency	2	5	10	MHz
	External PDM clock duty cycle	40	50	60	%
Percent flicker ranges	White LED, 4000 K (DC level) from 1 to 5 Lux	20		100	%
	White LED, 4000 K (DC level) from 5 to 4000 Lux	3		100	
AC flicker frequency detection range	For above percent flicker ranges	100		2000	Hz
AC flicker frequency detection accuracy	Frequency range = 100 Hz to 2000 Hz Light waveform = square (PWM)		1	3.3	%
	Frequency range = 100 Hz / 120 Hz Light waveform = sine wave		1	3.3	

8 Optical characteristics

8.1 Photodiode matrix

The sensing matrix is 25 photodiodes in total (5x5).

Figure 17. Photodiode matrix for VD6283TX45/1

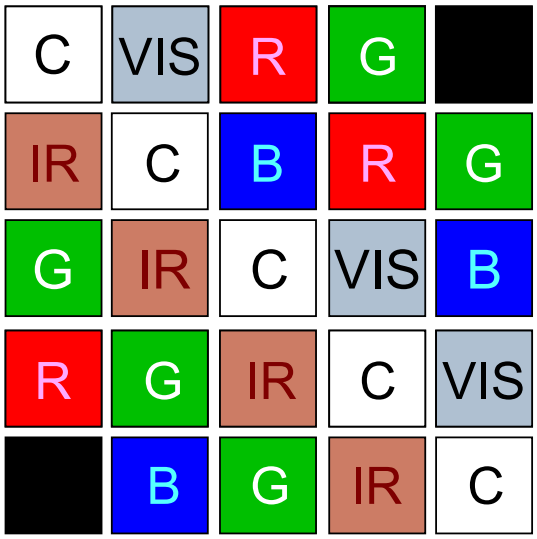


Figure legends:

- B = blue
- R = red
- G = green
- I = IR
- VIS = visible
- C = clear photodiode (no filter)
- D = dark channel

8.2 Channel sensitivity

Unless otherwise stated: Tamb = 25 °C, typical supply (VDD) voltage = 1.8 V, and EXTIME = 50 ms. ST performs a light calibration of every part in production, with individual adjustment of counts into the product memory. A calibration factor is stored in the VD6283TX OTP memory and calibrated data can be retrieved through the software driver.

Table 18. Clear channel

Parameter	Conditions	Min.	Typ.	Max.	Unit
Clear channel, irradiance responsivity before calibration	White LED (CCT = 4000 K) 16-bit ADC readout AGAIN = 5x	49.9	62.3	74.8	Counts/(µW/cm²)
Clear channel, irradiance responsivity after calibration		56.1	62.3	68.6	

Table 19. Visible channel

Parameter	Conditions	Min.	Typ.	Max.	Unit
Visible channel, irradiance responsivity before calibration	White LED (CCT = 4000 K) 16-bit ADC readout AGAIN = 10x	39.7	49.7	59.6	Counts/(µW/cm²)
Visible channel, irradiance responsivity after calibration		44.7	49.7	54.6	

Table 20. Red channel

Parameter	Conditions	Min.	Typ.	Max.	Unit
Red channel, irradiance responsivity before calibration	White LED (CCT = 4000 K) 16-bit ADC readout AGAIN = 10x	11.7	14.6	17.5	Counts/(µW/cm²)
Red channel, irradiance responsivity after calibration		13.1	14.6	16.0	

Table 21. Green channel

Parameter	Conditions	Min.	Typ.	Max.	Unit
Green channel, irradiance responsivity before calibration	White LED (CCT = 4000 K) 16-bit ADC readout AGAIN = 10x	23.6	29.5	35.4	Counts/(µW/cm²)
Green channel, irradiance responsivity after calibration		26.5	29.5	32.4	

Table 22. Blue channel

Parameter	Conditions	Min.	Typ.	Max.	Unit
Blue channel, irradiance responsivity before calibration	White LED (CCT = 4000 K) 16-bit ADC readout AGAIN = 10x	11.6	14.6	17.4	Counts/(µW/cm²)
Blue channel, irradiance responsivity after calibration		13.1	14.6	16.0	

Table 23. IR channel

Parameter	Conditions	Min.	Typ.	Max.	Unit
IR channel, irradiance responsivity before calibration	IR LED (λ_P = 850 nm) 16-bit ADC readout AGAIN = 10x	68.8	86.0	103.2	Counts/(µW/cm²)
IR channel, irradiance responsivity after calibration		77.4	86.0	94.6	

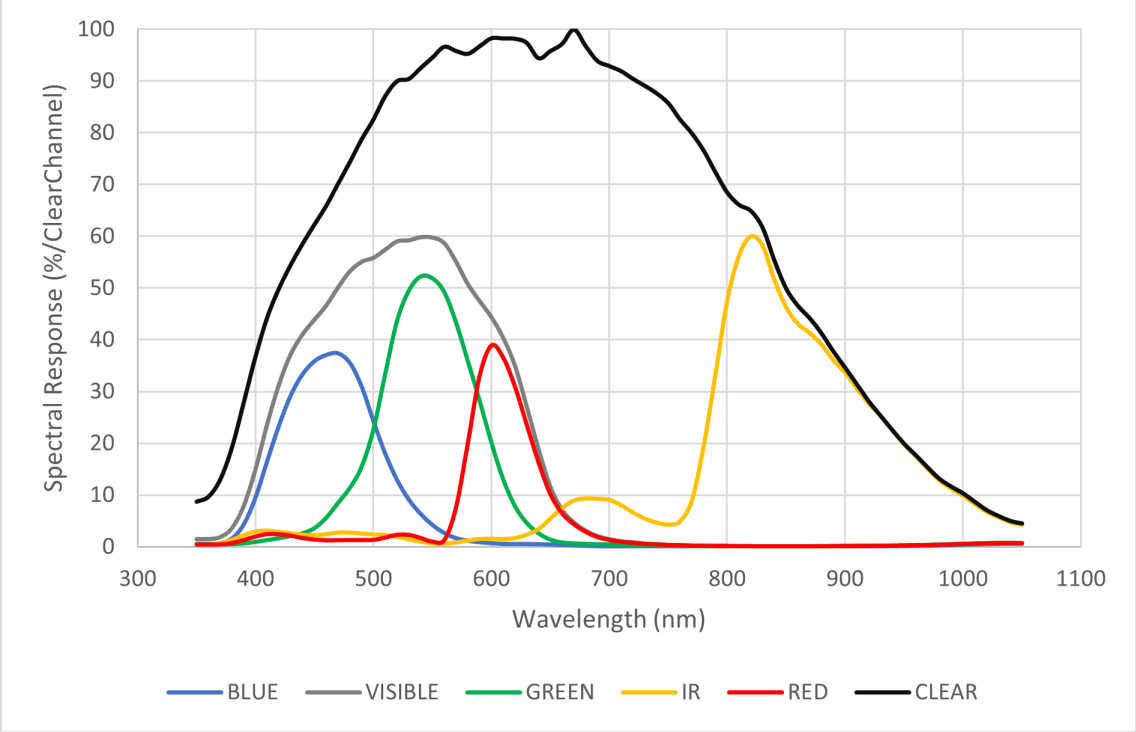
Note: Irradiance measurements are performed with an R203 radiometer RFF-Cos filter in the ST laboratories.

Note: The main characteristic of white LED is a nominal color temperature of 4000 K (reference: L130-4080001400001).

Note: The main characteristics of IR LED are: peak wavelength of λ_P = 850 nm, and spectral half width $\Delta\lambda_{IR}$ = 30 nm (reference: MTE8600MT).

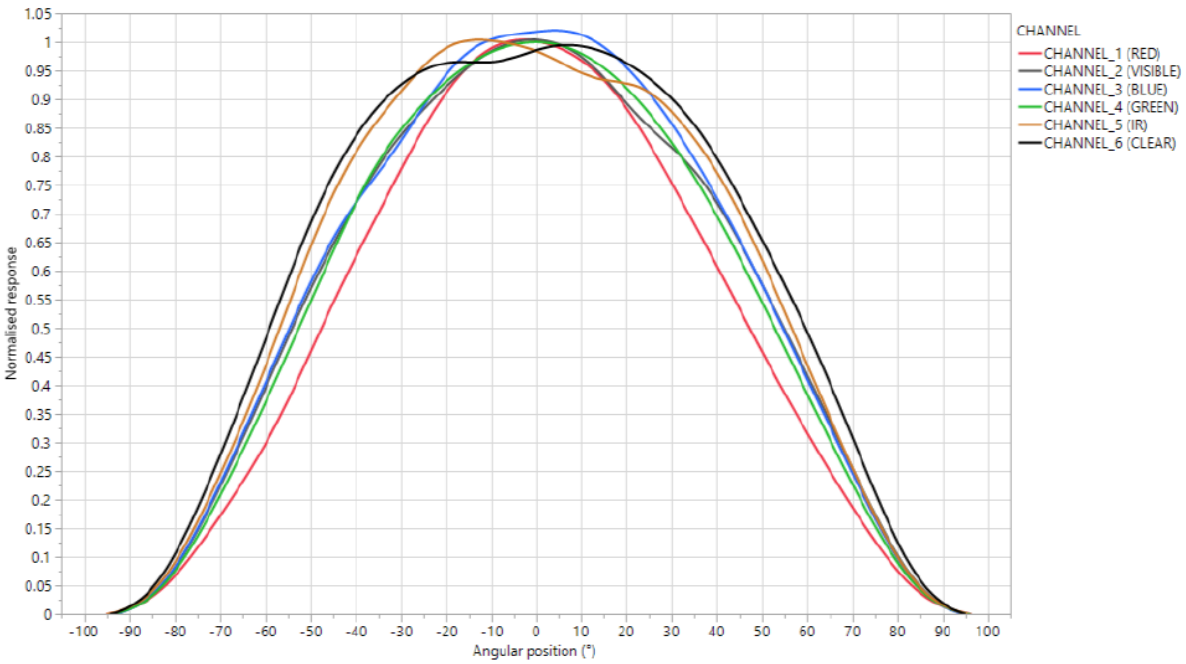
8.3 Spectral response

Figure 18. **VD6283TX45/1 spectral response (full color set RGBIRClear)**



8.4 Angular response

Figure 19. **VD6283TX normalized angular response for each channel without diffuser and without aperture**



9 Outline drawings

Figure 20. **Outline drawing - FoV 60 °**

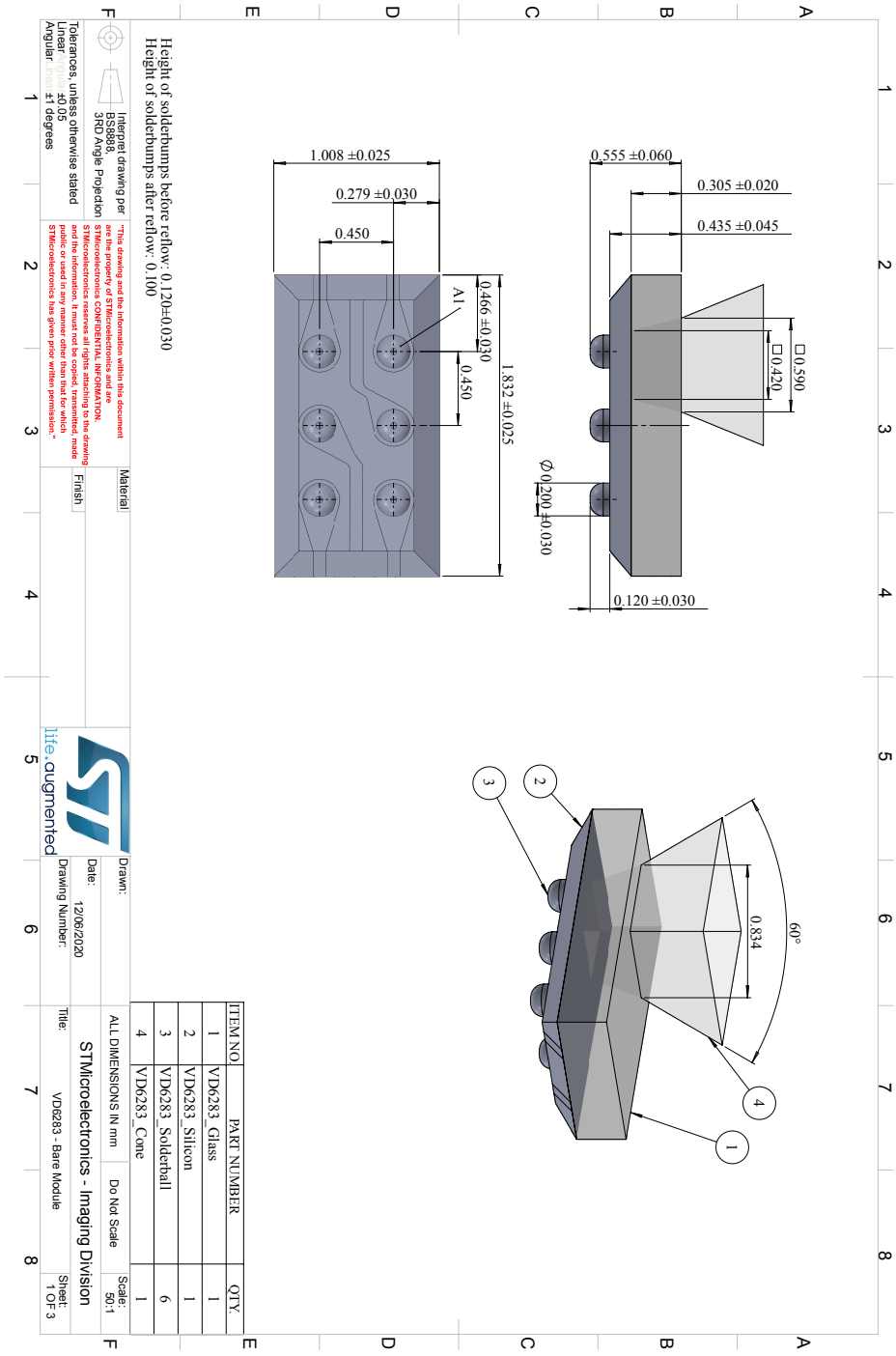


Figure 21. **Outline drawing - FoV 90 °**

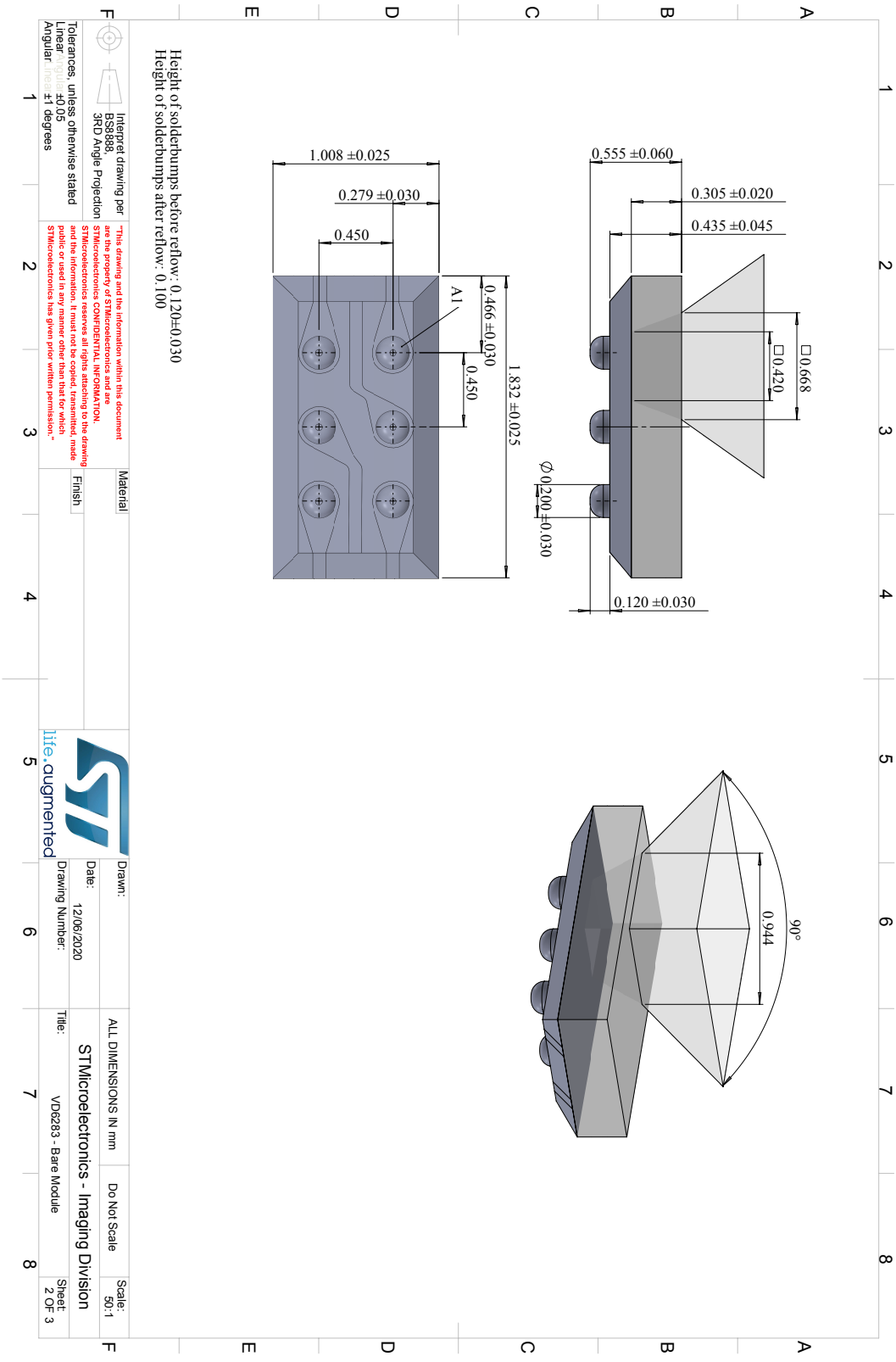
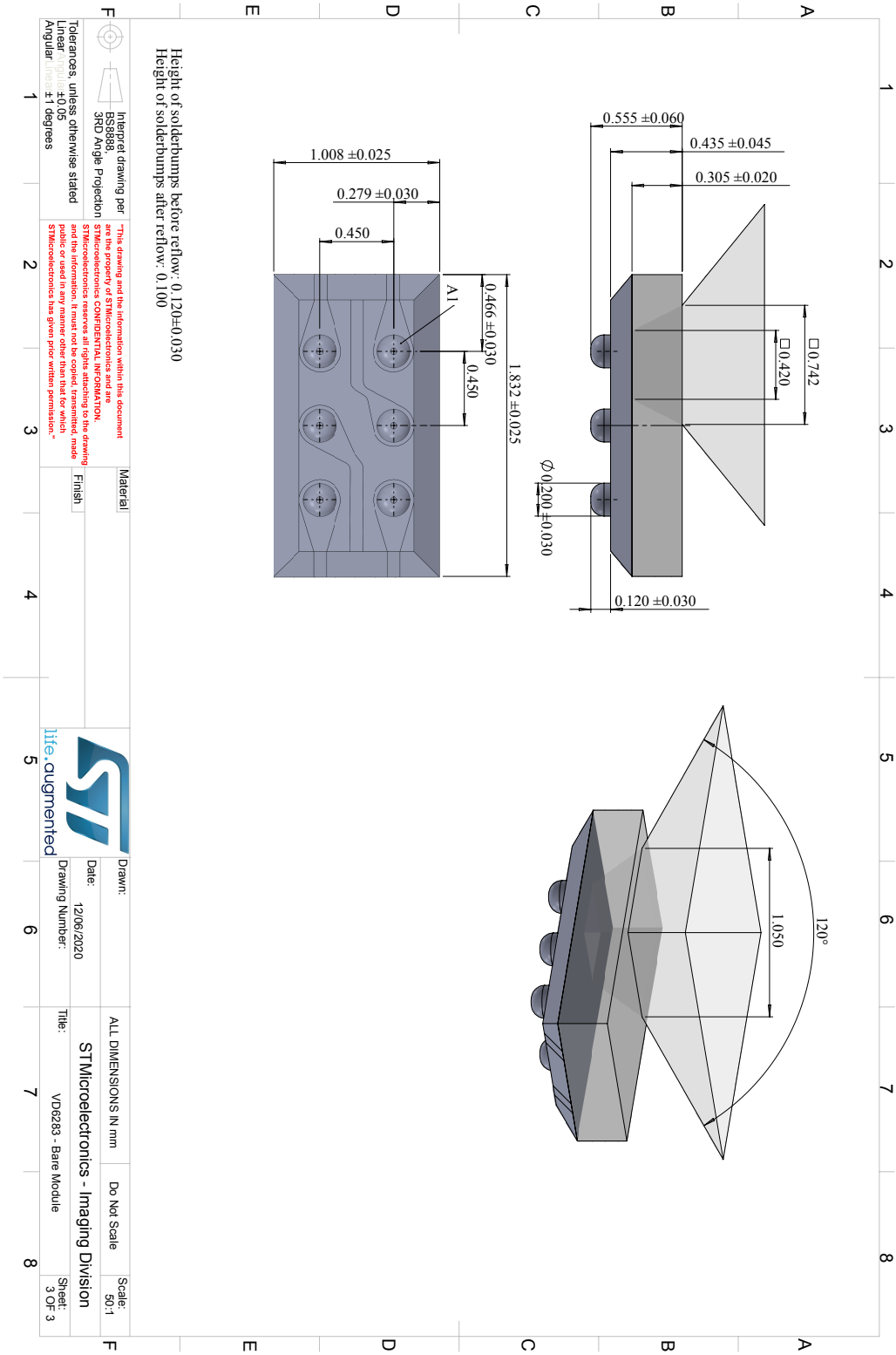


Figure 22. **Outline drawing - FoV 120 °**



10 Package information

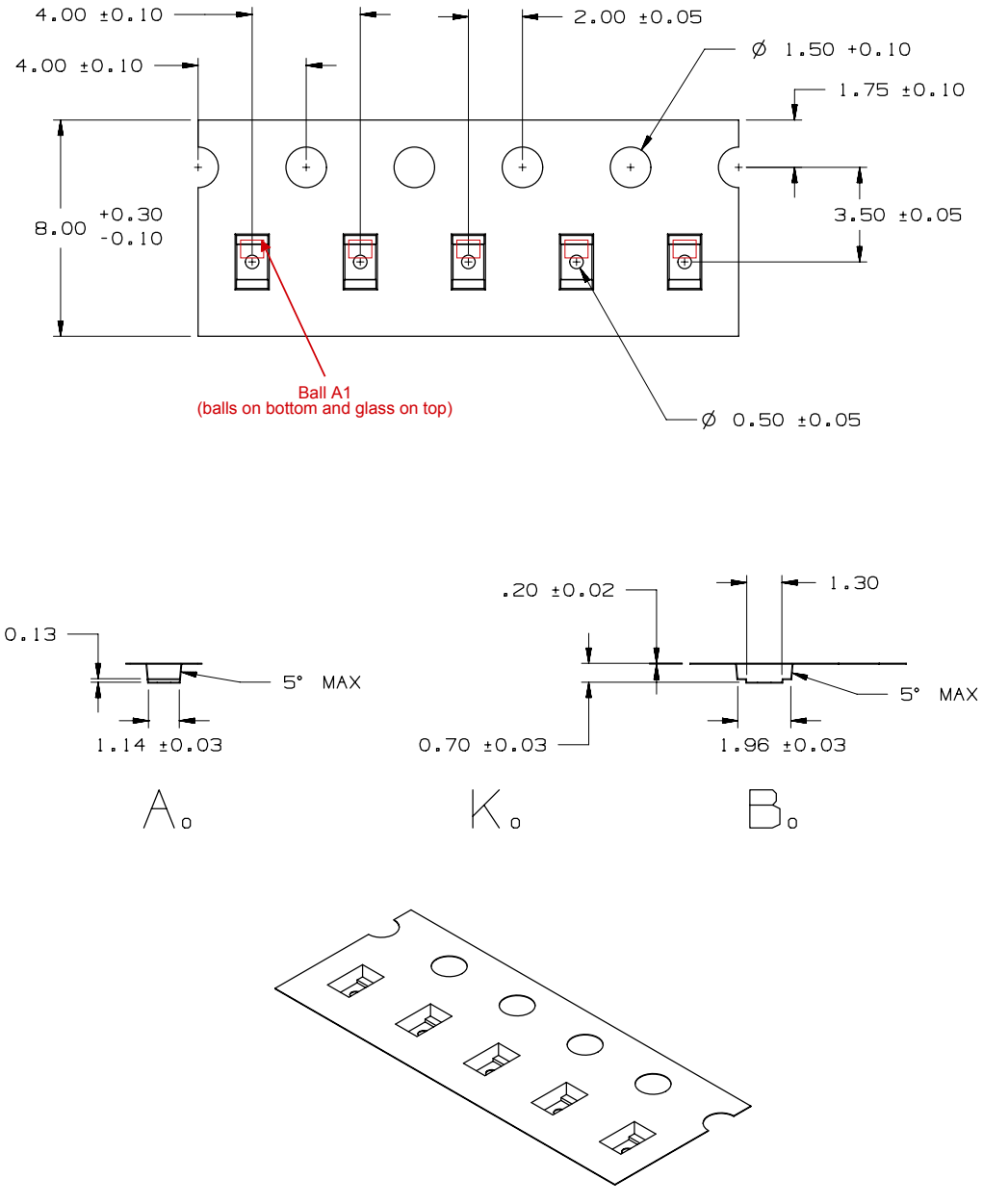
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

10.1 ECOPACK®2

The VD6283TX is an ECOPACK® grade 2 product.

10.2 Tape and reel outline drawing

Figure 23. Tape and reel



Note: The drawing above is proposed. The dimensions may vary slightly from the actual carrier.

10.3 Optical BGA 6-ball reflowable package information

Figure 24. **Optical BGA 6-ball reflowable package outline**

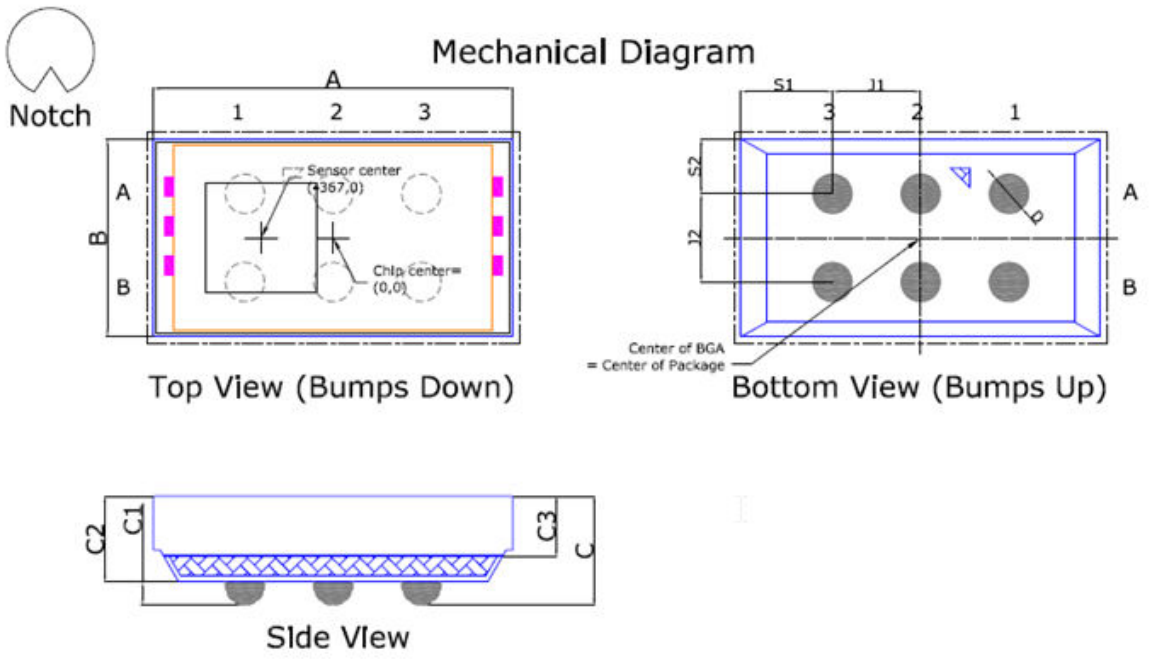
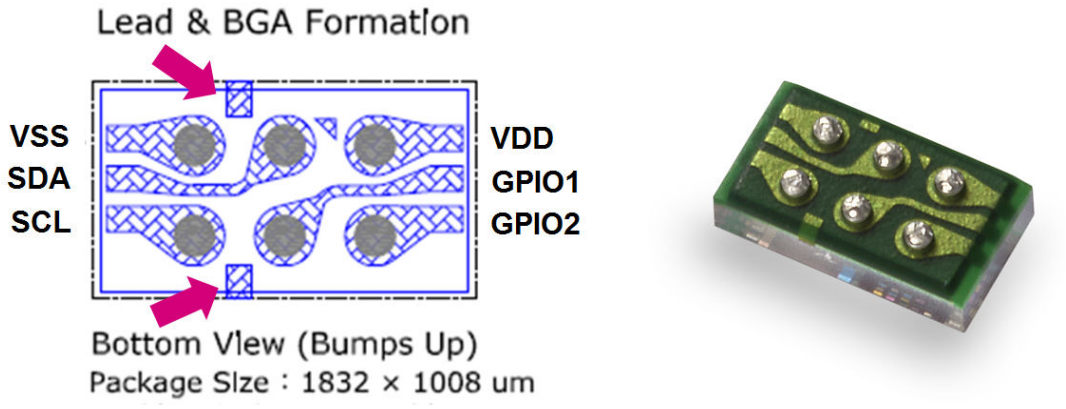


Table 24. **Optical BGA 6-ball reflowable mechanical data**

Ref.	Symbol	Dimension (µm)		
		Min.	Typ.	Max.
Package body dimension X	A	1807	1832	1857
Package body dimension Y	B	983	1008	1033
Package height	C	495	555	615
Ball height	C1	90	120	150
Package body thickness	C2	390	435	480
Thickness of glass surface to wafer	C3	285	305	325
Ball diameter	D	170	200	230
Total ball count	N		6	
Ball count X-axis	N1		3	
Ball count Y-axis	N2		2	
Ball pitch X-axis	J1		450	
Ball pitch Y-axis	J2		450	
Edge-to-ball center distance along X	S1	436	466	496
Edge-to-ball center distance along Y	S2	249	279	309

Figure 25. **Visual anti-rotation mark**



10.4 Solder ball information

Figure 26. **Solder ball information**

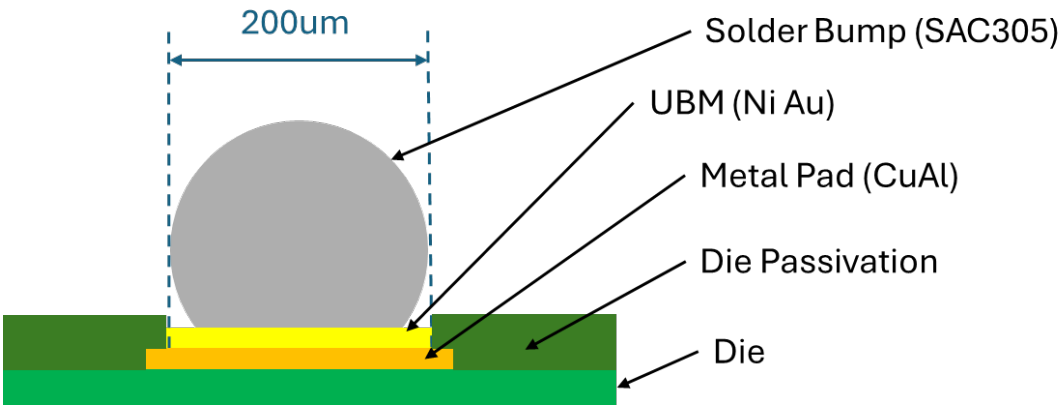


Table 25. **Solder ball information**

Layer	Material		Dimensions (µm)		
			Min.	Typ.	Max.
Solder ball	SAC305	Sn = 96.5%	170	200	230
		Ag = 3%			
		Cu = 0.5%			
UBM	NiAu		—	200	—
Metal pad	CuAl		—	—	—

10.5 PCB layout and stencil drawing

Figure 27. **PCB layout**

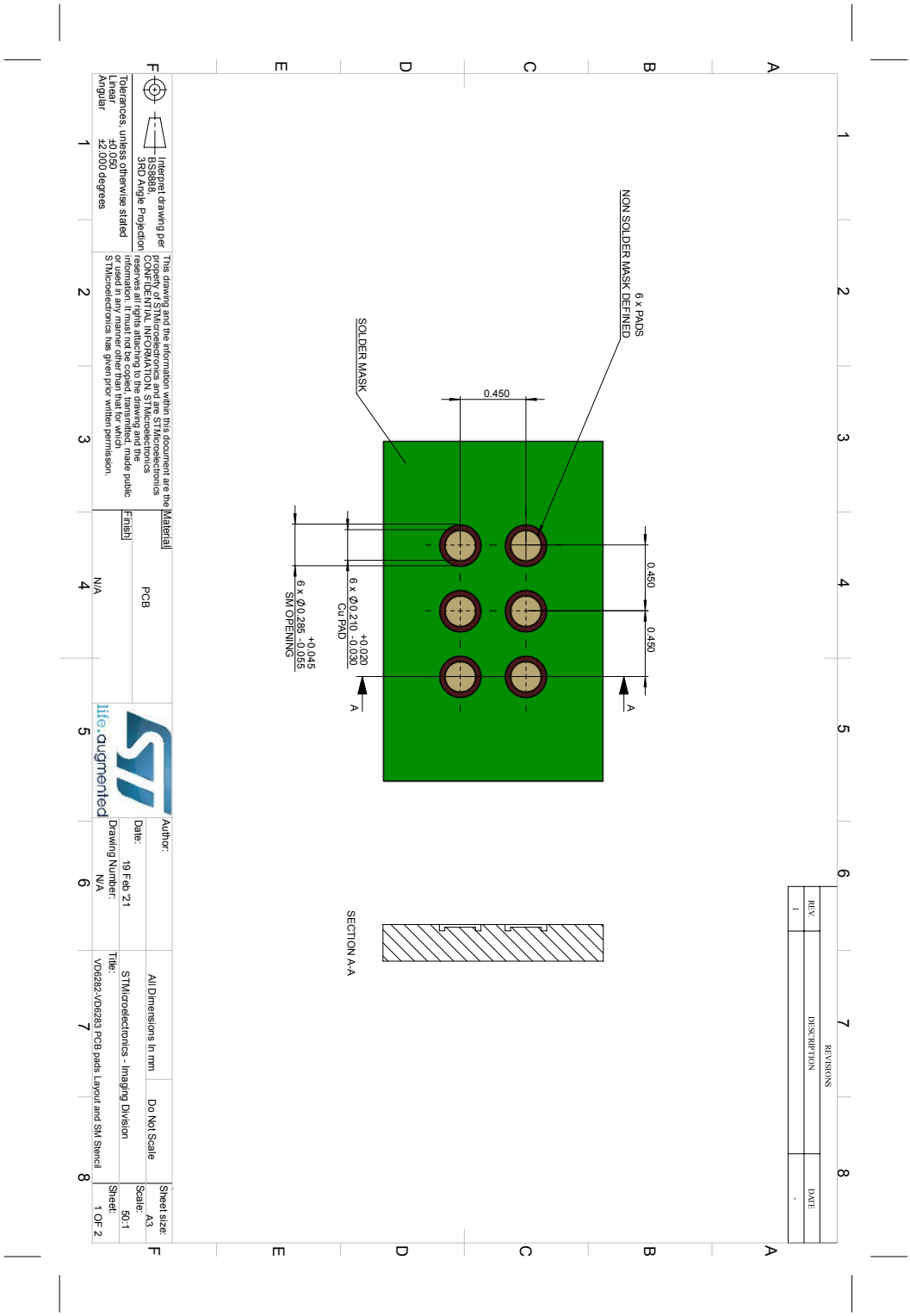
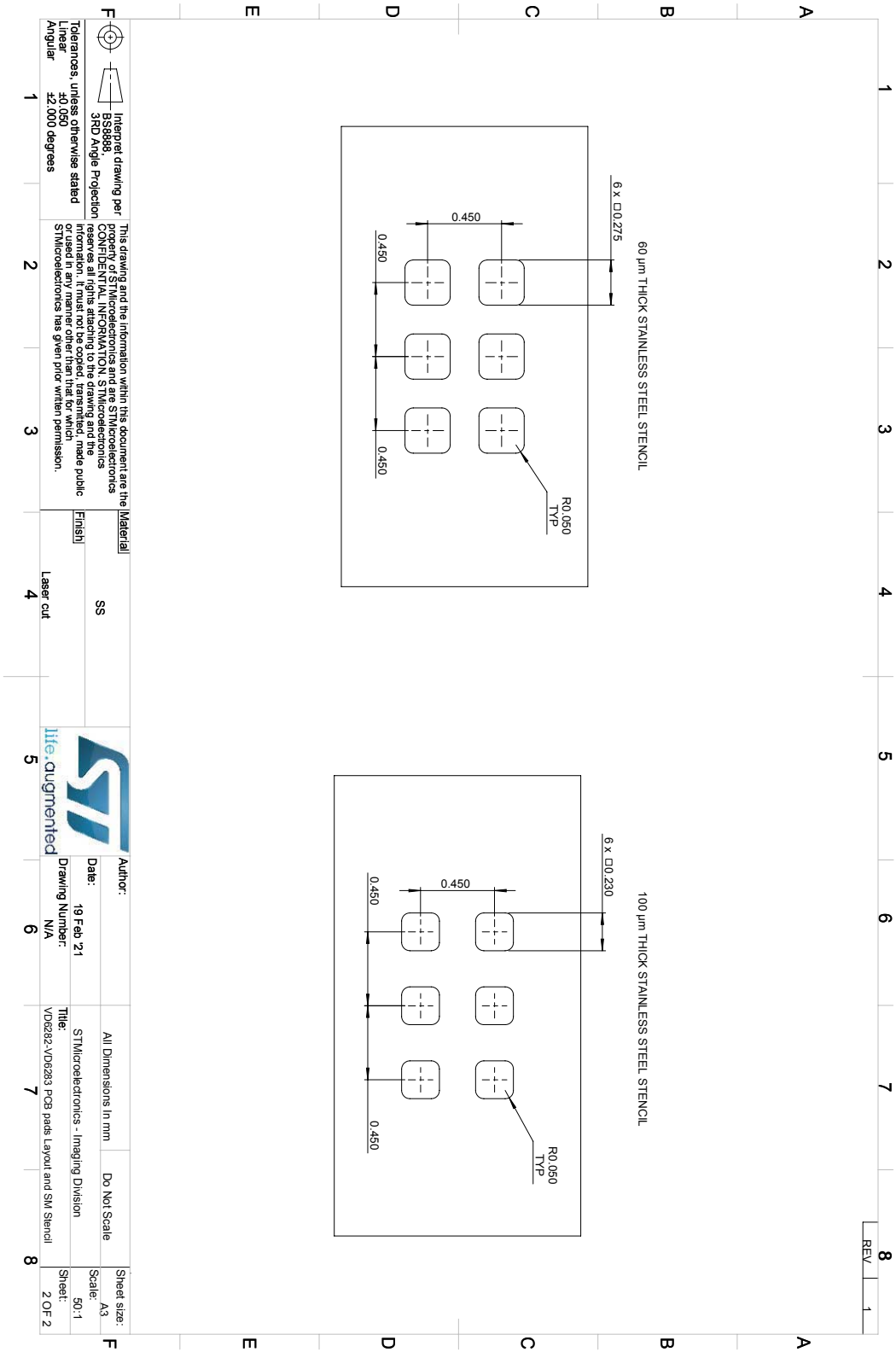


Figure 28. **PCB stencil drawing**



Note: The above PCB stencil drawing is recommended in ST. However, it is permissible to work with a different stencil drawing in the production line.

10.6 Lead-free solder reflow process

The table and figure below show the recommended and maximum values for the solder profile. Customers will have to tune the reflow profile depending on the PCB, solder paste, and material used. We expect customers to follow the “recommended” reflow profile, which is specifically tuned for the VD6283TX package. For any reason, if a customer must perform a reflow profile which is different from the “recommended” one (especially peak >240 °C), this new profile must be qualified by the customer at their own risk. In any case, the profile has to be within the “maximum” profile limit described in the figure below.

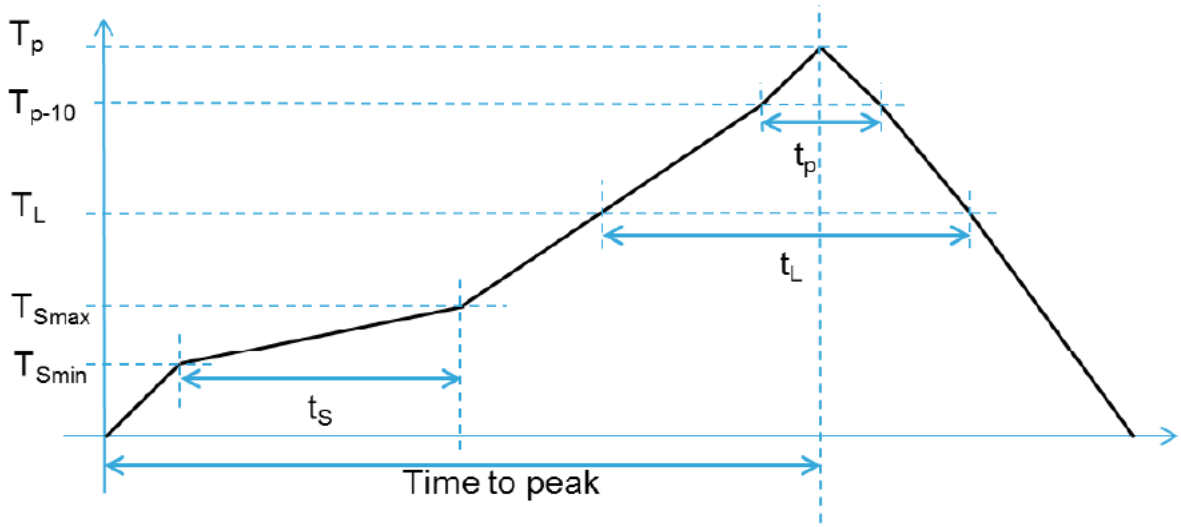
Table 26. Recommended soldering profile

Parameters	Recommended	Maximum	Units
Minimum temperature (T_{Smin})	100	150	°C
Maximum temperature (T_{Smax})	180	200	°C
Time ts (T_{Smin} to T_{Smax})	80	60-120	s
Temperature (T_L)	180	217	°C
Time (t_L)	110	60-150	s
Ramp up	1.5	3	°C/s
Temperature (T_{p-10})	230	250	°C
Time (as index)	—	30	s
Ramp up	0.5	3	°C/s
Peak temperature (T_p)	240	260	°C
Time to peak	220	480	s
Ramp down (peak to T_L)	-2	-6	°C/s

Note: The temperature mentioned in the above table is measured on top of the VD6283TX package.

Note: The VD6283TX can sustain up to three passes maximum through the recommended solder reflow profile.

Figure 29. Soldering profile



10.7 Handling and storage precautions

10.7.1 Part handling

The parts must be handled with non-marring ESD safe carbon, plastic, or teflon tweezers. Ranging modules are susceptible to damage or contamination. The customer is advised to use a clean assembly process after removing the tape from the parts, and until a protective cover glass is mounted.

10.7.2 Moisture sensitivity level

Moisture sensitivity for the VD6283TX is level 3 (MSL) as described in IPC/JEDEC JSTD-020-E.

10.7.3 Storage temperature conditions

Table 27. Recommended storage conditions

Parameter	Min.	Typ.	Max.	Unit
Storage temperature	-40	23	125	°C

11 Ordering information

Table 28. **Order codes**

Order code	Package	Comment
VD6283TX45/1	Optical WLCSP BGA 6-ball	Red, green, blue, IR, clear, and visible

12 Acronyms and abbreviations

Table 29. **Acronyms and abbreviations**

Acronym/abbreviation	Definition
ALS	ambient light sensing
AWB	auto white balance
CCT	correlated color temperature
CWL	central wavelength
ESD	electrostatic discharge
FFT	fast Fourier transform
FoV	field of view
FWHM	full width at half maximum
I²C	inter-integrated circuit (serial bus)
PCB	printed circuit board
PDM	pulse density modulation
RMS	root mean square
UBM	under bump metallurgy
VCSEL	Vertical-cavity surface-emitting laser

Revision history

Table 30. **Document revision history**

Date	Version	Changes
21-May-2021	1	Initial release
25-Mar-2024	2	Added flicker digital mode (also replaced VD6283 with VD6283TX throughout the document). Updated the following: Features, Applications, Description, Device summary, Table 3. Key functional parameters, Table 4. Ball description, the title of Figure 5. Application schematic, ALS, and flicker in analog format (mode 2), Section 3.3: Operating modes, Section 3.3.4: Saturation, Section 3.3.5: AC light flicker extraction, Section 3.3.6: Flicker mapping configuration, Section 4.3.21: AC mode control register, Section 6: Electrical characteristics, Section 7: ALS and flicker performances, Section 9: Outline drawings, Section 10.5: PCB layout and stencil drawing, and Table 29. Acronyms and abbreviations. Added Figure 4. Application schematic, ALS, and flicker in digital PDM format (mode 1), Section 3.5: Pulse density modulation (PDM) interface, and Section 10.4: Solder ball information.

Contents

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