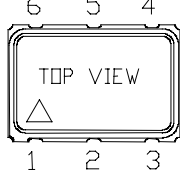




VDSGLD @ 38.88 MHz

Voltage Controlled Crystal Oscillator

Pin Information

Table 1. Pin Function			
Pin	Symbol	Function	
1	V_C	Control Voltage	
2	Tri-State	TTL logic low disables output TTL logic high enables output waveform	
3	GND	Case Ground	
4	Output	Output waveform	
5	TTL/CMOS	TTL logic low for CMOS optimized symmetry TTL logic high or no connection for TTL optimized symmetry	
6	V_{CC}	Power Supply Voltage (3.3 V $\pm 10\%$)	

Performance Characteristics

Table 2. Electrical Performance					
Parameter	Symbol	Minimum	Typical	Maximum	Units
Nominal Output Frequency	f_0	-	38.88	-	MHz
Supply Voltage ¹	V_{DD}	2.97	3.3	3.63	V
Operating Temperature Range	T_O	-40		85	$^{\circ}\text{C}$
Supply Current	I_{DD}			20	mA
Output Voltage Levels Output Logic High Output Logic Low	V_{OH} V_{OL}	$0.9 \cdot V_{DD}$		$0.1 \cdot V_{DD}$	V
Output Rise/Fall Time ²	T_R/T_F			5	nS
Output Duty Cycle or Symmetry ³	D	45	50	55	%
Absolute Pull Range, $V_C = 1.0$ to 2.0 V	APR	± 5			ppm
Absolute Pull Range, $V_C = 0.3$ to 3.0 V	APR	± 50			ppm
Initial Accuracy ($V_C = 1.65\text{V}$ @ 25°C)		-20		+20	ppm
Linearity				20	%
Start up time (To reach 90% of final amplitude)				10	ms
Control Voltage Input Impedance		10			$\text{M}\Omega$
Control Voltage Leakage Current				100	nA
Control Voltage Bandwidth (-3 dB, $V_C = 1.65$ V)	BW	10			KHz
Output Load				15	pf

1. A $0.1 \mu\text{F}$ low frequency tantalum bypass capacitor in parallel with a $0.01 \mu\text{F}$ high frequency ceramic capacitor is recommended.

2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions.

3. Duty cycle is defined as (on time/period) per Figure 1.

4. Maximum control Voltage Leakage Current is by design.

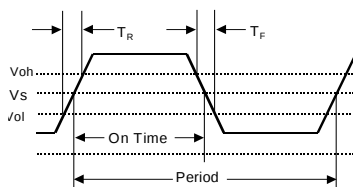


Figure 1. Output Waveform

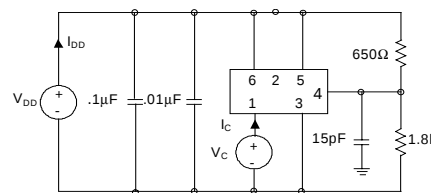


Figure 2. Output Test Conditions (25 $\pm$ 5 $^{\circ}\text{C}$)

Outline Diagram

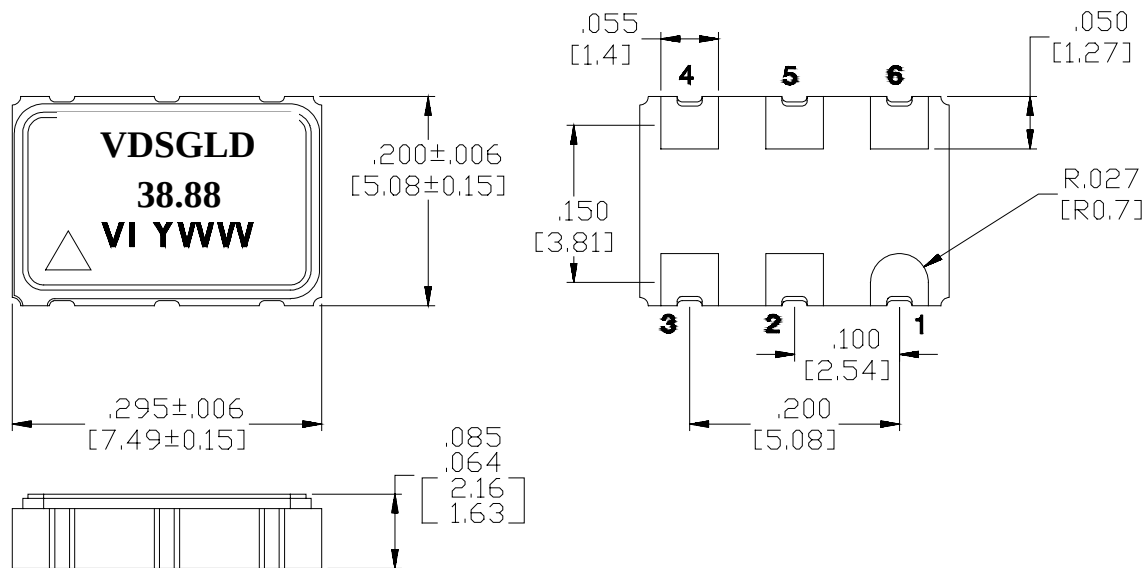


Figure 3. Outline Diagram

Table 3. Ordering Information

V	D	S	G	L	D	38.88
Package	Supply Voltage (V)	Oscillator Type & Special Requirements	APR	Operating Temperature	Duty Cycle Min/Max	Frequency (MHz)
6 Pin Ceramic Leadless Chip Carrier	3.3 ± 10%	Initial Accuracy Vc = 1.65V @ 25°C	±50ppm	-40°C to +85°C	45/55% Tri-State on Pin # 2	Nominal Output Frequency

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