4-Line (Quad) ESD Protection Diode Array in LLP1010-6L

Features

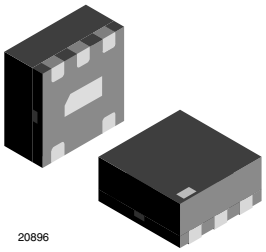
- Ultra compact LLP1010-6L package
- Low package height < 0.4 mm
- 4-line ESD protection (quad)
- Low leakage current < 0.1 µA
- Low load capacitance C_D = 6 pF
- ESD-protection acc. IEC 61000-4-2
  - ± 8 kV contact discharge
  - ± 10 kV air discharge
- Surge current acc. IEC 6100-4-5 I_{PP} > 1.5 A
- Soldering can be checked by standard vision inspection. No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- Compliant to RoHS directive 2002/95/EC and in accordance to WEEE 2002/96/EC

Pb-free

e4

RoHS COMPLIANT

GREEN (5-2008)**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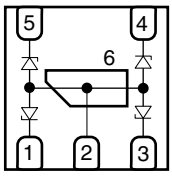

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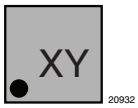
Marking (example only)



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Dot = Pin 1 marking
X = Date code
Y = Type code (see table below)

Ordering Information

Device name	Ordering code	Taped units per reel (8 mm tape on 7" reel)	Minimum order quantity
VESD09A4A-HS4	VESD09A4A-HS4-GS08	5000	5000

Package Data

Device name	Package name	Type code	Weight	Molding compound flammability rating	Moisture sensitivity level	Soldering conditions
VESD09A4A-HS4	LLP1010-6L	B	1.07 mg	UL 94 V-0	MSL level 1 (according J-STD-020)	260 °C/10 s at terminals

** Please see document “Vishay Material Category Policy”: www.vishay.com/doc?99902

Absolute Maximum Ratings

Rating	Test conditions		Symbol	Value	Unit
Peak pulse current	BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot		I_{PPM}	1.5	A
Peak pulse power	BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; t_p = 8/20 µs; single shot		P_{PP}	30	W
ESD immunity	Acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6)	Contact discharge	V_{ESD}	± 8	kV
		Air discharge	V_{ESD}	± 10	kV
Operating temperature	Junction temperature		T_J	- 40 to + 125	°C
Storage temperature			T_{STG}	- 55 to + 150	°C

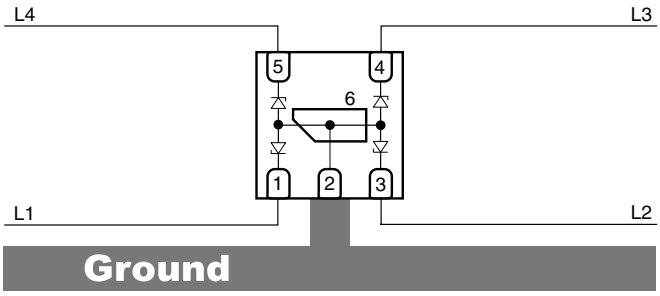
BiAs-Mode (4-line Bidirectional Asymmetrical protection mode)

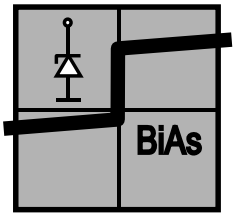
With the **VESD09A4A-HS4** up to 4 signal- or data-lines (L1 to L4) can be protected against voltage transients. With pin 2 and 6 connected to ground and pin 1, 3, 4 and 5 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified **M**aximum **R**everse **W**orking **V**oltage (V_{RWM}) the protection diode between data line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The **C**lamping **V**oltage (V_C) is defined by the **BR**eakthrough **V**oltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low **F**orward **V**oltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the **VESD09A4A-HS4** clamping behaviour is **Bi**directional and **As**ymmetrical (**BiAs**).





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Electrical Characteristics

Ratings at 25 °C, ambient temperature unless otherwise specified

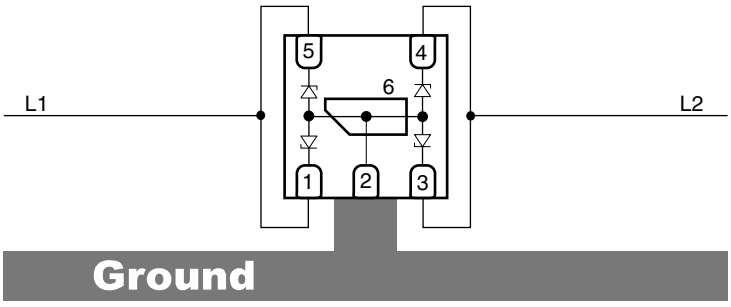
VESD09A4A-HS4

BiAs mode: each input (pin 1, 3, 4 and 5) to ground (pin 2 and/or 6)

Parameter	Test conditions/remarks	Symbol	Min.	Typ.	Max.	Unit
Protection paths	Number of line which can be protected	N_{lines}			4	lines
Reverse stand-off voltage	at I_R = 0.1 µA	V_{RWM}	9			V
Reverse current	at $V_R = V_{RWM}$ = 9 V	I_R		< 0.01	0.1	µA
Reverse breakdown voltage	at I_R = 1 mA	V_{BR}	11.2		13	V
Clamping voltage	at I_{PP} = 1.5 A acc. IEC 61000-4-5	V_C			23	V
Forward clamping voltage	at I_F = 1.5 A acc. IEC 61000-4-5	V_F			2	V
Capacitance	at V_R = 0 V; f = 1 MHz	C_D		6.2	10	pF
	at V_R = 4.5 V; f = 1 MHz	C_D		3.2	4	pF

If a higher surge current or peak pulse current (I_{PP}) is needed, some protection diodes in the **VESD09A4A-HS4** can also be used in parallel in order to "multiply" the performance.
If two diodes are switched in parallel you get

- double surge power = double peak pulse current (2 x I_{PPM})
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line Capacitance (2 x C_D)
- double Reverse leakage current (2 x I_R)



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Typical Characteristics (T_{amb} = 25 °C, unless otherwise specified)

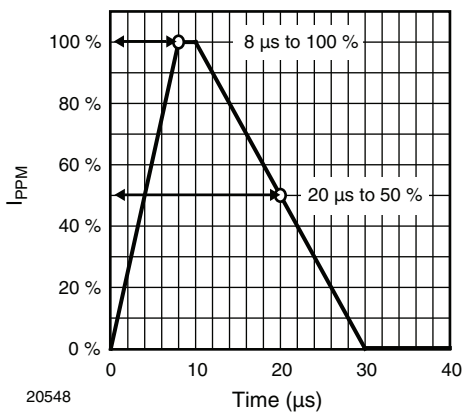


Figure 1. 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

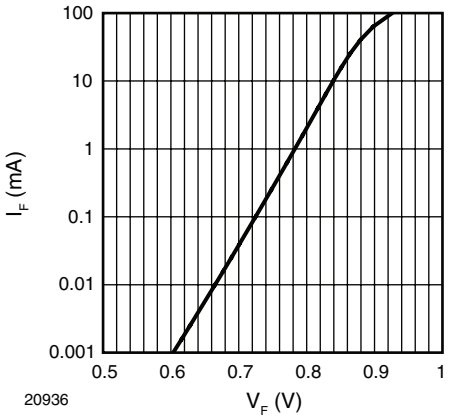


Figure 4. Typical Forward Current I_F vs. Forward Voltage V_F

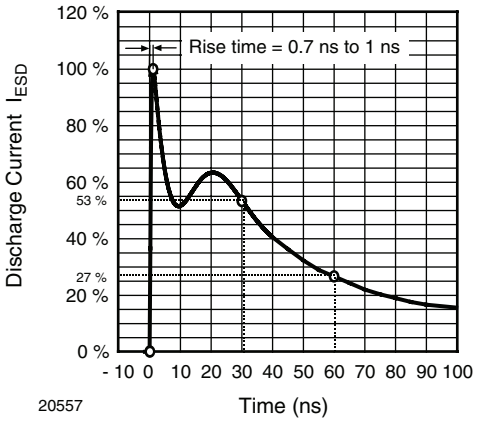


Figure 2. ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω/150 pF)

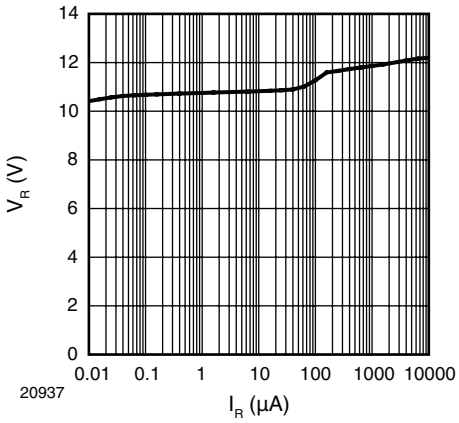


Figure 5. Typical Reverse Voltage V_R vs. Reverse Current I_R

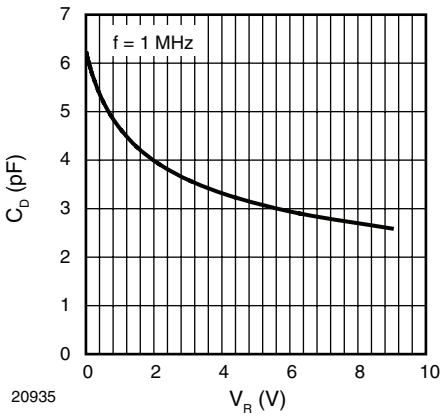


Figure 3. Typical Capacitance C_D vs. Reverse Voltage V_R

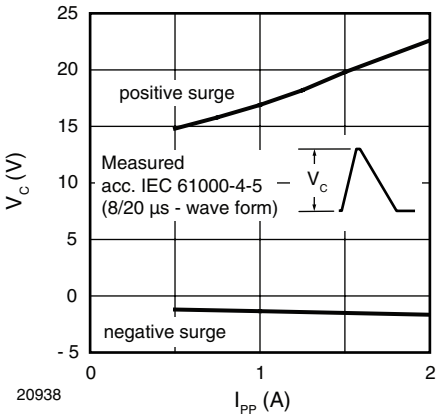


Figure 6. Typical Peak Clamping Voltage V_C vs. Peak Pulse Current I_{PP}

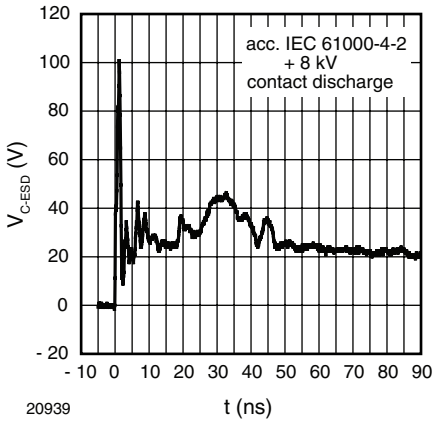


Figure 7. Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

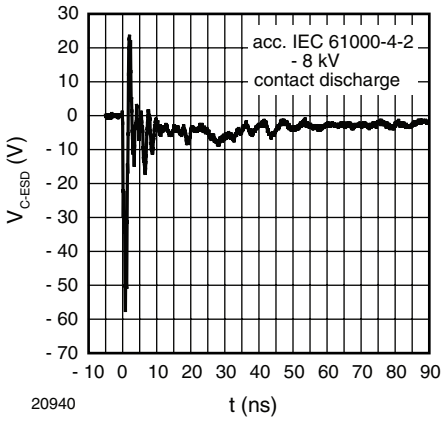


Figure 8. Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

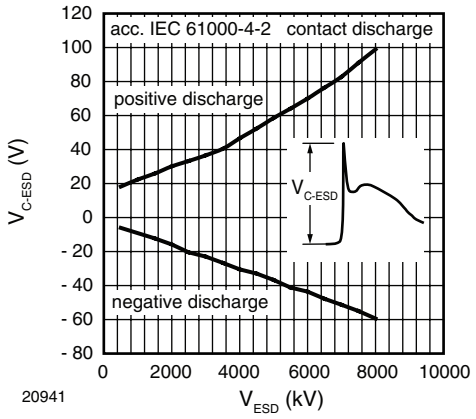
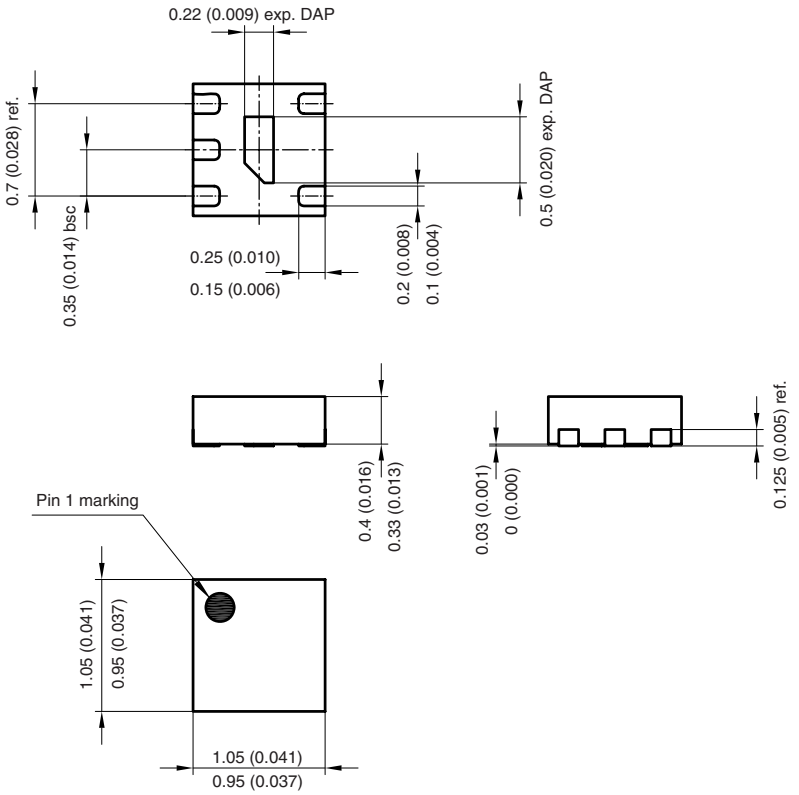
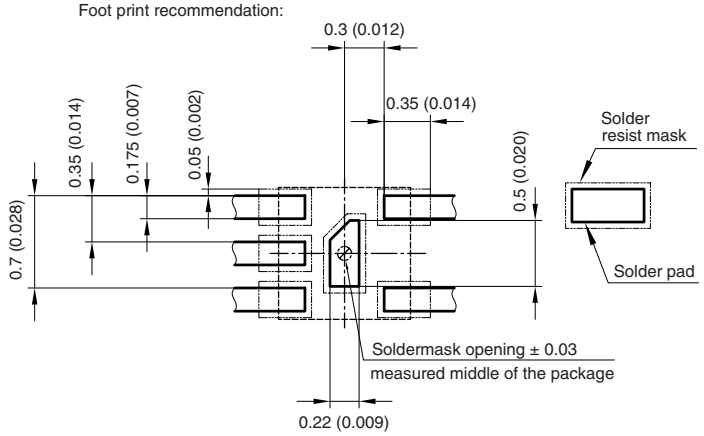


Figure 9. Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

Package Dimensions in millimeters (inches): LLP1010-6L



Foot print recommendation:



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