Description

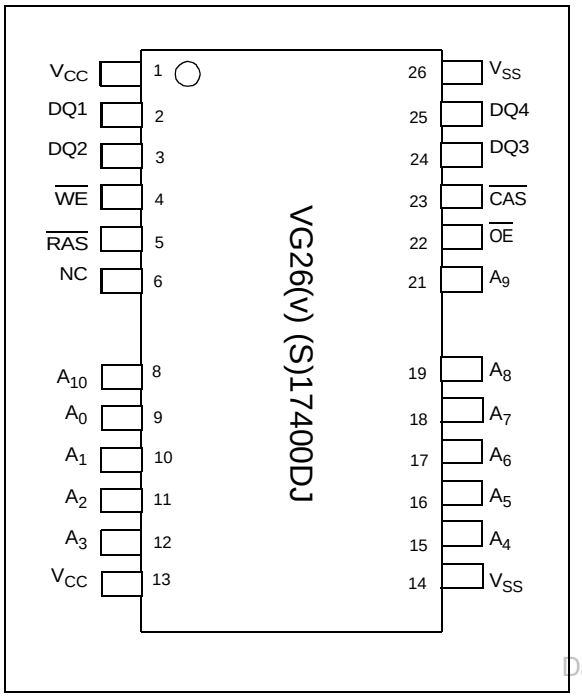
The device is CMOS Dynamic RAM organized as 4,194,304 words x 4 bits. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 5V only or 3.3V only power supply. Low voltage operation is more suitable to be used on battery backup, portable electronic application. A new refresh feature called " self-refresh " is supported and very slow CBR cycles are being performed. It is packaged in JEDEC standard 26/24 - pin plastic SOJ or TSOP (II).

Features

- Single 5V (±10 %) or 3.3V (±10 %) only power supply
- High speed t_{RAC} access time : 50/60 ns
- Low power dissipation
  - Active mode : 5V version 605/550 mW (Max.)
    3.3V version 396/360 mW (Max.)
  - Standby mode : 5V version 1.375 mW (Max.)
    3.3V version 0.54 mW (Max.)
- Fast Page Mode access
- I/O level : TTL compatible (Vcc = 5V)
  LVTTL compatible (Vcc = 3.3V)
- 2048 refresh cycles in 32 ms (Std) or 128ms (S - version)
- 4 refresh mode :
  - $\overline{RAS}$ only refresh
  - $\overline{CAS}$-before-$\overline{RAS}$ refresh
  - Hidden refresh
  - Self - refresh (S - version)

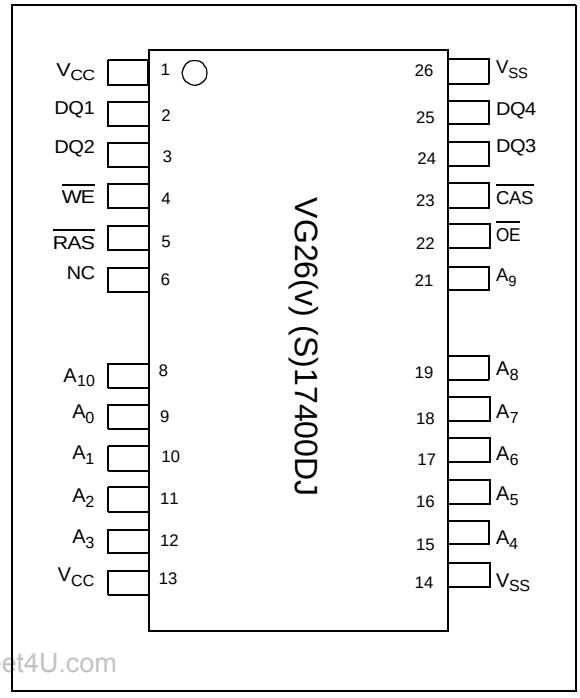
Pin configuration

26/24 - PIN 300mil Plastic SOP



Pin configuration

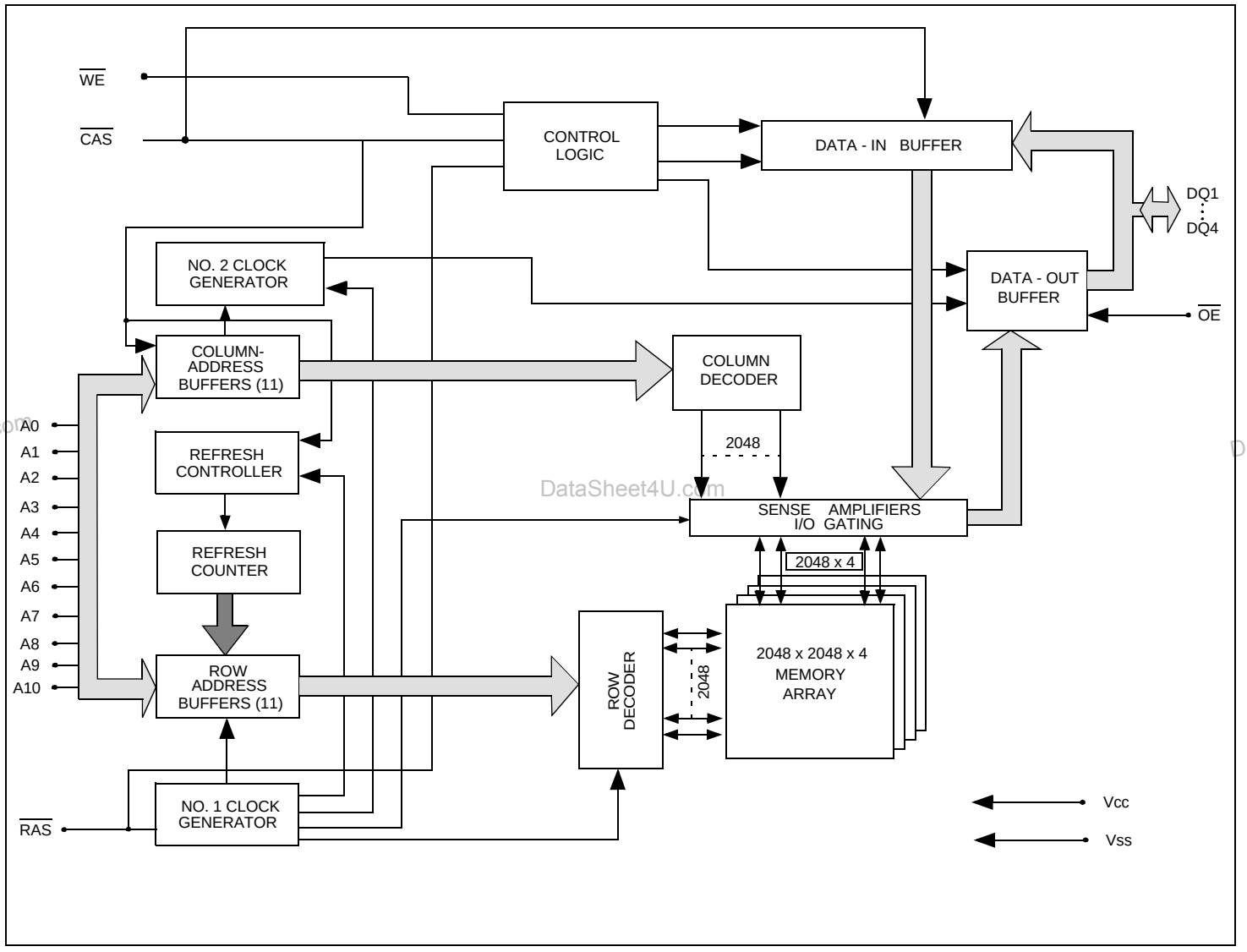
26/24 - PIN 300mil Plastic TSOP (II)



Pin Description

Pin Name	Function
A0 - A10	Address inputs - Row address A0 - A10 - Column address A0 - A10 - Refresh address A0 - A10
DQ1 ~ DQ4	Data - in/data - out
$\overline{RAS}$	Row address strobe
$\overline{CAS}$	Column address strobe
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
V_{cc}	Power (+ 5V or + 3.3V)
V_{ss}	Ground

Block Diagram



Truth Table

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES ROW	ADDRESSES COL	DQ_S	Notes
STANDBY		H	H → X	X	X	X	X	High - Z	
READ		L	L	H	L	ROW	COL	Data - Out	
WRITE : (EARLY WRITE)		L	L	L	X	ROW	COL	Data - In	
READ WRITE		L	L	H → L	L → H	ROW	COL	Data - Out, Data - In	
PAGE - MODE READ	1st Cycle	L	H → L	H	L	ROW	COL	Data - Out	
	2st Cycle	L	H → L	H	L	n/a	COL	Data - Out	
PAGE - MODE WRITE	1st Cycle	L	H → L	L	X	ROW	COL	Data - In	
	2st Cycle	L	H → L	L	X	n/a	COL	Data - In	
PAGE - MODE READ - WRITE	1st Cycle	L	H → L	H → L	L → H	ROW	COL	Data - Out, Data - In	
	2st Cycle	L	H → L	H → L	L → H	n/a	COL	Data - Out, Data - In	
HIDDEN REFRESH	READ	L → H → L	L	H	L	ROW	COL	Data - Out	
	WRITE	L → H → L	L	L	X	ROW	COL	Data - In	1
$\overline{RAS}$ - ONLY REFRESH		L	H	X	X	ROW	n/a	High - Z	
CBR REFRESH		H → L	L	H	X	X	X	High - Z	

Notes : 1. EARLY WRITE only.

Absolute Maximum Rating

Parameter		Symbol	Value	Unit
Voltage on any pin relative to Vss	5V 3.3V	V_T	-1.0 to + 7.0 -0.5 to + 4.6	V
Supply voltage relative to Vss	5V 3.3V	V_{cc}	-1.0 to + 7.0 -0.5 to + 4.6	V
Short circuit output current		I_{OUT}	50	mA
Power dissipation		P_D	1.0	W
Operating temperature		T_{OPT}	0 to + 70	°C
Storage temperature		T_{STG}	-55 to + 125	°C

Recommended DC Operating Conditions

Parameter/Condition	Symbol	5 Volt Version			3.3 Volt Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V_{cc}	4.5	5.0	5.5	3.0	3.3	3.6	V
Input High Voltage, all inputs	V_{IH}	2.4	-	V_{CC} + 1.0	2.0	-	V_{CC} + 0.3	V
Input Low Voltage, all inputs	V_{IL}	-1.0	-	0.8	-0.3	-	0.8	V

Capacitance

Ta = 25°C, V_{CC} = 5V±10% or 3.3V±10 %, f = 1MHz

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C_{I1}	-	5	pF	1
Input capacitance (RAS, CAS, OE, WE)	C_{I2}	-	7	pF	1
Output capacitance (Data - in, Data - out)	$C_{I/O}$	-	7	pF	1,2

Note : 1. Capacitance measured with effective capacitance measuring method.
2. $\overline{CAS}$ = V_{IH} to disable Dout.

DC Characteristics; 5 - Volt verion

(T_a= 0 to 70°C, V_{CC} = + 5V±10%, V_{ss} = 0V)

Parameter		Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
				-5		-6			
				Min	Max	Min	Max		
Operating current		I_{CC1}	$\overline{RAS}$ cycling $\overline{CAS}$ cycling t_{RC} = min.	-	110	-	100	mA	1, 2
Standby Current	Low power S - version	I_{CC2}	TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} - 0.2V Dout = high - Z	-	0.25	-	0.25	mA	
	Standard power version		TTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} - 0.2V Dout = high - Z	-	1	-	1	mA	
$\overline{RAS}$ - only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min.	-	110	-	100	mA	1, 2
Fast page mode current		I_{CC4}	t_{PC} = min.	-	80	-	70	mA	1,3
$\overline{CAS}$ - before - $\overline{RAS}$ refresh current		I_{CC5}	t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling	-	110	-	100	mA	1, 2
Self - refresh currant (S - Version)		I_{CC8}	t_{RASS} ≥ 100µS	-	350	-	350	µA	
$\overline{CAS}$ - before - $\overline{RAS}$ long refresh current (S - Version)		I_{CC9}	Standby : V_{CC} - 0.2V ≤ $\overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 2048 cycles/128ms $\overline{RAS}$, $\overline{RAS}$: 0V ≤ V_{IL} ≤ 0.2V V_{CC} - 0.2V ≤ V_{IH} ≤ V_{IH} (Max) Dout = high - Z, t_{RAS} ≤ 300ns	-	500	-	500	µA	

DC Characteristics ; 5 - Volt Version (cont.)

(T_a = 0 to 70°C, V_{CC} = + 5V±10%, V_{ss} = 0V)

Parameter	Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Input leakage current	I_{LI}	$0V \le Vin \le V_{CC}$ + 0.5V	-5	5	-5	5	µA	
Output leakage current	I_{LO}	$0V \le Vout \le V_{CC}$ + 0.5V Dout = Disable	-5	5	-5	5	µA	
Output high voltage	V_{OH}	I_{OH} = -5mA	2.4	-	2.4	-	V	
Output low voltage	V_{OL}	I_{OL} = + 4.2mA	-	0.4	-	0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. For I_{CC4}, address can be changed once or less within one Fast page mode cycle time.

DC Characteristics ; 3.3 - Volt Verion

(T_a = 0 to 70°C, V_{CC} = + 3.3V±10%, V_{ss} = 0V)

Parameter		Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
				-5		-6			
				Min	Max	Min	Max		
Operating current		I_{CC1}	$\overline{RAS}$ cycling $\overline{CAS}$ cycling t_{RC} = min.	-	110	-	100	mA	1, 2
Standby Current	Low power S - version	I_{CC2}	LVTTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = high - Z	-	0.5	-	0.5	mA	
			CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} - 0.2V Dout = high - Z	-	0.25	-	0.25	mA	
	Standard power version		LVTTL interface $\overline{RAS}$, $\overline{CAS}$ = V_{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface $\overline{RAS}$, $\overline{CAS}$ ≥ V_{CC} - 0.2V Dout = high - Z	-	0.5	-	0.5	mA	
$\overline{RAS}$ - only refresh current		I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IH} t_{RC} = min.	-	110	-	100	mA	1, 2
Fast page mode current		I_{CC4}	t_{PC} = min.	-	80	-	70	mA	1,3
$\overline{CAS}$ - before - $\overline{RAS}$ refresh current		I_{CC5}	t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling	-	110	-	100	mA	1, 2
Self - refresh currant (S - Version)		I_{CC8}	t_{RASS} ≥ 100µS	-	250	-	250	µA	
$\overline{CAS}$ - before - $\overline{RAS}$ long refresh current (S - Version)		I_{CC9}	Standby : V_{CC} - 0.2V ≤ $\overline{RAS}$ $\overline{CAS}$ before $\overline{RAS}$ refresh : 2048 cycles/128ms $\overline{RAS}$, $\overline{RAS}$: 0V ≤ V_{IL} ≤ 0.2V V_{CC} - 0.2V ≤ V_{IH} ≤ V_{IH} (Max) Dout = high - Z, t_{RAS} ≤ 300ns	-	300	-	300	µA	

DC Characteristics ; 3.3 - Volt Version (cont.)

(T_a = 0 to 70°C, V_{CC} = + 3.3V±10%, V_{SS}= 0V)

Parameter	Symbol	Test Conditions	VG26 (V) (S) 17400D				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Input leakage current	I_{LI}	$0V \le Vin \le V_{CC}$ + 0.3V	-5	5	-5	5	µA	
Output leakage current	I_{LO}	$0V \le Vout \le V_{CC}$ + 0.3V Dout = Disable	-5	5	-5	5	µA	
Output high voltage	V_{OH}	I_{OH} = -2mA	2.4	-	2.4	-	V	
Output low voltage	V_{OL}	I_{OL} = + 2mA	-	0.4	-	0.4	V	

Notes :

1. I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. For I_{CC4}, address can be changed once or less within one Fast page mode cycle time.

AC Characteristics

(Ta = 0 to + 70°C, V_{CC} = 5V±10% or 3.3V±10%, V_{SS} = 0V) * 1, * 2, * 3, * 4

Test conditions

- Output load : two TTL Loads and 100pF(V_{CC} = 5.0V±10%)

  one TTL Load and 100pF(V_{CC} = 3.3V±10%)
- Input timing reference levels :

  V_{IH} = 2.4V, V_{IL} = 0.8V (V_{CC} = 5.0V±10%); V_{IH} = 2.0V, V_{IL} = 0.8V (V_{CC} = 3.3V±10%)
- Output timing reference levels :

  V_{OH} = 2.0V, V_{OL} = 0.8V (V_{CC} = 5V±10%, 3.3V±10%)

Read, Write, Read - Modify - Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	90	-	110	-	ns	
$\overline{RAS}$ precharge time	t_{RP}	30	-	40	-	ns	
$\overline{CAS}$ precharge time in normal mode	t_{CPN}	10	-	10	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	50	10000	60	10000	ns	5
$\overline{CAS}$ pulse width	t_{CAS}	12	10000	15	10000	ns	6
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	8	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	7
Column address hold time	t_{CAH}	8	-	10	-	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	12	37	14	45	ns	8
$\overline{RAS}$ to column address delay time	t_{RAD}	10	25	12	30	ns	9
Column address to $\overline{RAS}$ lead time	t_{RAL}	25	-	30	-	ns	
$\overline{RAS}$ hold time	t_{RSH}	13	-	15	-	ns	
$\overline{CAS}$ hold time	t_{CSH}	50	-	60	-	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	-	5	-	ns	10
$\overline{OE}$ to Din delay time	t_{OED}	12	-	15	-	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	11
Refresh period	t_{REF}	-	32	-	32	ms	
Refresh period (S - Version)	t_{REF}	-	128	-	128	ms	
$\overline{CAS}$ to output in Low-Z	t_{CLZ}	0	-	0	-	ns	
$\overline{CAS}$ delay time from Din	t_{DZC}	0	-	0	-	ns	
$\overline{OE}$ delay time from Din	t_{DZO}	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Access time from $\overline{RAS}$	t_{RAC}	-	50	-	60	ns	12
Access time from $\overline{CAS}$	t_{CAC}	-	13	-	15	ns	13,14
Access time from column address	t_{AA}	-	25	-	30	ns	14,15
Access time from $\overline{OE}$	t_{OEA}	-	13	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	7
Read command hold time to $\overline{CAS}$	t_{RCH}	0	-	0	-	ns	10,16
Read command hold time to $\overline{RAS}$	t_{RRH}	0	-	0	-	ns	16
Output buffer turn-off time	t_{OFF}	0	13	0	15	ns	17
Output buffer turn-off time from $\overline{OE}$	t_{OEZ}	0	13	0	15	ns	17

Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	ns	7,18
Write command hold time	t_{WCH}	8	-	10	-	ns	
Write command pulse width	t_{WP}	8	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	-	15	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	8	-	10	-	ns	
Data-in setup time	t_{DS}	0	-	0	-	ns	19
Data-in hold time	t_{DH}	8	-	10	-	ns	19

Read - Modigy - Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Read - modify - write cycle time	t_{RWC}	125	-	150	-	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	65	-	80	-	ns	18
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	30	-	35	-	ns	18
Column address to $\overline{WE}$ delay time	t_{AWD}	40	-	50	-	ns	18
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	8	-	10	-	ns	

Refresh Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
$\overline{CAS}$ setup time (CBR refresh)	t_{CSR}	10	-	10	-	ns	
$\overline{CAS}$ hold time (CBR refresh)	t_{CHR}	10	-	10	-	ns	10
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	5	-	5	-	ns	7
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	-	100	-	µs	
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	90	-	110	-	ns	
$\overline{CAS}$ hold time (CBR self refresh)	t_{CHS}	-50	-	-50	-	ns	
$\overline{WE}$ setup time	t_{WSR}	0	-	0	-	ns	
$\overline{WE}$ hold time	t_{WHR}	10	-	10	-	ns	

Fast Page Mode Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	35	-	40	-	ns	
Fast page mode $\overline{CAS}$ Precharge time	t_{CP}	10	-	10	-	ns	
Fast page mode $\overline{RAS}$ pulse width	t_{RASP}	50	10^5	60	10^5	ns	20
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	30	-	35	ns	10,14
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	30	-	35	-	ns	

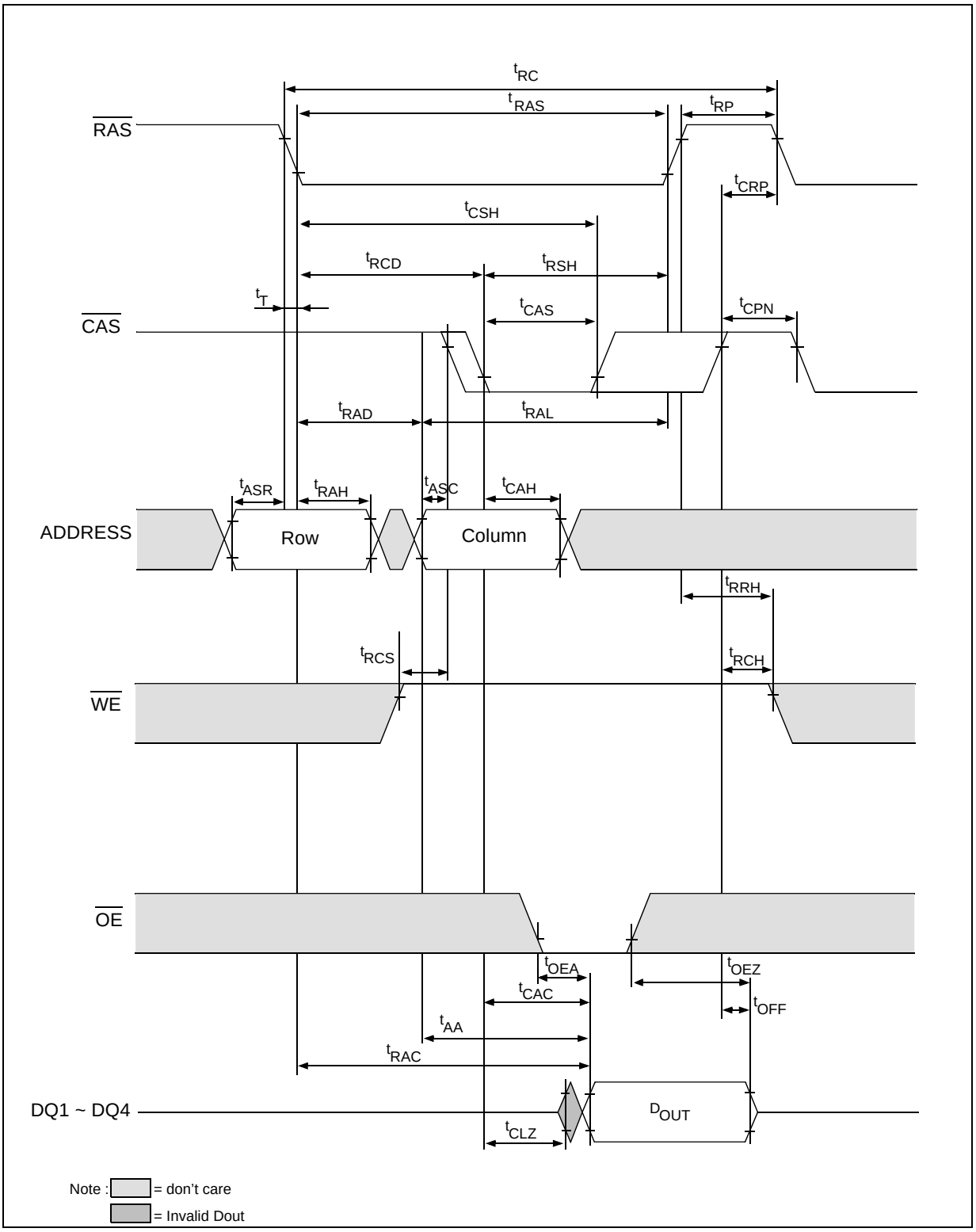
Fast Page Mode Read Modify Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400D				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Fast page mode read - modify - write cycle $\overline{CAS}$ precharge to $\overline{WE}$ delay time	t_{CPW}	45	-	55	-	ns	11
Fast page mode read - modify - write cycle time	t_{PRWC}	70	-	80	-	ns	

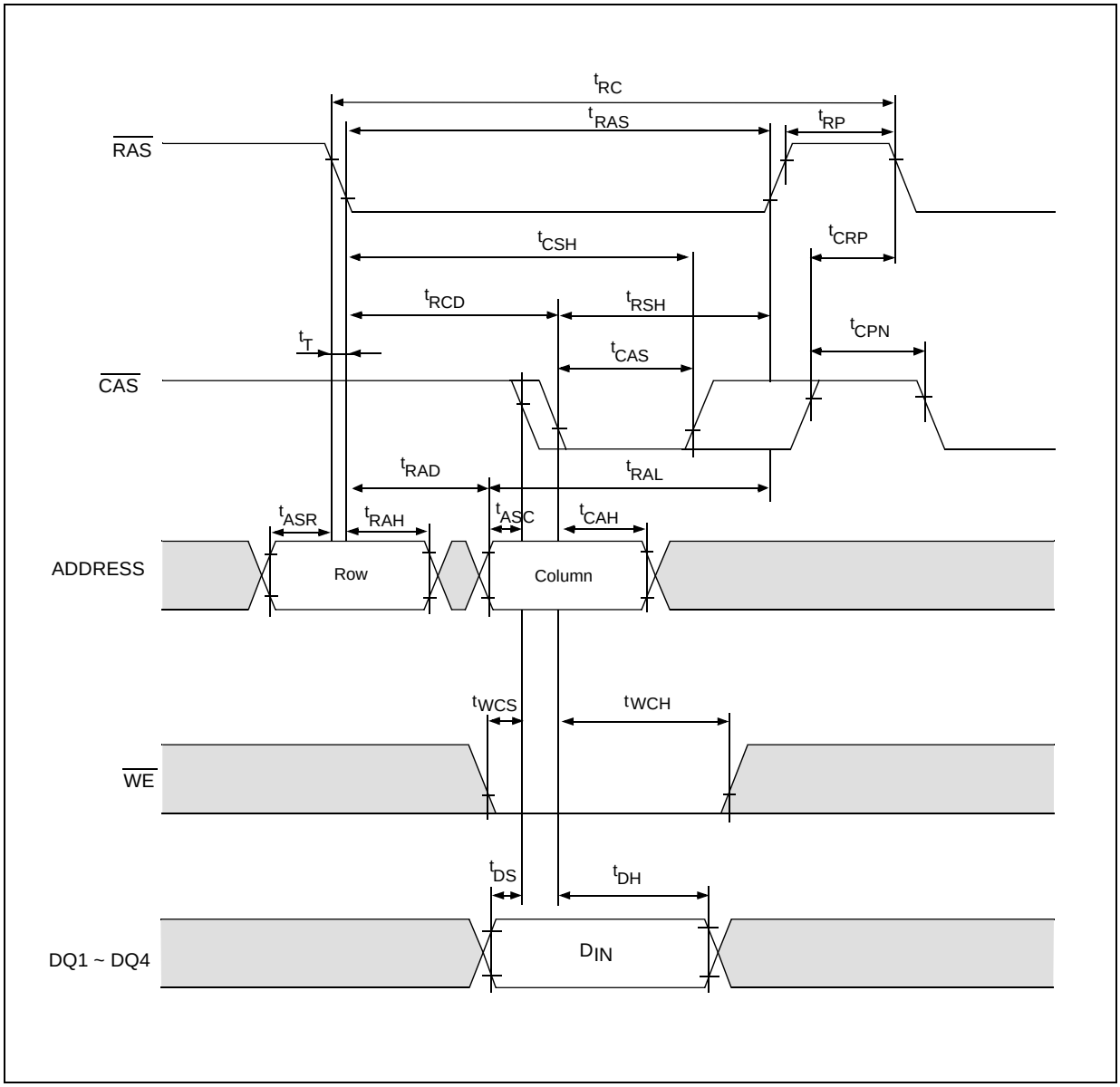
Notes :

1. AC measurements assume t_T = 5ns.
2. An initial pause of 100 μs is required after power up, and it followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
4. All the V_{CC} and V_{SS} pins shall be supplied with the same voltage.
5. $t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T$ in read - modify-write cycle.
6. $t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T$ in read - modify-write cycle.
7. $t_{ASC}(min)$, $t_{RCS}(min)$, $t_{WCS}(min)$ and t_{RPC} are determined by the falling edge of $\overline{CAS}$.
8. $t_{RCD}(max)$ is specified as a reference point only, and $t_{RAC}(max)$ can be met with the $t_{RCD}(max)$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{CAC} if t_{RCD} is greater than the specified $t_{RCD}(max)$ limit.
9. $t_{RAD}(max)$ is specified as a reference point only, and $t_{RAC}(max)$ can be met with the $t_{RAD}(max)$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{AA} if t_{RAD} is greater than the specified $t_{RAD}(max)$ limit.
10. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the rising edge of $\overline{CAS}$.
11. $V_{IH}(min)$ and $V_{IL}(max)$ are reference levels for measuring timing or input signals. Therefore, transition time is measured between V_{IH} and V_{IL}.
12. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
13. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
14. Access time is determined by the maximum among t_{AA}, t_{CAC}, t_{CPA}.
15. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. $t_{OFF}(max)$ and $t_{OEZ}(max)$ define the time at which the output achieves the open circuit condition (high impedance).
18. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(min)$, the cycle is an early write cycle and the data output will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}(min)$, $t_{CWD} \geq t_{CWD}(min)$, $t_{AWD} \geq t_{AWD}(min)$, and $t_{CPW} \geq t_{CPW}(min)$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
19. These parameters are referenced to $\overline{CAS}$ in an early write cycle and to $\overline{WE}$ edge in a delayed write or a read-modify-write cycle.
20. t_{RASP} defines $\overline{RAS}$ pulse width in Fast page mode cycles.

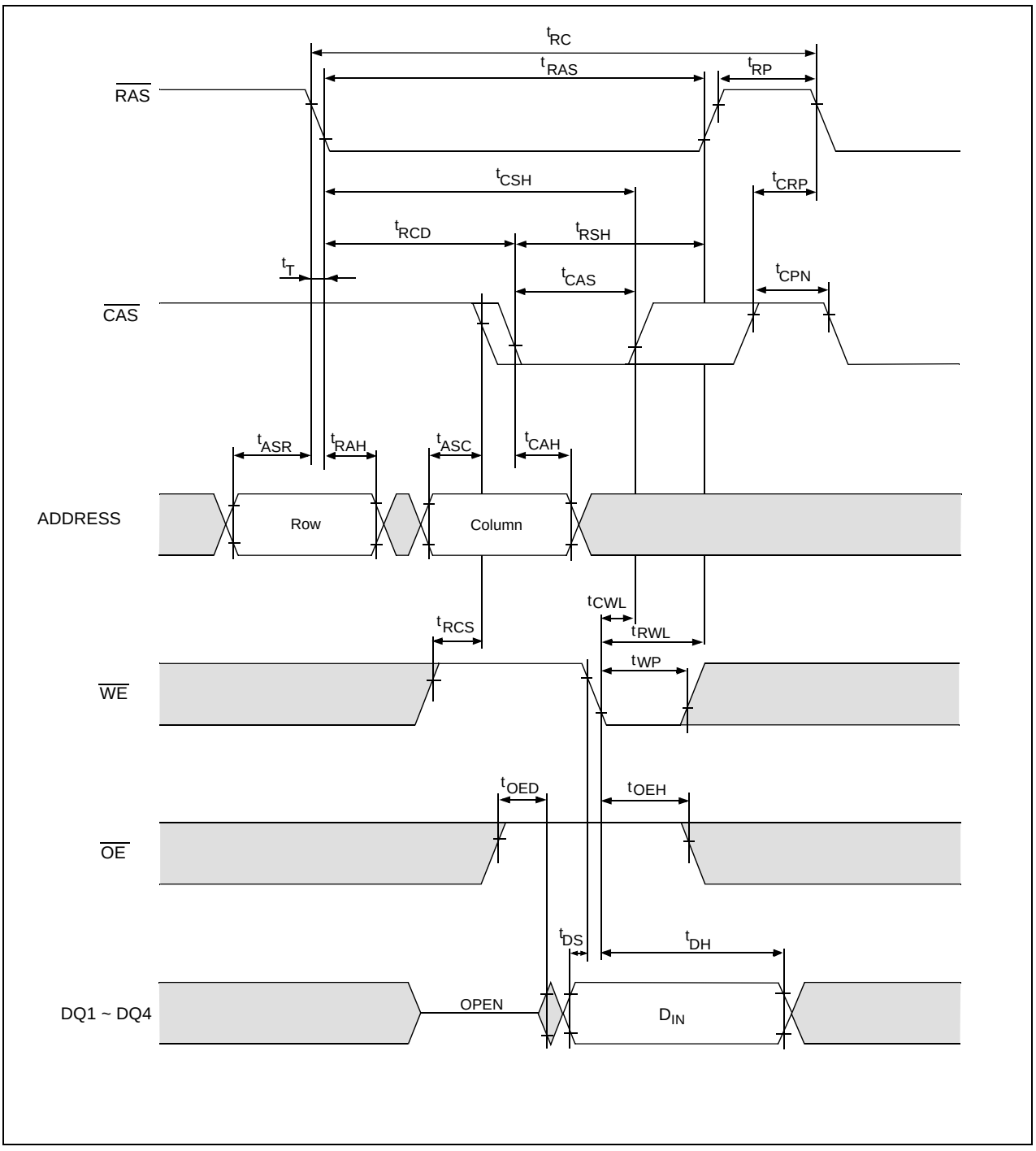
Timing Waveforms
• Read Cycle



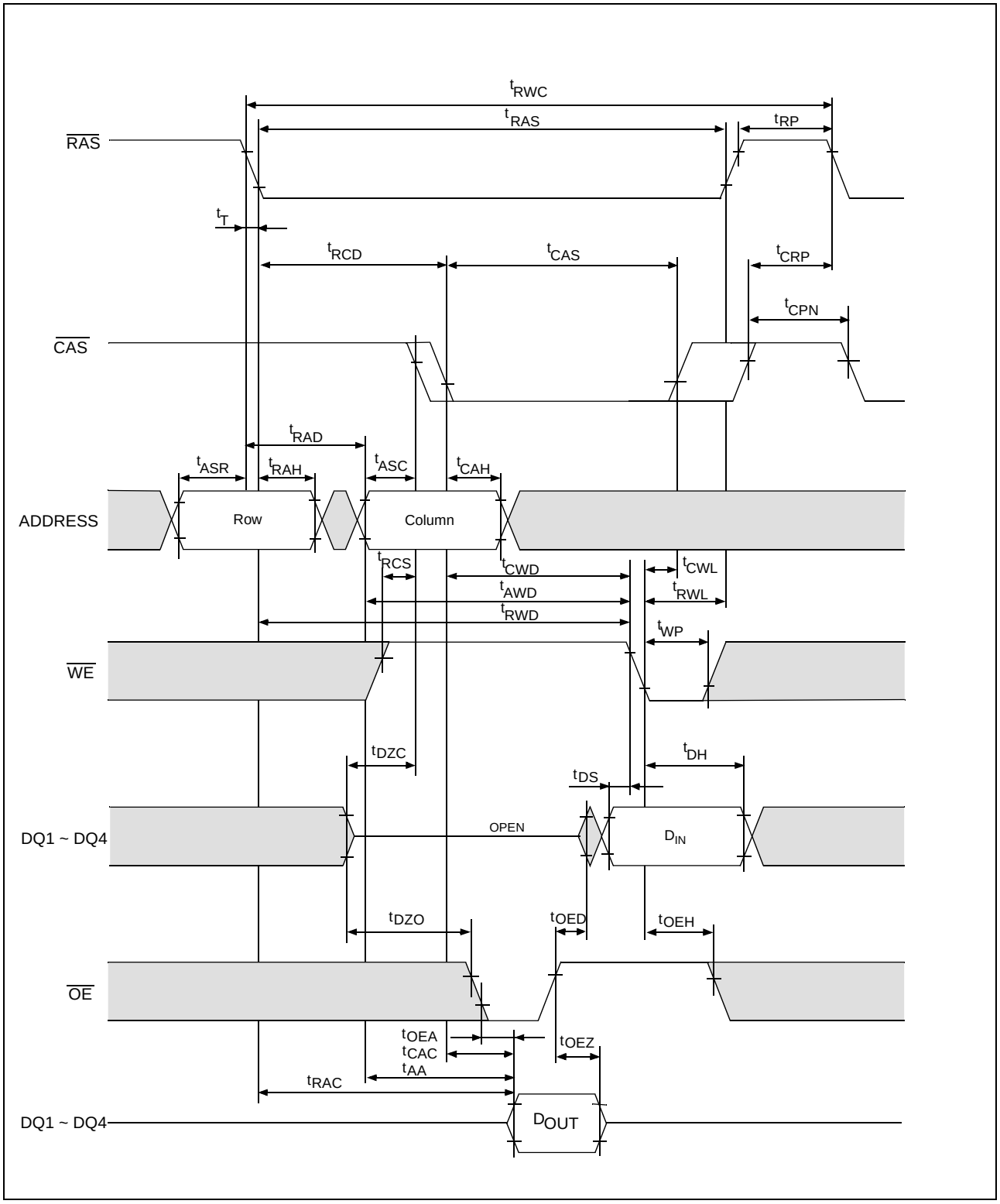
•Early Write Cycle



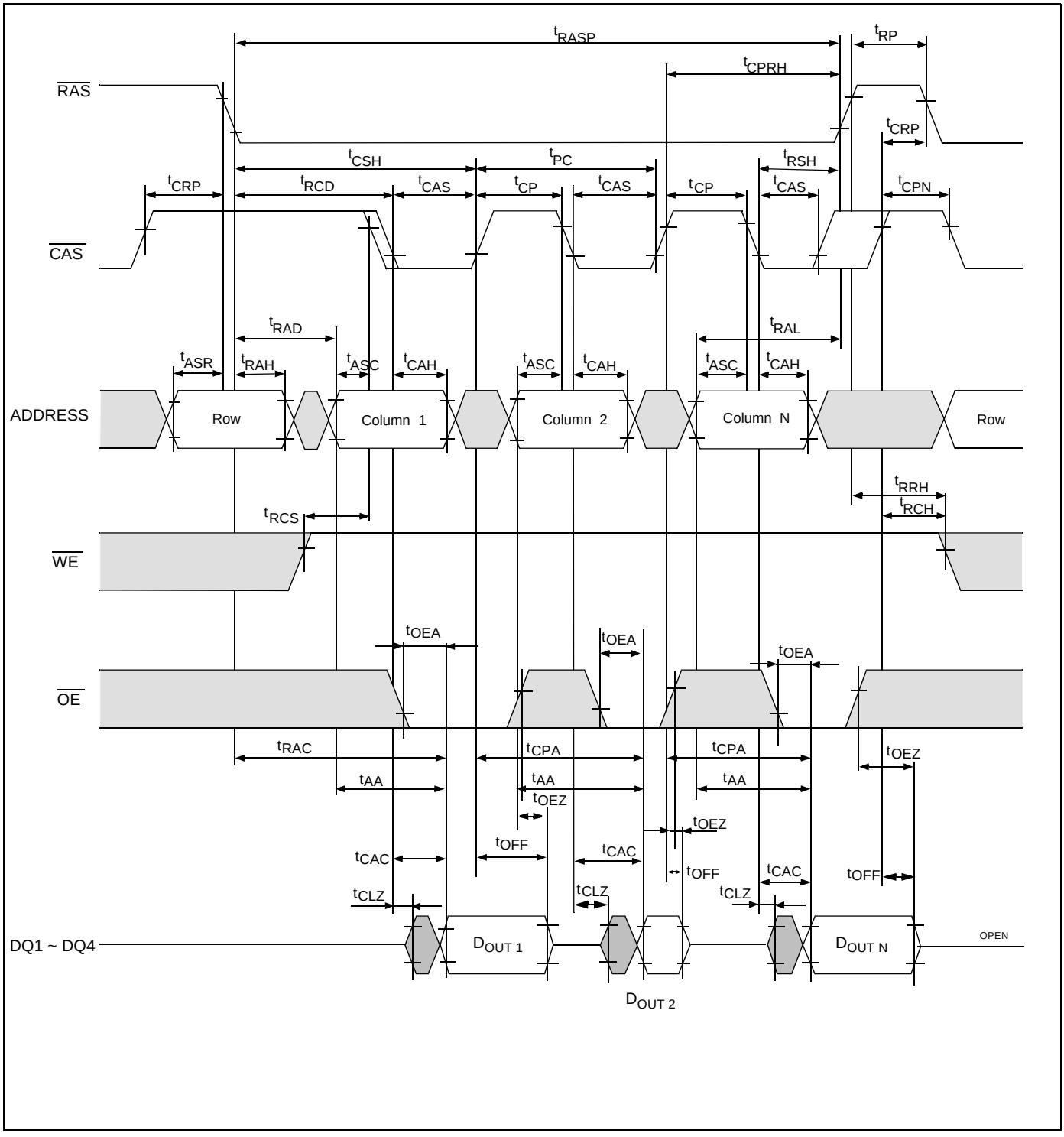
• **Delayed Write Cycle**



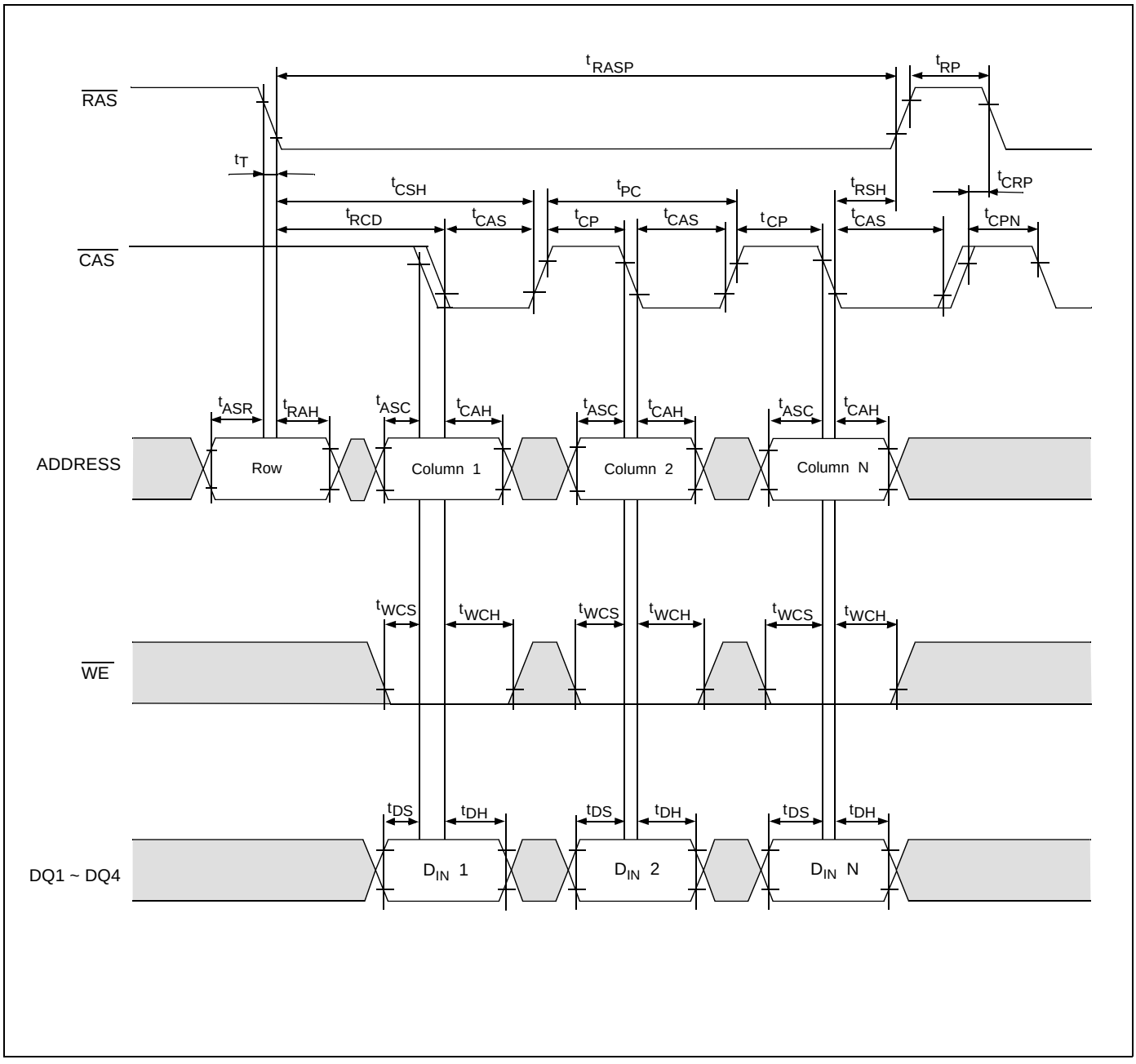
- **Read - Modify - Write Cycle**



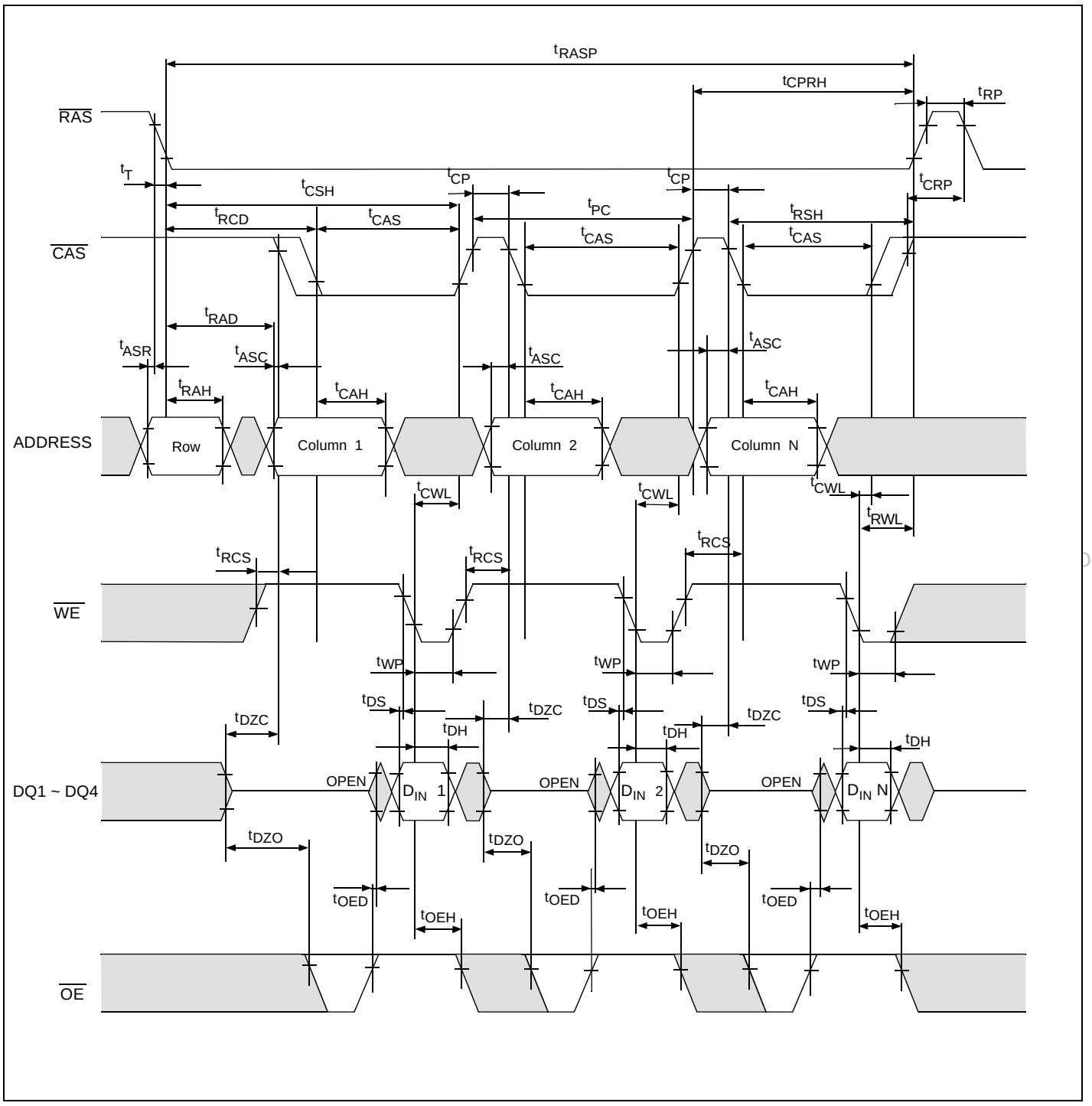
• **Fast Page Mode Read Cycle**



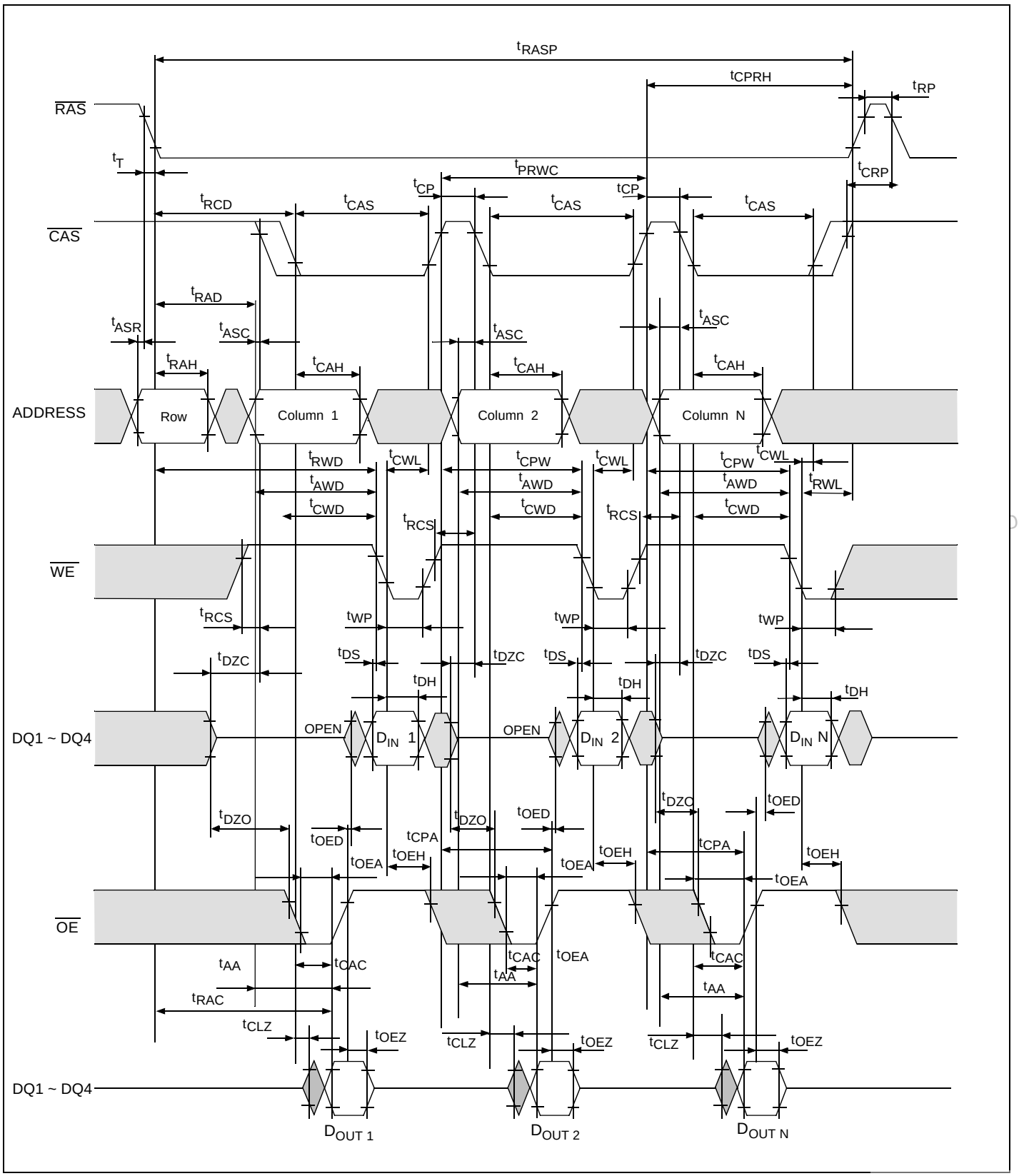
• Fast Page Mode Early Write Cycle



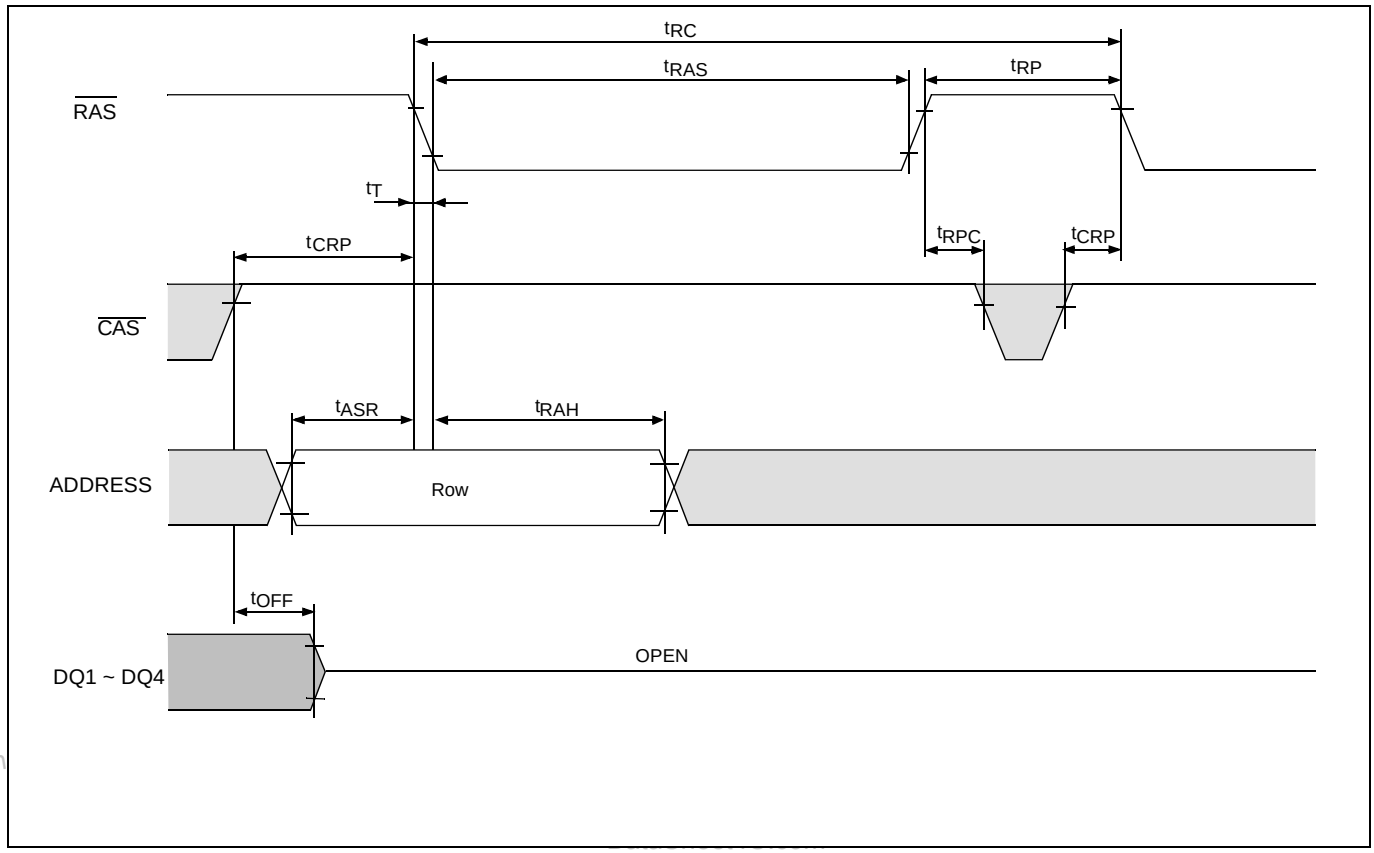
• Fast Page Mode Delayed Write Cycle



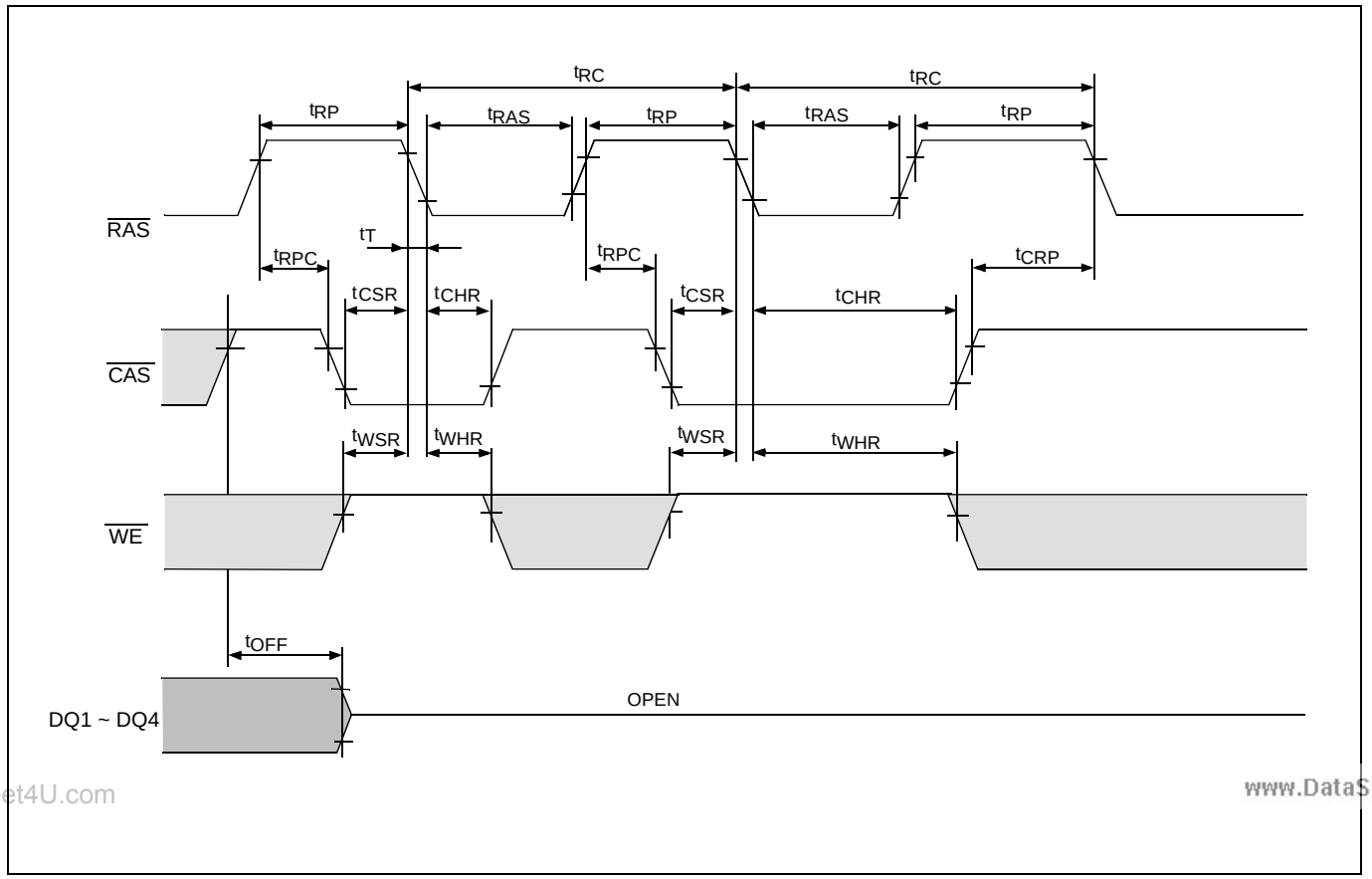
• Fast Page Mode Read - Modify - Write Cycle



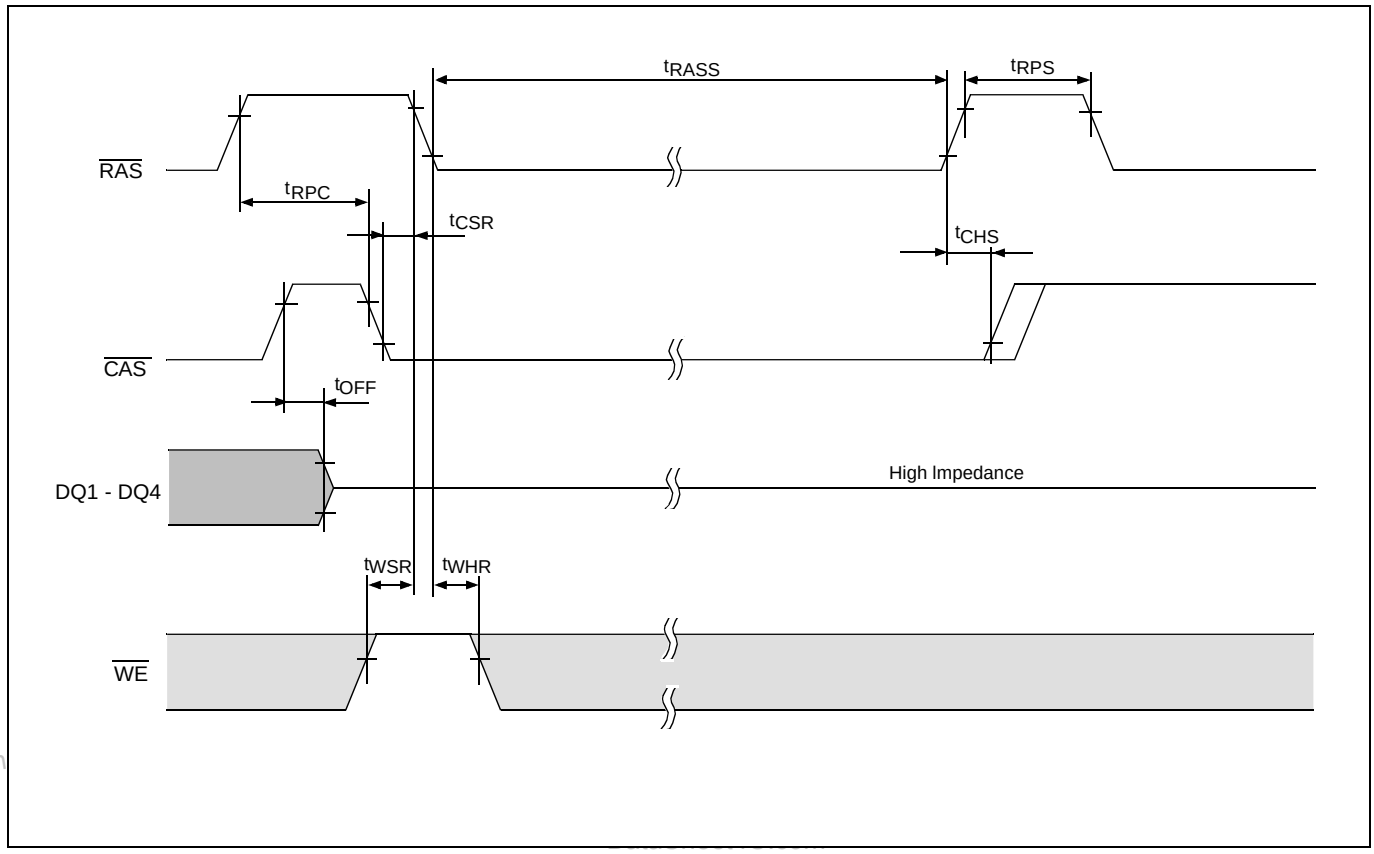
$\overline{RAS}$ - Only Refresh Cycle



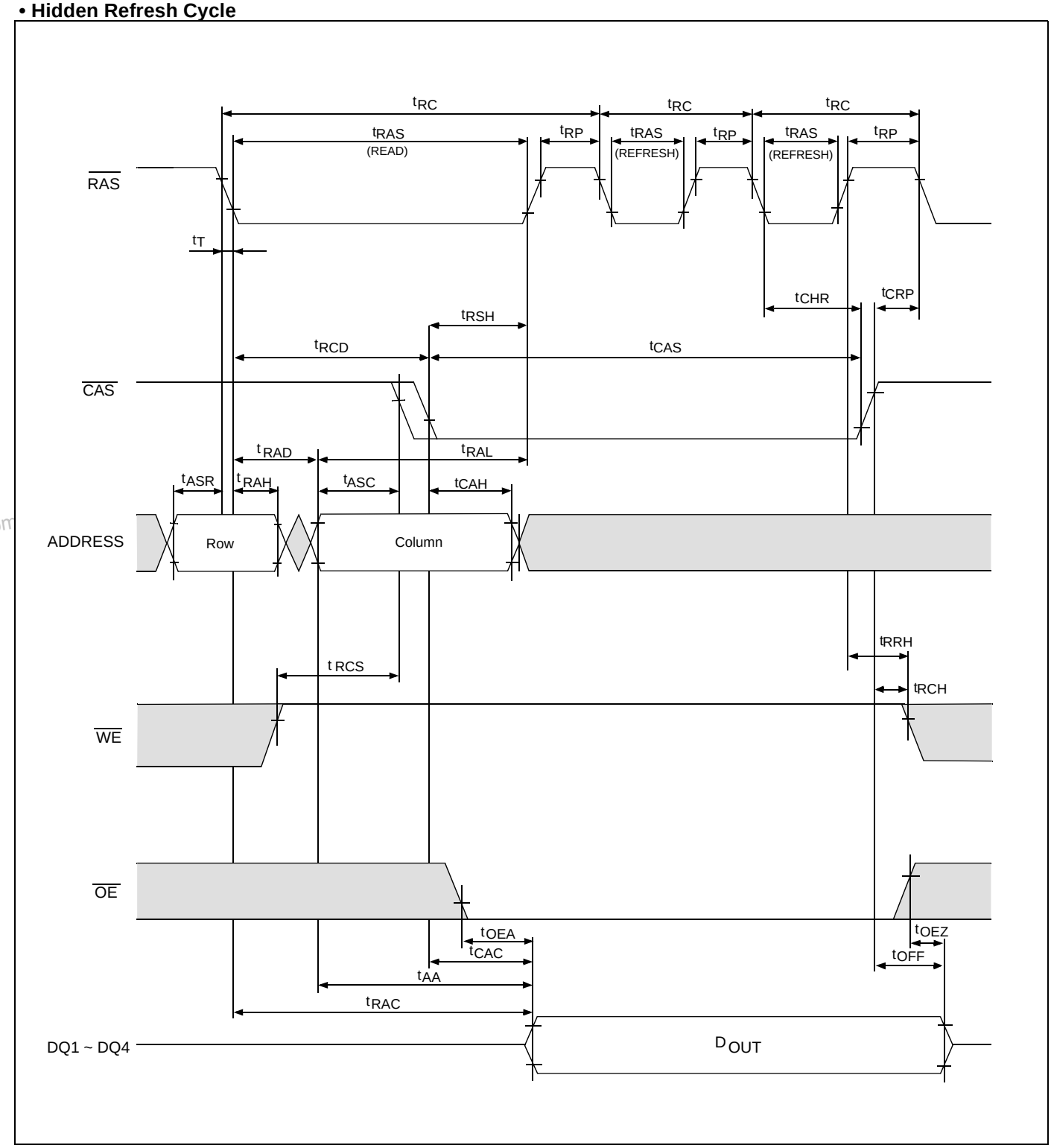
$\overline{CAS}$ - Before - $\overline{RAS}$ Refresh Cycle



CBR Self - Refesh Cycle



• Hidden Refresh Cycle



Ordering information

Part Number	Access Time	Package
VG26 (V) (S) 17400DJ - 5	50 ns	300mil 26/24 - Pin
VG26 (V) (S) 17400DJ - 6	60 ns	Plastic SOJ

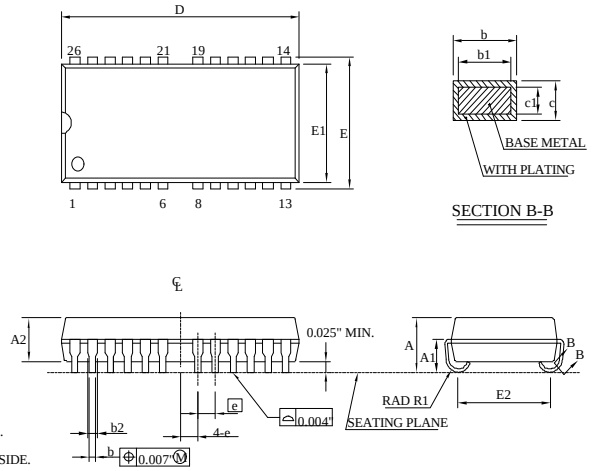
VG26 (V) (S) 17400DJ - 5

- VG → • VIS Memory Product
- 26 → • Technology
- V → • 3.3V version
- S → • Self refresh
- 17400 → • Device Type and Configuration
- D → • Revision
- J → • Package Type (J : SOJ , T : TSOJ II)
- 5 → • Speed (5 : 50 ns, 6 : 60 ns)

Packaging information

• 300 mil, 26/24-Pin Plastic SOJ

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	3.25	3.51	3.76	0.128	0.138	0.148
A1	2.08	---	---	0.082	---	---
A2	2.54 REF.			0.100 REF.		
b	0.41	---	0.51	0.016	---	0.020
b1	0.41	0.46	0.48	0.016	0.018	0.019
b2	0.66	---	0.81	0.026	---	0.032
c	0.18	---	0.30	0.007	---	0.012
c1	0.18	---	0.28	0.007	---	0.011
D	17.02	17.15	17.27	0.670	0.675	0.680
E	8.51 BASIC			0.335 BASIC		
E1	7.49	7.62	7.75	0.295	0.300	0.305
E2	6.78 BASIC			0.267 BASIC		
e	1.27 BASIC			0.050 BASIC		
R1	0.76	---	1.02	0.030	---	0.040



NOTE:
1. CONTROLLING DIMENSION : INCHES
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. MOLD PROTRUSION SHALL NOT EXCEED 0.006"(0.15mm) PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION. INTERLEAD PROTRUSION SHALL NOT EXCEED 0.01"(0.25mm) PER SIDE.
3. DIMENSION b2 DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE SHOULDER WIDTH TO EXCEED b2 MAX BY MORE THAN 0.005"(0.127mm) DAMBAR INTRUSION SHALL NOT REDUCE THE SHOULDER WIDTH TO LESS THAN 0.001"(0.025mm) BELOW b2 MIN.