



Description

The device is CMOS Dynamic RAM organized as 4,194,304 words x 4 bits. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 5V only or 3.3V only power supply. Low voltage operation is more suitable to be used on battery backup, portable electronic application. A new refresh feature called "self-refresh" is supported and very slow CBR cycles are being performed. It is packaged in JEDEC standard 26/24 - pin plastic SOJ or TSOP (II).

Features

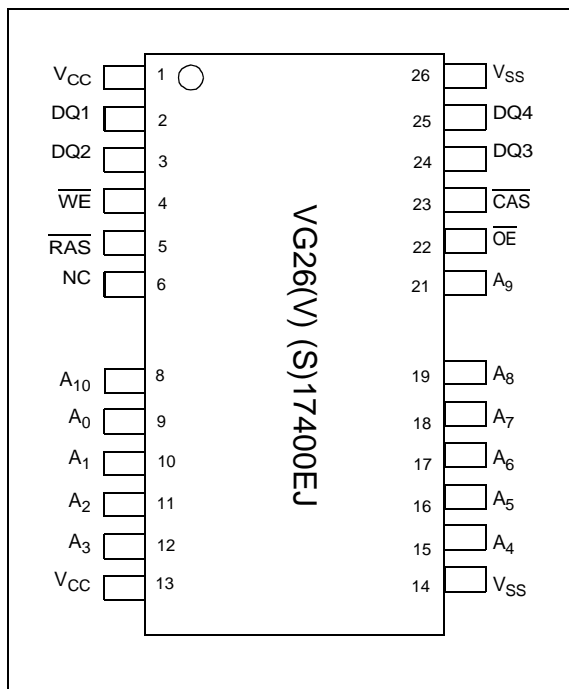
- Single 5V ($\pm 10\%$) or 3.3V (+10%, -5%) only power supply
- High speed t_{RAC} access time : 50/60 ns
- Low power dissipation
 - Active mode : 5V version 605/550 mW (Max.)
3.3V version 396/360 mW (Max.)
 - Standby mode : 5V version 1.375 mW (Max.)
3.3V version 0.54 mW (Max.)
- Fast Page Mode access
- I/O level : TTL compatible ($V_{cc} = 5V$)
LVTTL compatible ($V_{cc} = 3.3V$)
- 2048 refresh cycles in 32 ms (Std) or 128ms (S - version)
- 4 refresh mode :
 - \overline{RAS} only refresh
 - \overline{CAS} -before- \overline{RAS} refresh
 - Hidden refresh
 - Self - refresh (S - version)

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Pin configuration

26/24 - PIN 300mil Plastic SOJ



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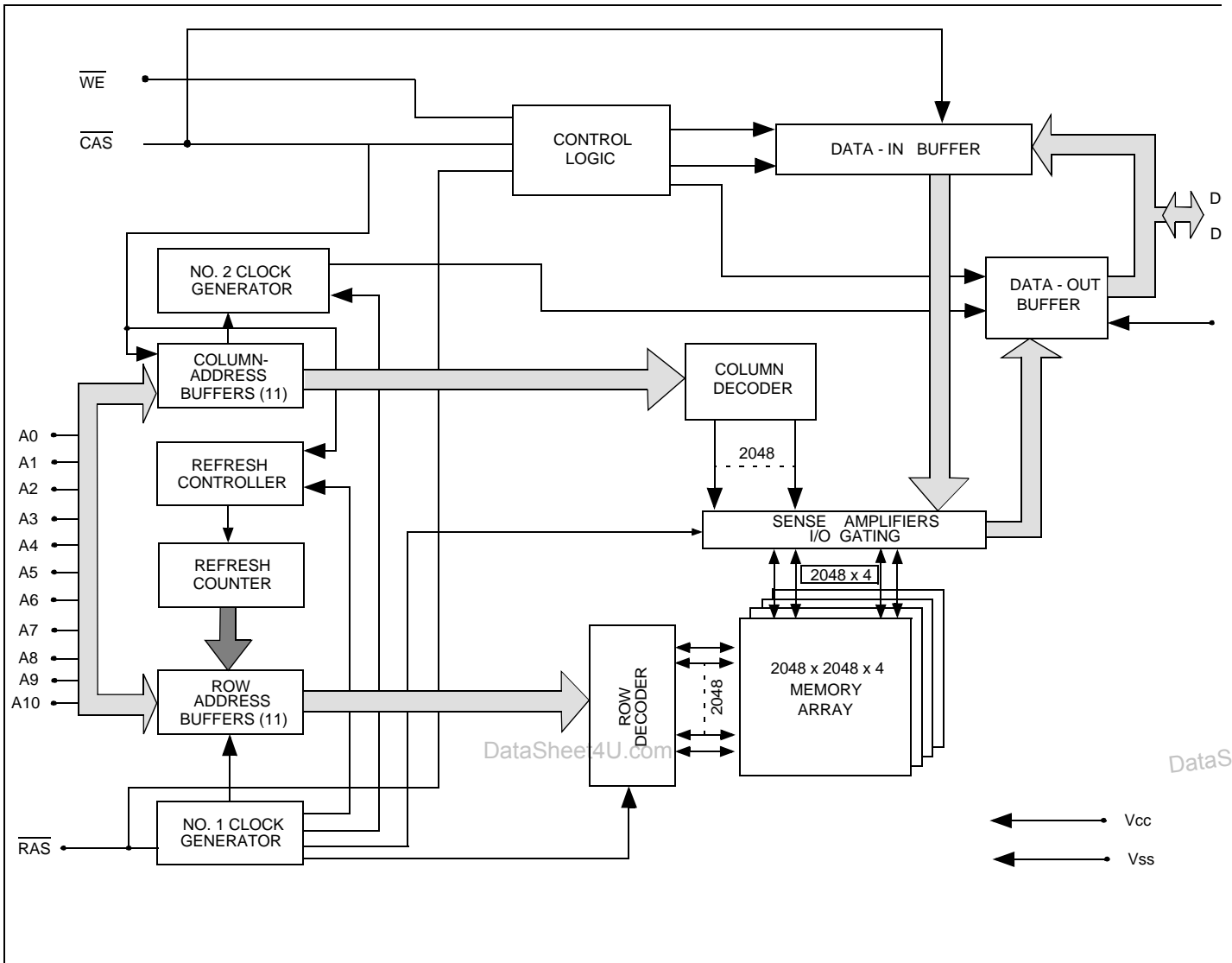
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Pin Description

Pin Name	Function
A0 - A10	Address inputs - Row address A0 - A10 - Column address A0 - A10 - Refresh address A0 - A10
DQ1 ~ DQ4	Data - in/data - out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{CAS}}$	Column address strobe
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power (+ 5V or + 3.3V)
V _{SS}	Ground



Block Diagram



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Truth Table

FUNCTION		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	ADDRESSES		DQ _S	Notes
						ROW	COL		
STANDBY		H	H → X	X	X	X	X	High - Z	
READ		L	L	H	L	ROW	COL	Data - Out	
WRITE : (EARLY WRITE)		L	L	L	X	ROW	COL	Data - In	
READ WRITE		L	L	H → L	L → H	ROW	COL	Data - Out, Data - In	
PAGE - MODE READ	1st Cycle	L	H → L	H	L	ROW	COL	Data - Out	
	2st Cycle	L	H → L	H	L	n/a	COL	Data - Out	
PAGE - MODE WRITE	1st Cycle	L	H → L	L	X	ROW	COL	Data - In	
	2st Cycle	L	H → L	L	X	n/a	COL	Data - In	
PAGE - MODE READ - WRITE	1st Cycle	L	H → L	H → L	L → H	ROW	COL	Data - Out, Data - In	
	2st Cycle	L	H → L	H → L	L → H	n/a	COL	Data - Out, Data - In	
HIDDEN REFRESH	READ	L → H → L	L	H	L	ROW	COL	Data - Out	
	WRITE	L → H → L	L	L	X	ROW	COL	Data - In	1
RAS - ONLY REFRESH		L	H	X	X	ROW	n/a	High - Z	
CBR REFRESH		H → L	L	H	X	X	X	High - Z	

Notes : 1. EARLY WRITE only.


Absolute Maximum Rating

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{ss}	V _T	5V	V
		3.3V	
Supply voltage relative to V _{ss}	V _{cc}	5V	V
		3.3V	
Short circuit output current	I _{OUT}	50	mA
Power dissipation	P _D	1.0	W
Operating temperature	T _{OPT}	0 to + 70	°C
Storage temperature	T _{STG}	-55 to + 125	°C

Recommended DC Operating Conditions

Parameter/Condition	Symbol	5 Volt Version			3.3 Volt Version			Unit
		Min	Typ	Max	Min	Typ	Max	
Supply Voltage	V _{cc}	4.5	5.0	5.5	3.15	3.3	3.6	V
Input High Voltage, all inputs	V _{IH}	2.4	-	V _{CC} + 1.0	2.0	-	V _{CC} + 0.3	V
Input Low Voltage, all inputs	V _{IL}	-1.0	-	0.8	-0.3	-	0.8	V

Capacitance

T_a = 25°C, V_{CC} = 5V±10% or 3.3V(+10%,-5%), f = 1MHz

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (Address)	C _{I1}	-	5	pF	1
Input capacitance (RAS, CAS, OE, WE)	C _{I2}	-	7	pF	1
Output capacitance (Data - in, Data - out)	C _{I/O}	-	7	pF	1,2

Note : 1. Capacitance measured with effective capacitance measuring method.

2. CAS = V_{IH} to disable Dout.

DC Characteristics; 5 - Volt verion
 $(T_a = 0 \text{ to } 70^\circ\text{C}, V_{CC} = +5\text{V} \pm 10\%, V_{SS} = 0\text{V})$

Parameter		Symbol	Test Conditions	VG26 (V) (S) 17400E				Unit	Notes
				-5		-6			
				Min	Max	Min	Max		
Operating current		I_{CC1}	$\overline{\text{RAS}}$ cycling CAS cycling $t_{RC} = \text{min.}$	-	145	-	135	mA	1, 2
Standby Current	Low power S - version	I_{CC2}	TTL interface RAS, CAS = V_{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{V}$ Dout = high - Z	-	0.25	-	0.25	mA	
	Standard power version		TTL interface RAS, CAS = V_{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface RAS, CAS $\geq V_{CC} - 0.2\text{V}$ Dout = high - Z	-	1	-	1	mA	
RAS - only refresh current		I_{CC3}	RAS cycling, CAS = V_{IH} $t_{RC} = \text{min.}$	-	145	-	135	mA	1, 2
Fast page mode current		I_{CC4}	$t_{PC} = \text{min.}$	-	100	-	90	mA	1,3
CAS - before - RAS refresh current		I_{CC5}	$t_{RC} = \text{min.}$ RAS, CAS cycling	-	145	-	135	mA	1, 2
Self - refresh currant (S - Version)		I_{CC8}	$t_{RASS} \geq 100\mu\text{S}$	-	350	-	350	μA	
CAS - before - RAS long refresh current (S - Version)		I_{CC9}	Standby : $V_{CC} - 0.2\text{V} \leq \overline{\text{RAS}}$ CAS before RAS refresh : 2048 cycles/128ms RAS, RAS : $0\text{V} \leq V_{IL} \leq 0.2\text{V}$ $V_{CC} - 0.2\text{V} \leq V_{IH} \leq V_{IH} (\text{Max})$ Dout = high - Z, $t_{RAS} \leq 300\text{ns}$	-	500	-	500	μA	

DC Characteristics ; 5 - Volt Version (cont.)
 $(T_a = 0 \text{ to } 70^\circ\text{C}, V_{CC} = +5\text{V} \pm 10\%, V_{SS} = 0\text{V})$

Parameter	Symbol	Test Conditions	VG26 (V) (S) 17400E				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Input leakage current	I_{LI}	$0\text{V} \leq V_{in} \leq V_{CC} + 0.5\text{V}$	-5	5	-5	5	μA	
Output leakage current	I_{LO}	$0\text{V} \leq V_{out} \leq V_{CC} + 0.5\text{V}$ Dout = Disable	-5	5	-5	5	μA	
Output high voltage	V_{OH}	$I_{OH} = -5\text{mA}$	2.4	-	2.4	-	V	
Output low voltage	V_{OL}	$I_{OL} = +4.2\text{mA}$	-	0.4	-	0.4	V	

Notes :

- I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
- Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
- For I_{CC4} , address can be changed once or less within one Fast page mode cycle time.

DC Characteristics ; 3.3 - Volt Verion
 $(T_a = 0 \text{ to } 70^\circ\text{C}, V_{CC} = + 3.3\text{V}(+10\%, -5\%), V_{SS} = 0\text{V})$

Parameter		Symbol	Test Conditions	VG26 (V) (S) 17400E				Unit	Notes
				-5		-6			
				Min	Max	Min	Max		
Operating current		I_{CC1}	$\overline{\text{RAS}}$ cycling CAS cycling $t_{RC} = \text{min.}$	-	145	-	135	mA	1, 2
Standby Current	Low power S - version	I_{CC2}	LVTTTL interface RAS, CAS = V_{IH} Dout = high - Z	-	0.5	-	0.5	mA	
			CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ Dout = high - Z	-	0.15	-	0.15	mA	
	Standard power version	I_{CC2}	LVTTTL interface RAS, CAS = V_{IH} Dout = high - Z	-	2	-	2	mA	
			CMOS interface $\overline{\text{RAS}}, \overline{\text{CAS}} \geq V_{CC} - 0.2\text{V}$ Dout = high - Z	-	0.5	-	0.5	mA	
RAS - only refresh current		I_{CC3}	$\overline{\text{RAS}}$ cycling, $\overline{\text{CAS}} = V_{IH}$ $t_{RC} = \text{min.}$	-	145	-	135	mA	1, 2
Fast page mode current		I_{CC4}	$t_{PC} = \text{min.}$	-	100	-	90	mA	1,3
CAS - before - RAS refresh current		I_{CC5}	$t_{RC} = \text{min.}$ $\overline{\text{RAS}}, \overline{\text{CAS}}$ cycling	-	145	-	135	mA	1, 2
Self - refresh currant (S - Version)		I_{CC8}	$t_{RASS} \geq 100\mu\text{S}$	-	250	-	250	μA	
CAS - before - RAS long refresh current (S - Version)		I_{CC9}	Standby : $V_{CC} - 0.2\text{V} \leq \overline{\text{RAS}}$ CAS before RAS refresh : 2048 cycles/128ms $\overline{\text{RAS}}, \overline{\text{CAS}} : 0\text{V} \leq V_{IL} \leq 0.2\text{V}$ $V_{CC} - 0.2\text{V} \leq V_{IH} \leq V_{IH} \text{ (Max)}$ Dout = high - Z, $t_{RAS} \leq 300\text{ns}$	-	300	-	300	μA	

DC Characteristics ; 3.3 - Volt Version (cont.)
 $(T_a = 0 \text{ to } 70^\circ\text{C}, V_{CC} = + 3.3\text{V}(+10\%, -5\%), V_{SS} = 0\text{V})$

Parameter	Symbol	Test Conditions	VG26 (V) (S) 17400E				Unit	Notes
			-5		-6			
			Min	Max	Min	Max		
Input leakage current	I_{LI}	$0\text{V} \leq V_{in} \leq V_{CC} + 0.3\text{V}$	-5	5	-5	5	μA	
Output leakage current	I_{LO}	$0\text{V} \leq V_{out} \leq V_{CC} + 0.3\text{V}$ Dout = Disable	-5	5	-5	5	μA	
Output high voltage	V_{OH}	$I_{OH} = -2\text{mA}$	2.4	-	2.4	-	V	
Output low voltage	V_{OL}	$I_{OL} = + 2\text{mA}$	-	0.4	-	0.4	V	

Notes :

- I_{CC} is specified as an average current. It depends on output loading condition and cycle rate when the device is selected. I_{CC} max is specified at the output open condition.
- Address can be changed once or less while $\overline{\text{RAS}} = V_{IL}$.
- For I_{CC4} , address can be changed once or less within one Fast page mode cycle time.

AC Characteristics

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$ or $3.3\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$) * 1, * 2, * 3, * 4

Test conditions

- Output load : two TTL Loads and 50pF ($V_{CC} = 5.0\text{V} \pm 10\%$)
one TTL Load and 30pF ($V_{CC} = 3.3\text{V} (+10\%, -5\%)$)
- Input timing reference levels :
 $V_{IH} = 2.4\text{V}$, $V_{IL} = 0.8\text{V}$ ($V_{CC} = 5.0\text{V} \pm 10\%$); $V_{IH} = 2.0\text{V}$, $V_{IL} = 0.8\text{V}$
($V_{CC} = 3.3\text{V} (+10\%, -5\%)$)
- Output timing reference levels :
 $V_{OH} = 2.0\text{V}$, $V_{OL} = 0.8\text{V}$ ($V_{CC} = 5\text{V} \pm 10\%$, $3.3\text{V} (+10\%, -5\%)$)

Read, Write, Read - Modify - Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	84	-	104	-	ns	
RAS precharge time	t_{RP}	30	-	40	-	ns	
CAS precharge time in normal mode	t_{CPN}	10	-	10	-	ns	
RAS pulse width	t_{RAS}	50	10000	60	10000	ns	5
CAS pulse width	t_{CAS}	8	10000	10	10000	ns	6
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	8	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	7
Column address hold time	t_{CAH}	8	-	10	-	ns	
RAS to CAS delay time	t_{RCD}	12	37	14	45	ns	8
RAS to column address delay time	t_{RAD}	10	25	12	30	ns	9
Column address to RAS lead time	t_{RAL}	25	-	30	-	ns	
RAS hold time	t_{RSH}	8	-	10	-	ns	
CAS hold time	t_{CSH}	38	-	60	-	ns	
CAS to RAS precharge time	t_{CRP}	5	-	5	-	ns	10
OE to Din delay time	t_{OED}	12	-	15	-	ns	
Transition time (rise and fall)	t_T	1	50	1	50	ns	11
Refresh period	t_{REF}	-	32	-	32	ms	
Refresh period (S - Version)	t_{REF}	-	128	-	128	ms	
CAS to output in Low-Z	t_{CLZ}	0	-	0	-	ns	
CAS delay time from Din	t_{DZC}	0	-	0	-	ns	
OE delay time from Din	t_{DZO}	0	-	0	-	ns	


Read Cycle

Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	-	50	-	60	ns	12
Access time from $\overline{\text{CAS}}$	t_{CAC}	-	13	-	15	ns	13,14
Access time from column address	t_{AA}	-	25	-	30	ns	14,15
Access time from $\overline{\text{OE}}$	t_{OEA}	-	12	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	7
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	-	0	-	ns	10,16
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	10	-	10	-	ns	16
Output buffer turn-off time	t_{OFF}	0	12	0	15	ns	17
Output buffer turn-off time from $\overline{\text{OE}}$	t_{OEZ}	0	12	0	15	ns	17

Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Write command setup time	t_{WCS}	0	-	0	-	ns	7,18
Write command hold time	t_{WCH}	8	-	10	-	ns	
Write command pulse width	t_{WP}	8	-	10	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	13	-	15	-	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	8	-	10	-	ns	
Data-in setup time	t_{DS}	0	-	0	-	ns	19
Data-in hold time	t_{DH}	8	-	10	-	ns	19

Read - Modify - Write Cycle

Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Read - modify - write cycle time	t_{RWC}	108	-	133	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	64	-	77	-	ns	18
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	26	-	32	-	ns	18
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	39	-	47	-	ns	18
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t_{OEH}	8	-	10	-	ns	


Refresh Cycle

Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
CAS setup time (CBR refresh)	t_{CSR}	5	-	10	-	ns	
CAS hold time (CBR refresh)	t_{CHR}	8	-	10	-	ns	10
RAS precharge to CAS hold time	t_{RPC}	5	-	5	-	ns	7
RAS pulse width (self refresh)	t_{RASS}	100	-	100	-	μs	
RAS precharge time (self refresh)	t_{RPS}	90	-	110	-	ns	
CAS hold time (CBR self refresh)	t_{CHS}	-50	-	-50	-	ns	
WE setup time	t_{WSR}	0	-	0	-	ns	
WE hold time	t_{WHR}	10	-	10	-	ns	

Fast Page Mode Cycle

Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Fast page mode cycle time	t_{PC}	20	-	25	-	ns	
Fast page mode CAS Precharge time	t_{CP}	10	-	10	-	ns	
Fast page mode RAS pulse width	t_{RASP}	50	10^5	60	10^5	ns	20
Access time from CAS precharge	t_{CPA}	-	30	-	35	ns	10,14
RAS hold time from CAS precharge	t_{CPRH}	30	-	35	-	ns	

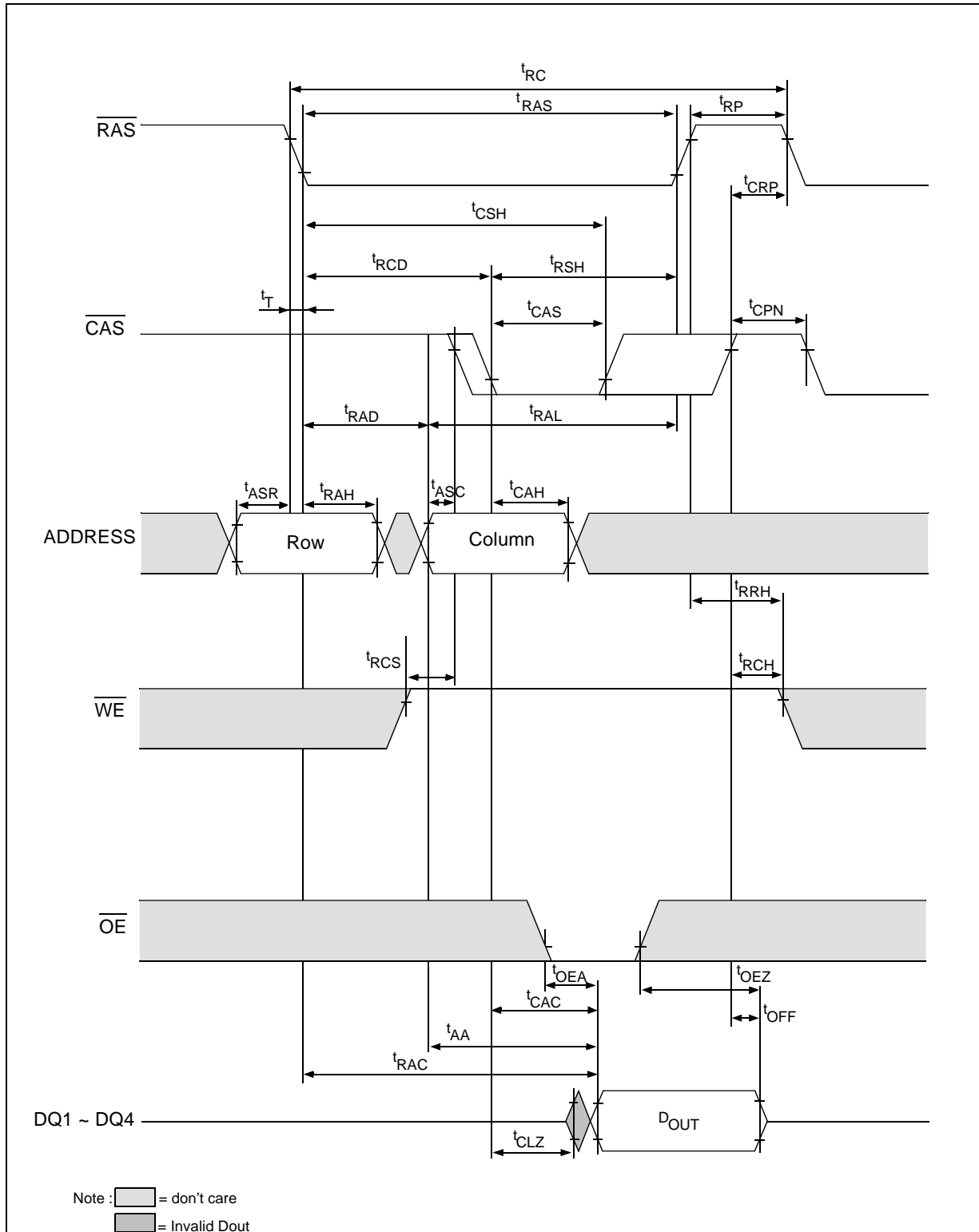
Fast Page Mode Read Modify Write Cycle

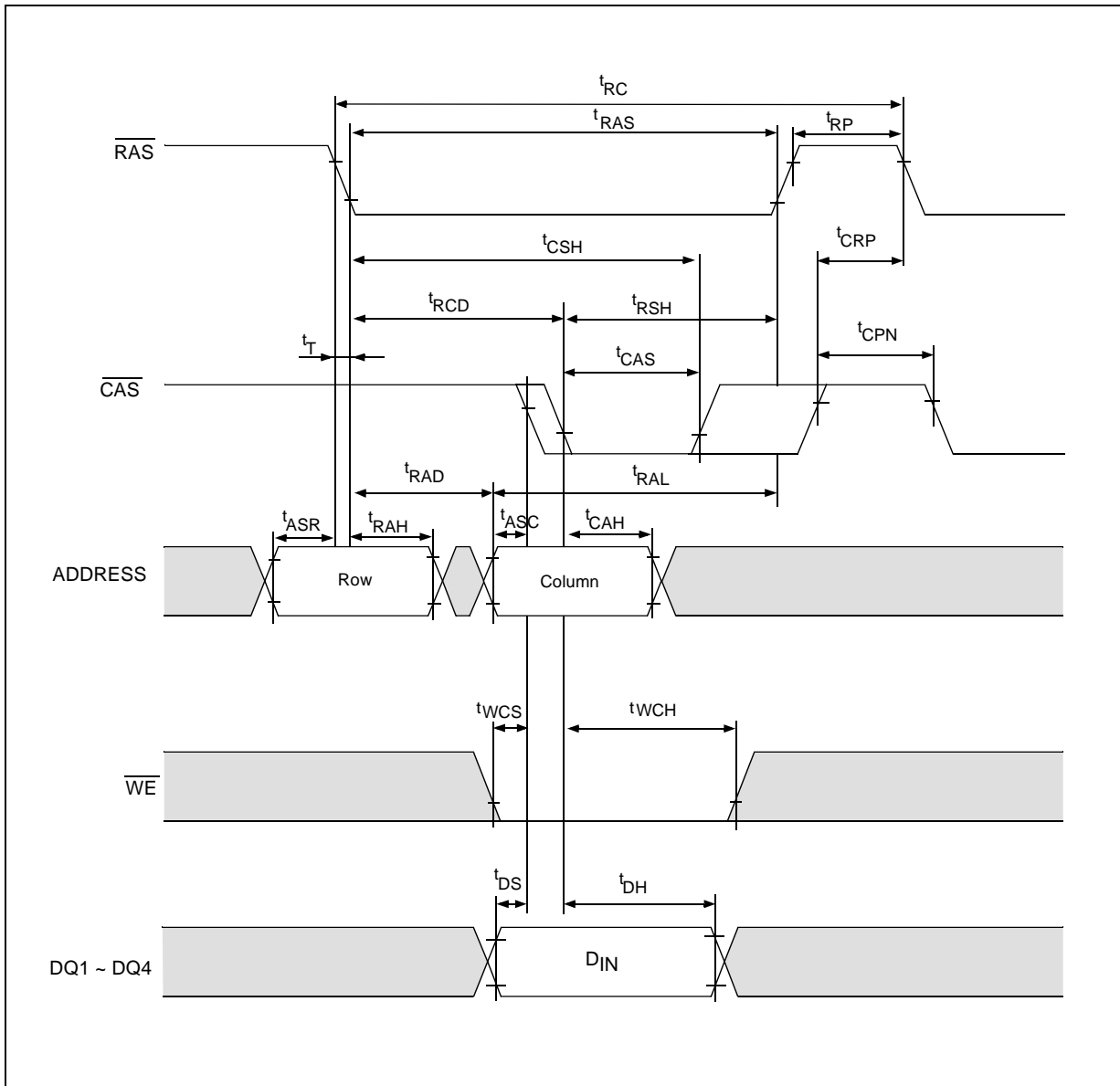
Parameter	Symbol	VG26 (V) (S) 17400E				Unit	Notes
		-5		-6			
		Min	Max	Min	Max		
Fast page mode read - modify - write cycle CAS precharge to WE delay time	t_{CPW}	45	-	55	-	ns	11
Fast page mode read - modify - write cycle time	t_{PRWC}	56	-	68	-	ns	

Notes :

1. AC measurements assume $t_T = 5\text{ns}$.
2. An initial pause of 100 μs is required after power up, and it followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
3. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
4. All the V_{CC} and V_{SS} pins shall be supplied with the same voltage.
5. $t_{\text{RAS}}(\text{min}) = t_{\text{RWD}}(\text{min}) + t_{\text{RWL}}(\text{min}) + t_T$ in read - modify-write cycle.
6. $t_{\text{CAS}}(\text{min}) = t_{\text{CWD}}(\text{min}) + t_{\text{CWL}}(\text{min}) + t_T$ in read - modify-write cycle.
7. $t_{\text{ASC}}(\text{min})$, $t_{\text{RCS}}(\text{min})$, $t_{\text{WCS}}(\text{min})$ and t_{RPC} are determined by the falling edge of $\overline{\text{CAS}}$.
8. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, and $t_{\text{RAC}}(\text{max})$ can be met with the $t_{\text{RCD}}(\text{max})$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{CAC} if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit.
9. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only, and $t_{\text{RAC}}(\text{max})$ can be met with the $t_{\text{RAD}}(\text{max})$ limit. Otherwise, t_{RAC} is controlled exclusively by t_{AA} if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit.
10. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the rising edge of $\overline{\text{CAS}}$.
11. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing or input signals. Therefore, transition time is measured between V_{IH} and V_{IL} .
12. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
13. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.
14. Access time is determined by the maximum among t_{AA} , t_{CAC} , t_{CPA} .
15. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.
16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
17. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition (high impedance).
18. t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data output will remain open circuit (high impedance) throughout the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, and $t_{\text{CPW}} \geq t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
19. These parameters are referenced to $\overline{\text{CAS}}$ in an early write cycle and to $\overline{\text{WE}}$ edge in a delayed write or a read-modify-write cycle.
20. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in Fast page mode cycles.

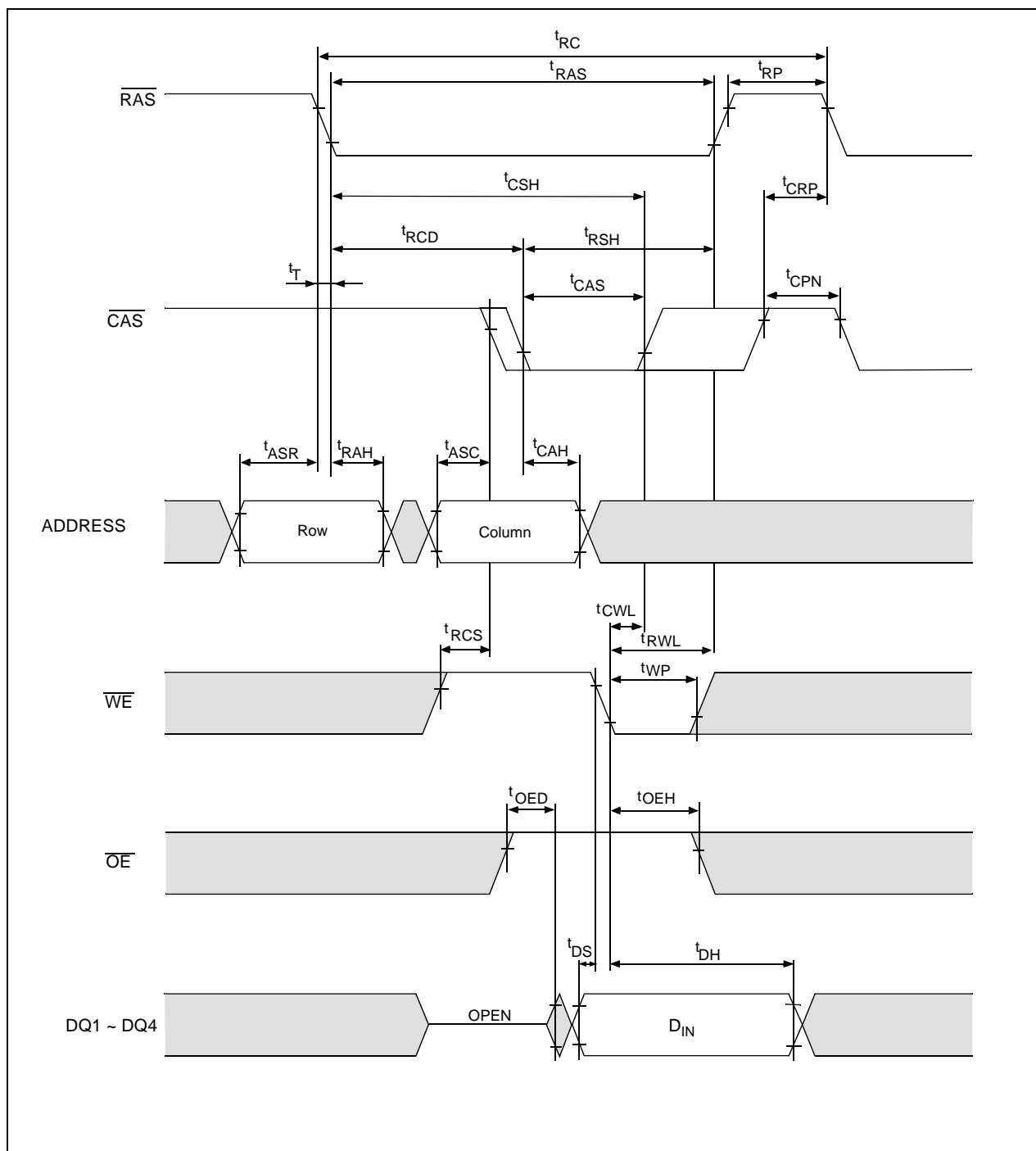
Timing Waveforms
• Read Cycle



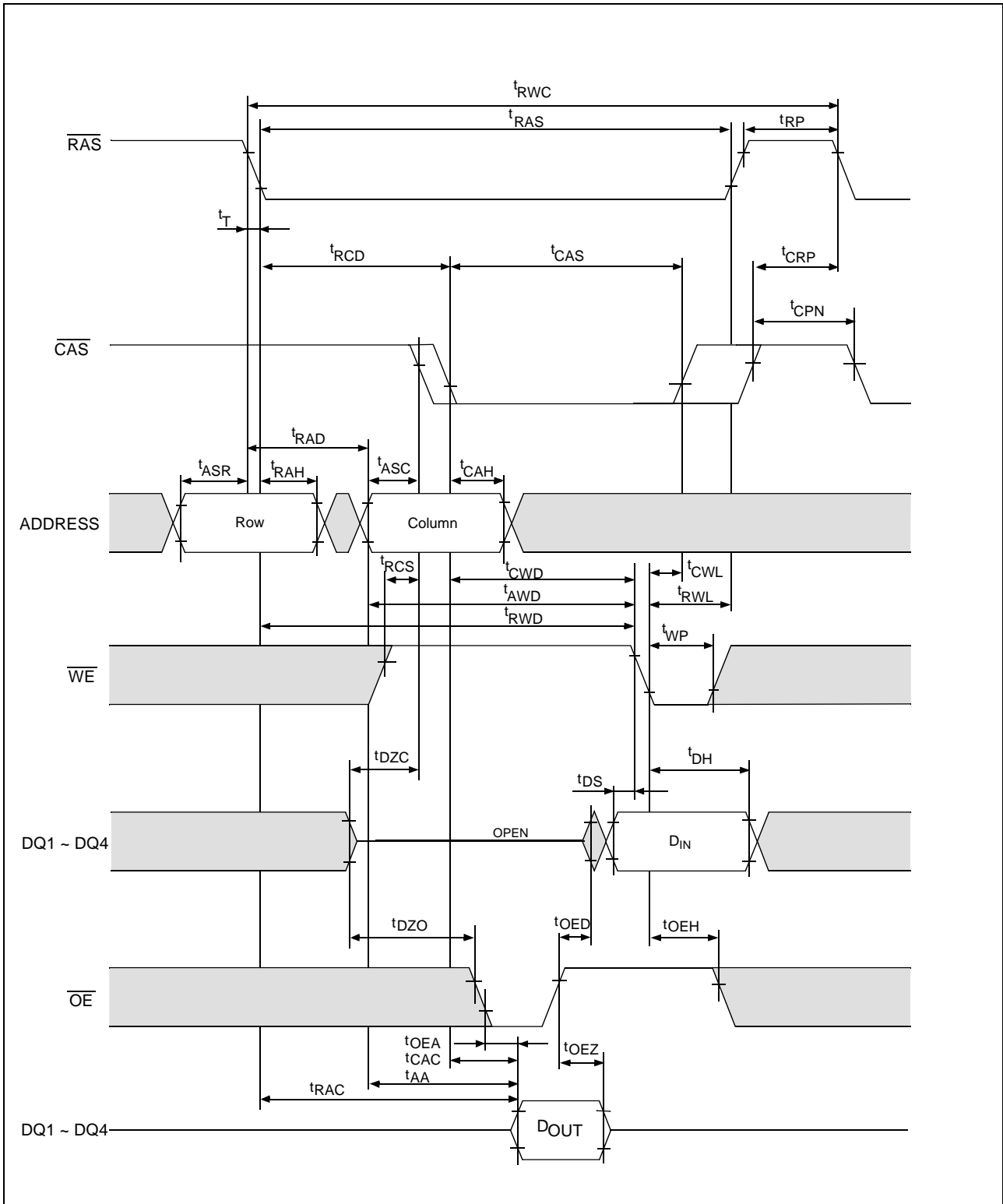
•Early Write Cycle


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• Delayed Write Cycle


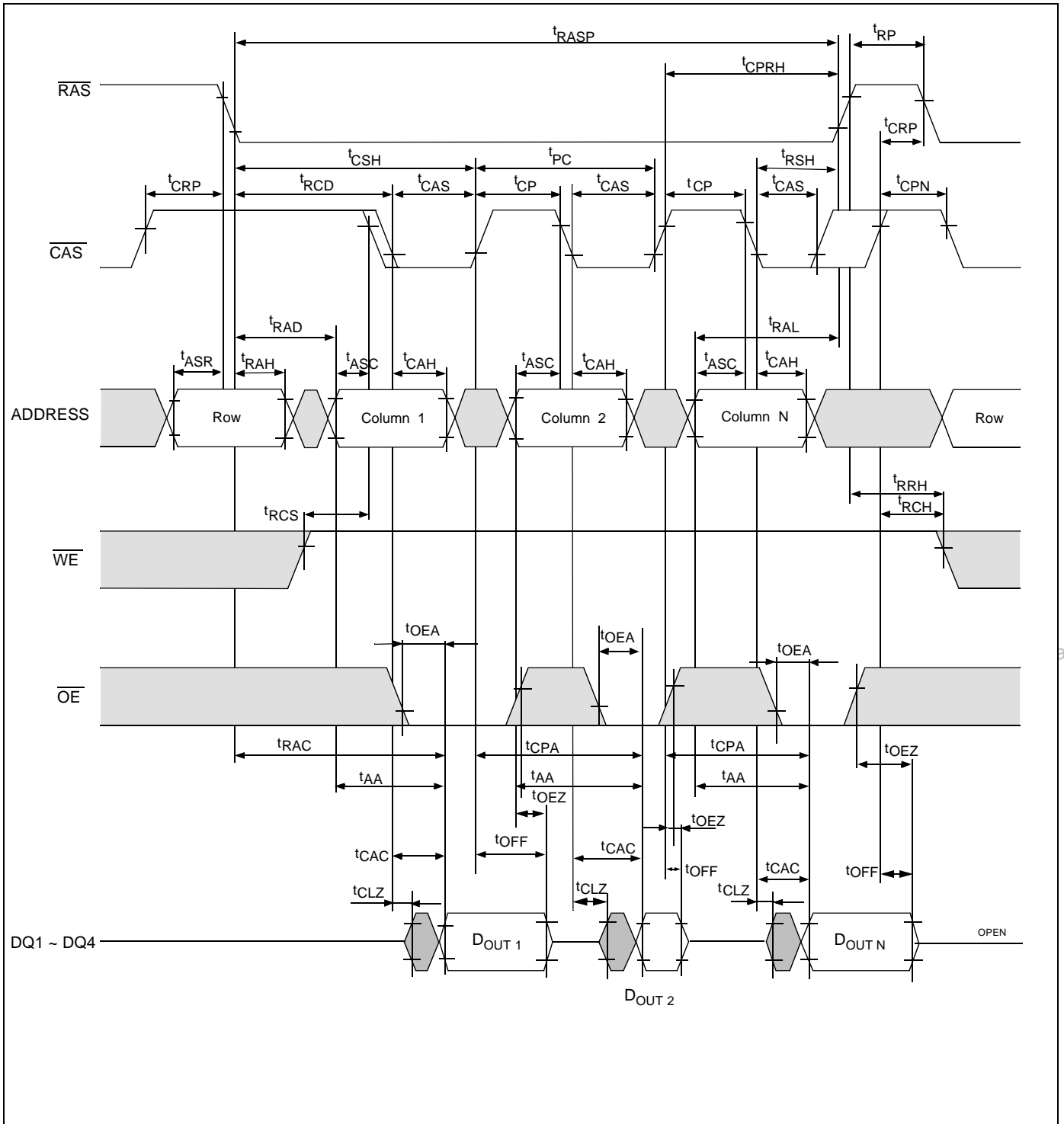
• Read - Modify - Write Cycle



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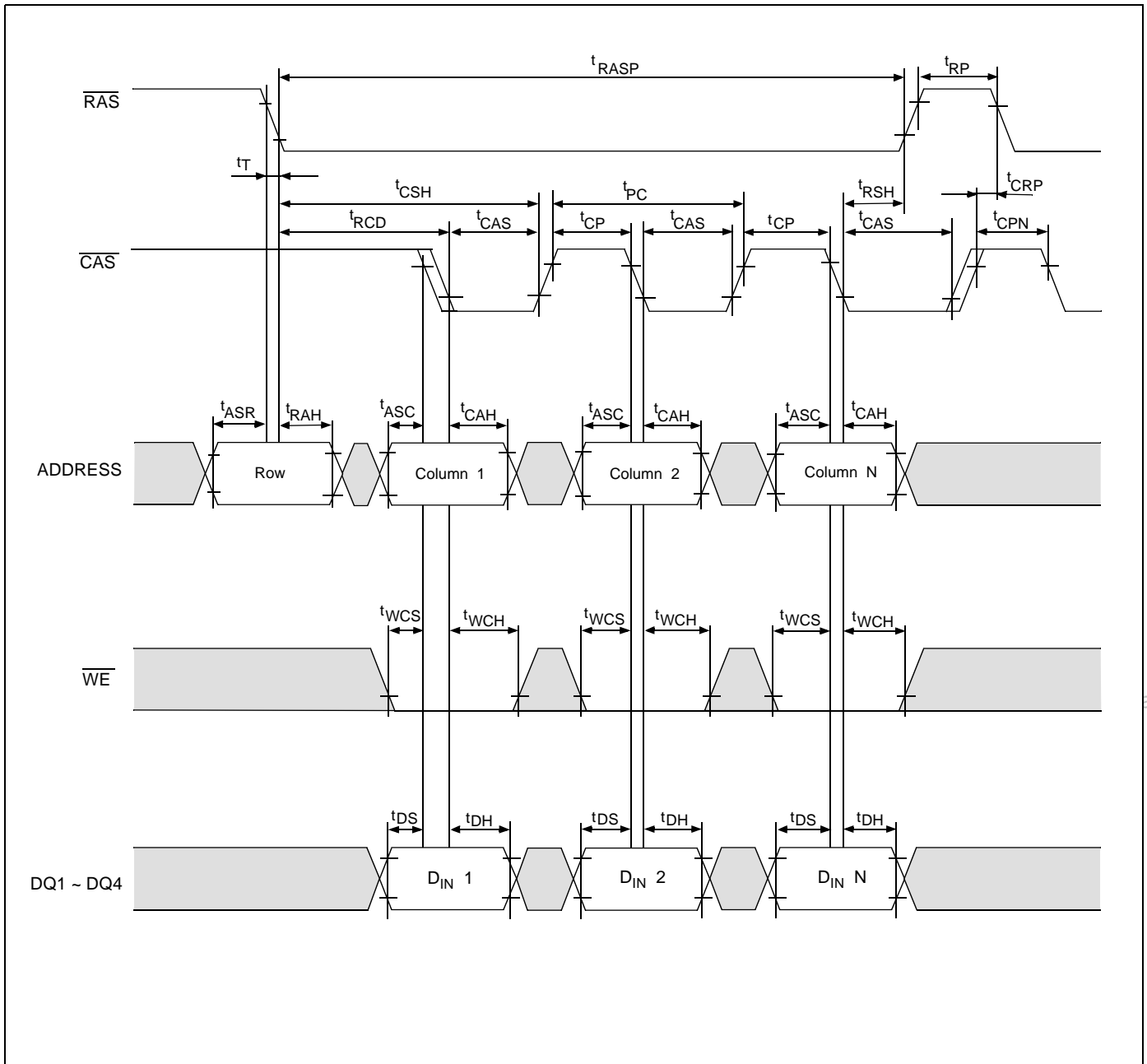
• Fast Page Mode Read Cycle



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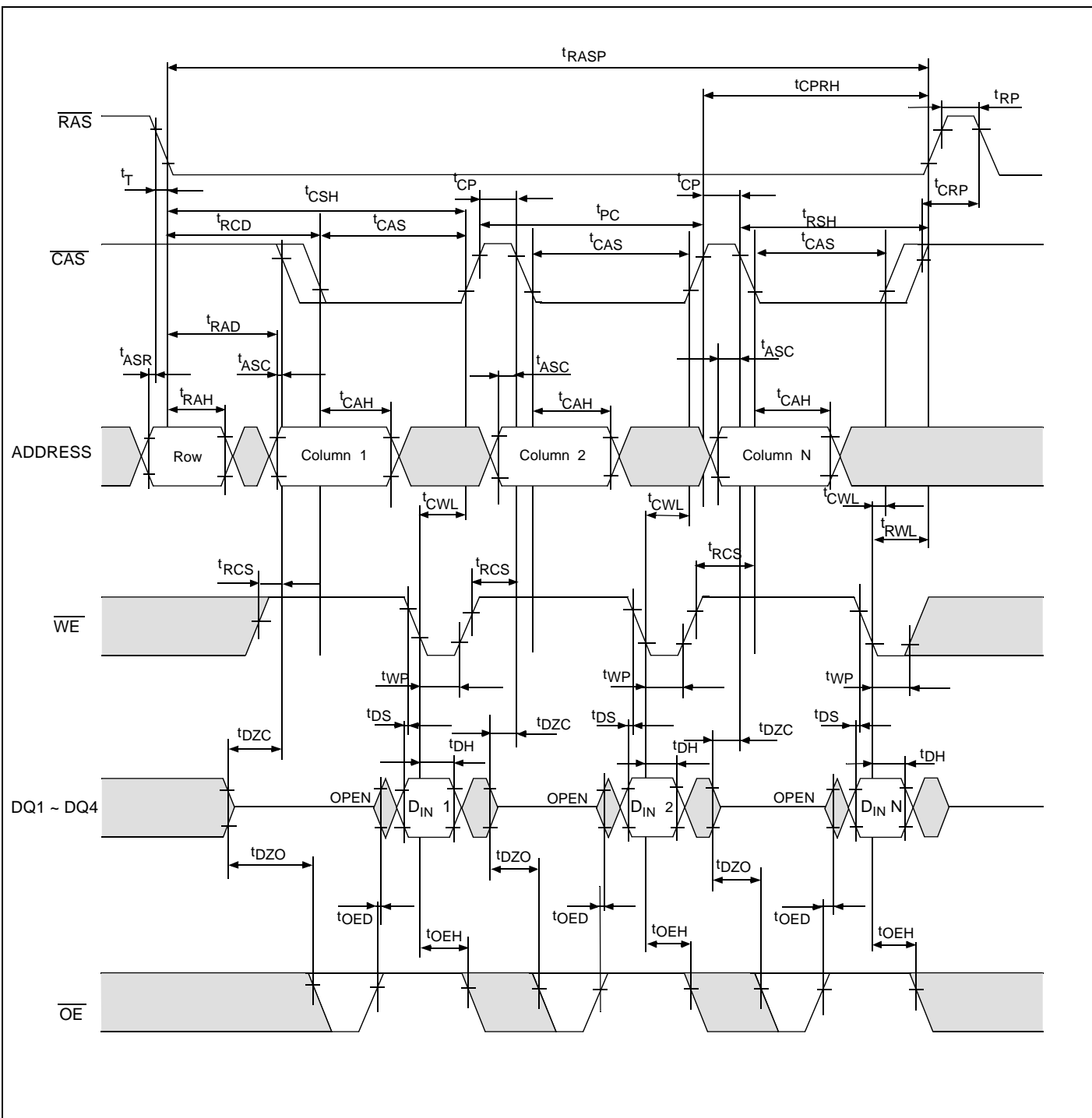
• **Fast Page Mode Early Write Cycle**



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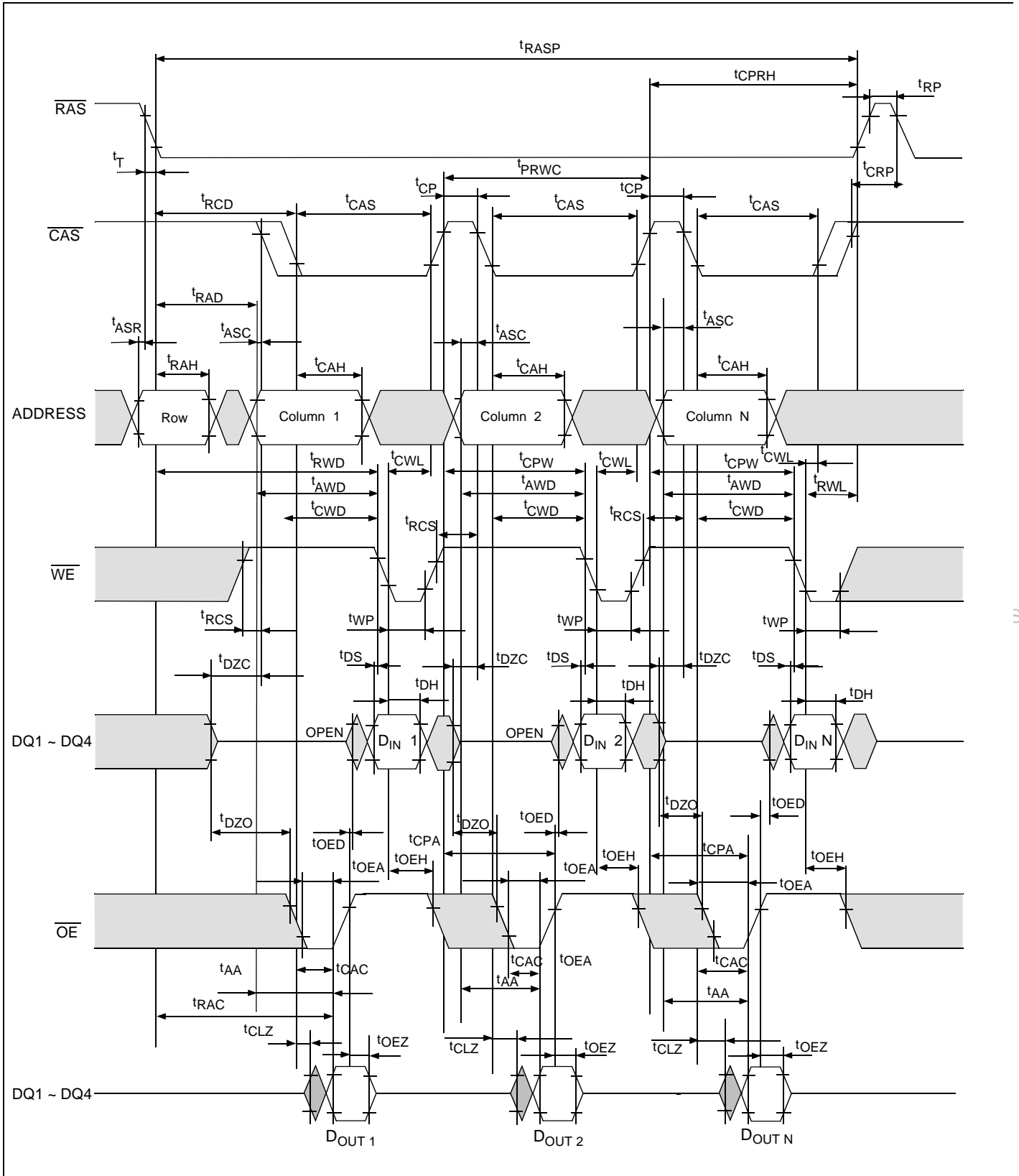
• Fast Page Mode Delayed Write Cycle



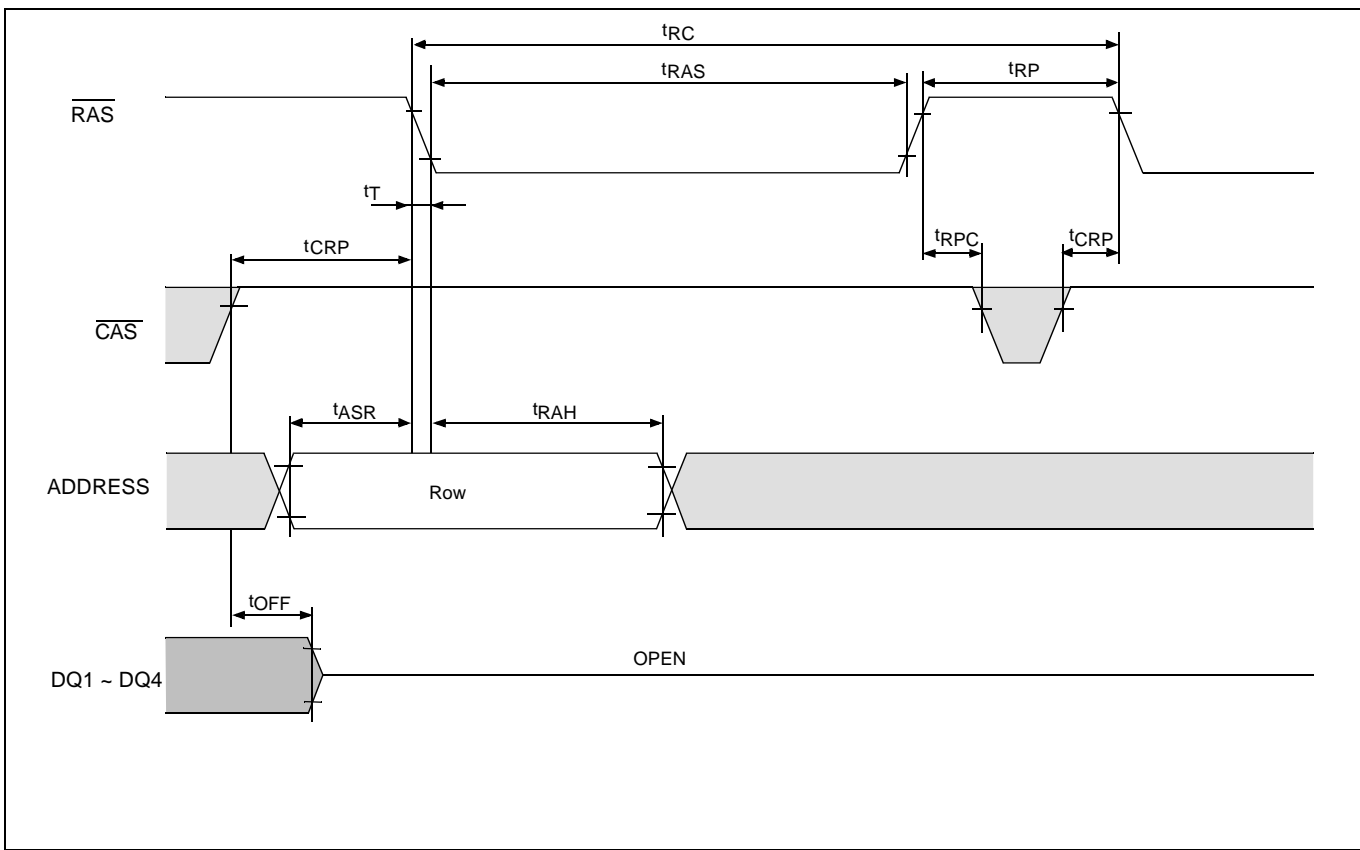
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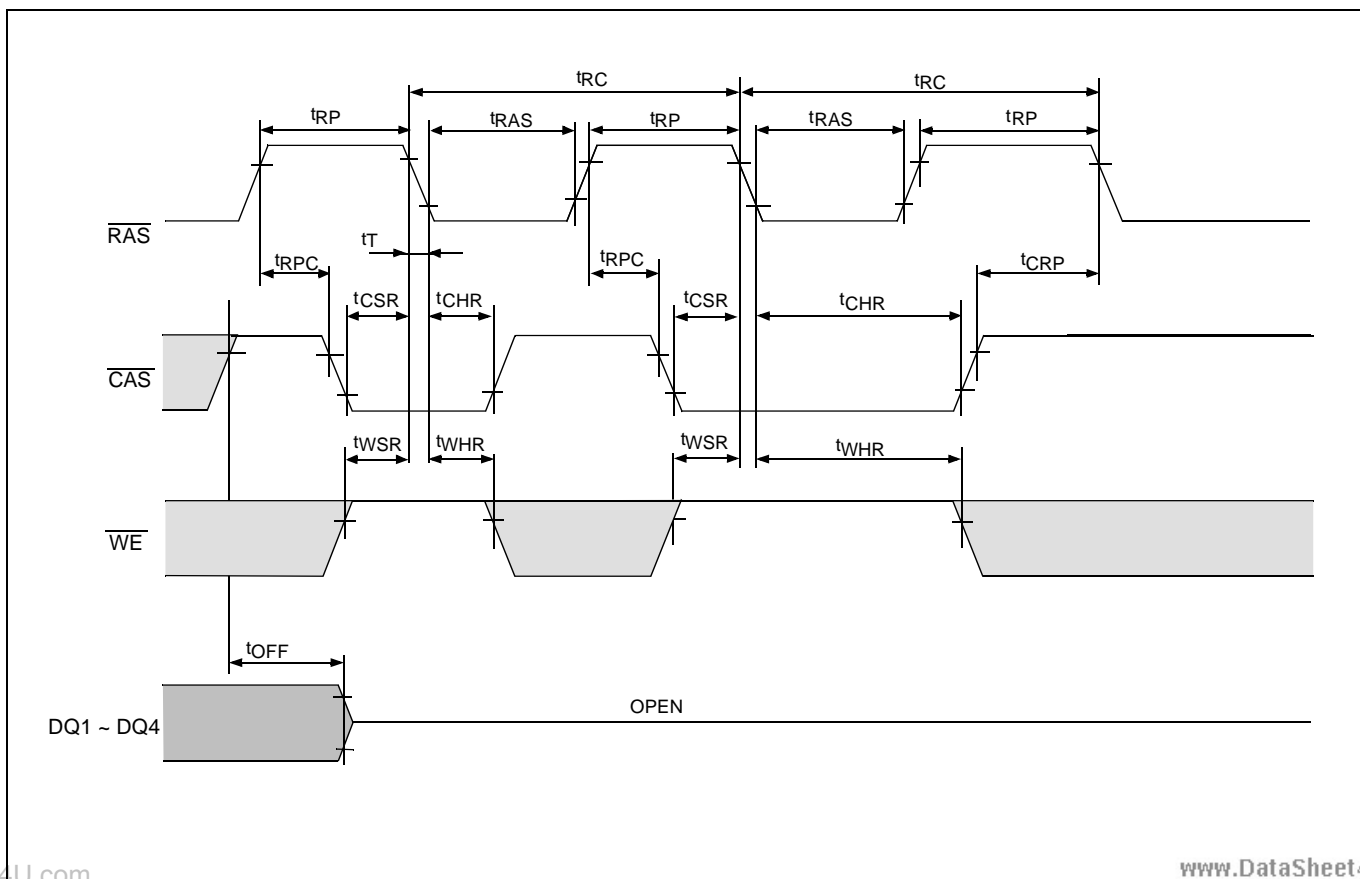
• **Fast Page Mode Read - Modify - Write Cycle**



RAS - Only Refresh Cycle

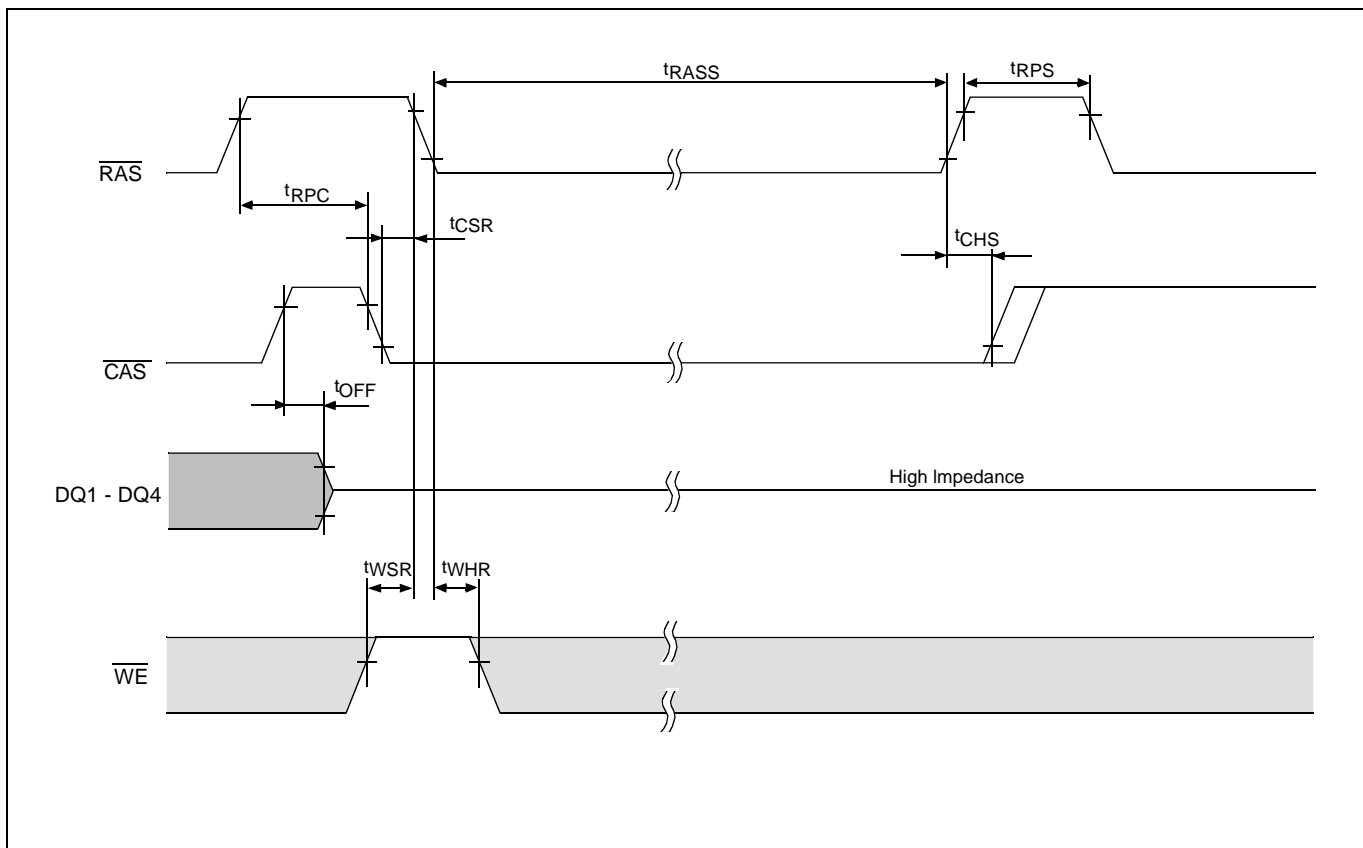


CAS - Before - RAS Refresh Cycle





CBR Self - Refresh Cycle (S - Version Only)

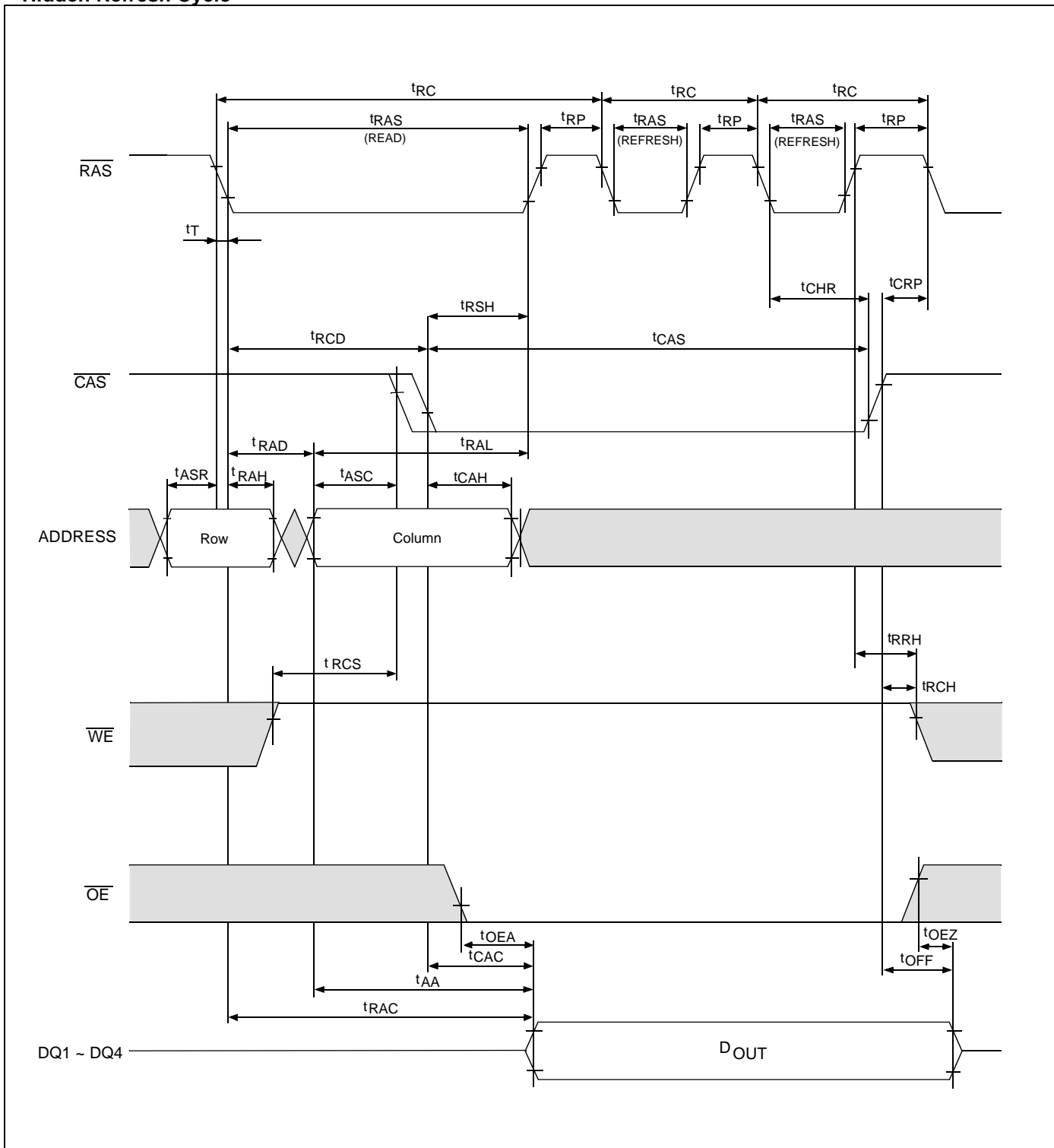


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• Hidden Refresh Cycle











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Ordering information

Part Number	Access Time	Package
VG26 (V) (S) 17400FJ - 5	50 ns	300mil 26/24 - Pin
VG26 (V) (S) 17400FJ - 6	60 ns	Plastic SOJ

VG26 (V) (S) 17400FJ - 5

- VG  • VIS Memory Product
- 26  • Technology
- V  • 3.3V version
- S  • Self refresh
- 17400  • Device Type and Configuration
- F  • Revision
- J  • Package Type (J : SOJ , T : TSOJ II)
- 5  • Speed (5 : 50 ns, 6 : 60 ns)

Packaging information

- 300 mil, 26/24-Pin Plastic SOJ

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