Description

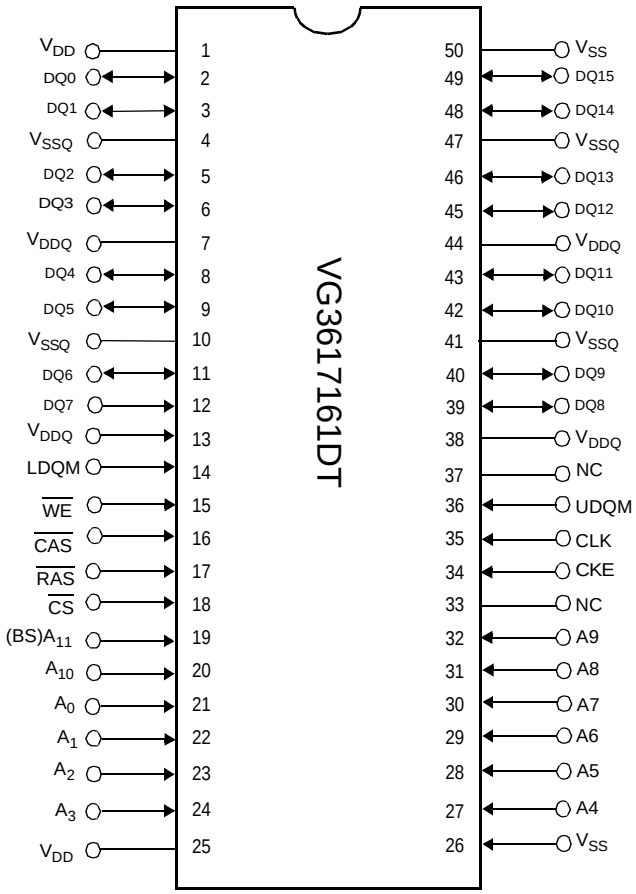
The VG3617161DT is CMOS Synchronous Dynamic RAM organized as 524,288-word X 16-bit X 2-bank. It is fabricated with an advanced submicron CMOS technology and designed to operate from a single 3.3V power supply. This SDRAM is delicately designed with performance concern for current high-speed application. Programmable CAS Latency and Burst Length make it possible to be used in widely various domains. It is packaged by using JEDEC standard pinouts and standard plastic 50-pin TSOP II.

Features

- Single 3.3V +/- 0.3V power supply
- Clock Frequency: 180MHz, 166MHz, 143MHz, 125MHz, 100MHz
- Fully synchronous with all signals referenced to a positive clock edge
- Programmable $\overline{\text{CAS}}$ latency (2,3)
- Programmable burst length (1,2,4,8,& Full page)
- Programmable wrap sequence (Sequential/Interleave)
- Automatic precharge and controlled precharge
- Auto refresh and self refresh modes
- Dual internal banks controlled by A11(Bank select)
- Simultaneous and independent two bank operation
- I/O level : LVTTL interface
- Random column access in every cycle
- X16 organization
- Byte control by LDQM and UDQM
- 4096 refresh cycles/64ms
- Burst termination by burst stop and precharge command

Pin Configuration

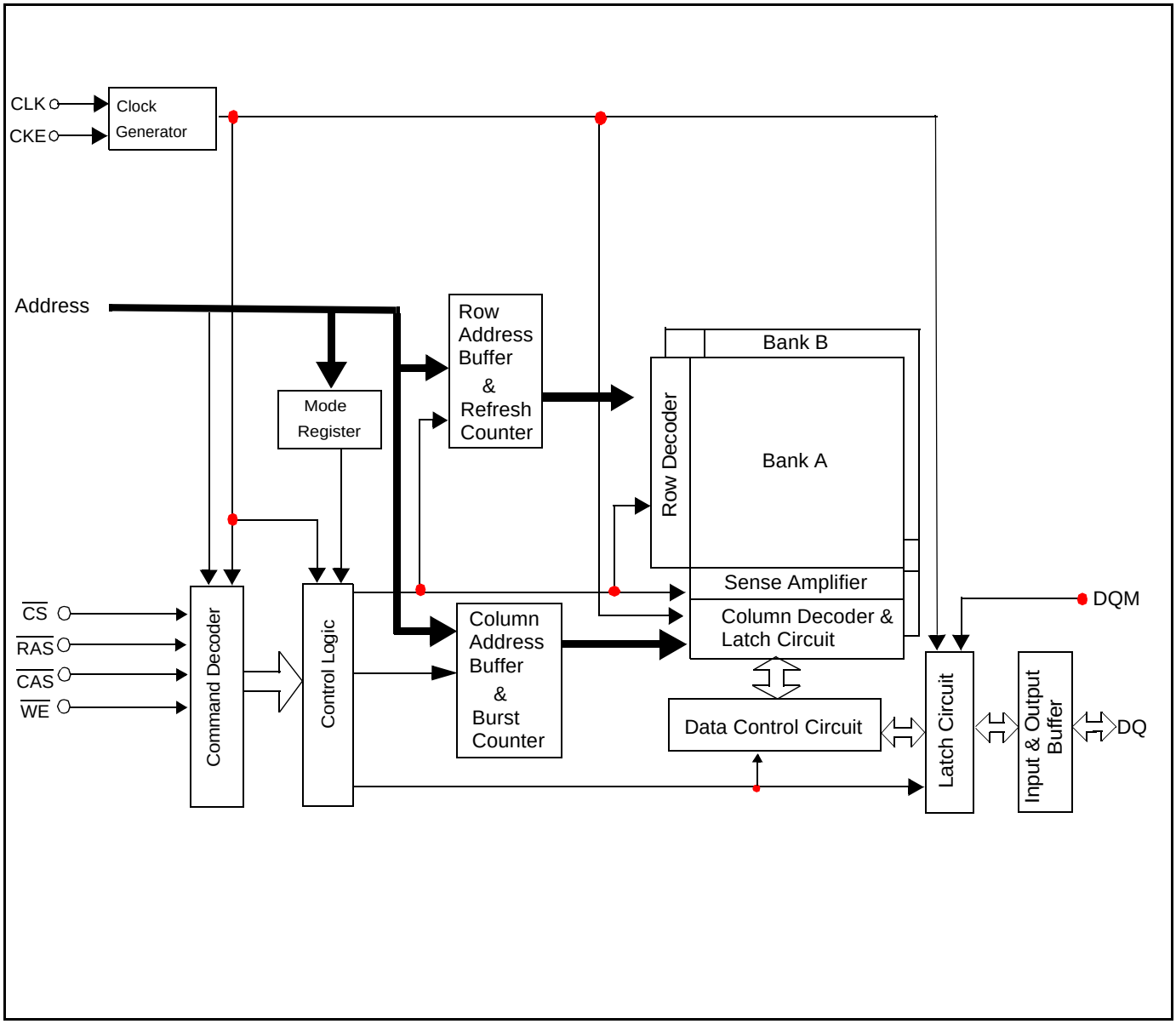
50-Pin Plastic TSOP(II)(400 mil)



Pin Description
(VG3617161DT)

Pin Name	Function	Pin Name	Function
A0-A11	Address inputs - Row address A0-A10 - Column address A0-A8 A11: Bank select	LDQM, UDQM	Lower DQ mask enable and Upper DQ mark enable
DQ0~DQ15	Data-in/data-out	CLK	Clock input
$\overline{RAS}$	Row address strobe	CKE	Clock enable
$\overline{CAS}$	Column address strobe	$\overline{CS}$	Chip select
$\overline{WE}$	Write enable	V_{DDQ}	Supply voltage for DQ
V_{SS}	Ground	V_{SSQ}	Ground for DQ
V_{DD}	Power		

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-1.0 to +4.6	V
Supply voltage relative to Vss	V_{DD},V_{DDQ}	-1.0 to +4.6	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_D	1.0	W
Operating temperature	T_{OPT}	0 to + 70	℃
Storage temperature	T_{STG}	-55 to + 125	℃

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	V_{DD}	3.0	3.3	3.6	V	
Input High Voltage, all inputs	V_{IH}	2.0	-	V_{DD}+0.3	V	1
Input Low Voltage, all inputs	V_{IL}	-0.3	-	0.8	V	2

Note 1.Overshoot limit : $V_{IH(MAX.)}$=V_{DDQ}+2.0V with a pulse width < 3ns
2.Undershoot limit : V_{IL}=V_{SSQ}-2.0V with a pulse < 3ns and -1.5V with a pulse < 5ns

Parameter	Description	Min.	Max.	Unit	Note
I_{IL}	Input Leakage Current ($0V \le V_{IN} \le V_{DD}$ All other pins not under test = OV)	-5	5	μA	
I_{OL}	Output Leakage Current Output disable, ($0V \le V_{OUT} \le V_{DDQ}$)	-5	5	μA	
V_{OH}	LVTTL Output "H" Level Voltage (I_{OUT} = -2mA)	2.4	-	V	
V_{OL}	LVTTL Output "L" Level Voltage (I_{OUT} = 2mA)	-	0.4	V	

Capacitance
(Ta=25°C,f=1MHZ)

Parameter	Symbol	Typ	Max	Unit
Input capacitance(CLK)	C_{11}	2.5	4	pF
Input capacitance(all input pins except data pins)	C_{12}	2.5	5	pF
Data input/output capacitance	$C_{I/O}$	4.0	6.5	pF

Recommended D.C. Operating Conditions (V_{DD} = 3.3V ±0.3V, Ta = 0 ~ 70°C)

Description/test condition	Symbol	-5.5		-6		-7		-8		Unit	Note
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Operating Current $t_{RC} \geq t_{RC(min)}$, Outputs Open Address changed once during $t_{CK(min)}$. Burst Length = 1 (One Bank Active)	I_{DD1}		190		185		165		145	mA	3,4
Precharge Standby Current in non power-down mode $t_{CK} = t_{CK(min)}$, $\overline{CS} \geq V_{IH(min)}$, $CKE \geq V_{IH(min)}$ Input signals are changed once during 30ns.	I_{DD2N}		95		85		75		65		3
Precharge Standby Current in non power-down mode $t_{CK} = \infty$, $CKE \geq V_{IH(min)}$, $CLK \leq V_{IL(max)}$ Input signals are stable	I_{DD2NS}		45		40		35		30		
Precharge Standby Current in power-down mode $t_{CK} = t_{CK}(min)$, $CKE \leq V_{IL(max)}$	I_{DD2P}		4		4		4		4		3
Precharge Standby Current in power-down mode $t_{CK} = \infty$, $CKE \leq V_{IL(max)}$, $CLK \leq V_{IL(max)}$	I_{DD2PS}		3.5		3.5		3.5		3.5		
Active Standby Current in non power down mode $CKE \geq V_{IH(min)}$, $t_{CK} = t_{CK(min)}$(Both Bank Actioe)	I_{DD3N}		85		75		65		55		3
Active Standby Current in power-down $CKE \leq V_{IL(max)}$, $t_{CK} = t_{CK(min)}$, $\overline{CS} \geq V_{IH(min)}$(Both Bank Active)	I_{DD3P}		6		6		6		6		
Operating Current (Page Burst, and All Bank activated) $t_{CCD} = t_{CCD(min)}$, Outputs Open, Multi-bank interleave, gapless data	I_{DD4}		195		185		175		165		4,5
Refresh Current $t_{RC} \geq t_{RC(min)}$ (t_{REF} = 64ms)	I_{DD5}		185		175		165		155		3
Self Refresh Current $CKE \leq 0.2V$	I_{DD6}		4		4		4		4		

A.C Characteristics:

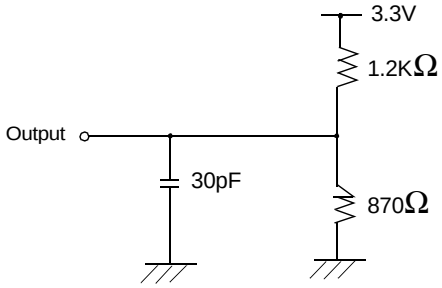
Test Conditions: (Ta=0 to 70°C V_{DD}=3.3V ±0.3V ,V_{SS}=0V)

symbol	A.C. Parameter		-5.5		-6		-7		-8		unit	note
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{CH}	Clock high time		2		2		2.5		3		ns	
t_{CL}	Clock low time		2		2		2.5		3			
t_T	Transition time (Rise and Fall)		0.5	10	0.5	10	0.5	10	0.5	10		
t_{CK3}	Clock cycle time	CL* = 3	5.5		6		7		8			
t_{CK2}		CL* = 2	8		8.5		10		12			
t_{IS}	Data/Address/Control Input setup time		2		2		2		2			
t_{IH}	Data/Address/Control Input hold time		1		1		1		1			
t_{LZ}	Data output low impedance		1		1		1		1			
t_{HZ3}	Data output high impedance	CL* = 3		4.5		5		5		7		
t_{HZ2}		CL* = 2		6		6.5		7		8		9
t_{AC3}	Access time from CLK (positive edge)	CL* = 3		5		5.5		6		7		
t_{AC2}		CL* = 2		7		7		7		8		
t_{OH}	Data output hold time		2.2		2.5		2.5		2.5			
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ delay		16.5		18		20		20			
t_{RRD}	Row activate to row activate delay		11		12		14		16			
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay time		1		1		1		1		CLK	
t_{WR}	Write recovery time		1t_{CK} +2ns		1t_{CK} +2ns		1		1		CLK	
t_{RAS}	Row activate to precharge time		33	100,000	36	100,000	40	100,000	48	100,000	ns	
t_{RP}	Precharge to refresh/row activate command		16.5		18		20			20	ns	
t_{DAL3}	Data-in to ACT (REF) Command (CL = 3)		2clk+ t_{RP}		2clk+ t_{RP}		2clk+ t_{RP}		2clk+ t_{RP}			
t_{DAL2}	Data-in to ACT (REF) Command (CL = 2)		1clk+t RP		1clk+ t_{RP}		1clk+ t_{RP}		1clk+ t_{RP}			
t_{RC}	Row cycle time		55		54		62		72		ns	
t_{RSC}	(Special) Mode Register Set Cycle time		2		2		2		2		CLK	
t_{REF}	Refresh time			64		64		64		64	ms	
t_{SRX}	Minimum CKE "High" for Self-Refresh exit		1		1		1		1		CLK	
t_{BDL}	Last data in to burst STOP command		1		1		1		1		CLK	
t_{PDE}	Power Down Exit set-up time		5		5		5		6		ns	

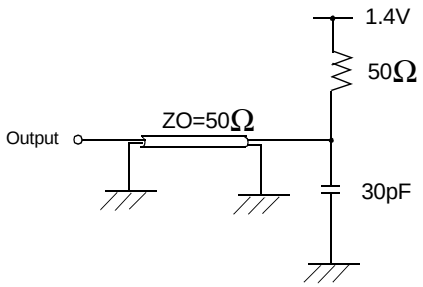
Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages are referenced to V_{SS}.
3. These parameters depend on the cycle rate and these values are measured by the cycle rate under the minimum value of t_{CK} and t_{RC}. Input signals are changed one time during t_{CK}. Assume that there are only one read/write cycle during t_{RC} (min).
4. These parameters depend on the output loading. Specified values are obtained with the output open.
5. Assume minimum column address update cycle t_{CCD} (min).
6. Power-up sequence is described in Note 10.
7. A.C. Test Conditions

Reference Level of Output Signals	1.4V / 1.4V
Output Load	Reference to the Under Output Load (B)
Input Signal Levels	3.0V / 0.0V
Transition Time (Rise and Fall) of Input Signals	1ns
Reference Level of Input Signals	1.4V



LVTTL D.C. Test Load (A)



LVTTL A.C. Test Load (B)

8. Transition times are measured between V_{IH} and V_{IL}. Transition (rise and fall) of input signals are fixed slope (1 ns).
9. t_{HZ} defines the time at which the outputs achieve the open circuit condition and are not reference levels.
10. Power up Sequence

    Power up must be performed in the following sequence.

    1) Power must be applied to V_{DD} and V_{DDQ} (simultaneously) when all input signals are held "NOP" state and CKE = "H", DQM = "H". The CLK signals must be started at the same time.

    2) After power-up, a pause of 200u secouds minimum is required. Then, it is recommended that DQM is held "high" (V_{DD} levels) to ensure DQ output to be in the high impedance.

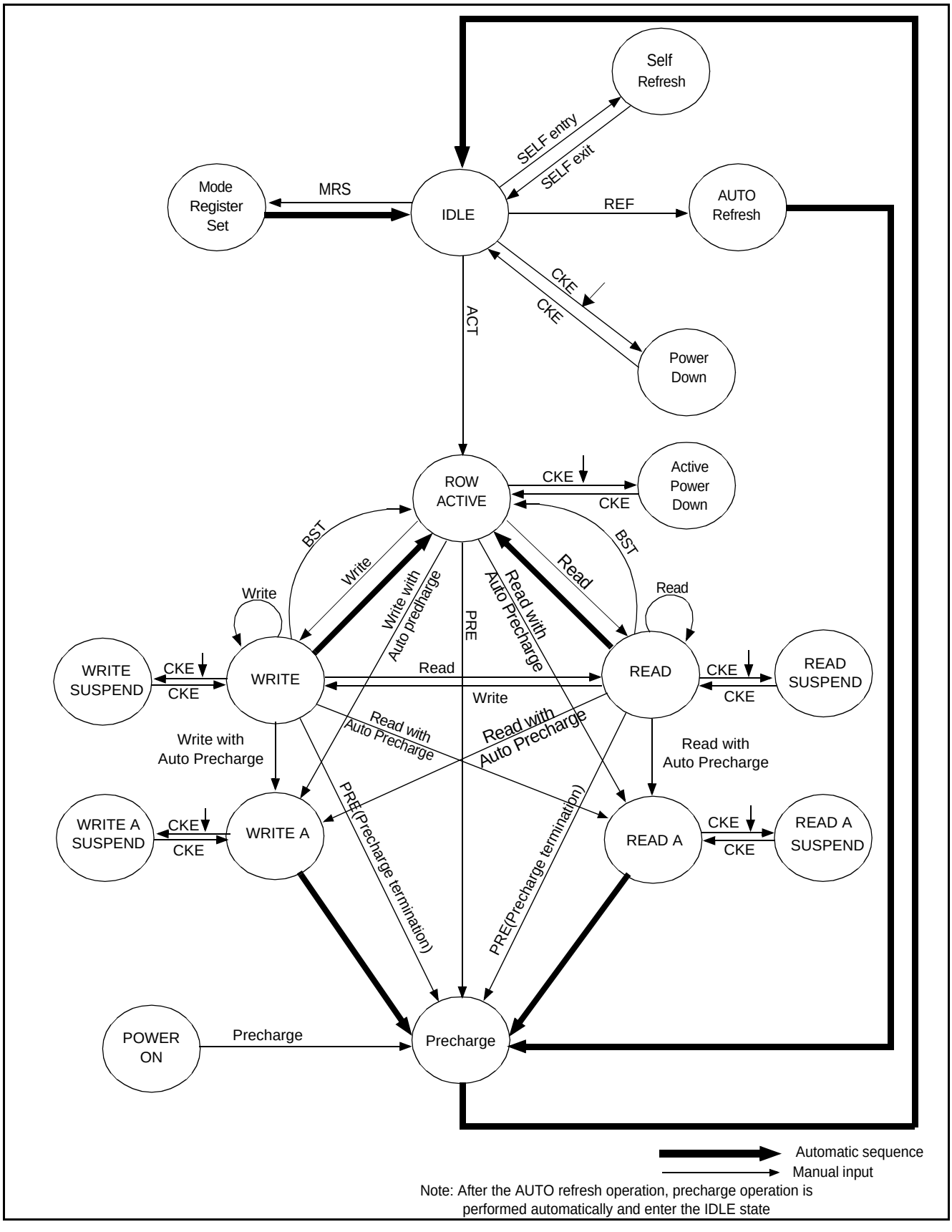
    3) Both banks must be precharged.

    4) Mode Register Set command must be asserted to initialize the Mode register.

5) A minimum of 8 Auto-Refresh dummy cycles must be required to stabilize the internal circuitry of the device. Sequence of 4 and 5 may be changed.

Basic Features and Function description

1.Simplified State Diagram



Note: After the AUTO refresh operation, precharge operation is performed automatically and enter the IDLE state

2.Truth Table

2.1 Command Truth Table

FUNCTION	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	A11	A10	A9-A0
		n-1	n							
Device deselect	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Mode register set	MRS	H	X	L	L	L	L	L	X	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto precharge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto precharge	WRITA	H	X	L	H	L	L	V	H	V
Precharge select bank	PRE	H	X	L	L	H	L	V	L	X
Precharge all banks	PALL	H	X	L	L	H	L	X	H	X
Burst stop	BST	H	X	L	H	H	L	X	X	X

2.2 DQM Truth Table

FUNCTION	Symbol	CKE		DQM	
		n-1	n-1	U	L
Data write/output enable	ENB	H	X	L	
Data mask/output disable	MASK	H	X	H	
Upper byte write enable/output enable	ENBU	H	X	L	X
Lower byte write enable/output enable	ENBL	H	X	X	L
Upper byte write inhibit/output disable	MASKU	H	X	H	X
Lower byte inhibit/output disable	MASKL	H	X	X	H

2.3 CKE Truth Table

Current State	Function	Symbol	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Add-ress
			n-1	n					
Activating	Clock suspend mode entry		H	L	X	X	X	X	X
Any	Clock suspend		L	L	X	X	X	X	X
Clock suspend	Clock suspend mode exit		L	H	X	X	X	X	X
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

H : High level, L : Low level
X : high or Low level(Dont care), V : Valid Data input

2.4 Operative Command Table

(1/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Command	Action	Notes
Idle	H	X	X	X	X	DESL	Nop or Power down	2
	L	H	H	X	X	NOP or BST	Nop or Power down	2
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BR,RA	ACT	Row active	
	L	L	H	L	BA,A10	PRE/PALL	Nop	
	L	L	L	H	X	REF/SELF	Refresh or Self refresh	4
	L	L	L	L	Op-Code	MPS	Mode register access	
Row active	H	X	X	X	X	DESL	Nop	
	L	H	H	X	X	NOP or BST	Nop	
	L	H	L	H	BA,CA,A10	READ/READA	Begin read:Determine AP	5
	L	H	L	L	BA,CA,A10	WRIT/WRITA	Begin write:Determine AP	5
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Precharge	6
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Read	H	X	X	X	X	DESL	Continue burst to end → Row active	
	L	H	H	H	X	NOP	Continue burst to end → Row active	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	READ/READA	Term burst, new read:Determine AP	7
	L	H	L	L	BA,CA,A10	WRIT/WRITA	Term burst, start write:Determine AP	7,8
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Term burst,precharging	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write	H	X	X	X	X	DESL	Continue burst to end → write recovering	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering	
	L	H	H	L	X	BST	Burst stop → Row active	
	L	H	L	H	BA,CA,A10	READ/READA	Term burst, start read: determine AP	7,8
	L	H	L	L	BA,CA,A10	WRIT/WRITA	Term burst, new write:Determine AP	7
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Term burst precharging	9
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(2/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CA}$	$\overline{WE}$	Address	Command	Action	Notes
Read with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Precharging	
	L	H	H	H	X	NOP	Continue burst to end → Precharging	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write with auto precharge	H	X	X	X	X	DESL	Continue burst to end → Write recovering with auto precharge	
	L	H	H	H	X	NOP	Continue burst to end → Write recovering with auto precharge	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-code	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESL	Nop → Enter idle after t_{RP}	
	L	H	H	H	X	NOP	Nop → Enter idle after t_{RP}	
	L	H	H	L	X	BST	Nop → Enter idle after t_{RP}	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	Nop → Enter idle after t_{RP}	
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESL	Nop → Enter row active after t_{RCD}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{RCD}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{RCD}	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3,10
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	

(3/3)

Current state	$\overline{CS}$	$\overline{RAS}$	$\overline{CA}$	$\overline{WE}$	Address	Command	Action	Notes
Write recovering	H	X	X	X	X	DESL	Nop → Enter row active after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter row active after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter row active after t_{DPL}	
	L	H	L	H	BA,CA,A10	READ/READA	Start read, Determine AP	8
	L	H	L	L	BA,CA,A10	WRIT/WRITA	New write, Determine AP	
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	PRE/PALL	ILLEGAL	3
	L	L	L	H	X	PEF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Write recovering with auto precharge	H	X	X	X	X	DESL	Nop → Enter precharge after t_{DPL}	
	L	H	H	H	X	NOP	Nop → Enter precharge after t_{DPL}	
	L	H	H	L	X	BST	Nop → Enter precharge after t_{DPL}	
	L	H	L	H	BA,CA,A10	READ/READA	ILLEGAL	3,8
	L	H	L	L	BA,CA,A10	WRIT/WRITA	ILLEGAL	3
	L	L	H	H	BA,RA	ACT	ILLEGAL	3
	L	L	H	L	BA,A10	REF/PALL	ILLEGAL	3
	L	L	L	H	X	REF/SELF	ILLEGAL	
	L	L	L	L	Op-Code	MRS	ILLEGAL	
Refreshing	H	X	X	X	X	DESL	Nop → Enter idle after t_{RC}	
	L	H	H	X	X	NOP/BST	Nop → Enter idle after t_{RC}	
	L	H	L	X	X	READ/WRIT	ILLEGAL	
	L	L	H	X	X	ACT/PRE/PALL	ILLEGAL	
	L	L	L	X	X	REF/SELF/MRS	ILLEGAL	
Mode register accessing	H	X	X	X	X	DESL	Nop → Enter idle after 2 Clocks	
	L	H	H	H	X	NOP	Nop → Enter idle after 2 Clocks	
	L	H	H	L	X	BST	ILLEGAL	
	L	H	L	X	X	READ/WRITE	ILLEGAL	
	L	L	X	X	X	ACT/PRE/PALL/ REF/SELF/MRS	ILLEGAL	

Note 1. All entries assume that CKE was active (High level)during the preceding clock cycle.
2. If both banks are idle, and CKE is inactive(Low level), the device will enter Power down mode. All input buffers except CKE will be disabled.
3. Illegal to bank in specified states; Function may be legal in the bank indicated by Bank Address (BA), depending on the state of that bank.
4. If both banks are idle, and CKE is inactive(Low level), the device will enter Self refresh mode. All input buffers except CKE will be disabled.
5. Illegal if t_{RCD} is not satisfied.
6. Illegal if t_{RAS} is not satisfied.
7. Must satisfy burst interrupt condition.
8. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
9. Must mask preceding data if t_{DPL} is not satisfied.
10. Illegal if t_{RRD} is not satisfied.

2.5 Command Truth Table for CKE

Current state	$\overline{CKE}$ n-1	$\overline{RAS}$ n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	Address	Action	Notes
Self refresh (S.R.)	H	X	X	X	X	X	X	INVALID,CLK(n-1)would exit S.R.	
	L	H	H	X	X	X	X	S.R. Recovery	2
	L	H	L	H	H	X	X	S.R. Recovery	2
	L	H	L	H	L	X	X	ILLEGAL	2
	L	H	L	L	X	X	X	ILLEGAL	2
	L	L	X	X	X	X	X	Maintain S.R.	
Self refresh recovery	H	H	H	X	X	X	X	Idle after t_{RC}	
	H	H	L	H	H	X	X	Idle after t_{RC}	
	H	H	L	H	L	X	X	ILLEGAL	
	H	H	L	L	X	X	X	ILLEGAL	
	H	L	H	X	X	X	X	Begin clock suspend next cycle	5
	H	L	L	H	H	X	X	Begin clock suspend next cycle	5
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	X	X	X	ILLEGAL	
	L	H	X	X	X	X	X	Exit clock suspend next cycle	2
	L	L	X	X	X	X	X	Maintain clock suspend	
Power down (P.D.)	H	X	X	X	X	X		INVALID, CLK(n-1) would exit P.D.	
	L	H	X	X	X	X	X	EXIT P.D. $\rightarrow$ Idle	2
	L	L	X	X	X	X	X	Maintain power down mode	
Both banks idle	H	H	H	X	X	X		Refer to operations in Operative Command Table	
	H	H	L	H	X	X		Refer to operations in Operative Command Table	
	H	H	L	L	H	X		Refer to operation in Operative Command Table	
	H	H	L	L	L	H	X	Refresh	
	H	H	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	H	L	H	X	X	X		Refer to operations in Operative Command Table	
	H	L	L	H	X	X		Refer to operations in Operative Command Table	
	H	L	L	L	H	X		Refer to operations in Operative Command Table	
	H	L	L	L	L	H	X	Self refresh	3
	H	L	L	L	L	L	Op-Code	Refer to operations in Operative Command Table	
	L	X	X	X	X	X	X	Power down	3
Any state other than listed above	H	H	X	X	X	X	X	Refer to operations in Operative Command Table	
	H	L	X	X	X	X	X	Begin clock suspend next cycle	4
	L	H	X	X	X	X	X	Exit clock suspend next cycle	
	L	L	X	X	X	X	X	Maintain clock suspend	

Note 1. H : Hight level, L : low level, X : High or low level(Don't care).
2. CKE Low to High transition will re-enable CLK and other inputs asynchronously. A minimum setup time must be satisfied before any command other than EXIT.
3. Power down and Self refresh can be entered only from the both banks idle state.
4. Must be legal command as defined in Operative Command Table.
5 .Illegal if t_{SRX} is not satisfied.

3.Initiallization

The synchronous DRAM is initialized in the power on sequence. Once power has been applied, a 100us minimum delay is needed in which stable power and input signals are maintained. During this delay, CKE and DQM recommend to be held high.

After the 100us delay, both banks must be precharged using the precharge command. Once precharge is completed and the minimum t_{RP} is satisfied, the mode register can be programmed.

Minimum two CBR refresh commands must be performed before or after the mode register set command.

4.Programming the Mode Register

The mode register is programmed by the mode register set command using address bits A11 through A0 as data inputs. The register retains data until it is reprogrammed or until the device loses power.

The mode register has four fields;

Options	: A11 through A7
CAS latency	: A6 through A4
Wrap type	: A3
Burst length	: A2 through A0

Following mode register programming, no command can be asserted befor at least two clock cycles have elapsed.

$\overline{\text{CAS}}$ Latency

$\overline{\text{CAS}}$ latency is the most critical parameter to be set. It tells the device how many clocks must elapse before the data will be available. The SDRAM is capable of reconfiguring its internal architecture based on the value of $\overline{\text{CAS}}$ latency.

The value is determined by the frequency of the clock and the speed grade of the device. The value can be programmed as 2 or 3.

Burst Length

Burst Length is the number of words that will be output or input in read or write cycle. After a read burst is completed, the output bus will become high impedance.

The burst length is programmable as 1,2,4,8 or full page.

Wrap Type (Burst Sequence)

The wrap type specifies the order in which the burst data will be addressed. The order is programmable as either "Sequential" or "Interleave". The method chosen will depend on the type of CPU in the system.

Some microprocessor cache systems are optimized for sequential addressing and others for interleaved addressing. Both sequences support bursts of 1,2,4 and 8. Only the sequential burst. supports the full-page length.

5.Mode Register

11	10	9	8	7	6	5	4	3	2	1	0	
0	0	0	0	1								Reserved Test Set
x	x	1	0	0	LTMODE			WT	BL			Burst Read and Single Write
x	x	0	0	0	LTMODE			WT	BL			Mode Register Set

X=Dont care

	Bits2-0	WT=0	WT=1
Burst length	000	1	1
	001	2	2
	010	4	4
	011	8	8
	100	R	R
	101	R	R
	110	R	R
	111	Full page	R

Wrap type	0	Sequential
	1	Interleave

	Bits6-4	$\overline{CAS}$ latency
Latency mode	000	R
	001	R
	010	2
	011	3
	100	R
	101	R
	110	R
	111	R

Remark R:Reserved

5.1 Burst Length and Sequence

(Burst of Two)

Starting Address (column address A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence(decimal)
0	0,1	0,1
1	1,0	1,0

(Burst of Four)

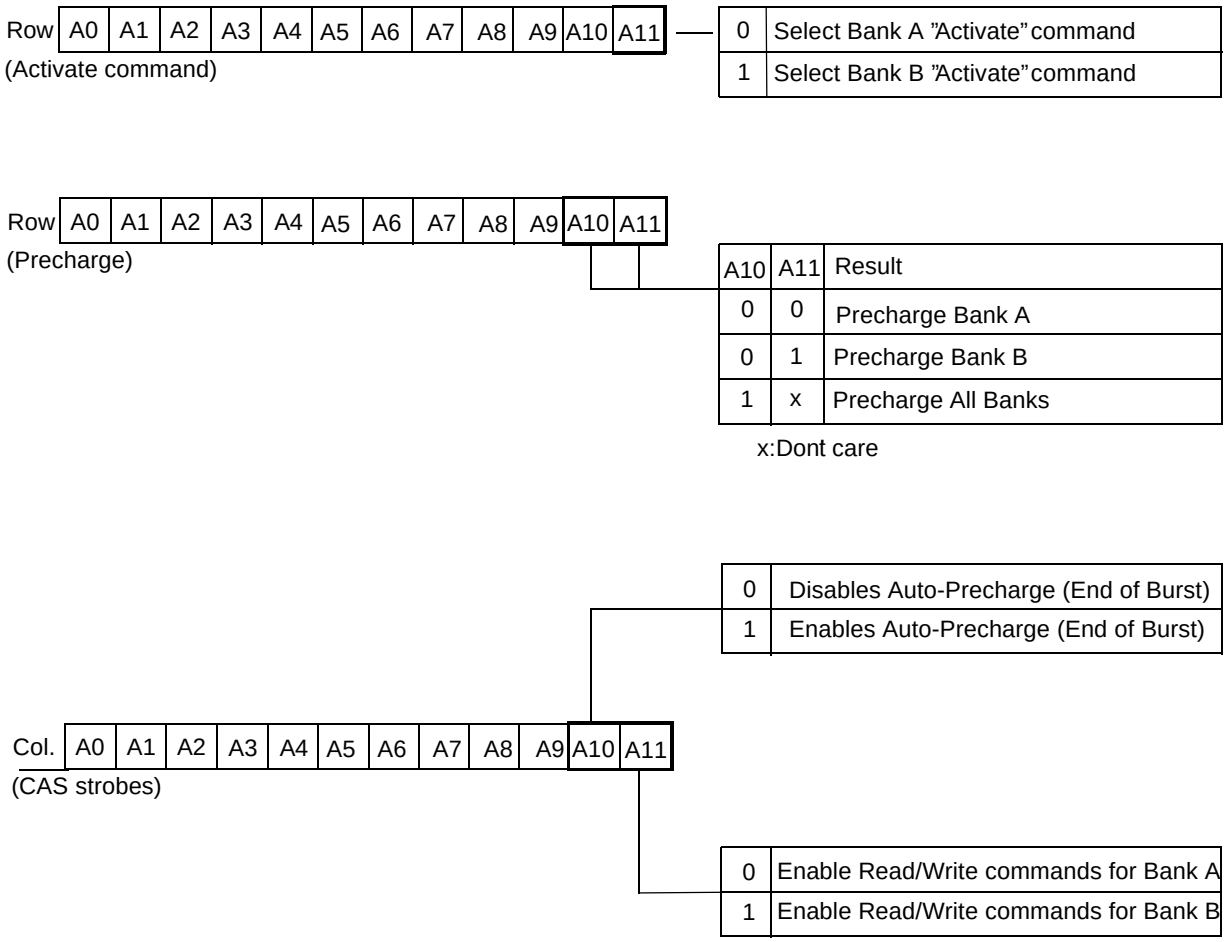
Starting Address (column address A1-A0, binary)	Sequential Addressing Sequence (decimal)	Interleave Addressing Sequence(decimal)
00	0,1,2,3	0,1,2,3
01	1,2,3,0	1,0,3,2
10	2,3,0,1	2,3,0,1
11	3,0,1,2	3,2,1,0

(Burst of Eight)

Starting Address (column address A2-A0, binary)	Sequential Addressing Sequence (decimal)	Interl eave Addressing Sequence(decimal)
000	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7
001	1,2,3,4,5,6,7,0	1,0,3,2,5,4,7,6
010	2,3,4,5,6,7,0,1	2,3,0,1,6,7,4,5
011	3,4,5,6,7,0,1,2	3,2,1,0,7,6,5,4
100	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3
101	5,6,7,0,1,2,3,4	5,4,7,6,1,0,3,2
110	6,7,0,1,2,3,4,5	6,7,4,5,2,3,0,1
111	7,0,1,2,3,4,5,6	7,6,5,4,3,2,1,0

Full page burst is an extension of the above tables of sequential addressing, with the length being 512/ 256 words for 2Mx8/1Mx16 devices, respectively.

6.Address Bits of Bank-Select and Precharge



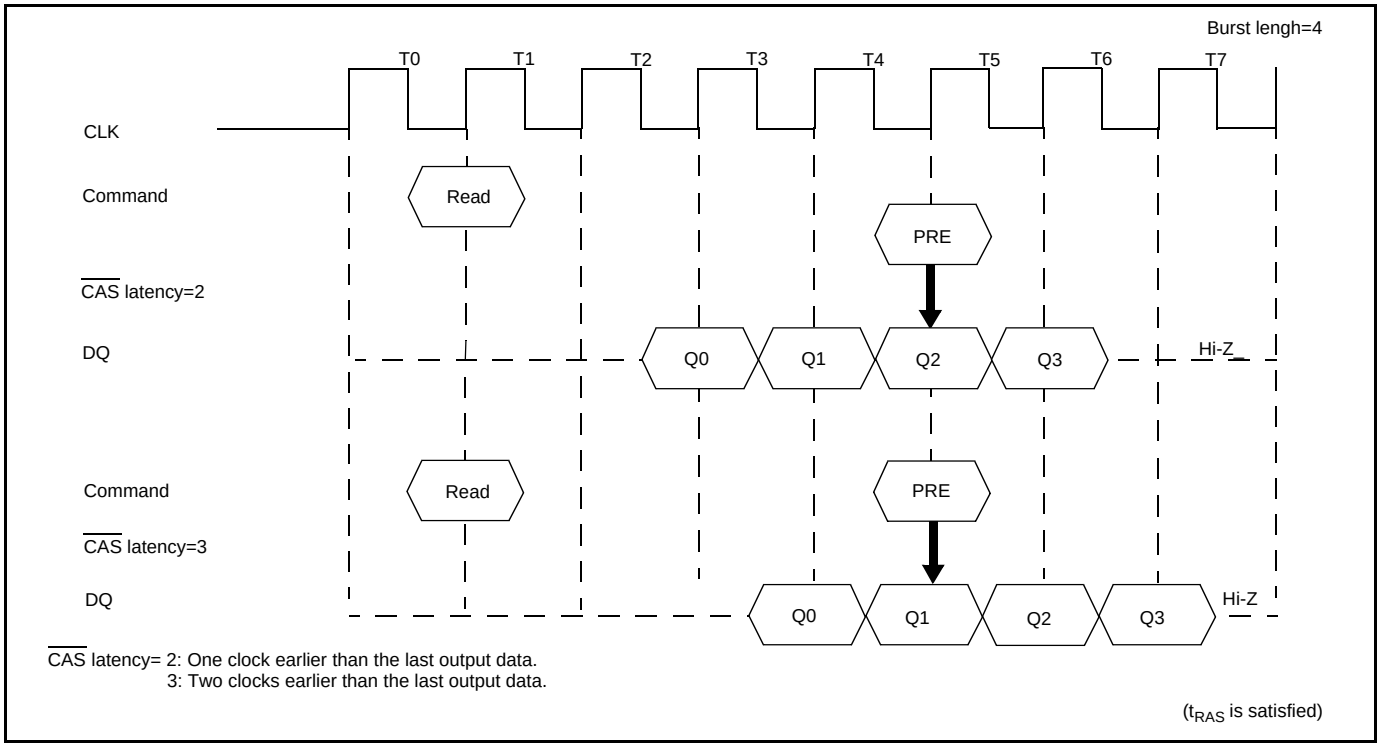
7.PRECHARGE

The PRECHARGE command can be asserted anytime after $t_{RAS(min)}$ is satisfied.

Soon after the PRECHARGE command is asserted, PRECHARGE operation is performed. The synchronous DRAM enters the idle state after $t_{RP(min)}$ is satisfied. The parameter t_{RP} is the time required to perform the PRECHARGE.

The earliest timing in a READ cycle that a PRECHARGE command can be asserted without losing any data in the burst is as followed.

PRECHARGE



In order to write all data to the memory cell correctly, the asynchronous parameter "t_{DPL}" must be satisfied. The $t_{DPL(MIN.)}$ specification defines the earliest time that a PRECHARGE command can be asserted after a WRITE cycle. The minimum number of clocks are calculated by dividing $t_{DPL(min.)}$ by the clock cycle time.

In summary, the PRECHARGE command can be asserted relative to the reference clock of the last valid data. In the following table, minus means clocks before the reference, plus means time after the reference.

$\overline{CAS}$ latency	READ	WRITE
2	-1	$+t_{DPL(min.)}$
3	-2	$+t_{DPL(min)}$

8.AUTO PRECHARGE

During a READ or WRITE command cycle, A10 controls whether AUTO PRECHARGE is selected. If A10 is high in the READ or WRITE command (READ with AUTO PRECHARGE command or WRITE with AUTO PRECHARGE command), AUTO PRECHARGE is selected and precharging begins automatically after the burst access.

In the WRITE cycle, $t_{DAL(min.)}$ must be satisfied to assert the next active command to the bank being precharged.

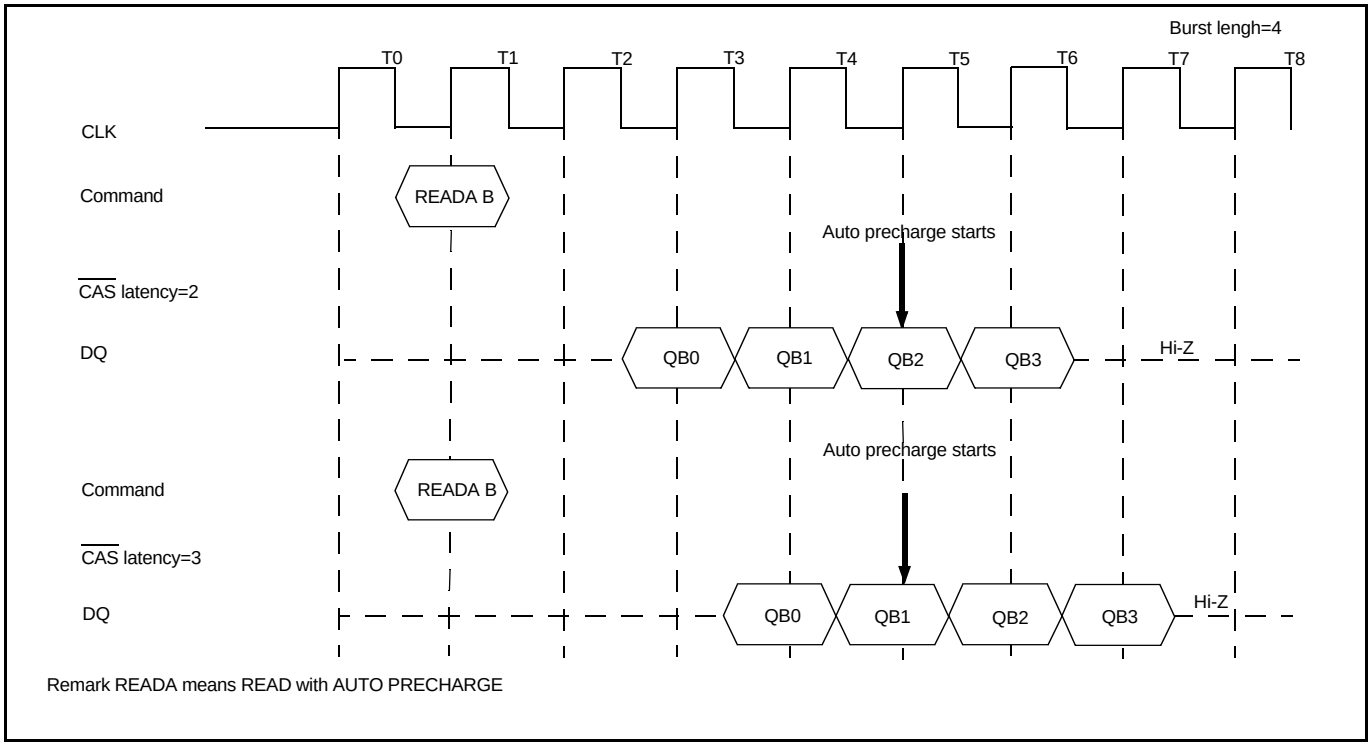
When using AUTO PRECHARGE in the READ cycle, knowing when the PRECHARGE starts is important because the t_{RAS} must be satisfied. Once AUTO PRECHARGE has started, an active command to the bank can be asserted after $t_{RP(min.)}$ has been satisfied.

The timing at which the AUTO PRECHARGE cycle begins depends both on the $\overline{CAS}$ latency programmed into the mode register and on whether the cycle is READ or WRITE.

8.1 READ with AUTO PRECHARGE

During a READA cycle, the AUTO PRECHARGE begins one clock earlier($\overline{CAS}$ latency of 2) or two clocks earlier($\overline{CAS}$ latency of 3) than the last data word output.

READ with AUTO PRECHARGE

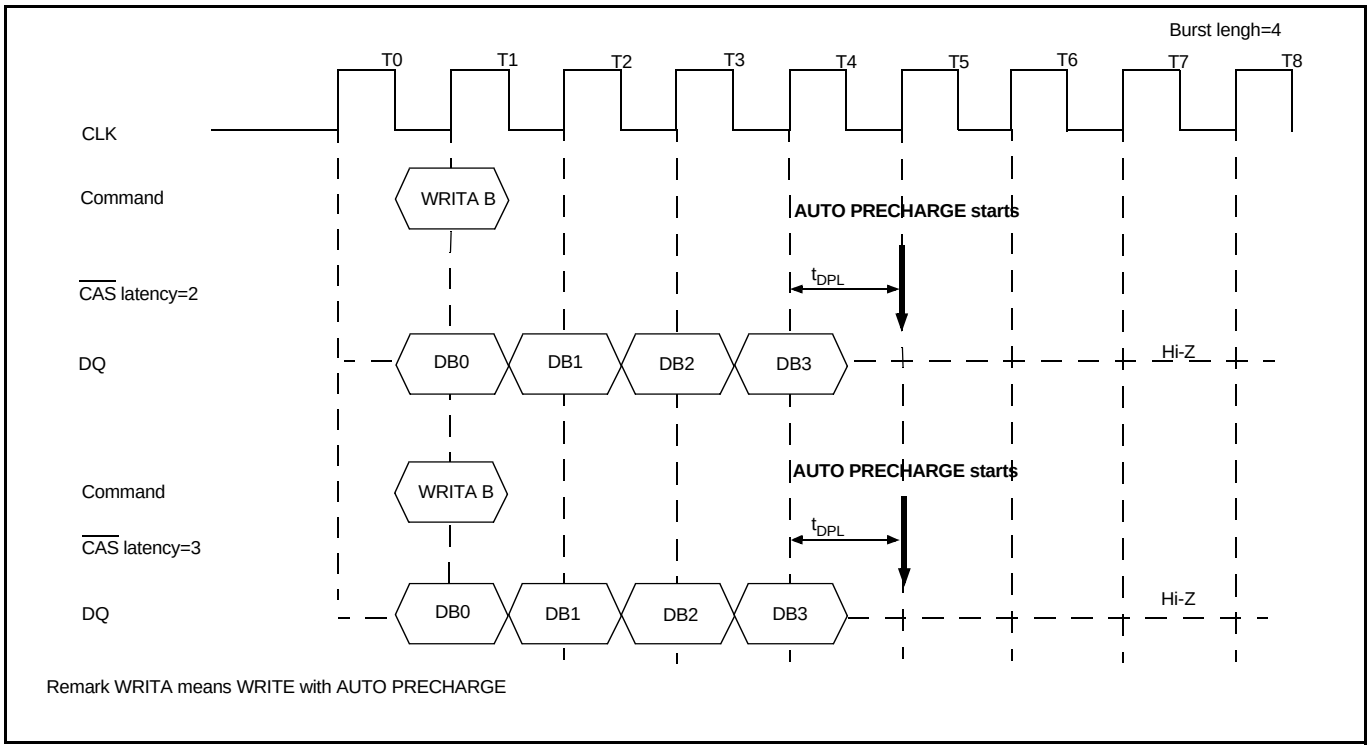


Remark READA means READ with AUTO PRECHARGE

8.2 WRITE with AUTO PRECHARGE

During a WRITA cycle, the AUTO PRECHARGE starts at $t_{DPL(min.)}$ after the last data word input to the device

WRITE with AUTO PRECHRGE



In summary, the auto precharge cycle begins relative to a reference clock that indicates the last data word is valid.
In the table below, minus means clocks before the reference; plus means clocks after the reference.

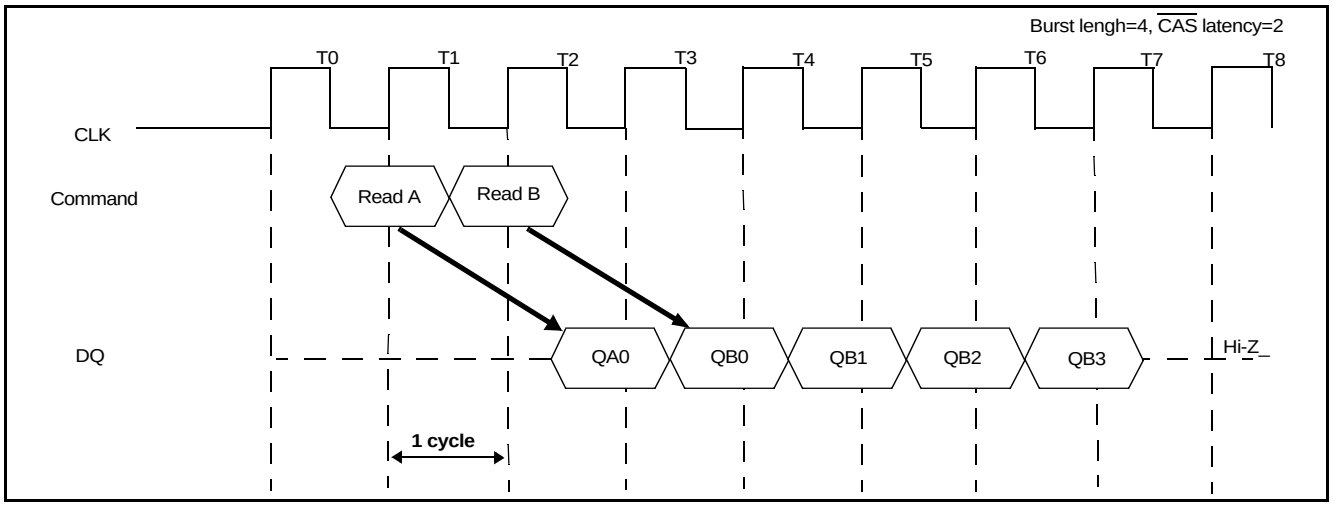
$\overline{CAS}$ latency	READ	WRITE
2	-1	$+t_{DPL(min.)}$
3	-2	$+t_{DPL(min)}$

9.READ/WRITE Command Interval

9.1 READ to READ command interval

When a new READ command is asserted during a READ cycle, it will be effective after the CAS latency, even if the previous READ operation has not completed. READ will be interrupted by another READ.
A READ command can be asserted in every clock without restriction.

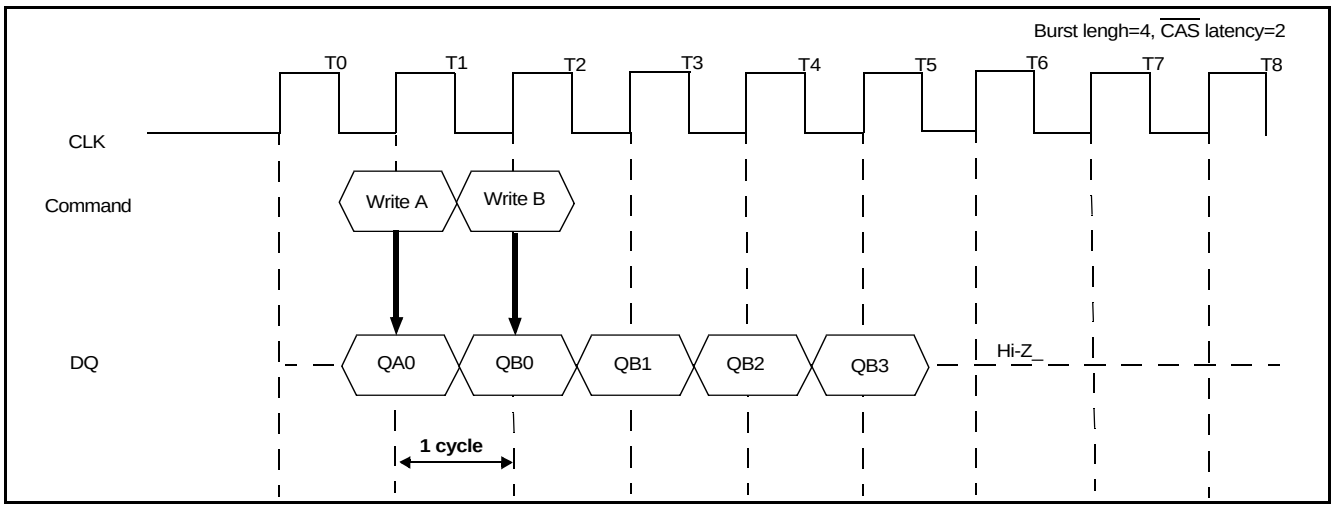
READ to READ Command Interval



9.2 WRITE to WRITE Command Interval

When a new WRITE command is asserted during a WRITE cycle, the previous burst will be terminated and the new burst will begin with the new WRITE command. WRITE will be interrupted by another WRITE.
A WRITE command can be asserted in every clock without restriction.

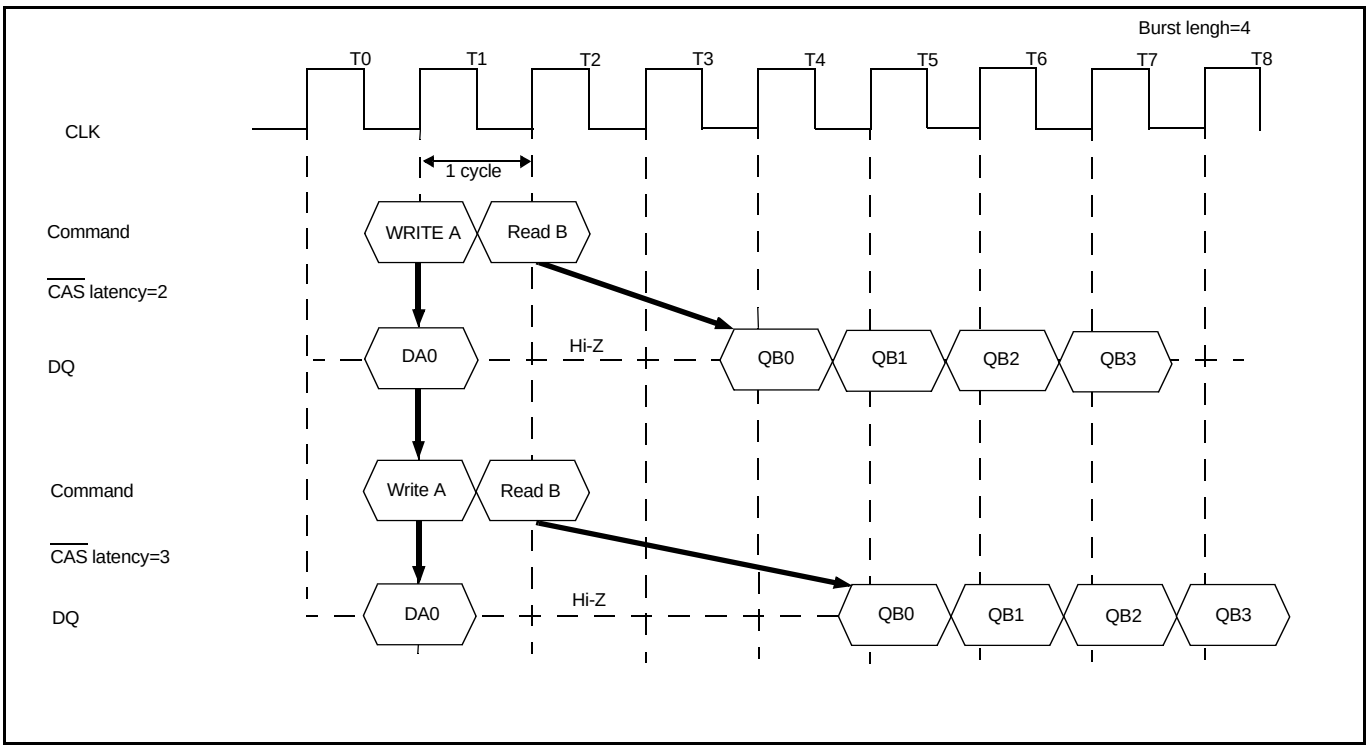
WRITE to WRITE Command Interval



9.3 WRITE to READ Command Interval

The WRITE command to READ command interval is a minimum of 1 cycle. Only the WRITE data preceding the READ command will be written. The data bus must be in high-impedance at least one cycle prior to the first D_{OUT}.

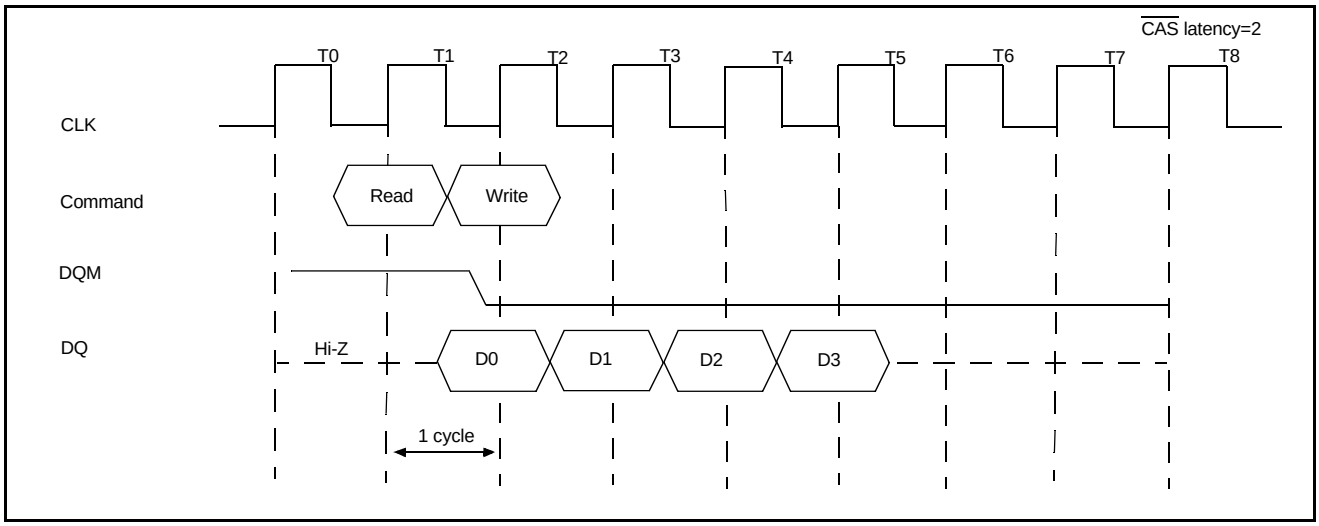
WRITE to READ Command Interval

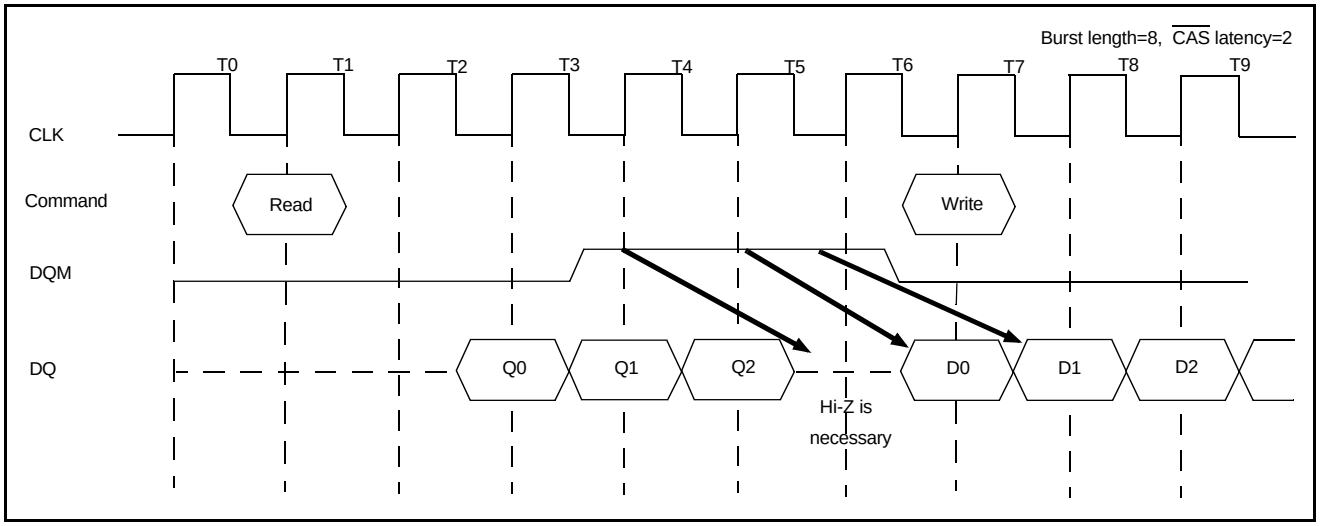


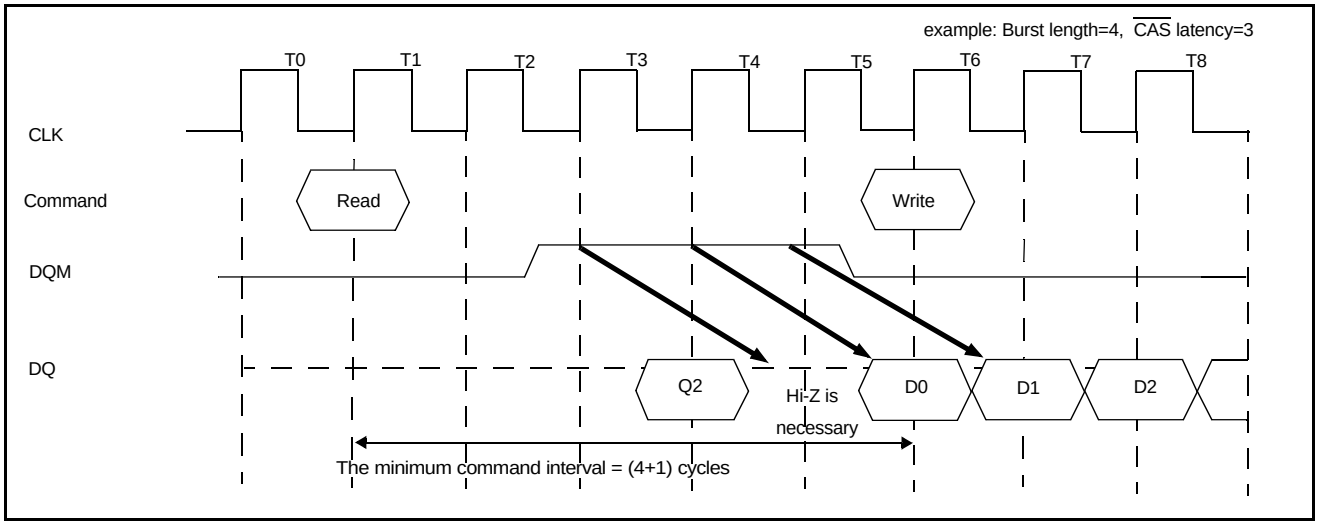
9.4 READ to WRITE Command Interval

During READ cycle, READ can be interrupted by WRITE. The data bus must be in high-impedance using DQM before the WRITE command. DQM must be high at least 3 clocks prior to the WRITE command. This restriction is necessary to avoid a data bus conflict.

READ to WRITE Command Interval







10.BURST TERMINATION

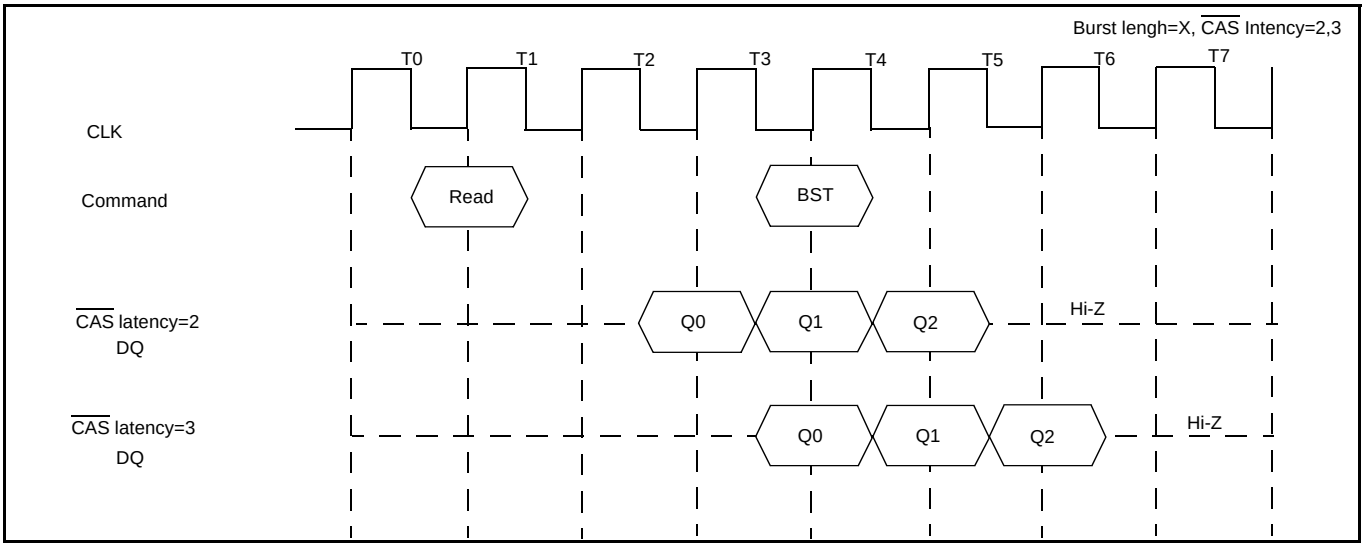
There are two methods to terminate a BURST operation other than using a READ or a WRITE command. One is the BURST STOP command and the other is the PRECHARGE command.

10.1 BURST STOP Command

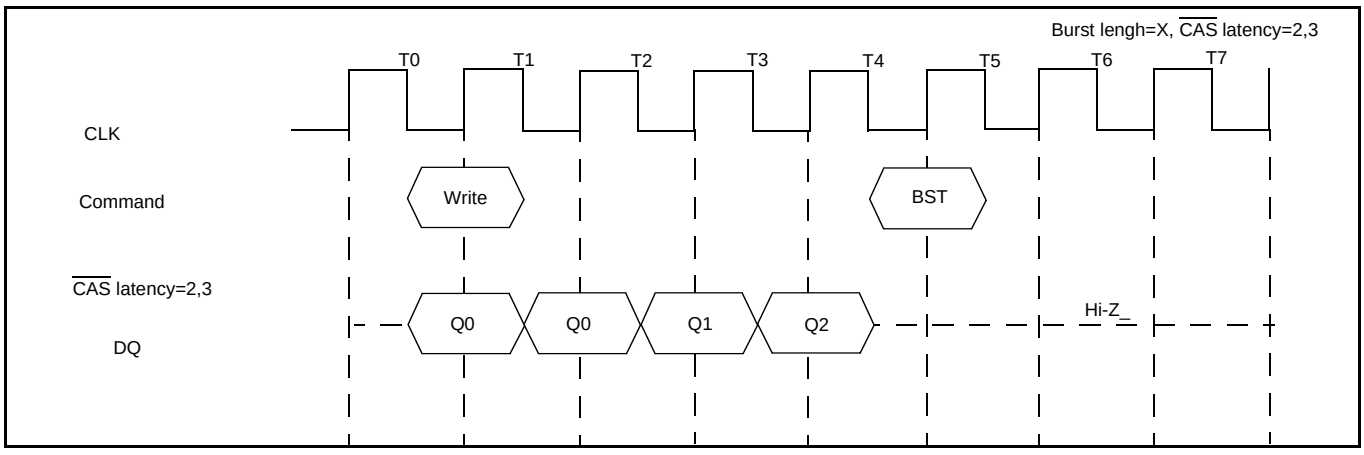
During a READ BURST. when the BURST STOP command is asserted, the BURST READ outputs are terminated and the data bus goes to high-impedance after the $\overline{\text{CAS}}$ latency from the BURST STOP command.

During a WRITE BURST. when the BURST STOP command is asserted, any data provided at that cycle will not be written. The BURST WRITE is effectively terminated and no further data can be written until a new WRITE command is asserted.

Burst Termination



Remark BST: Burst stop command



Remark BST: Burst stop command

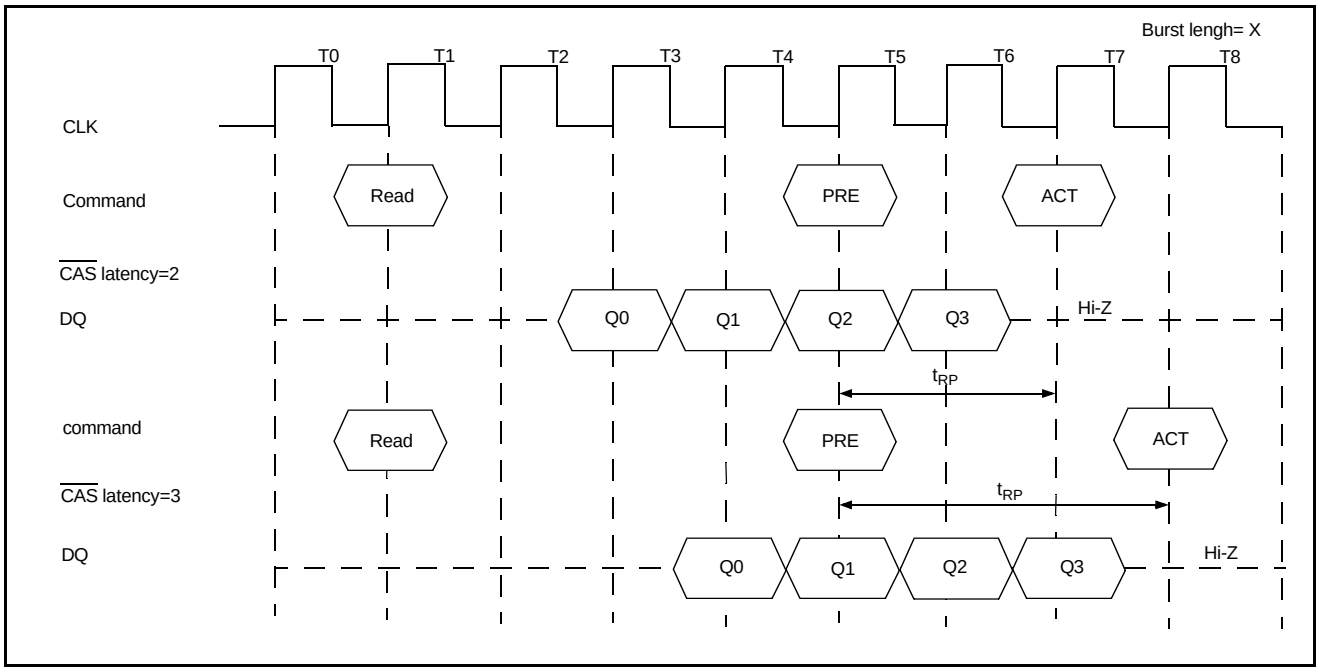
10.2 PRECHARGE TERMINATION

10.2.1 PRECHARGE TERMINATION in READ Cycle

During a READ cycle, the BURST READ operation can be terminated by a PRECHARGE command. When the PRECHARGE command is asserted, the BURST READ operation is terminated and PRECHARGE starts.

Read data will remain valid until one clock($\overline{CAS}$ latency of 2)or two clocks($\overline{CAS}$ latency of 3) after the PRECHARGE command and the same bank can be activated again after $t_{RP(min)}$ from the PRECHARGE command.

PRECHARGE TERMINATION in READ Cycle



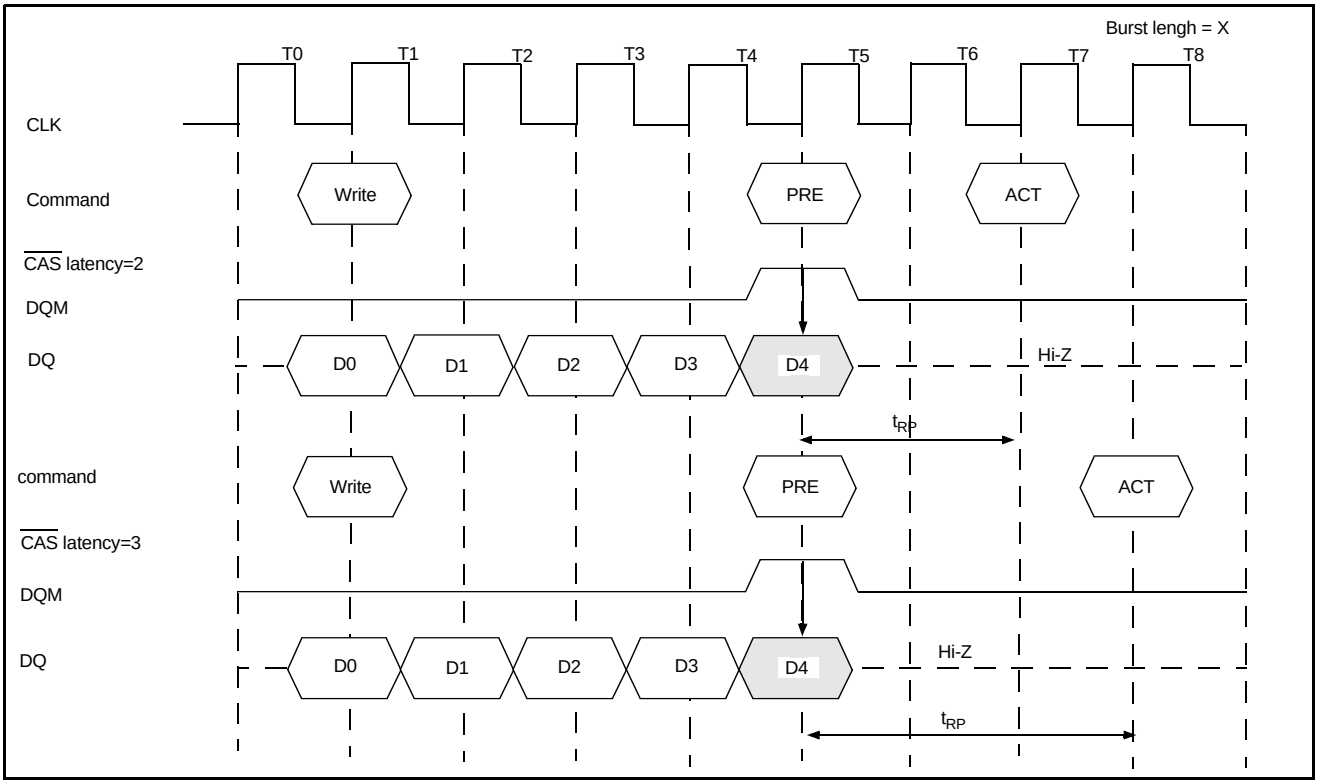
10.2.2 PRECHARGE TERMINATION in WRITE Cycle

During a WRITE cycle, the BURST WRITE operation can be terminated by a PRECHARGE command. when the PRECHARGE command is asserted, the BURST WRITE operation in immediately terminated and PRECHARGE starts.

The same bank can be activated again after tRP(min.) from the PRECHARGE command. The DQM must be high to mask invalid data in.

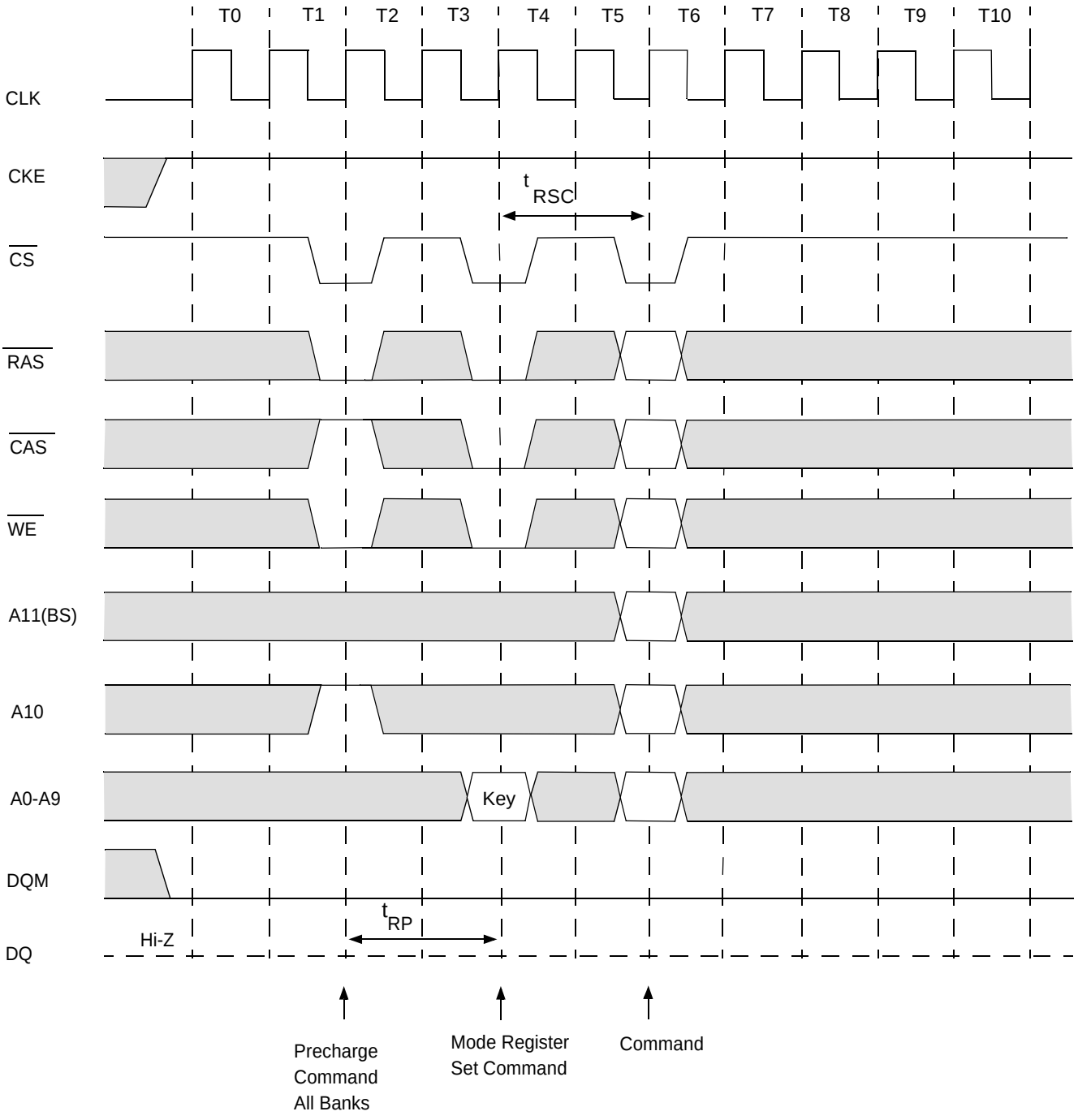
When CAS latency is 2 or 3, the data written prior to the PRECHARGE command will be correctly stored. However, invalid data may be written at the same clock as the PRECHARGE command. To prevent this from happening, DQM must be high at the same clock as the PRECHARGE command. This will mask the invalid data.

PRECHARGE TERMINATION in WRITE Cycle



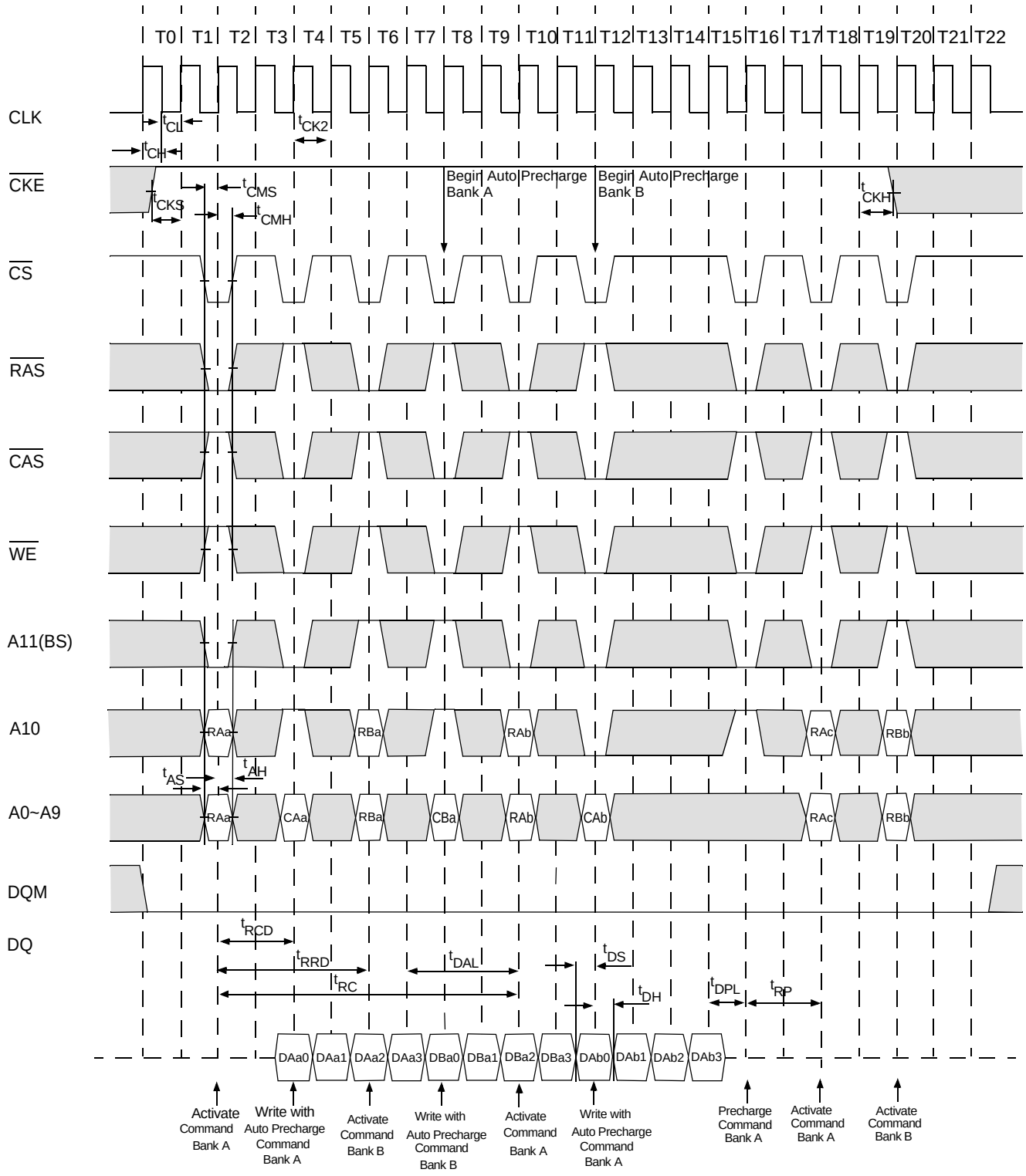
Timing Diagram

Mode Register Set



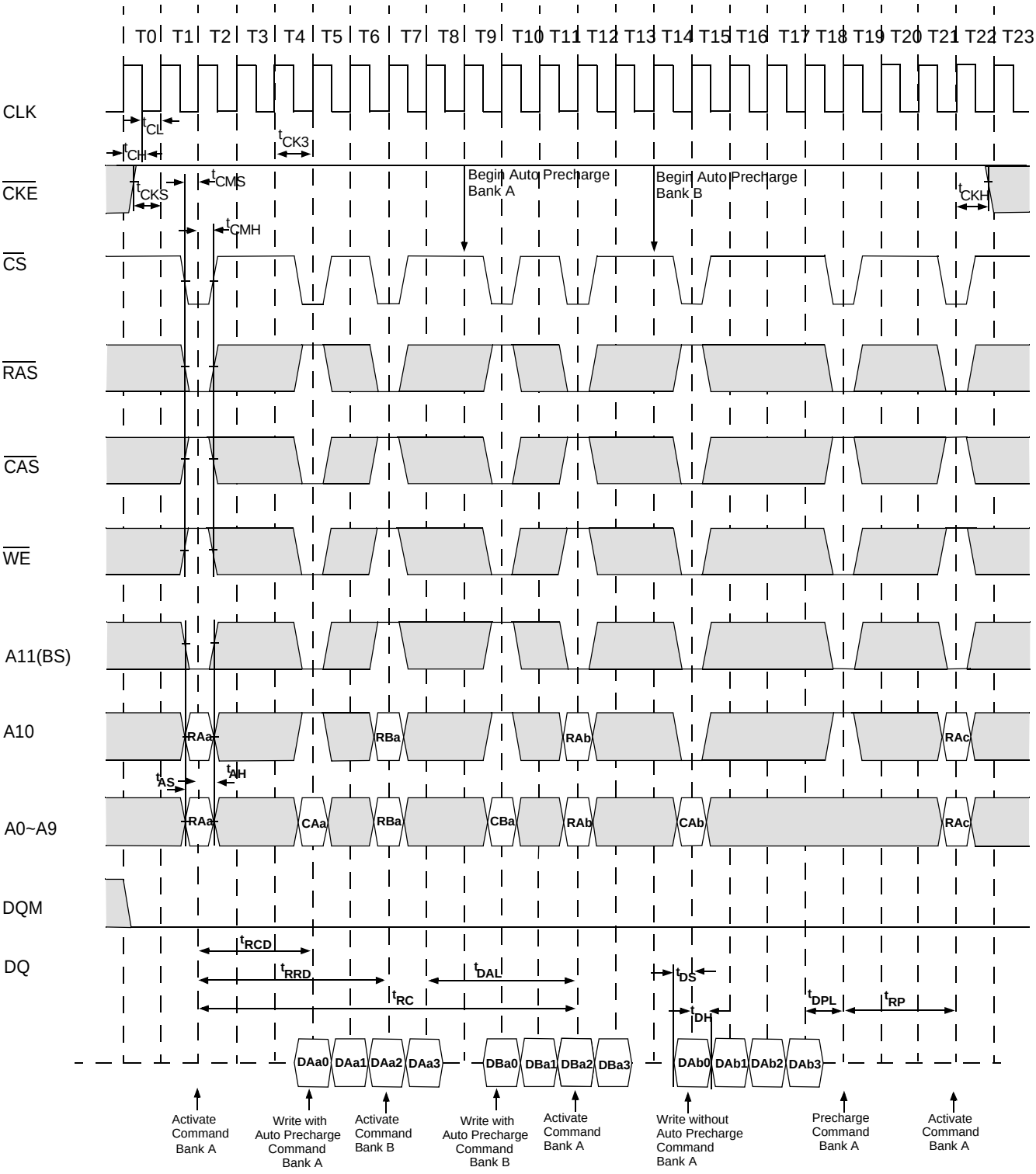
AC Parameters for Write Timing (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



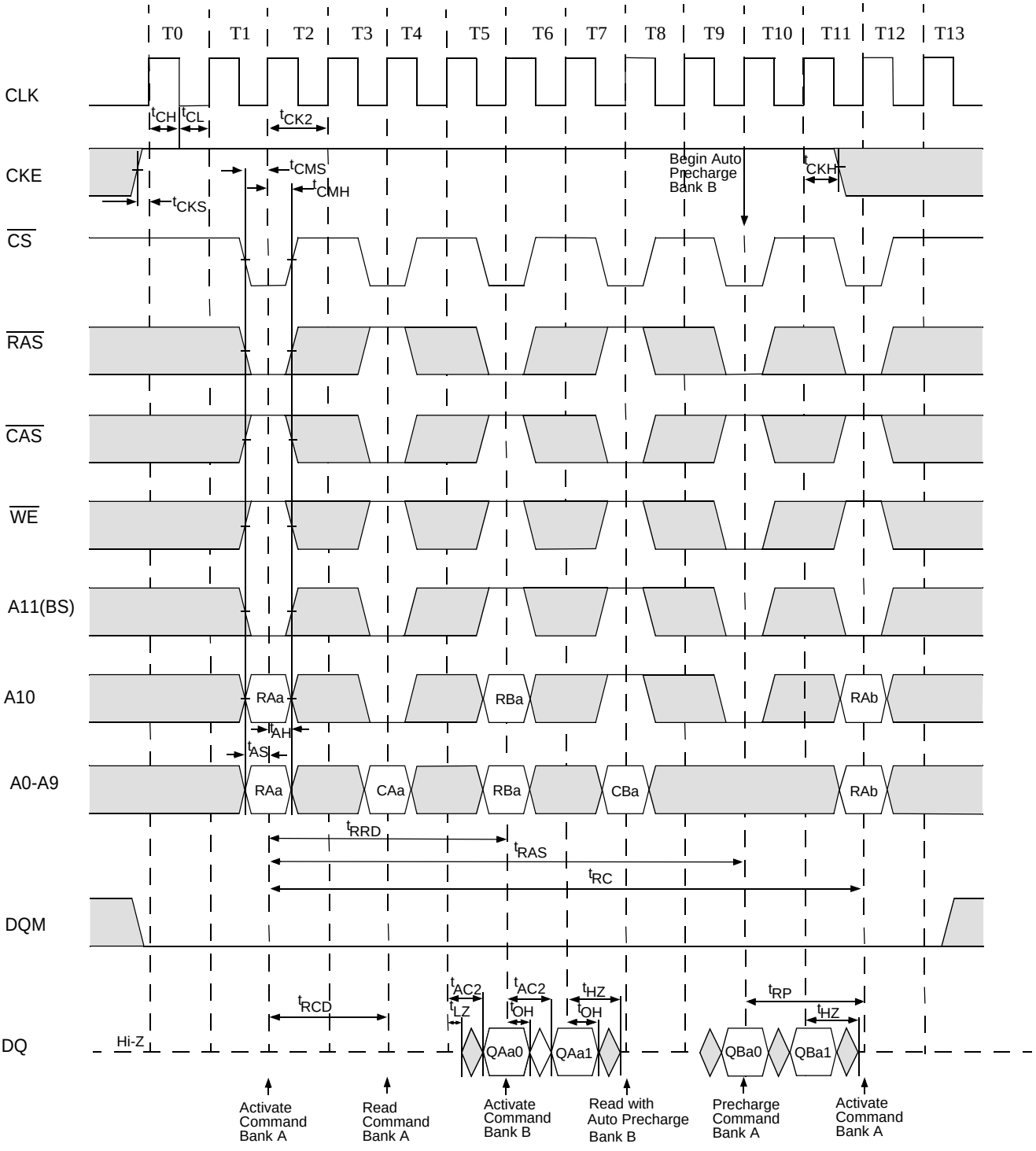
AC Parameters for Write Timing (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



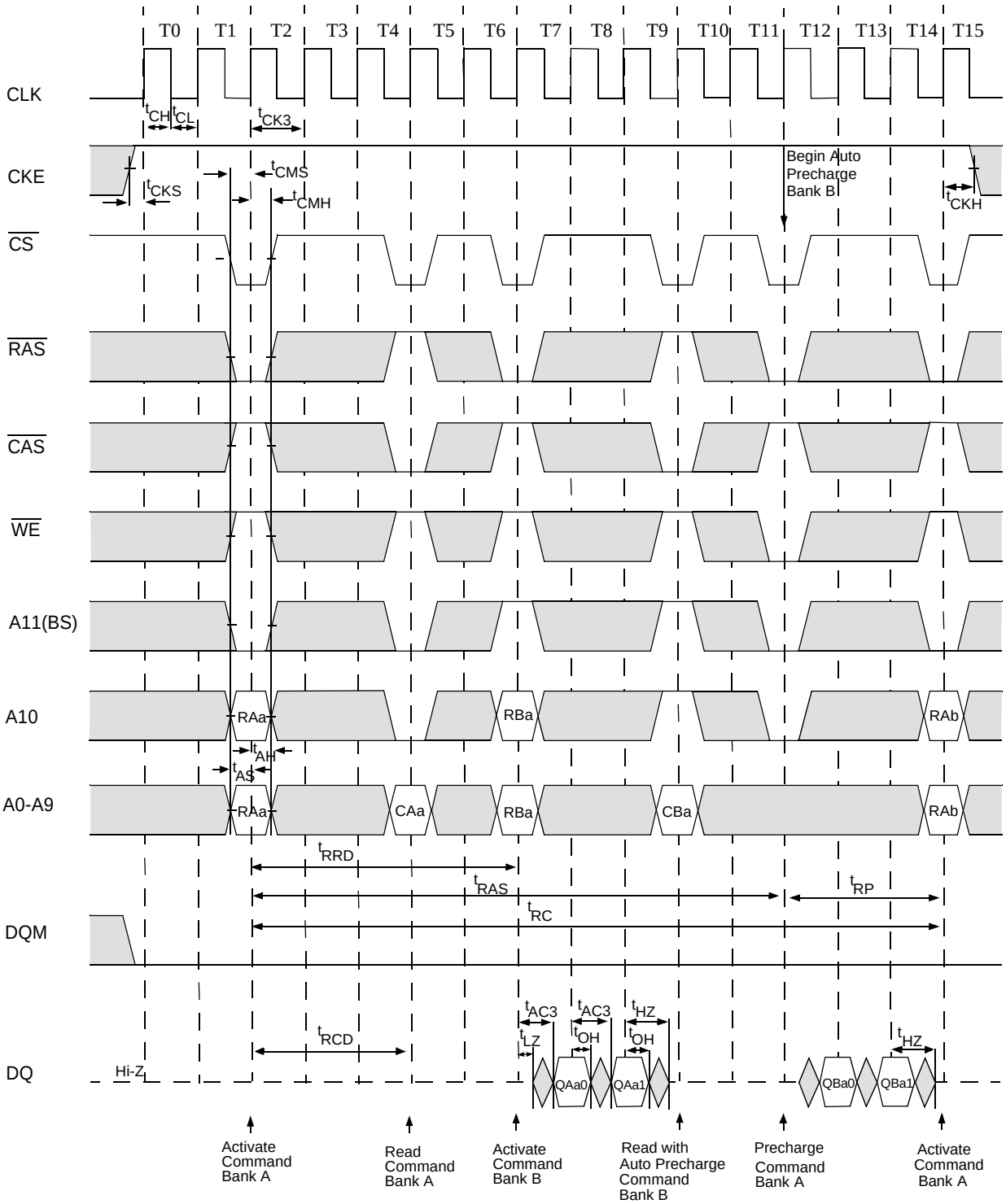
AC Parameters for Read Timing (1 of 2)

Burst Length=2, $\overline{CAS}$ Latency=2

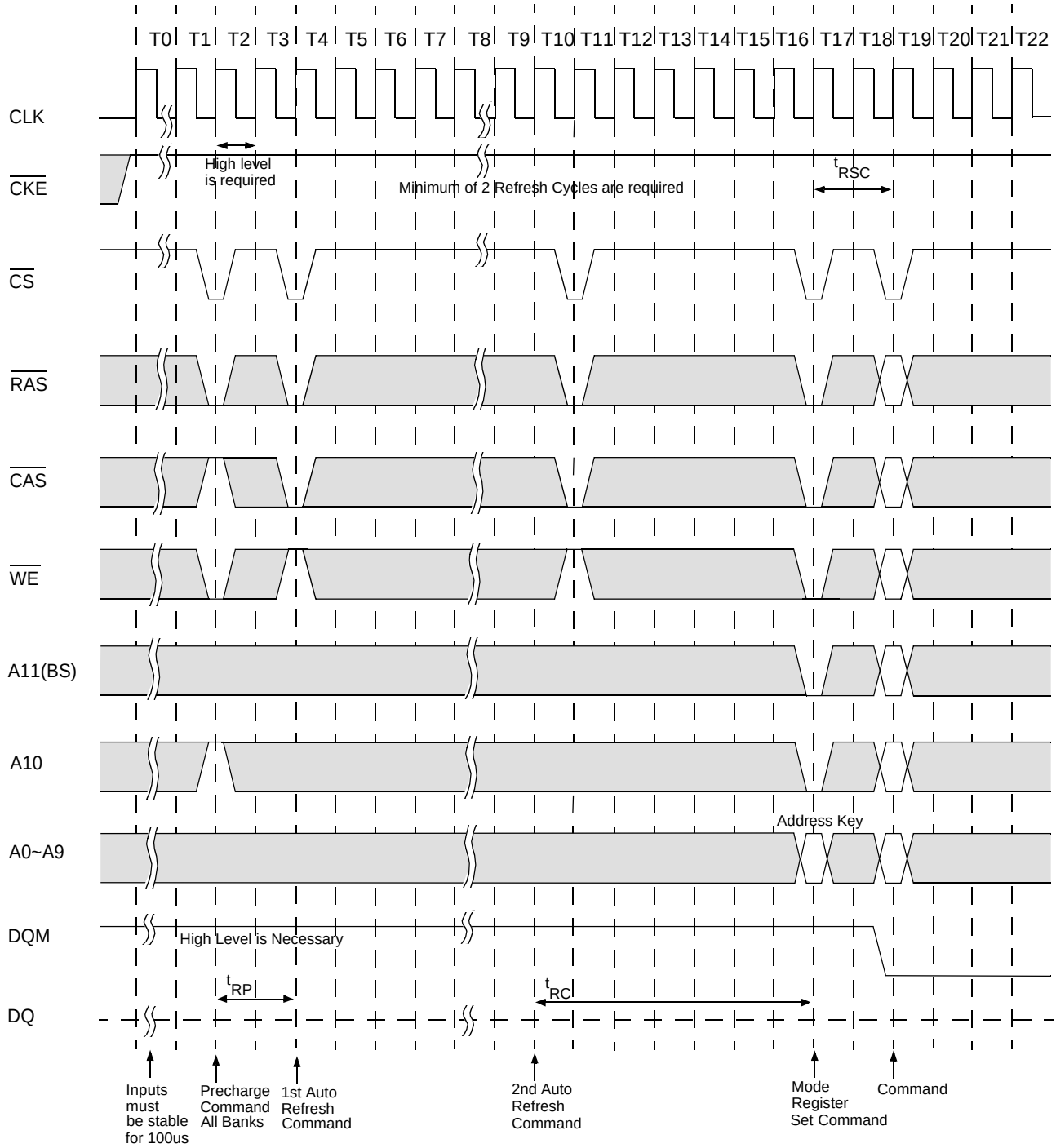


AC Parameters for Read Timing (2 of 2)

Burst Length=2, $\overline{CAS}$ Latency=3

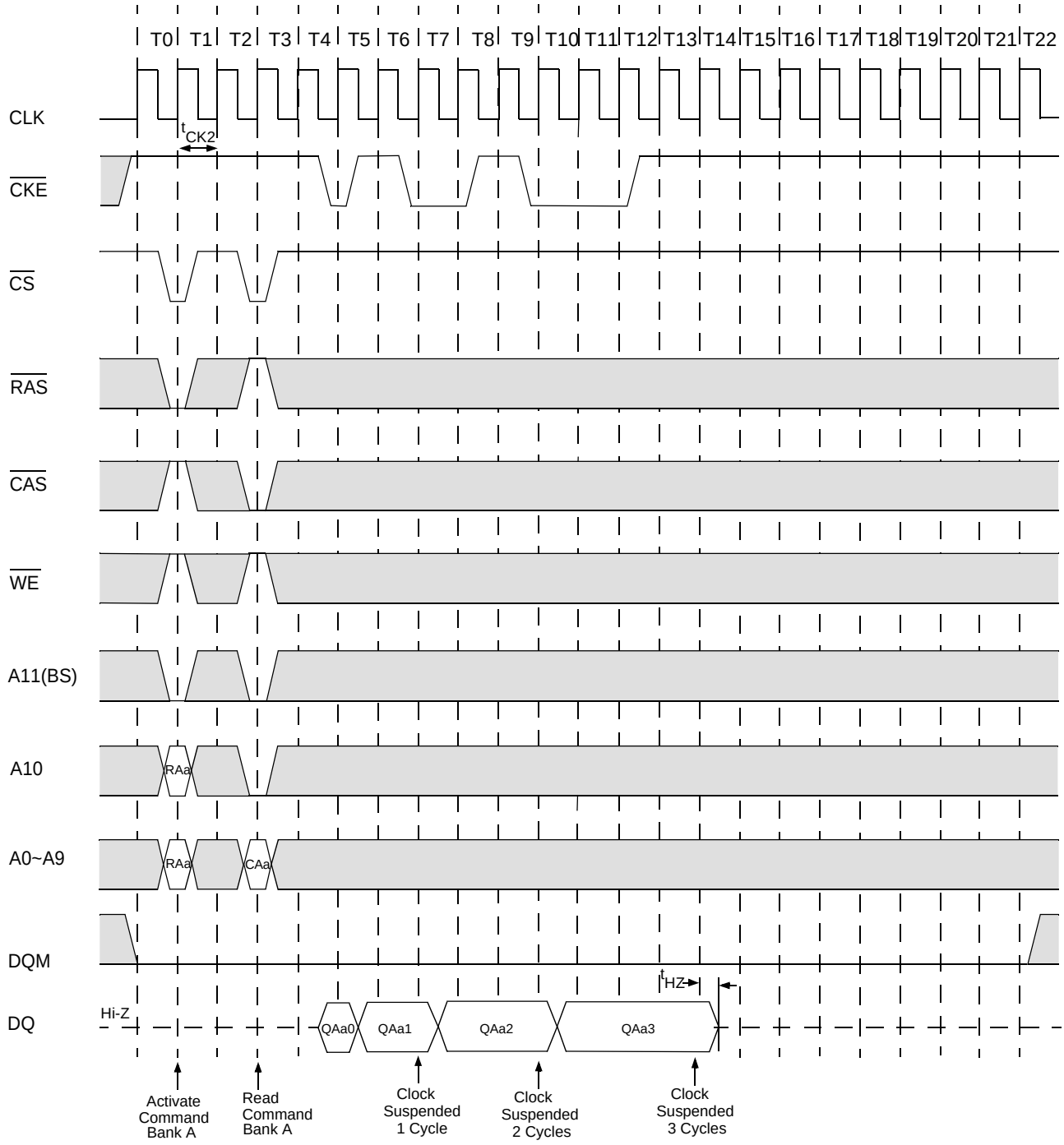


Power on Sequence and Auto Refresh (CBR)



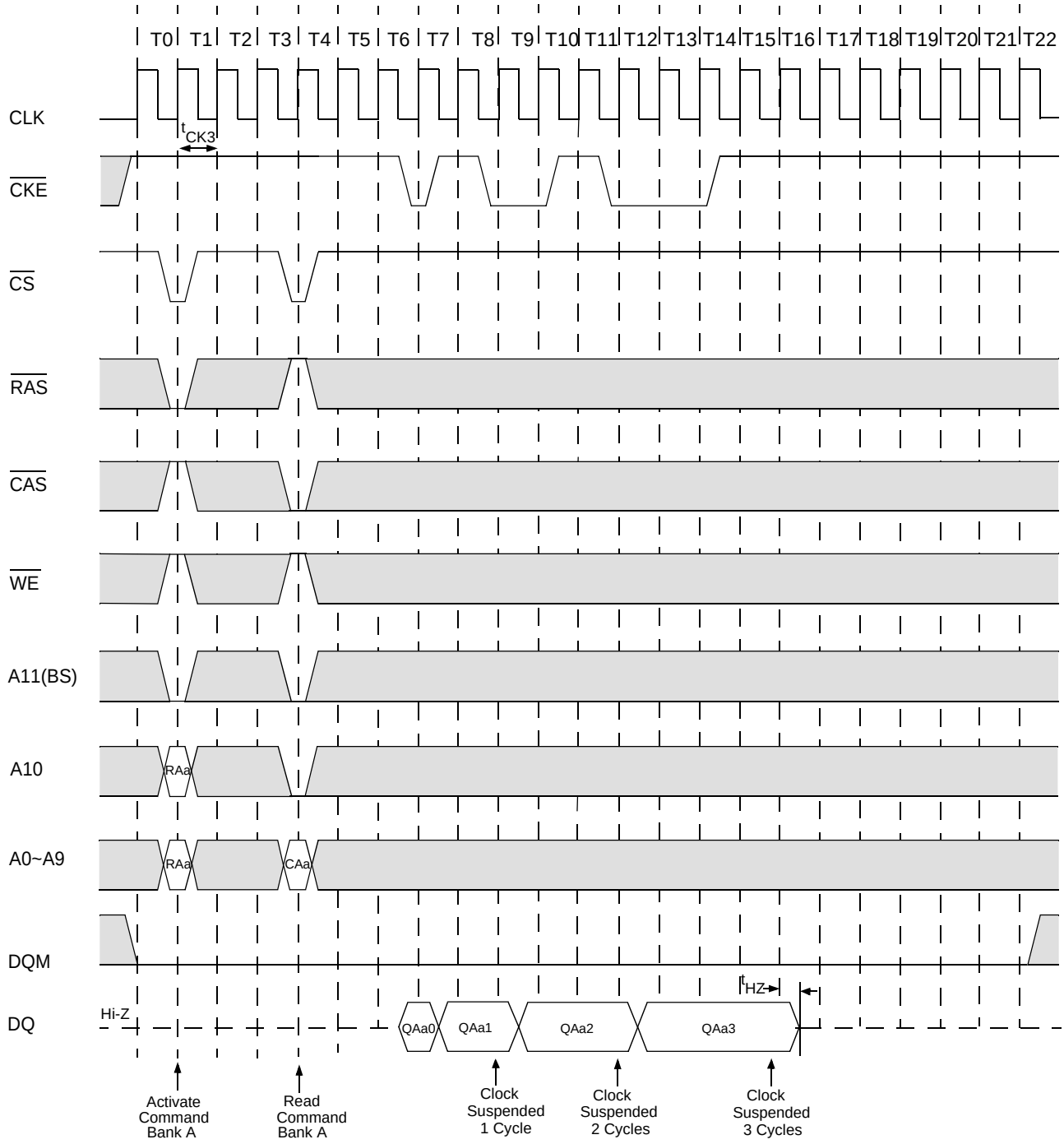
Clock Suspension During Burst Read (Using CKE) (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



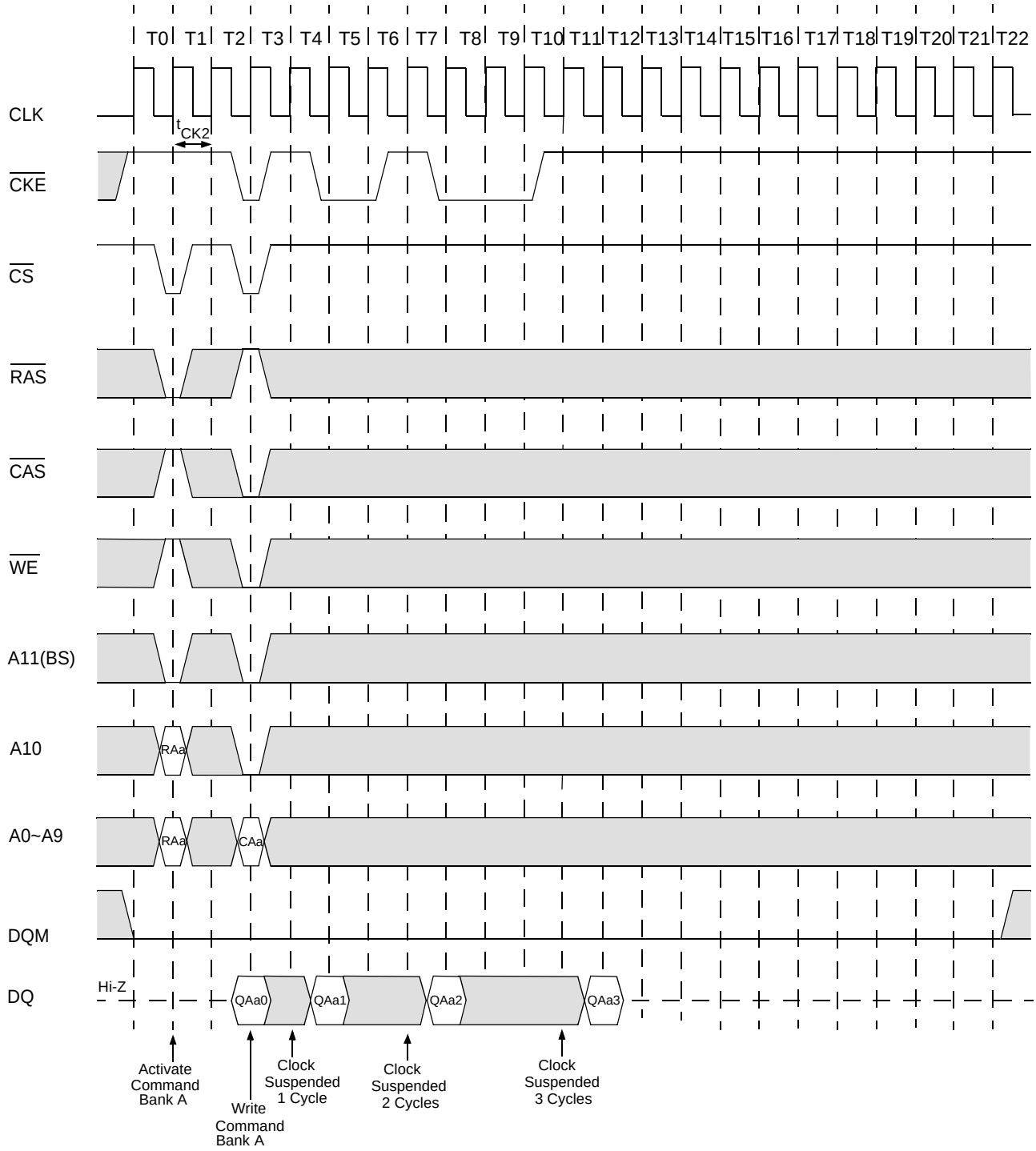
Clock Suspension During Burst Read (Using CKE) (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



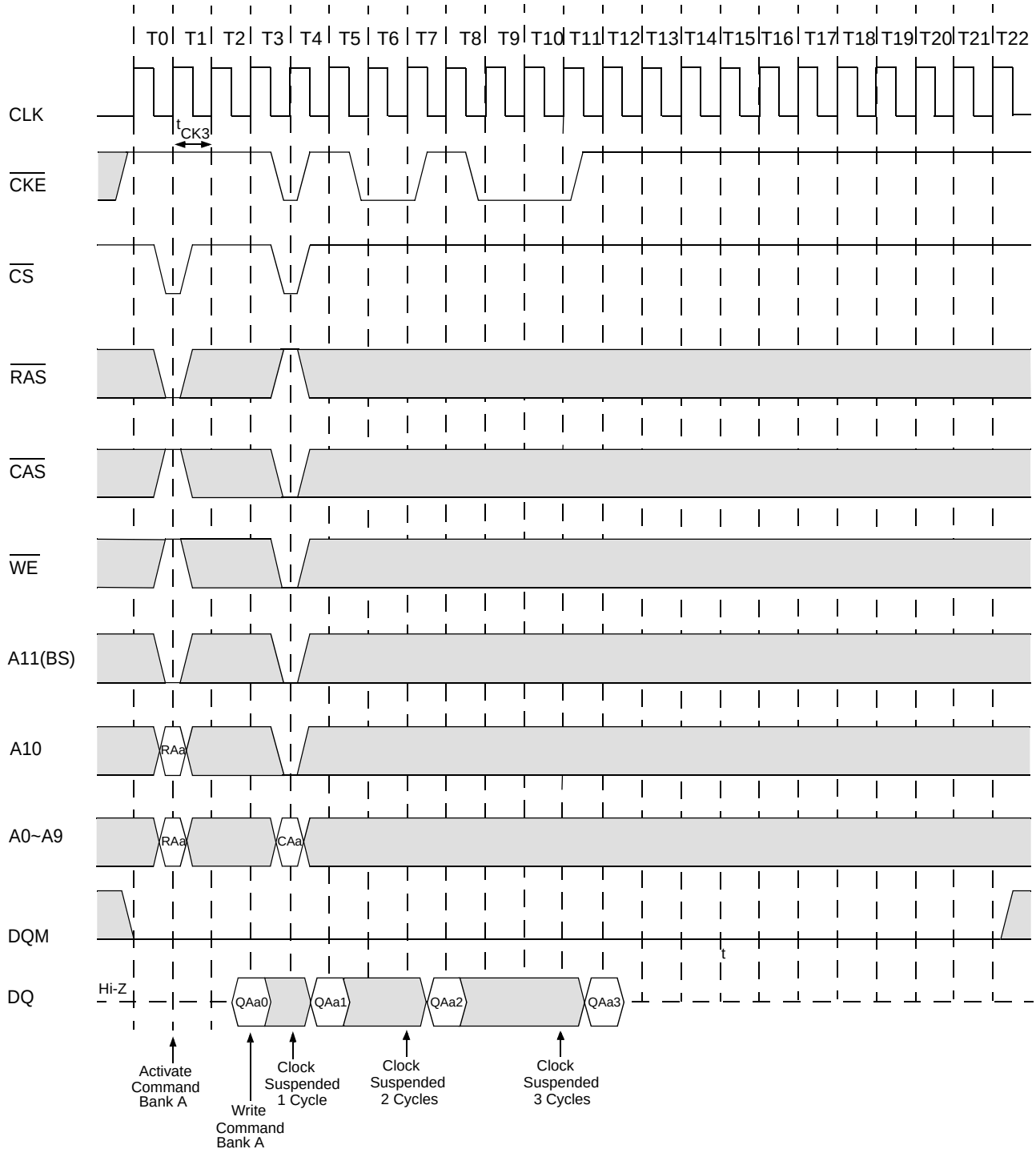
Clock Suspension During burst Write (Using CKE) (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



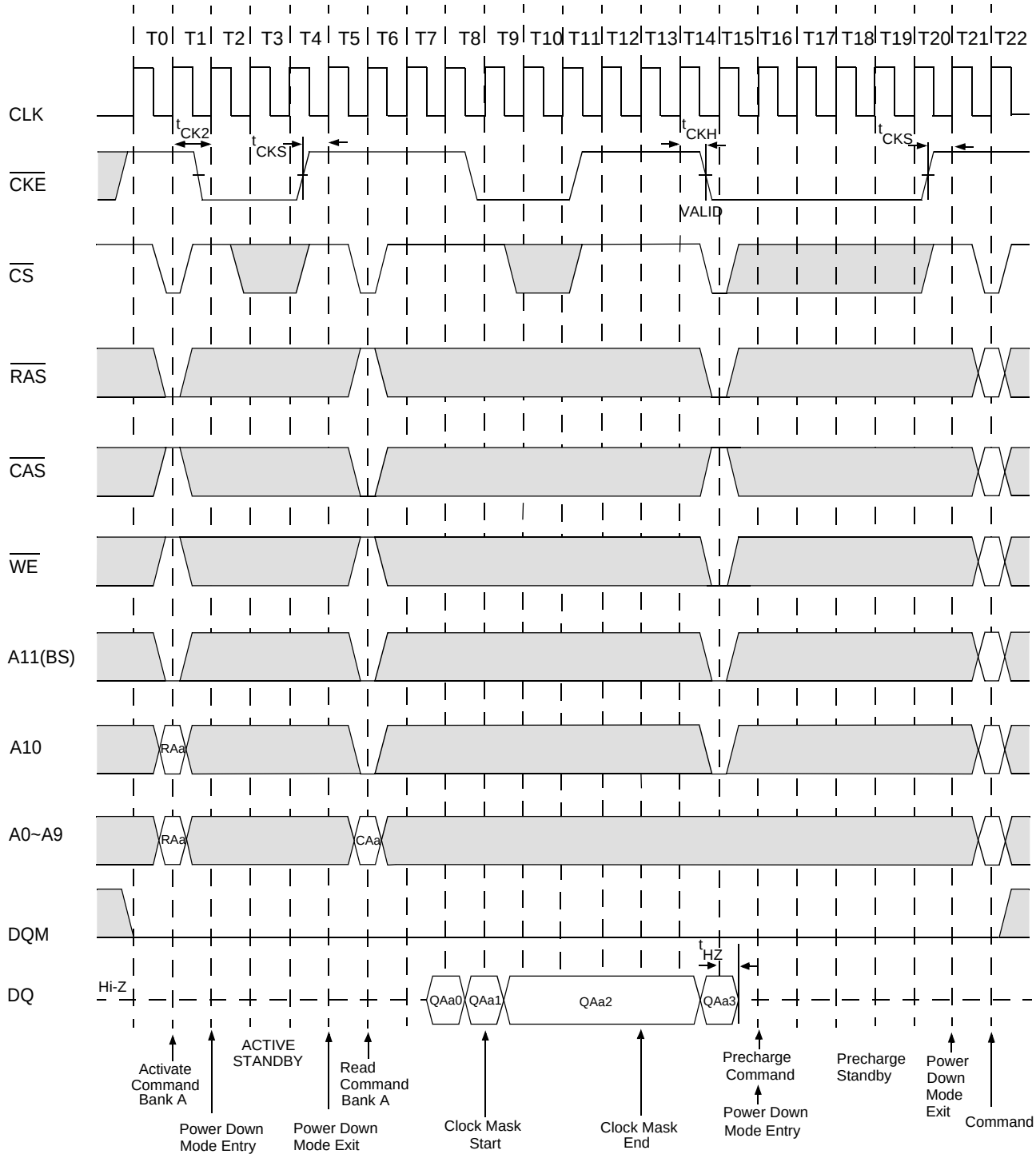
Clock suspension during Burst write (Using CKE) (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



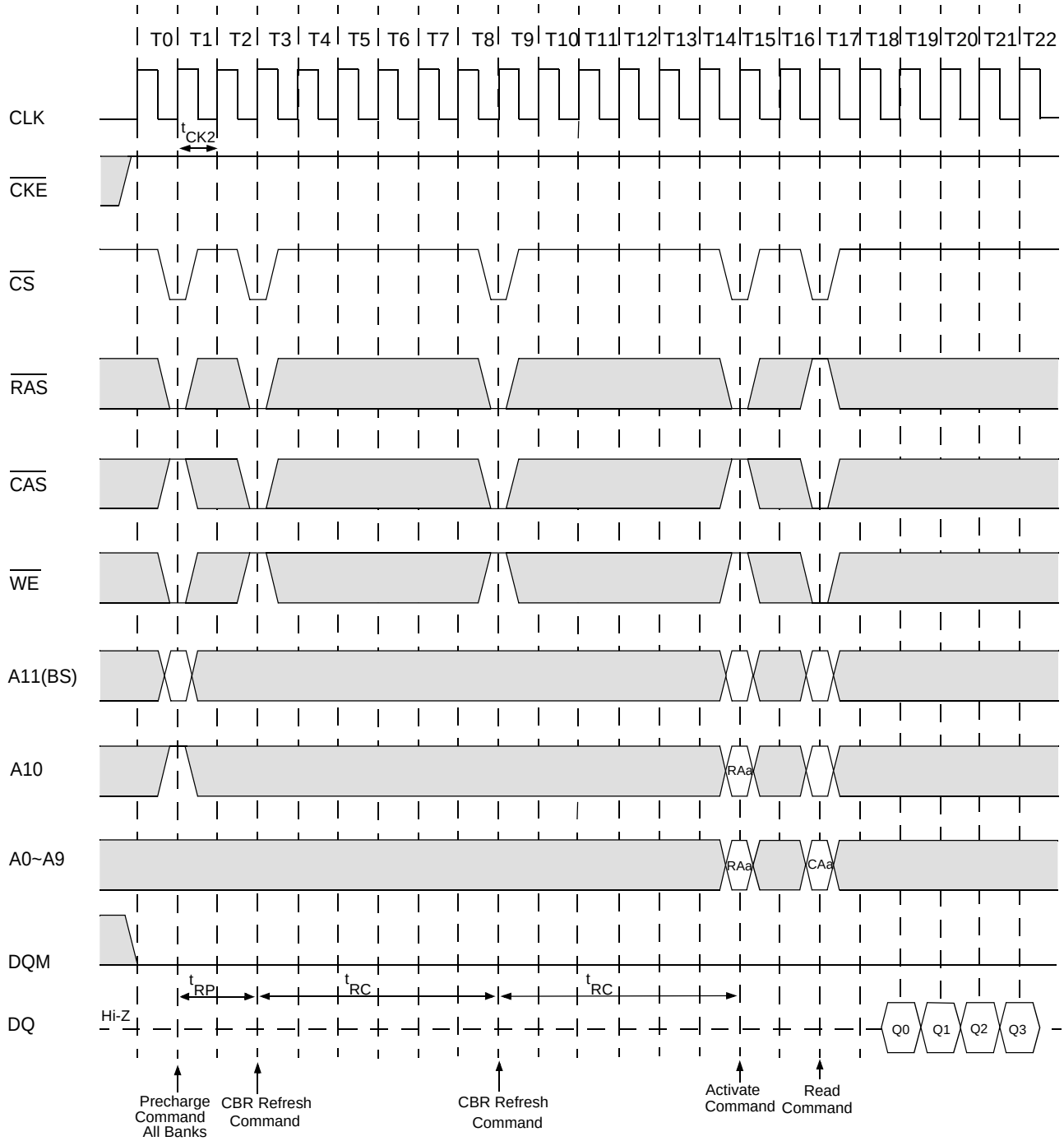
Power Down Mode and Clock Mask

Burst Length=4, $\overline{CAS}$ Latency=2

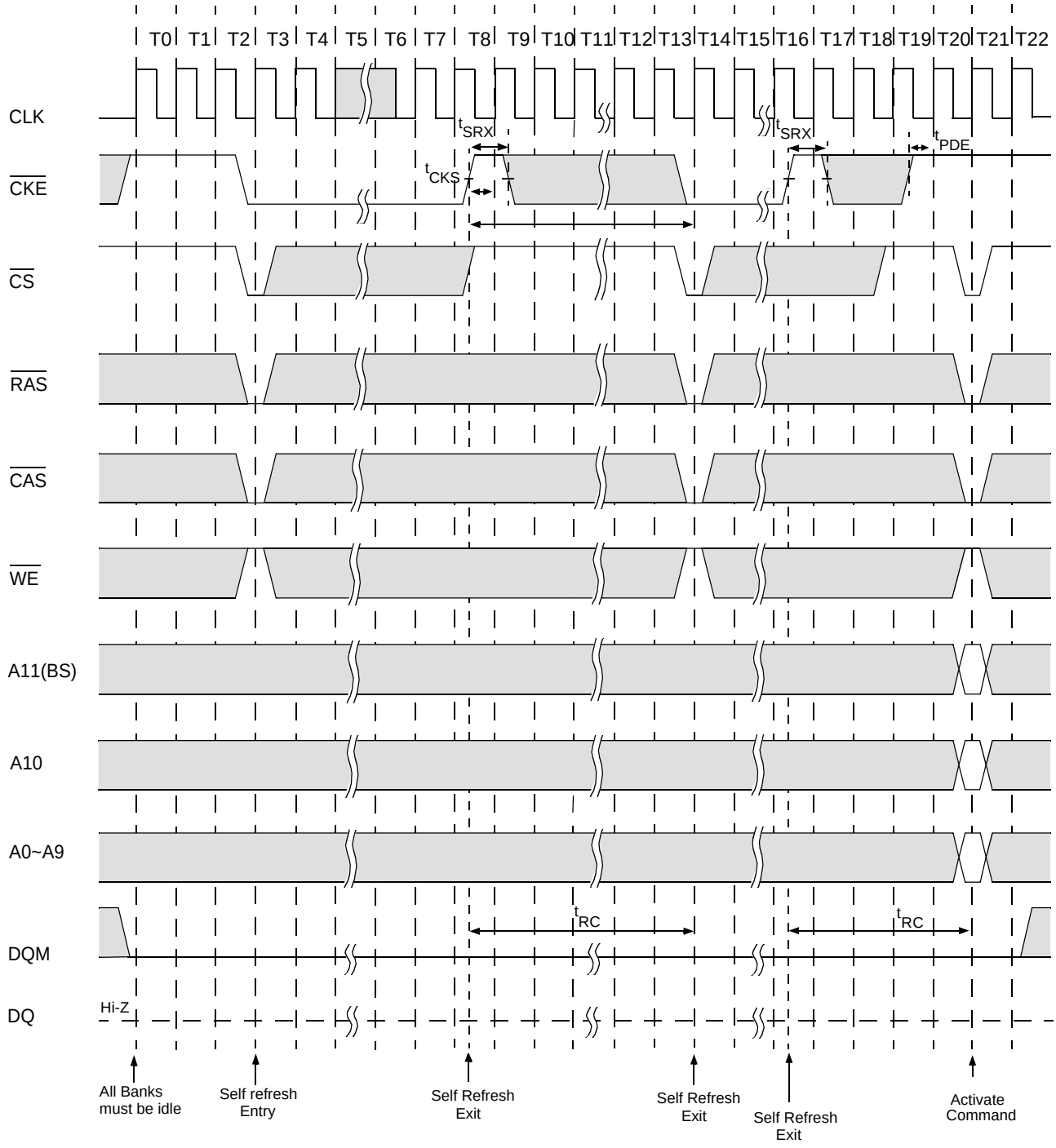


Auto Refresh (CBR)

Burst Length=4, $\overline{CAS}$ Latency=2

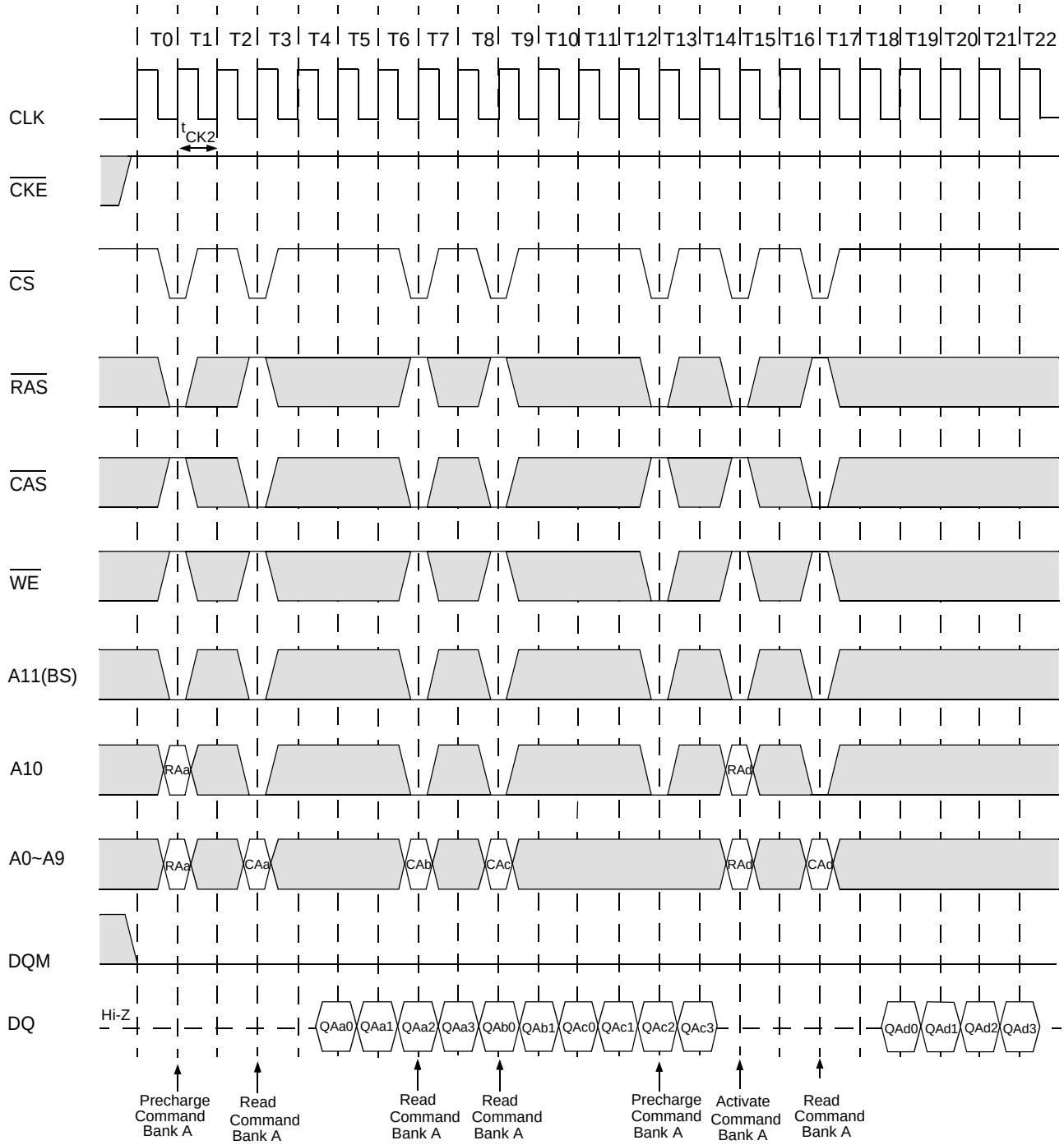


Self Refresh (Entry and Exit)



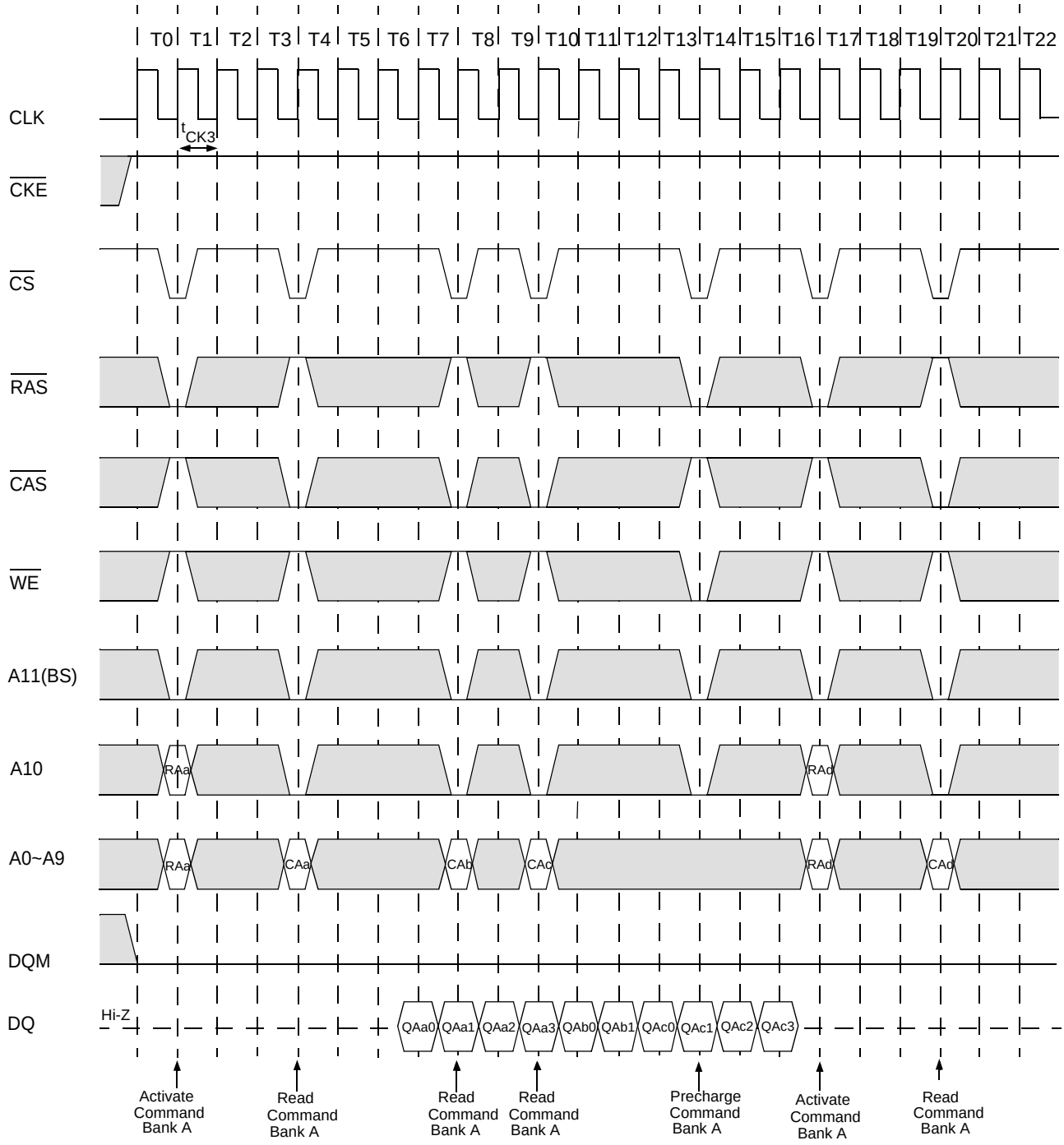
Random Column Read (Page Within same Bank)(1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



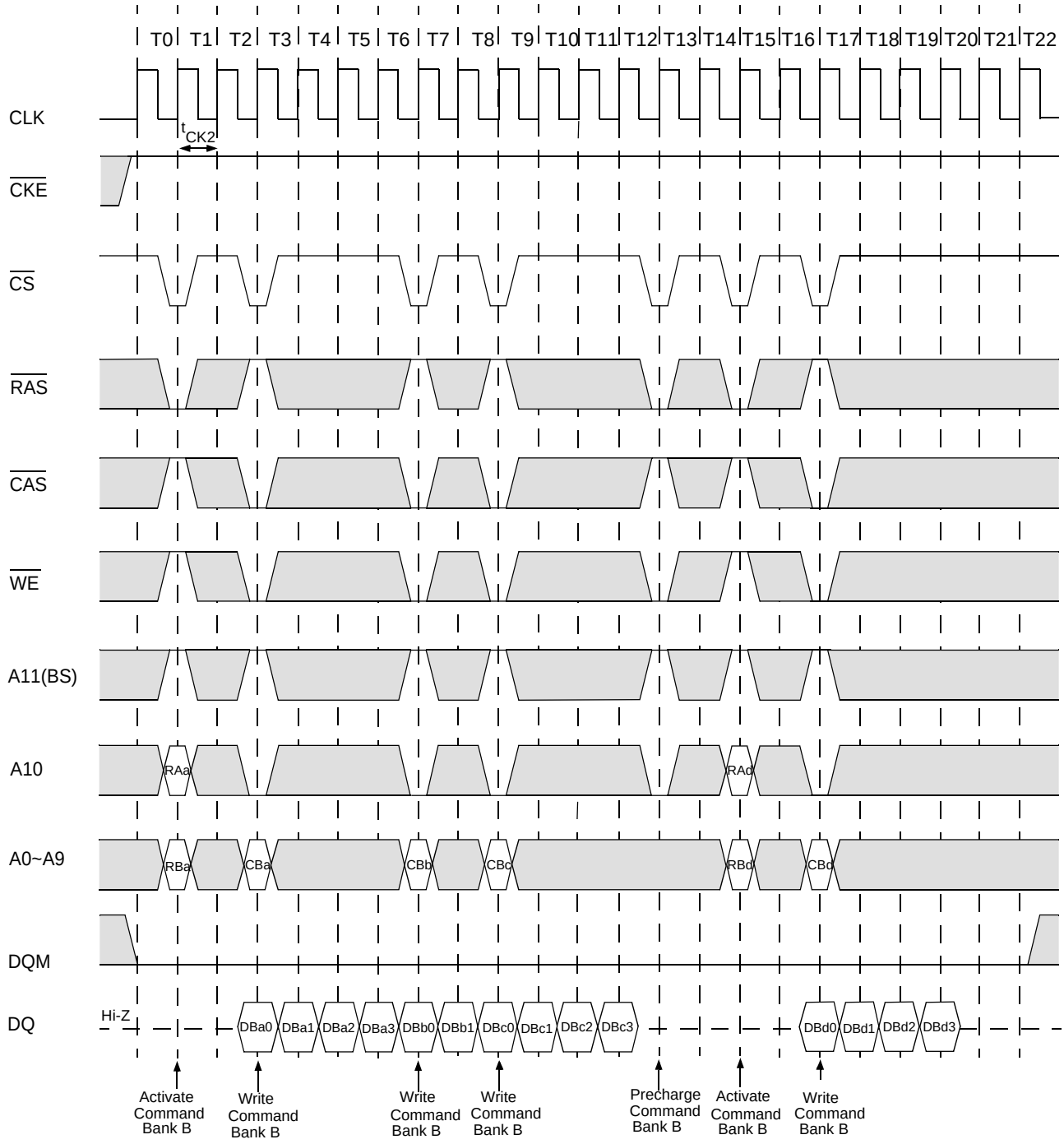
Random Column Read (Page Within same Bank)(2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



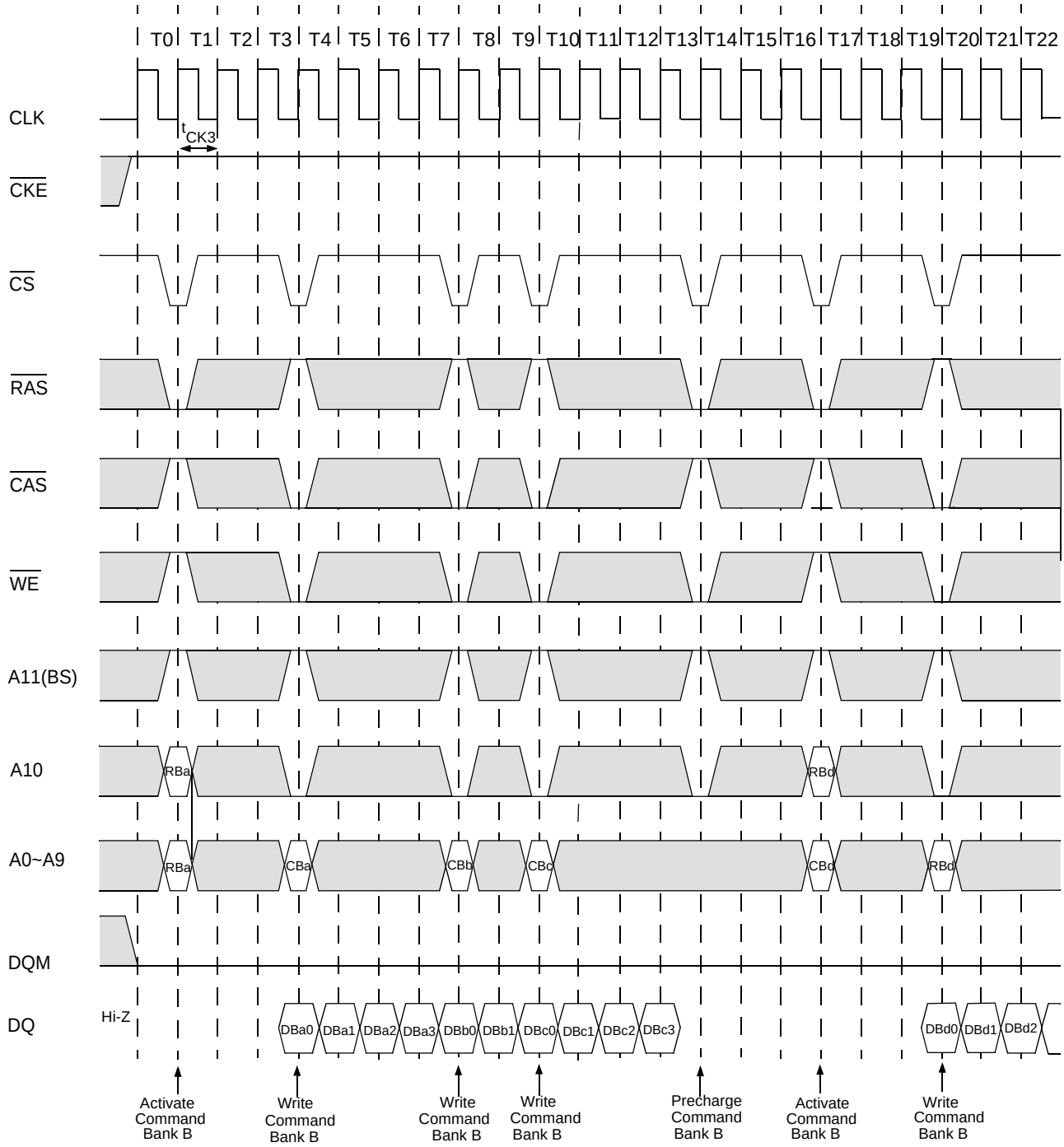
Random Column Write (Page Within same Bank) (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



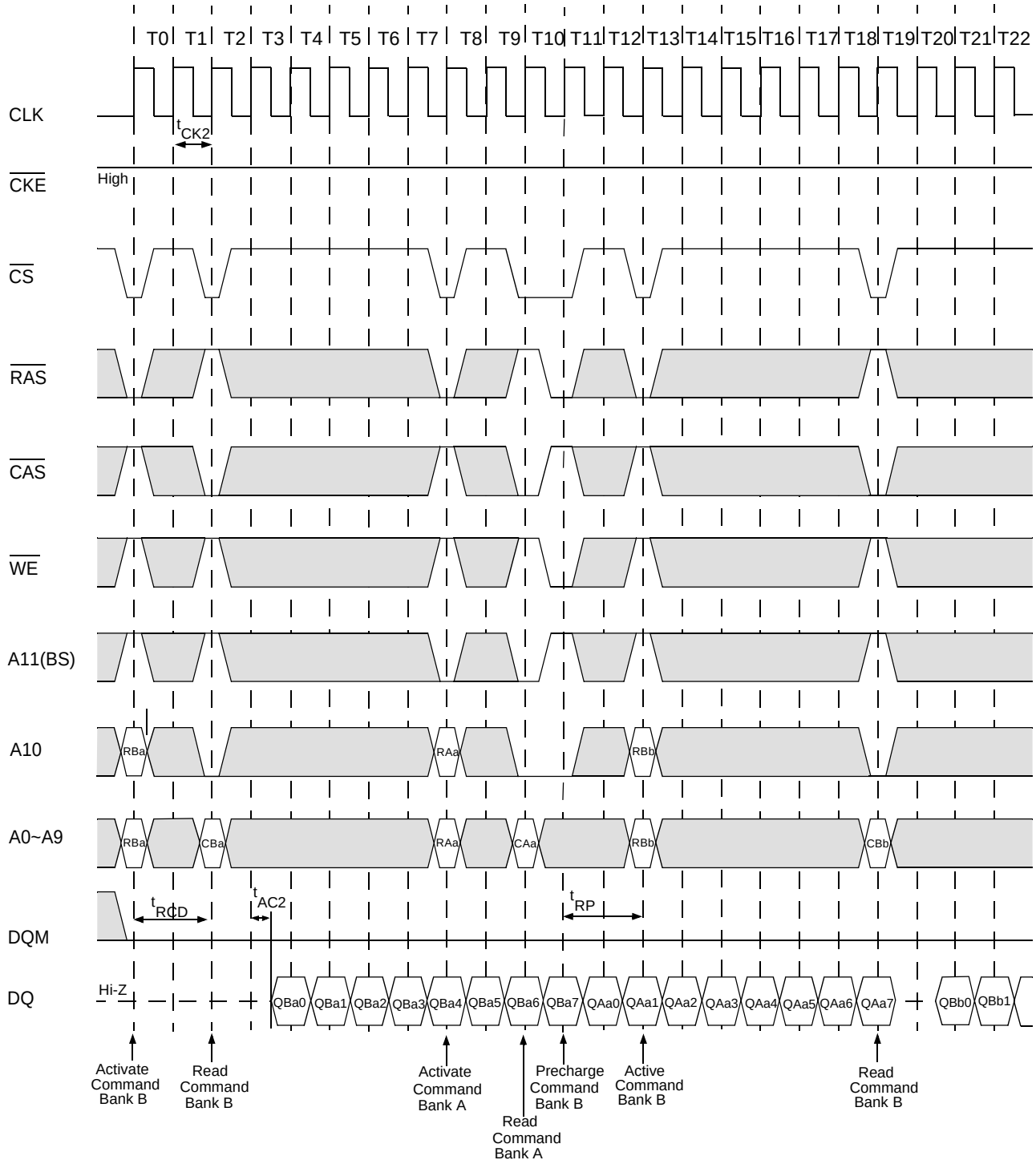
Random Column Write (Page Within same Bank) (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



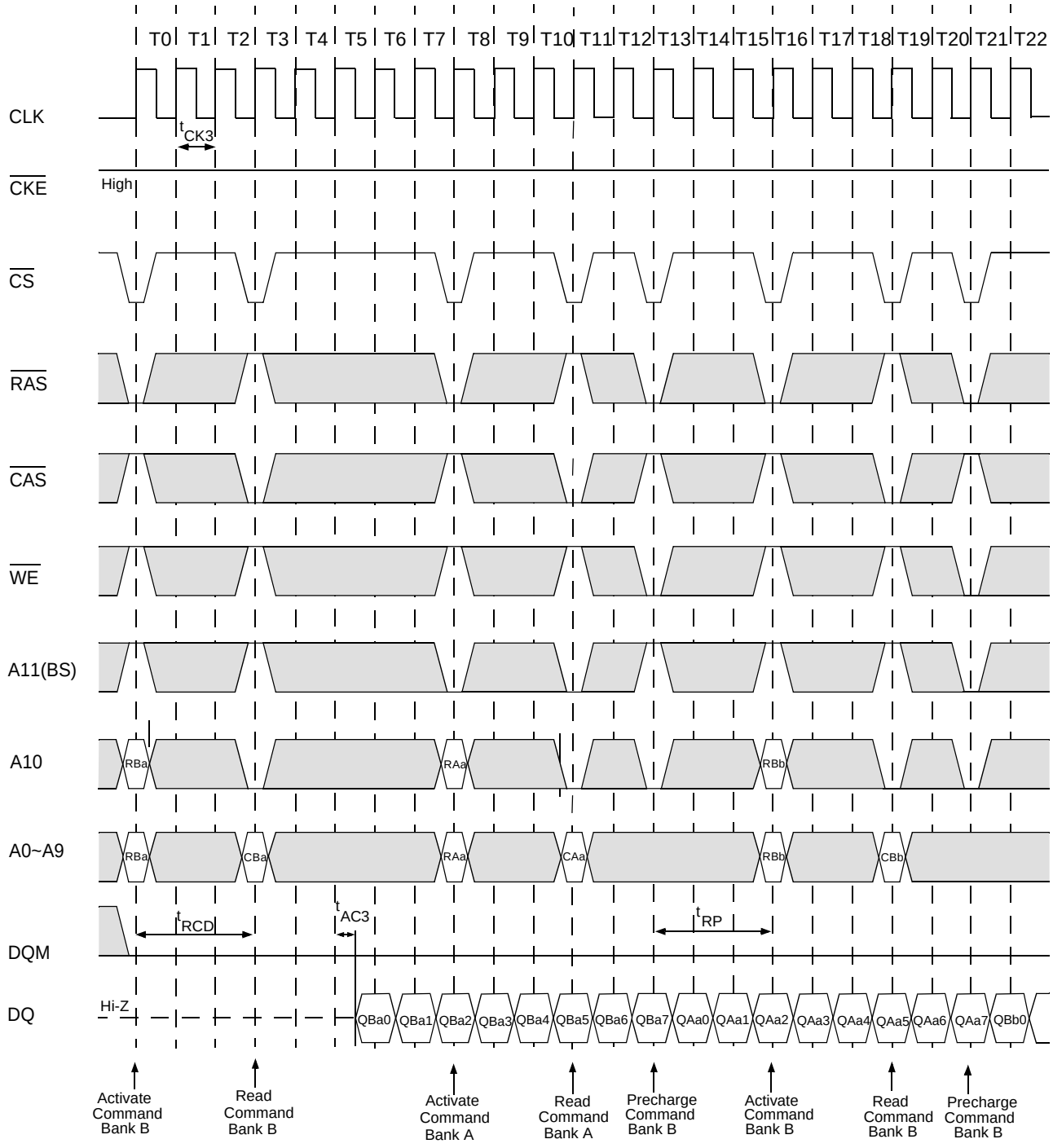
Random Row Read (Interleaving Banks) (1 of 2)

Burst Length=8, $\overline{CAS}$ Latency=2



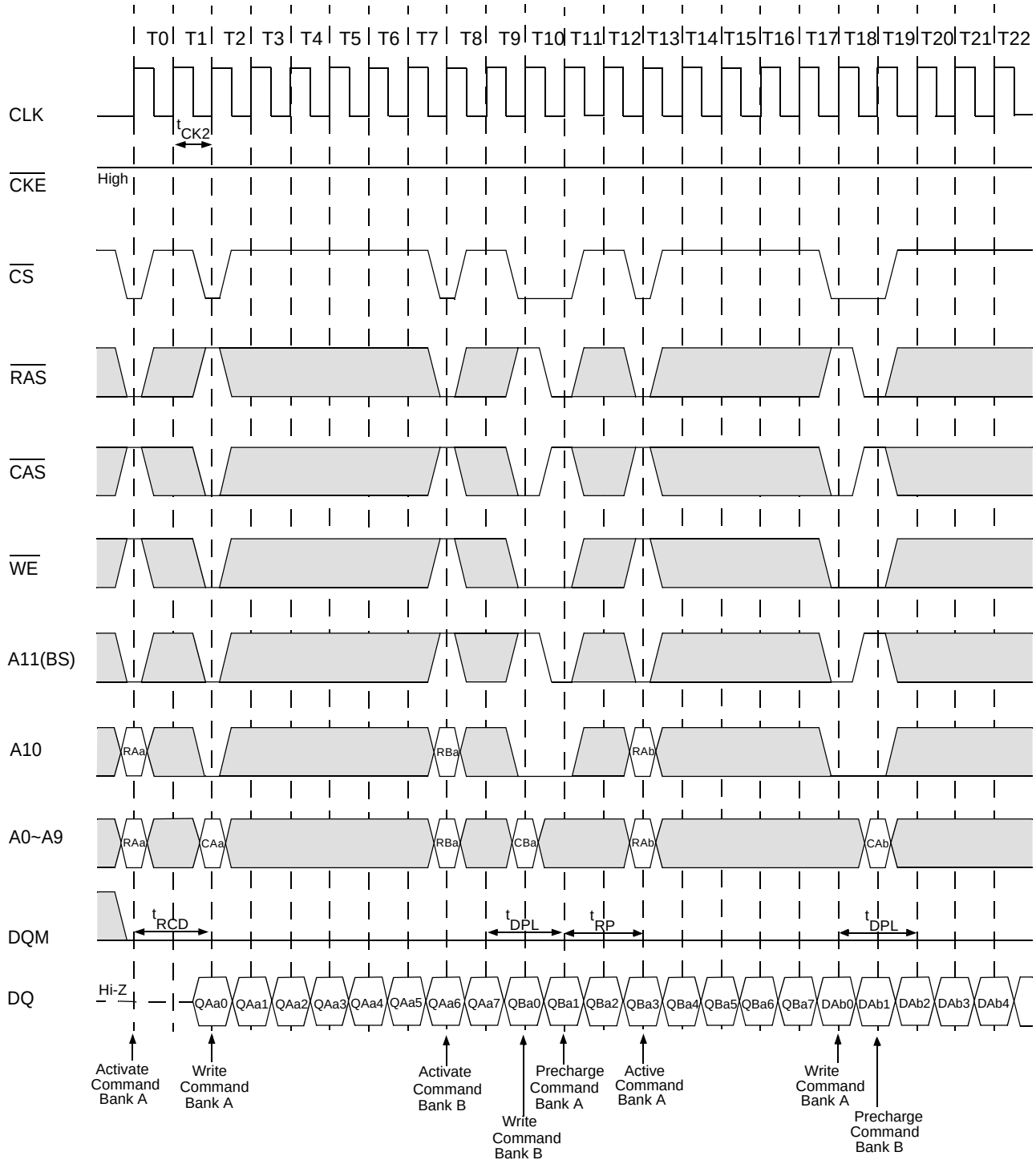
Random Row Read (Interleaving Banks) (2 of 2)

Burst Length=8, $\overline{CAS}$ Latency=3



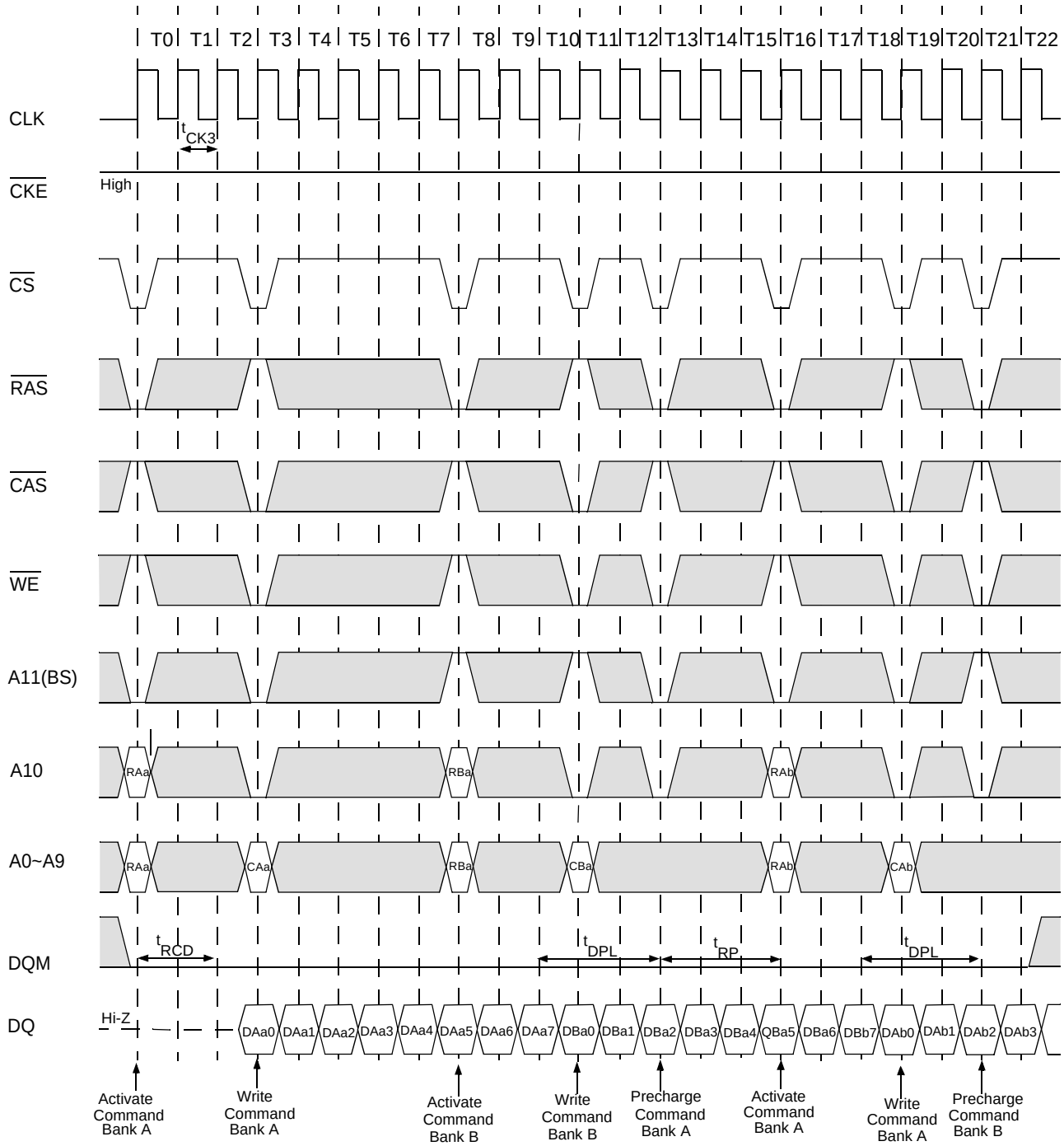
Random Row Write (Interleaving Banks) (1 of 2)

Burst Length=8, $\overline{CAS}$ Latency=2



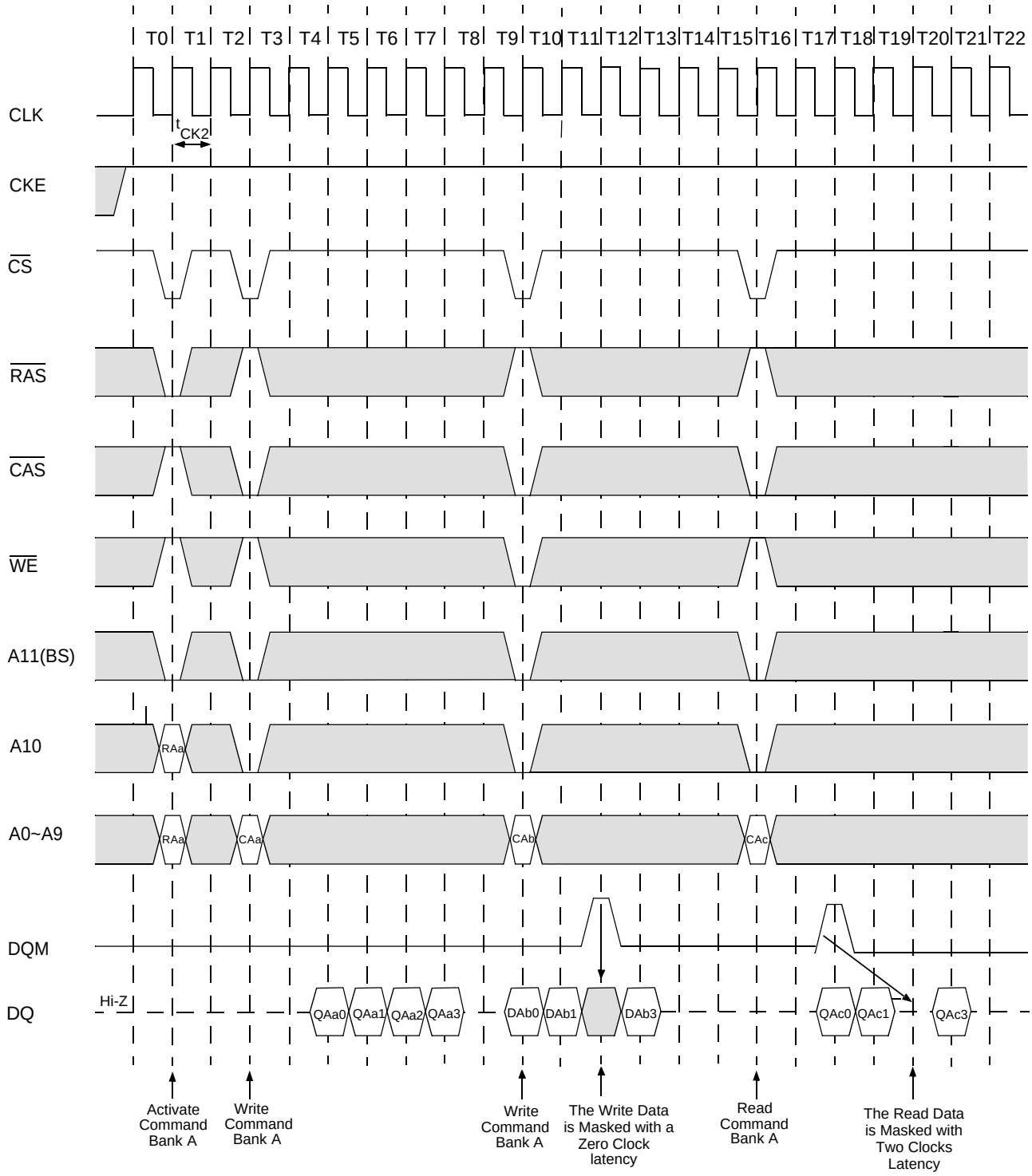
Random Row Write (Interleaving Banks) (2 of 2)

Burst Length=8, $\overline{CAS}$ Latency=3



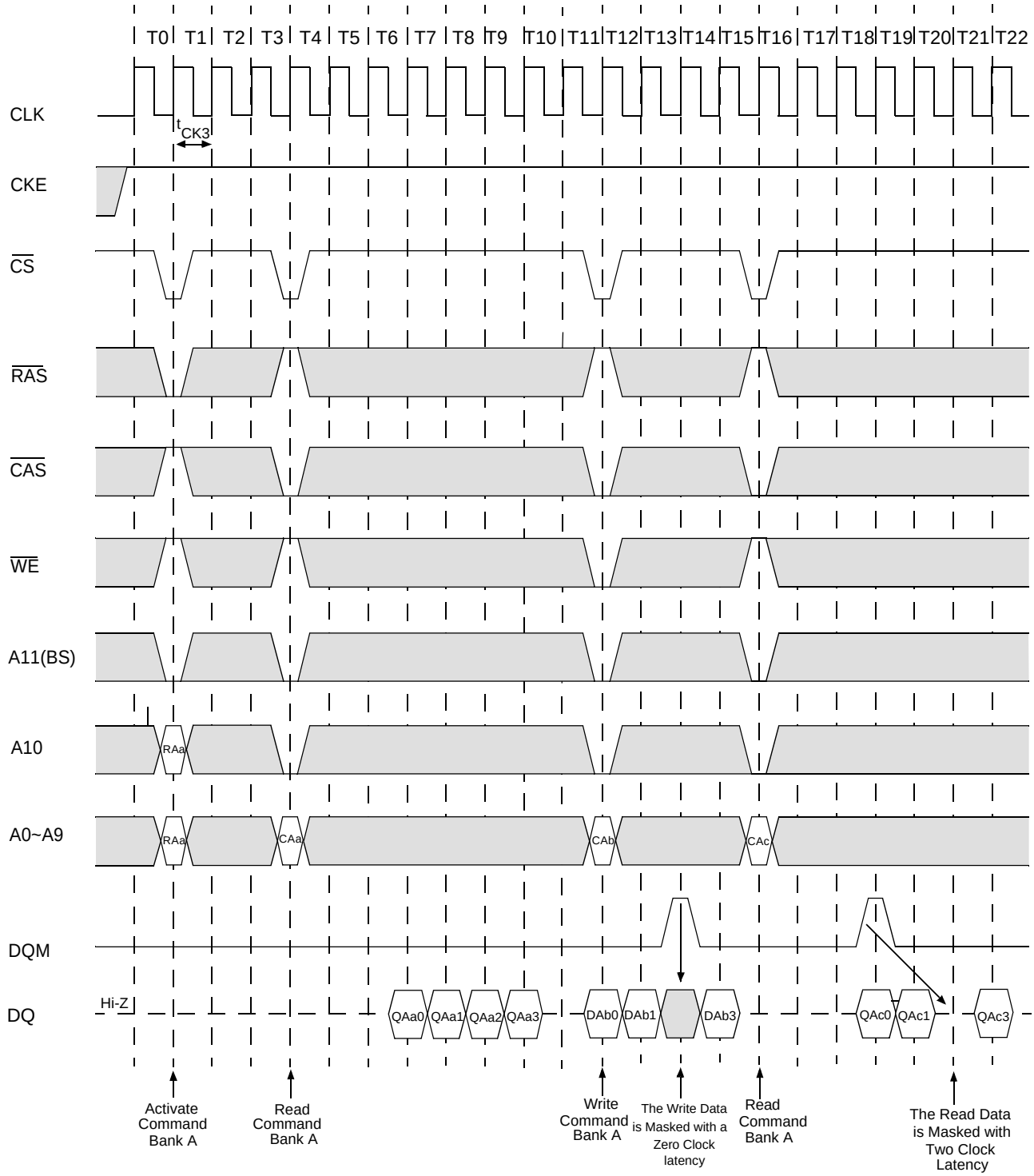
Read and Write Cycle (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



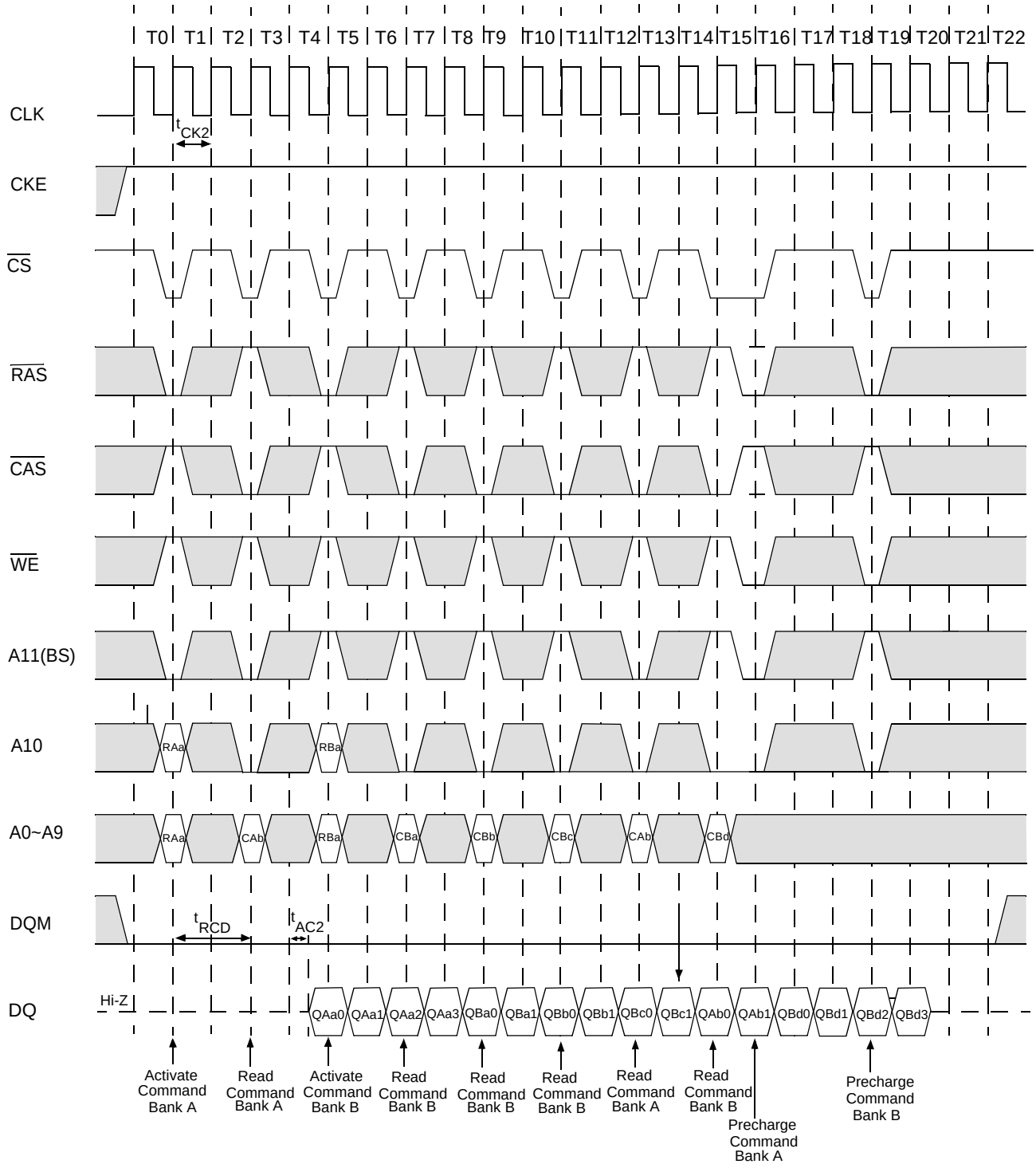
Read and Write Cycle (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



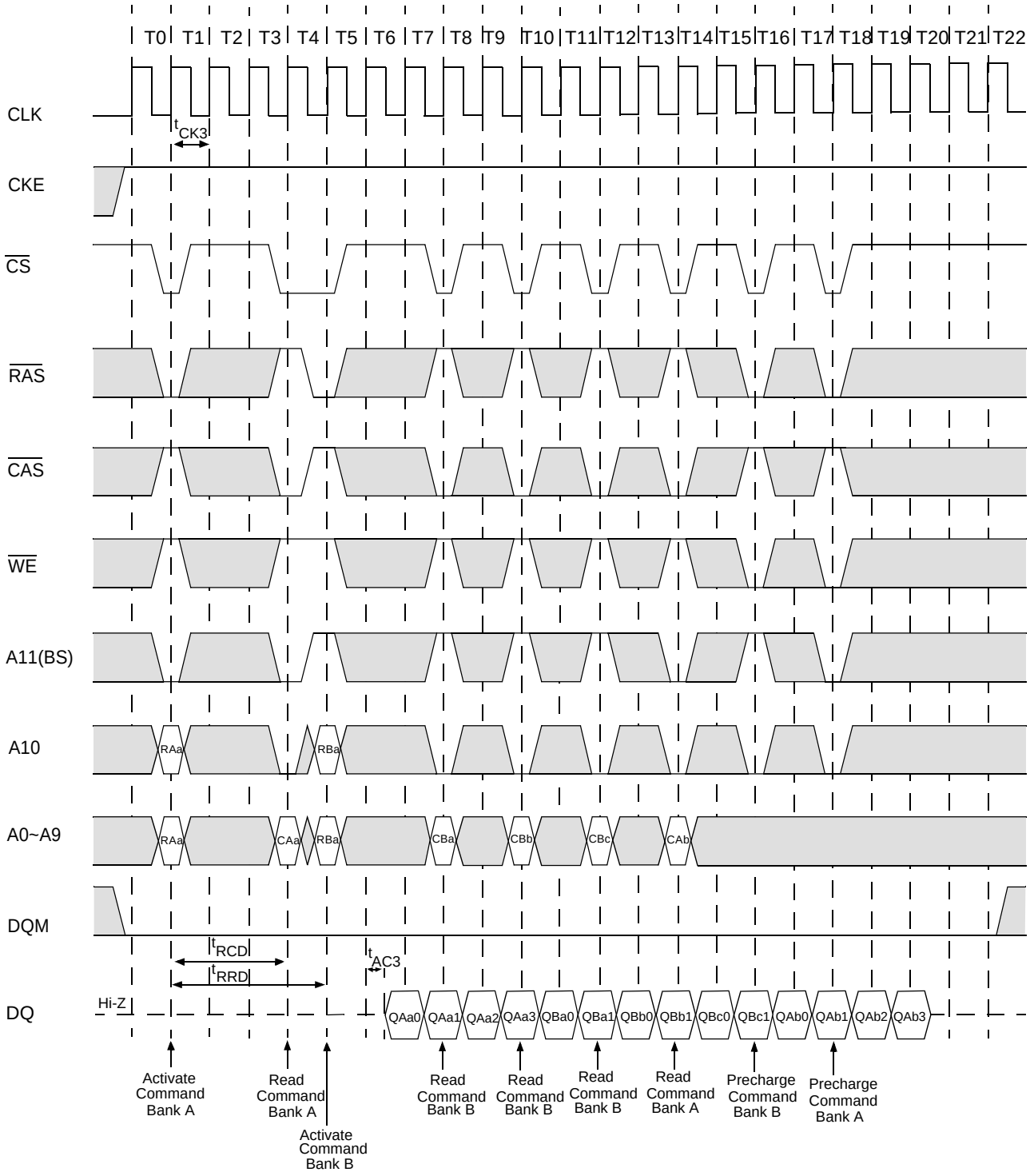
Interleaved Column Read Cycle (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



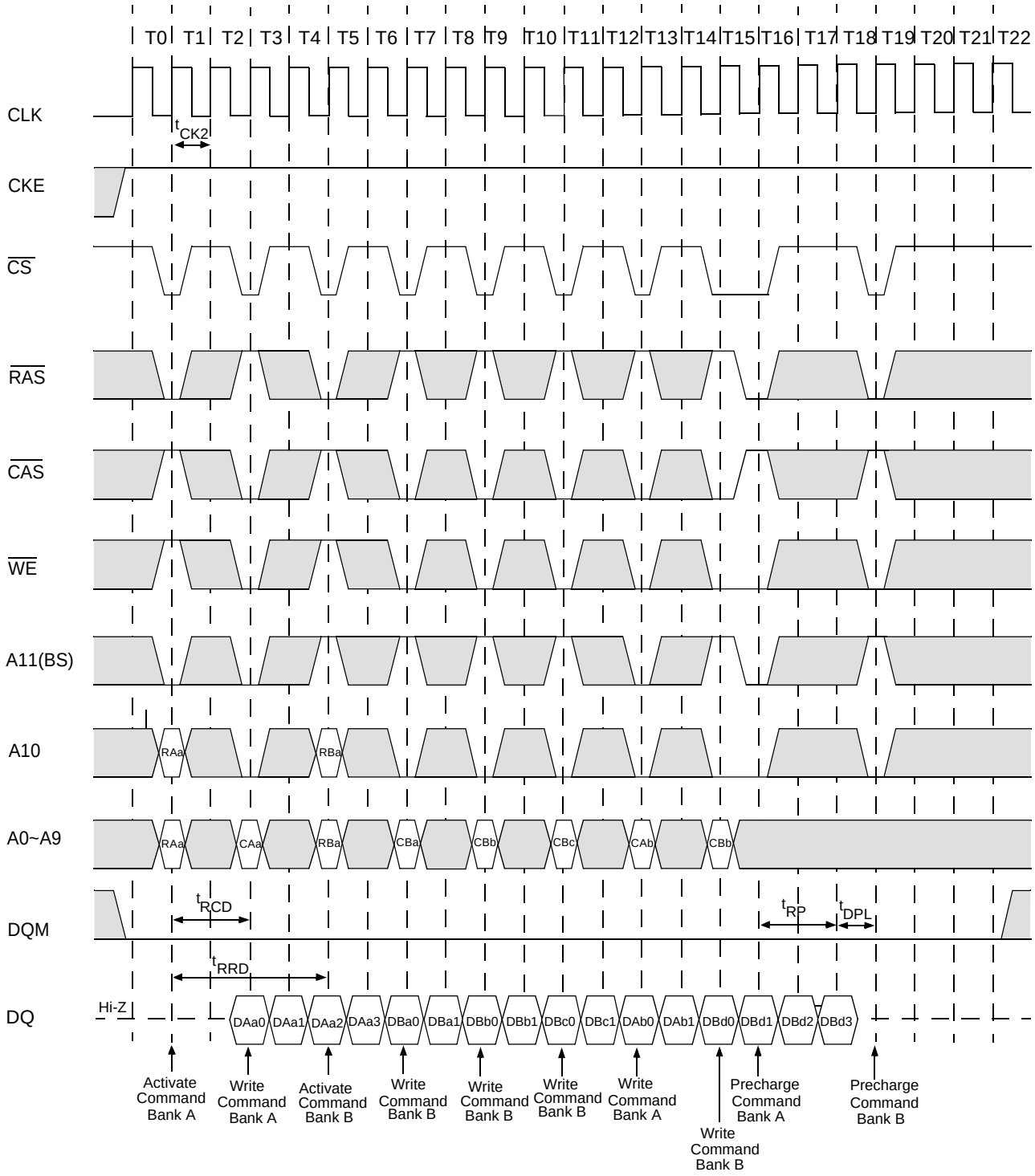
Interleaved Column Read Cycle (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



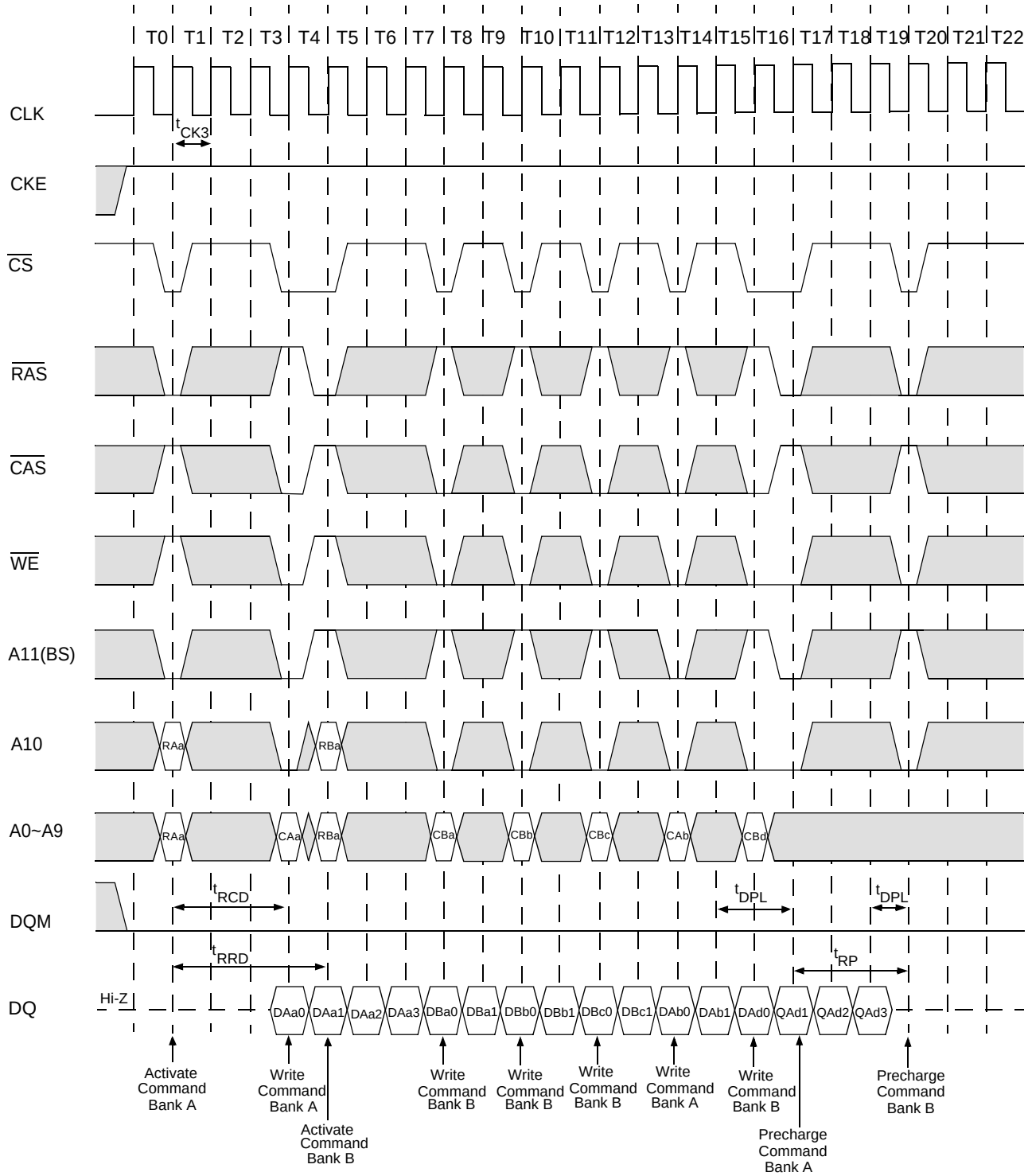
Interleaved Column Write Cycle (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



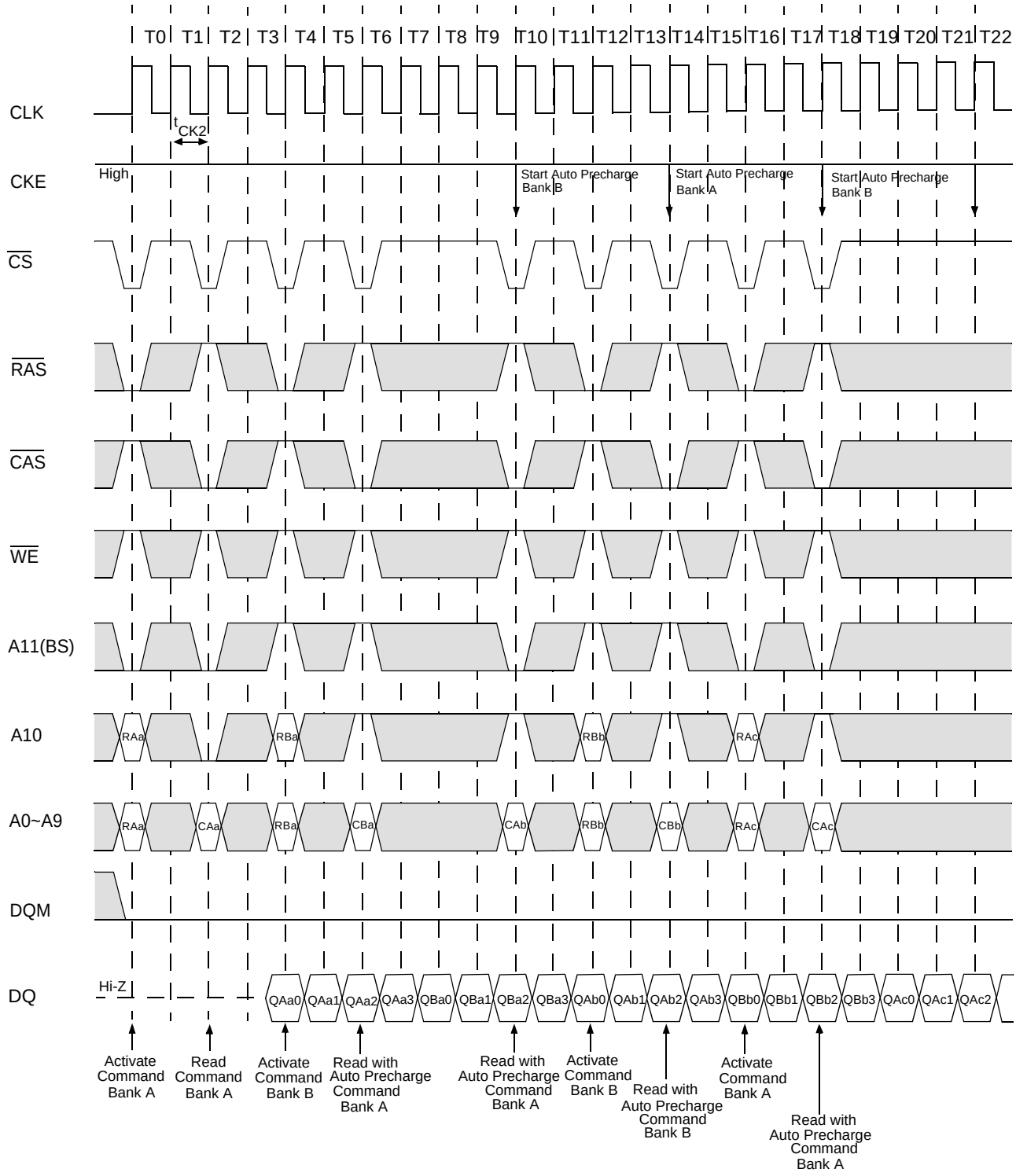
Interleaved Column Write Cycle (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



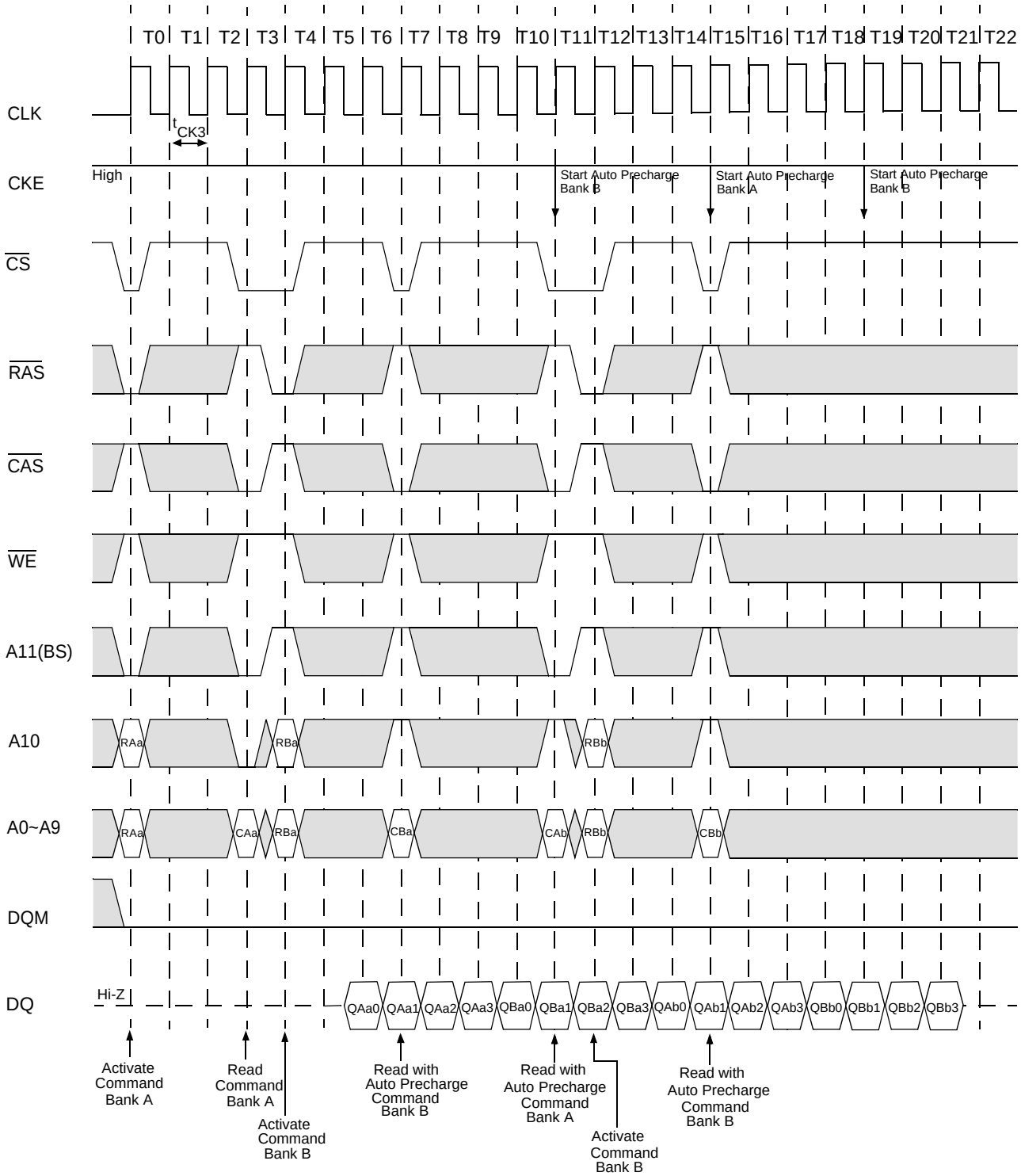
Auto Precharge after Read Burst (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



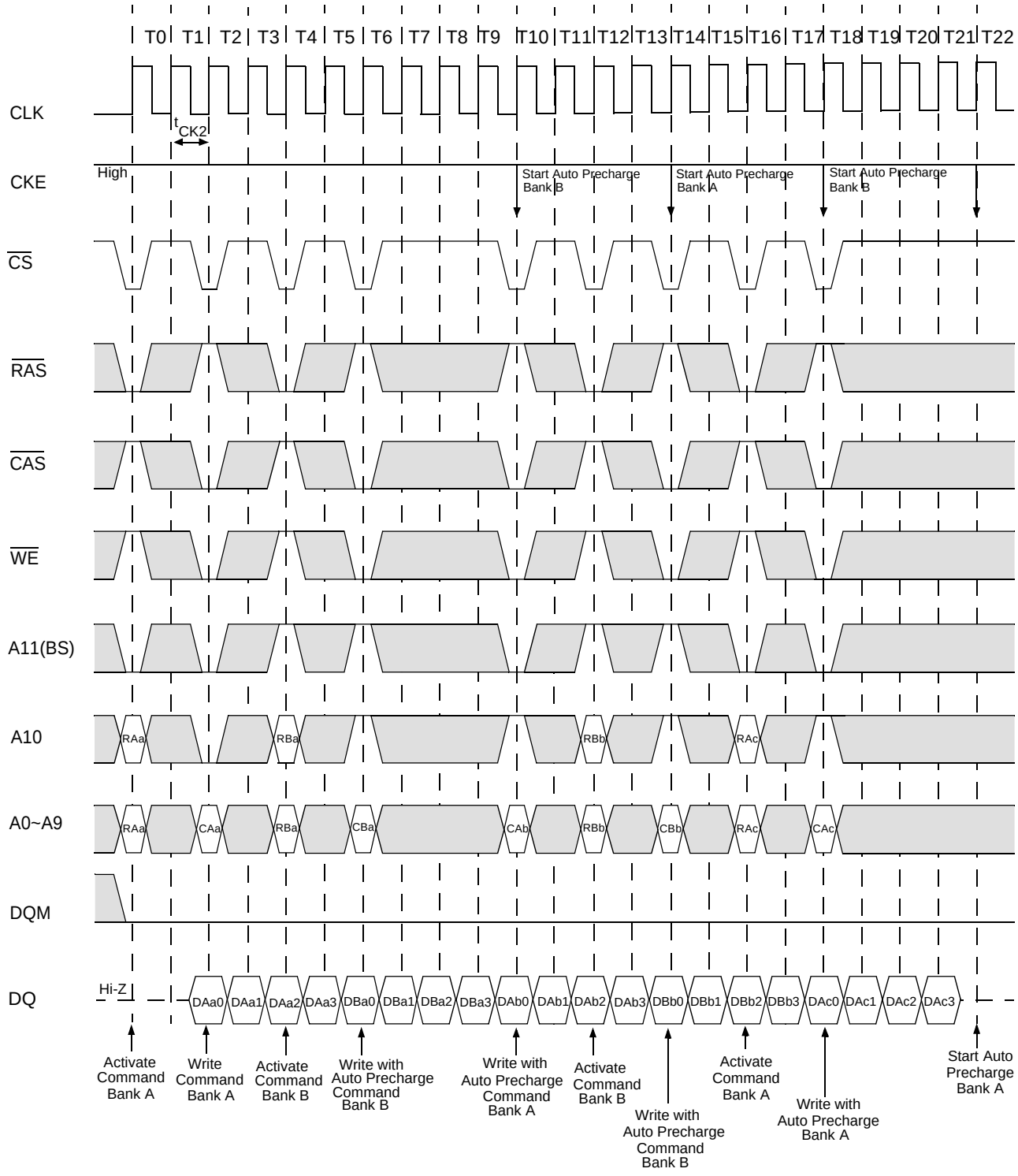
Auto Precharge after Read Burst (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



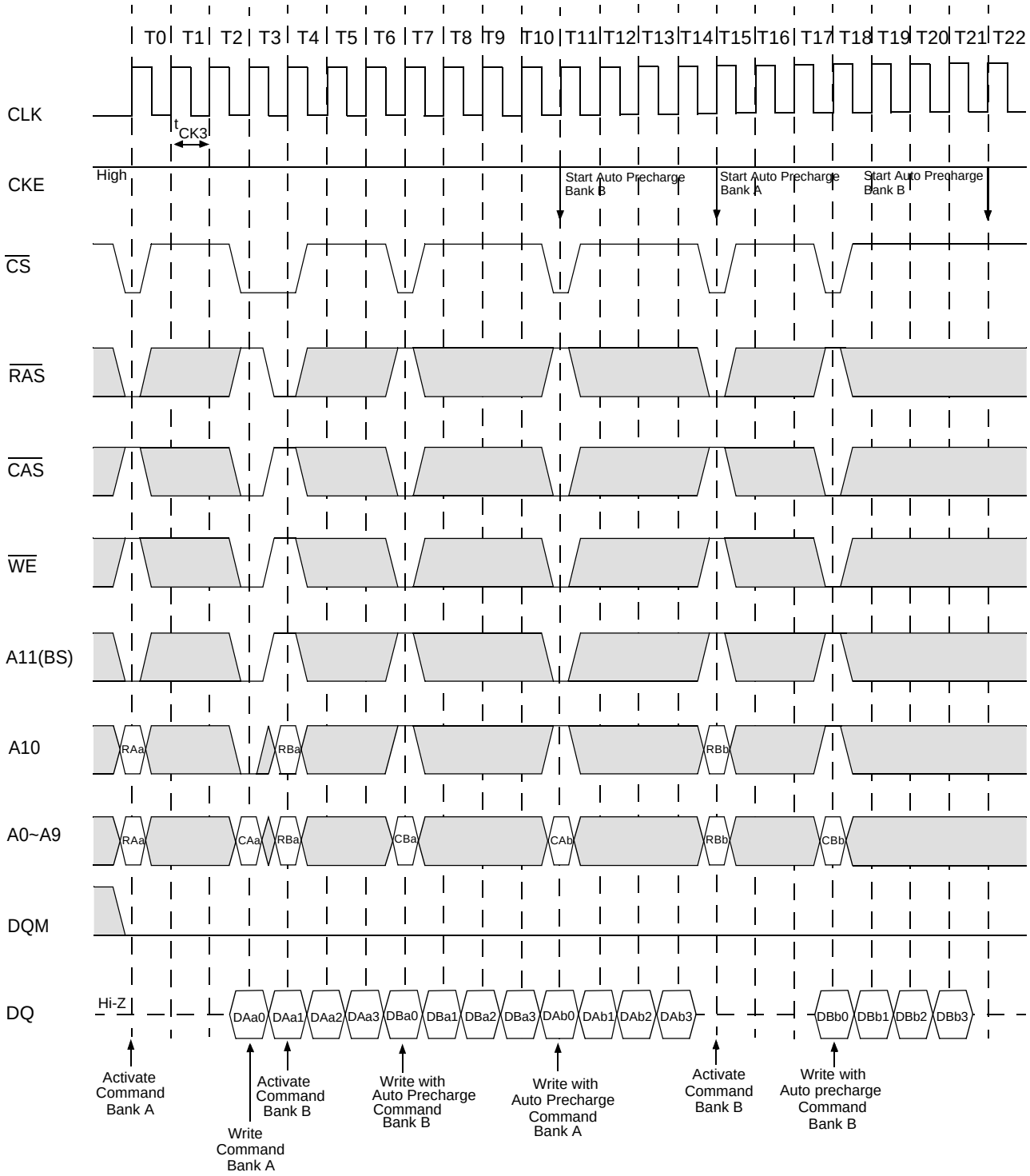
Auto Precharge after Write Burst (1 of 2)

Burst Length=4, $\overline{CAS}$ Latency=2



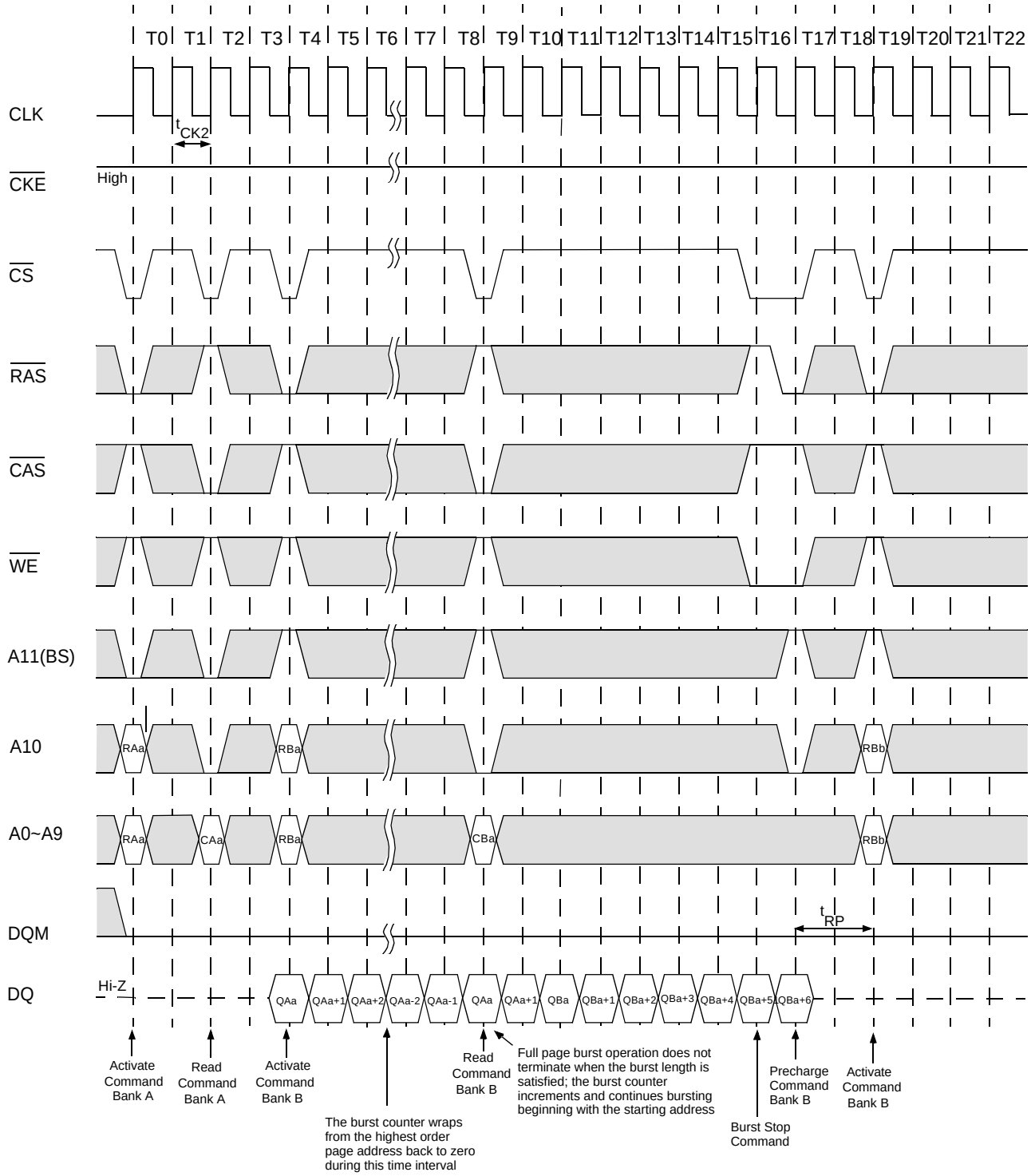
Auto Precharge after Write Burst (2 of 2)

Burst Length=4, $\overline{CAS}$ Latency=3



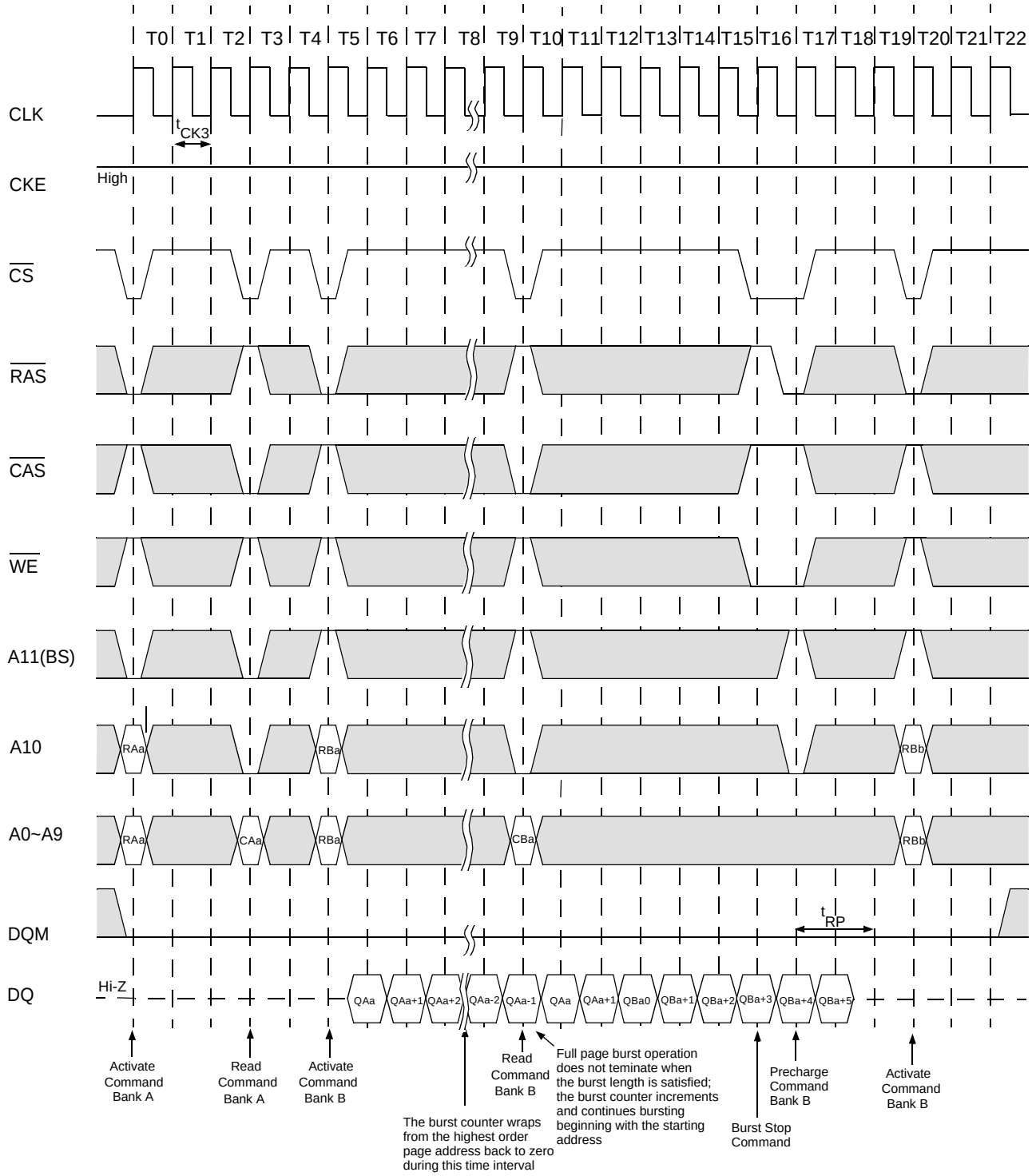
Full Page Read Cycle (1 of 2)

Burst Length=Full Page, $\overline{CAS}$ Latency=2



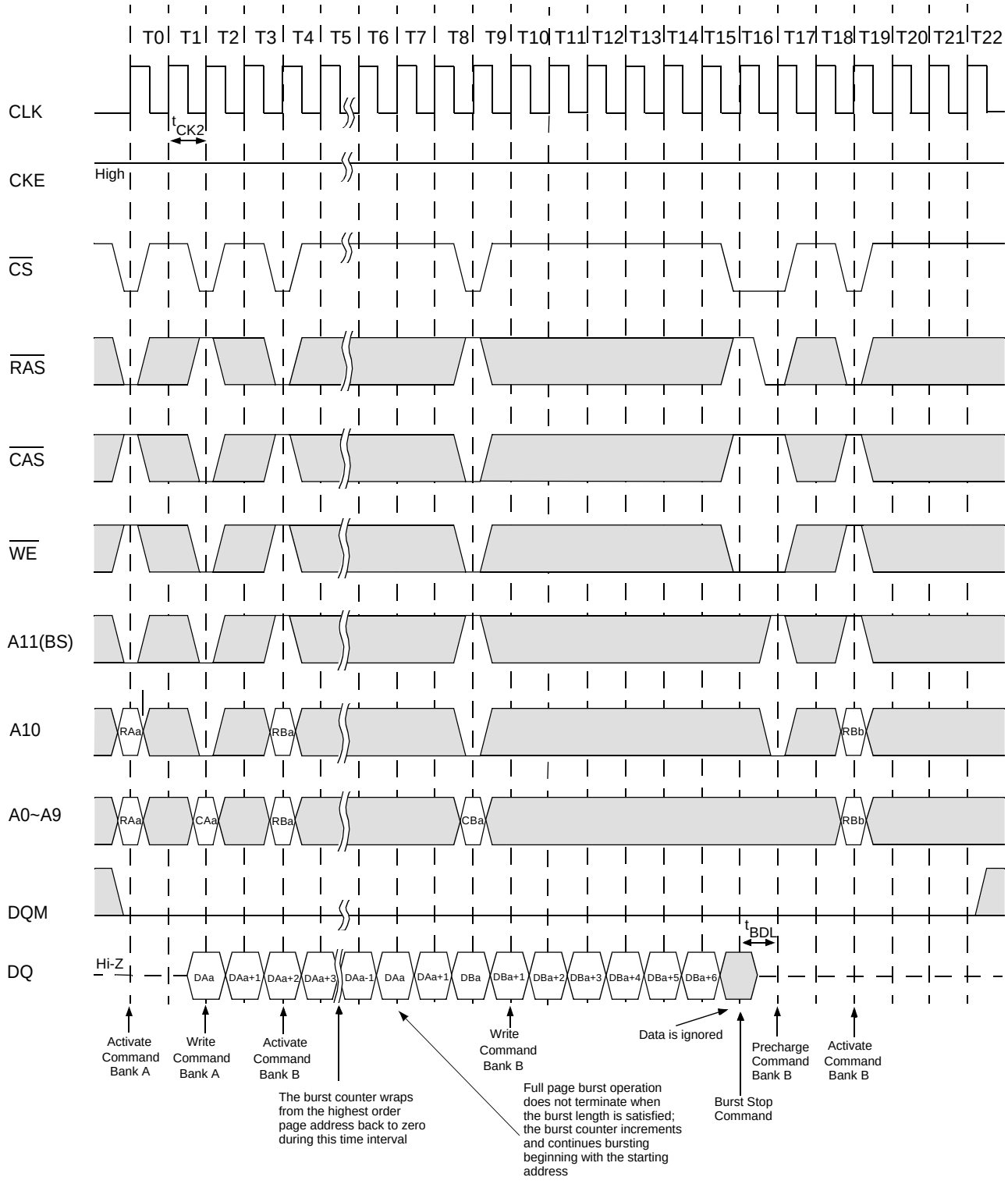
Full Page Read Cycle (2 of 2)

Burst Length=Full Page, $\overline{CAS}$ Latency=3



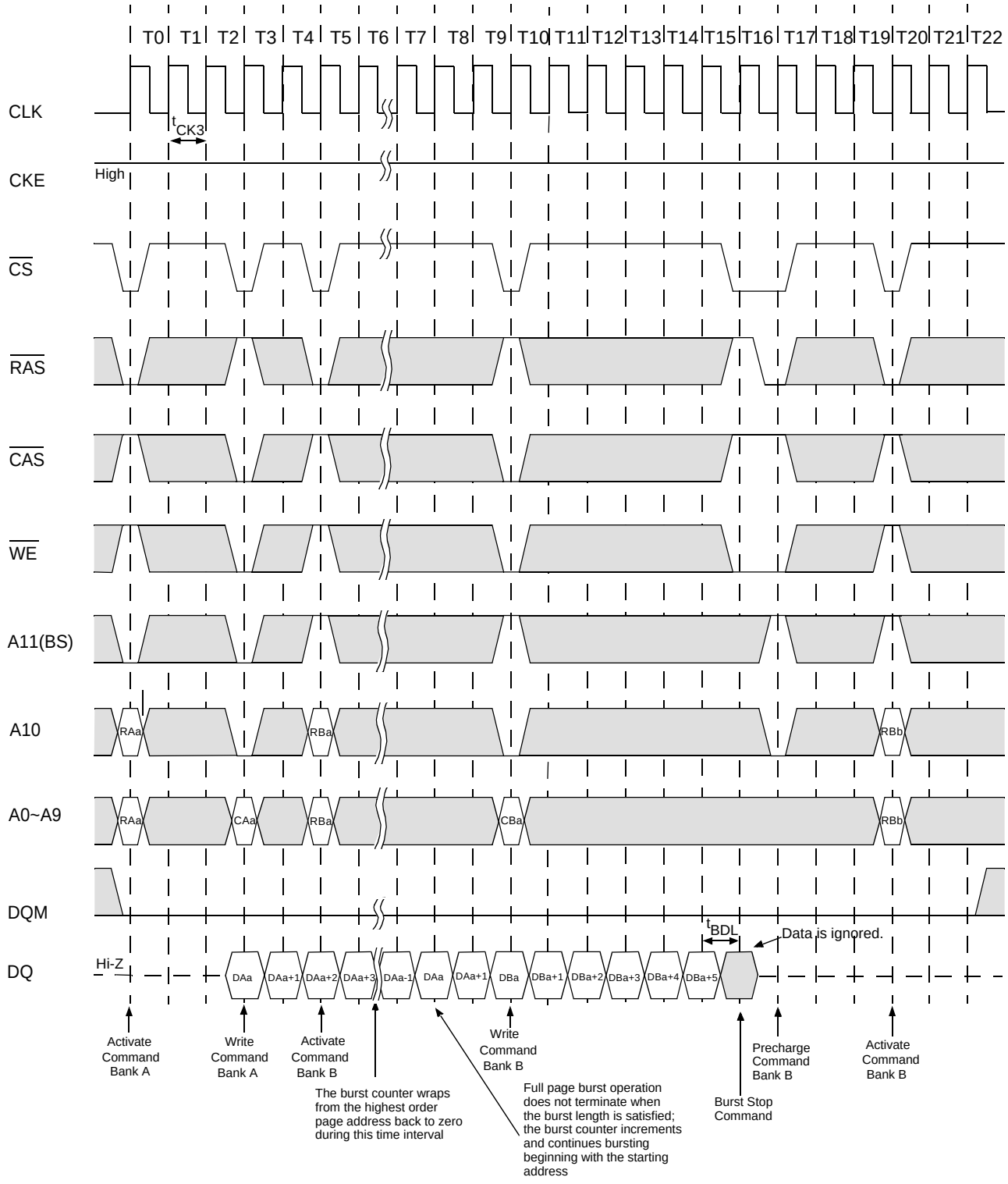
Full Page Write Cycle (1 of 2)

Burst Length=Full Page, $\overline{CAS}$ Latency=2



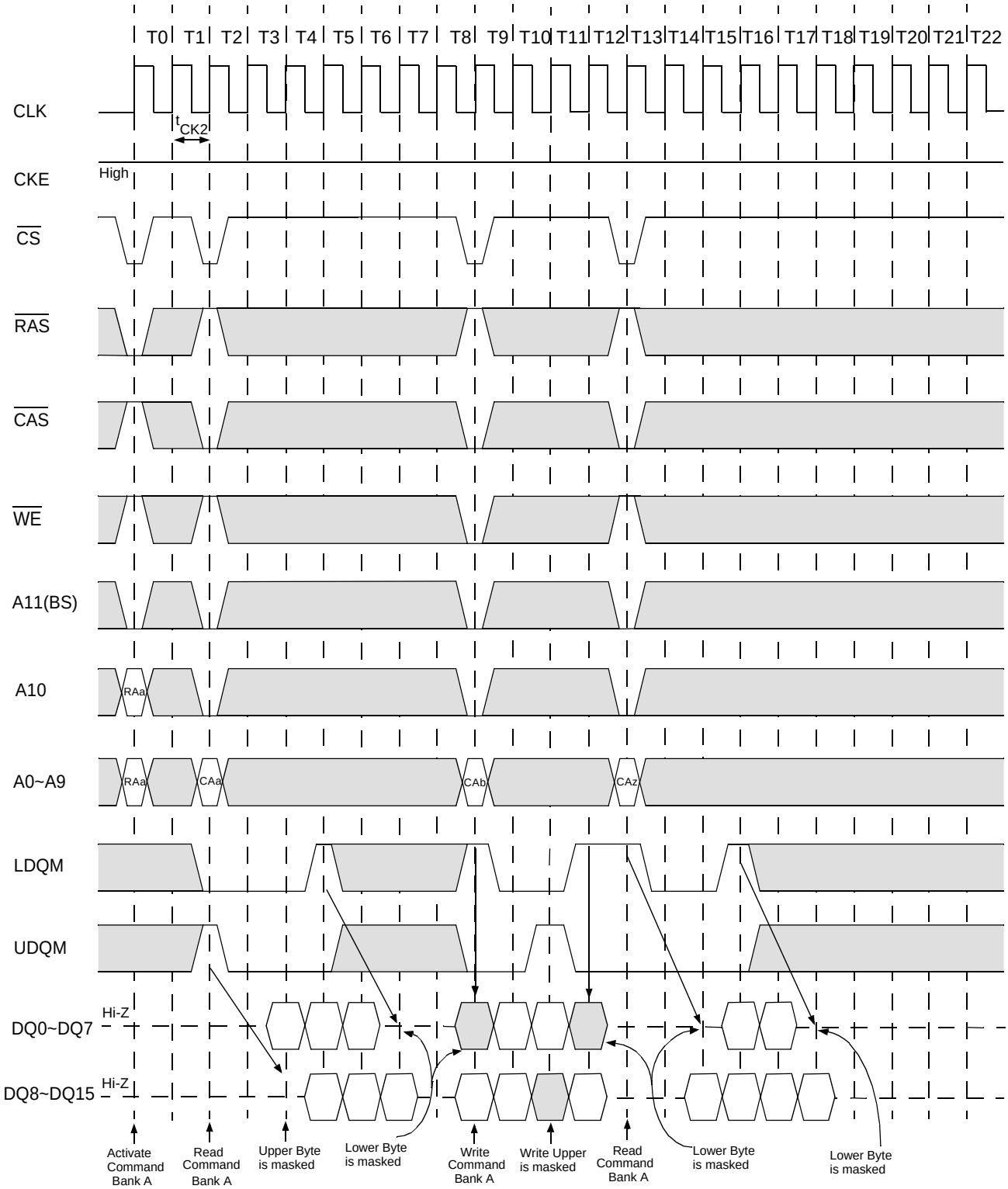
Full Page Write Cycle (2 of 2)

Burst Length=Full Page, $\overline{CAS}$ Latency=3



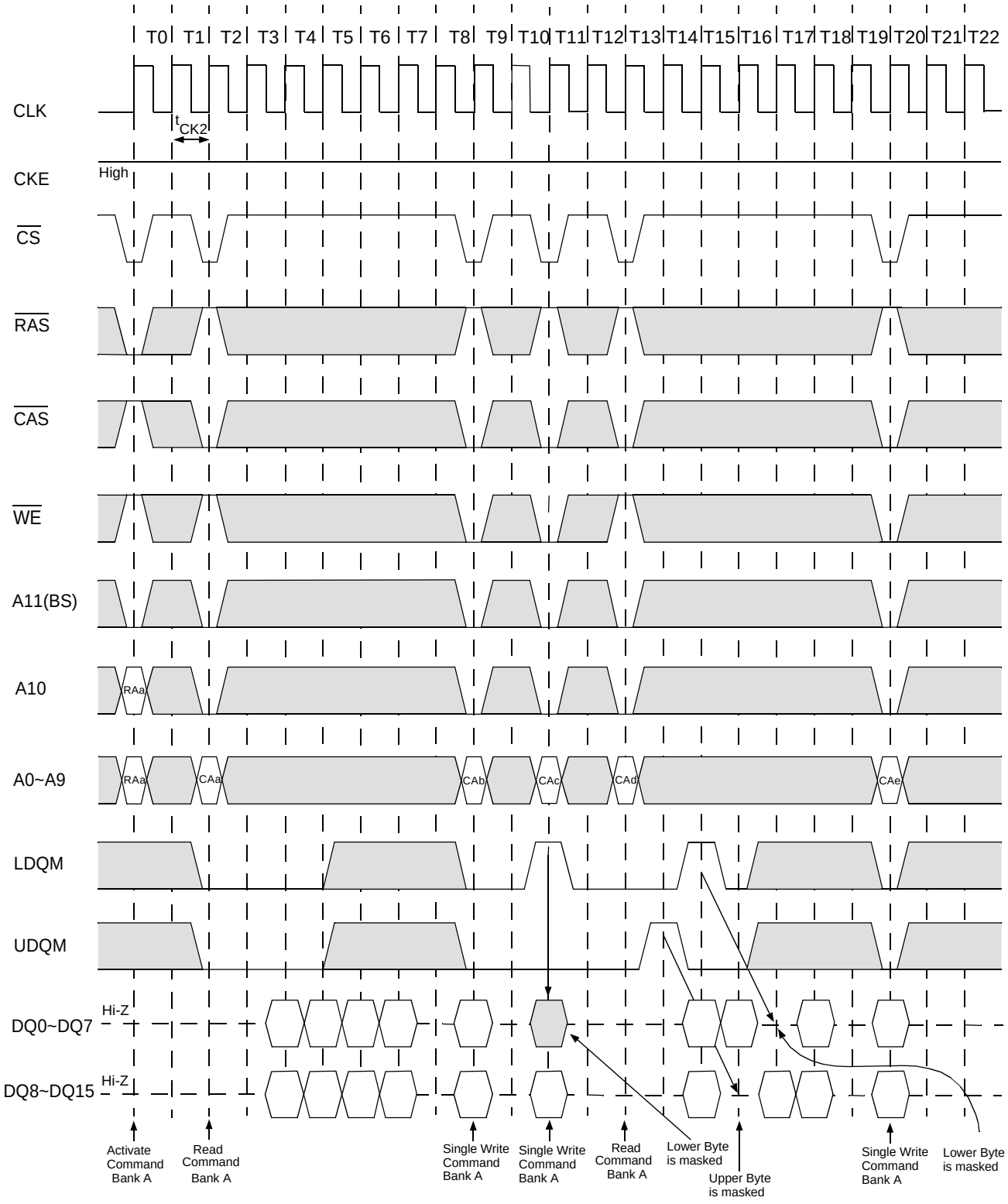
Byte Write Operation

Burst Length=4, $\overline{CAS}$ Latency=2



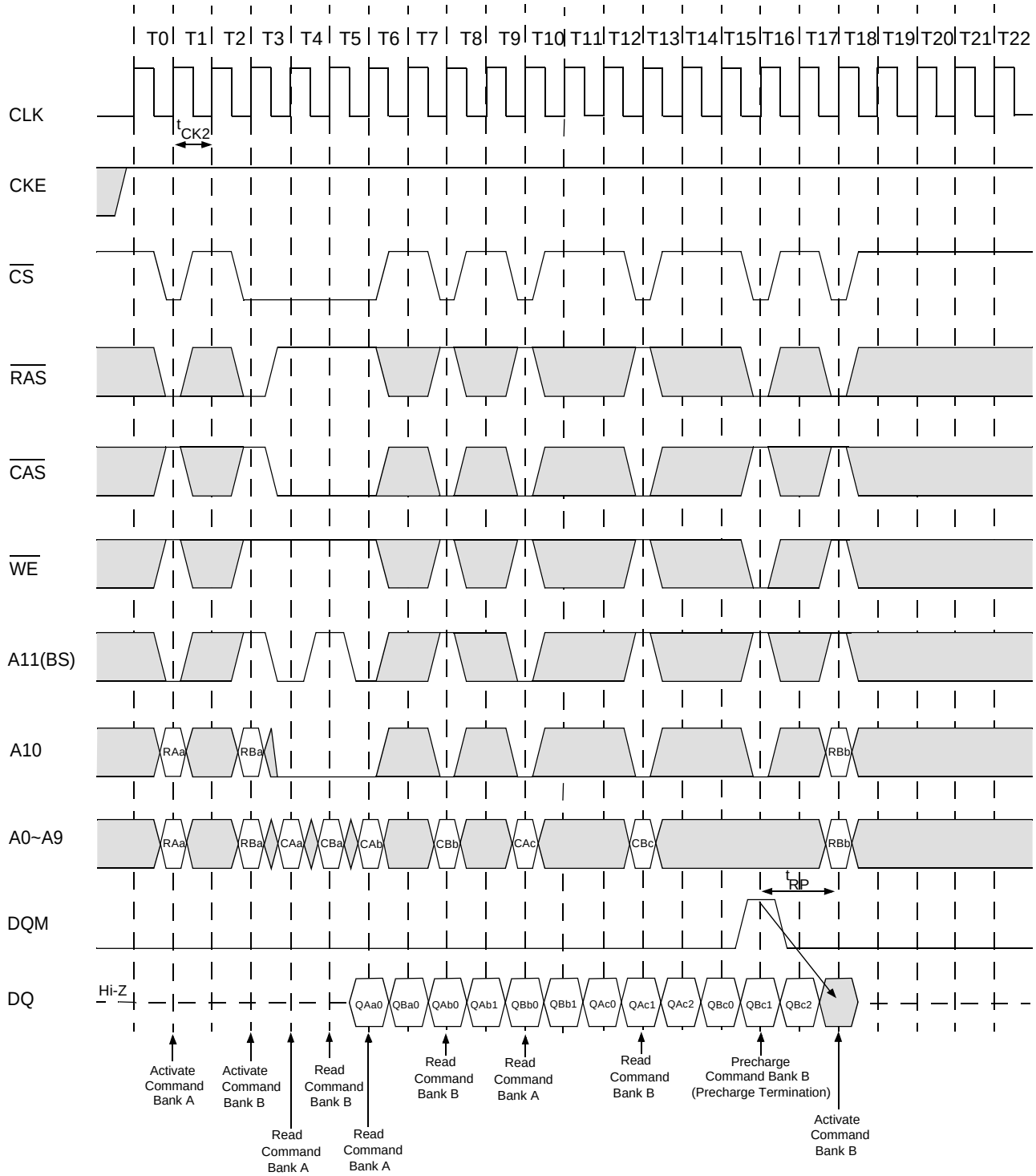
Burst Read and Single Write Operation

Burst Length=4, $\overline{CAS}$ Latency=2



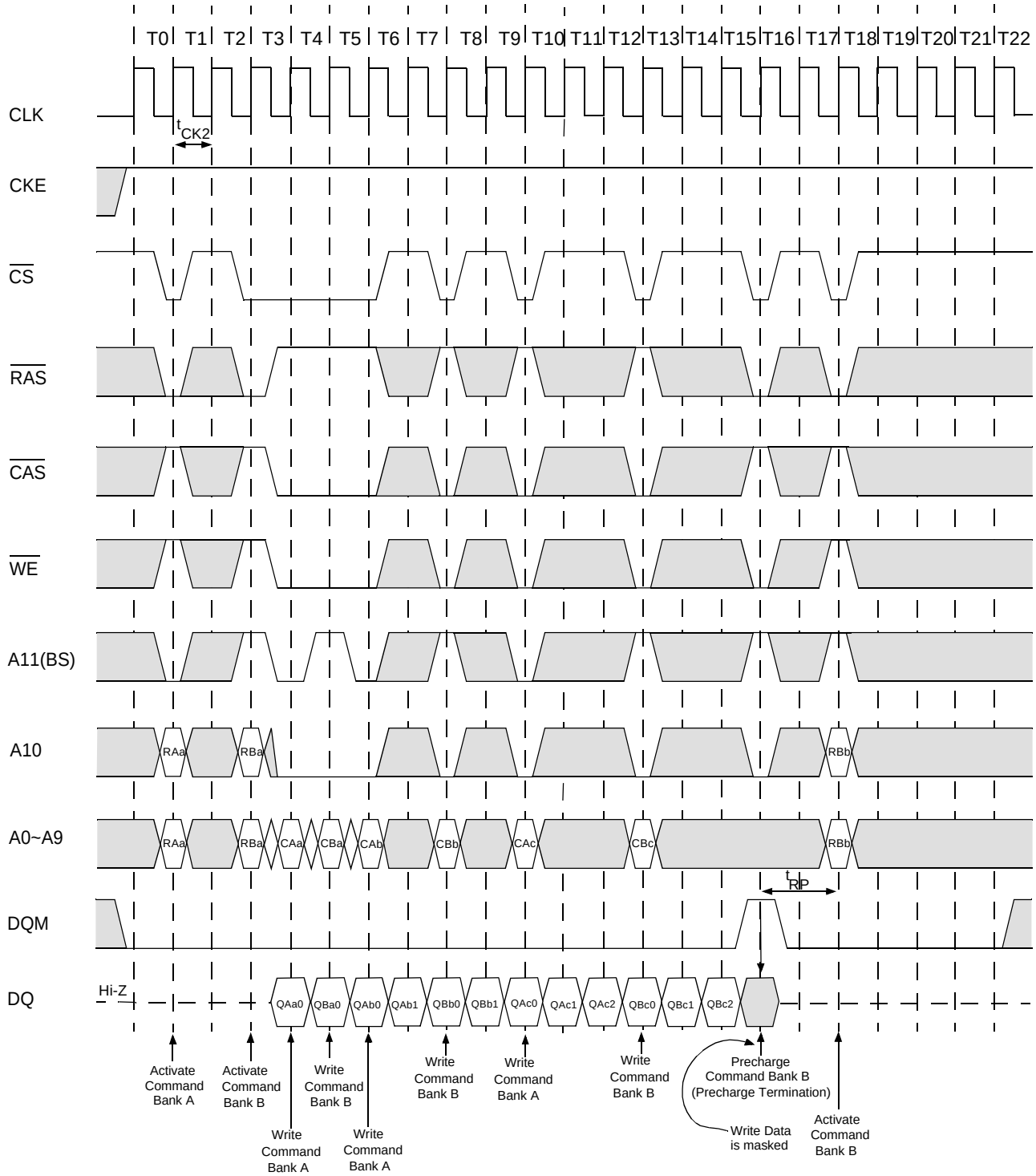
Full Page Random Column Read

Burst Length=Full Page, $\overline{CAS}$ Latency=2



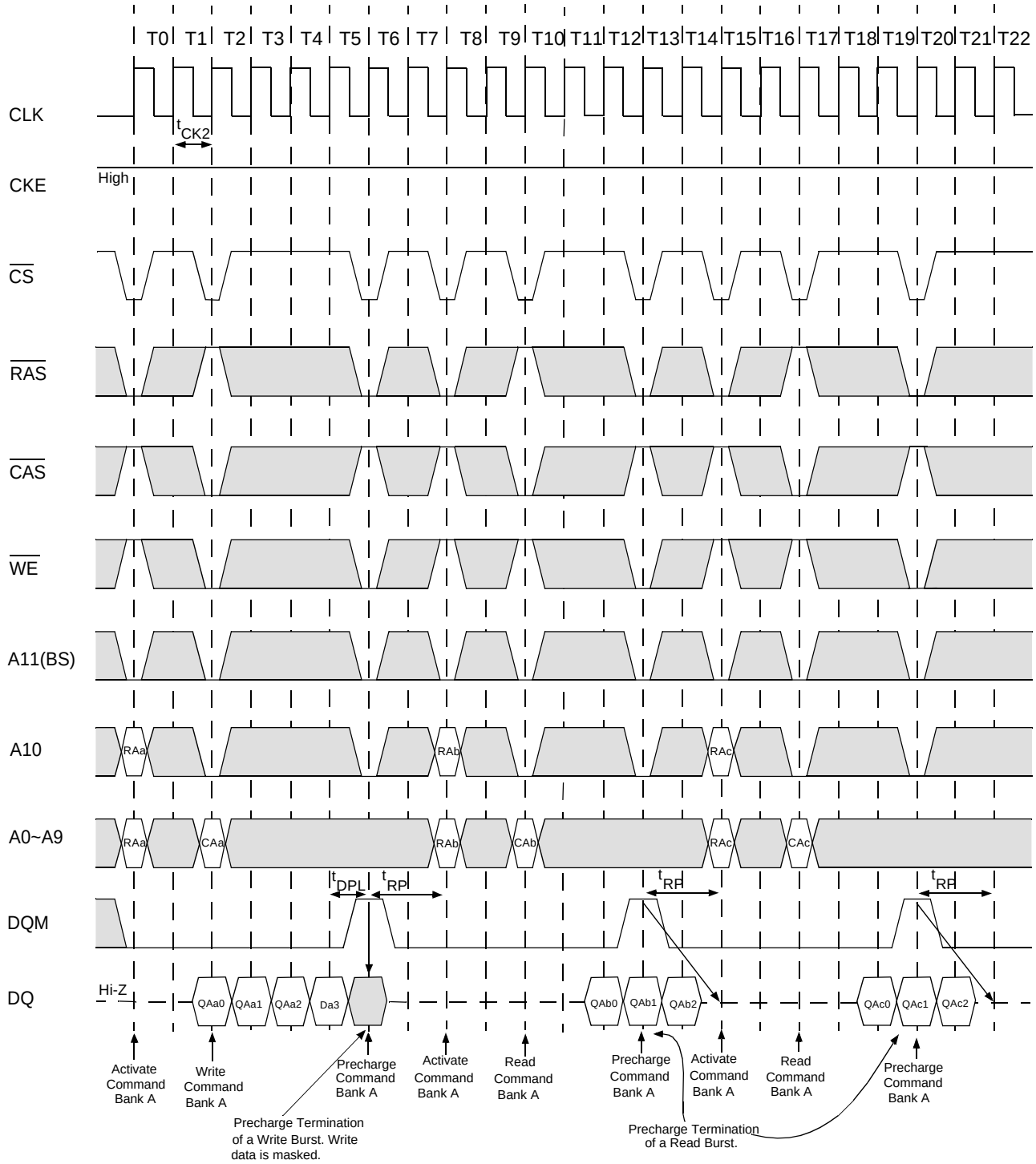
Full Page Random Column Write

Burst Length=Full Page, $\overline{CAS}$ Latency=2



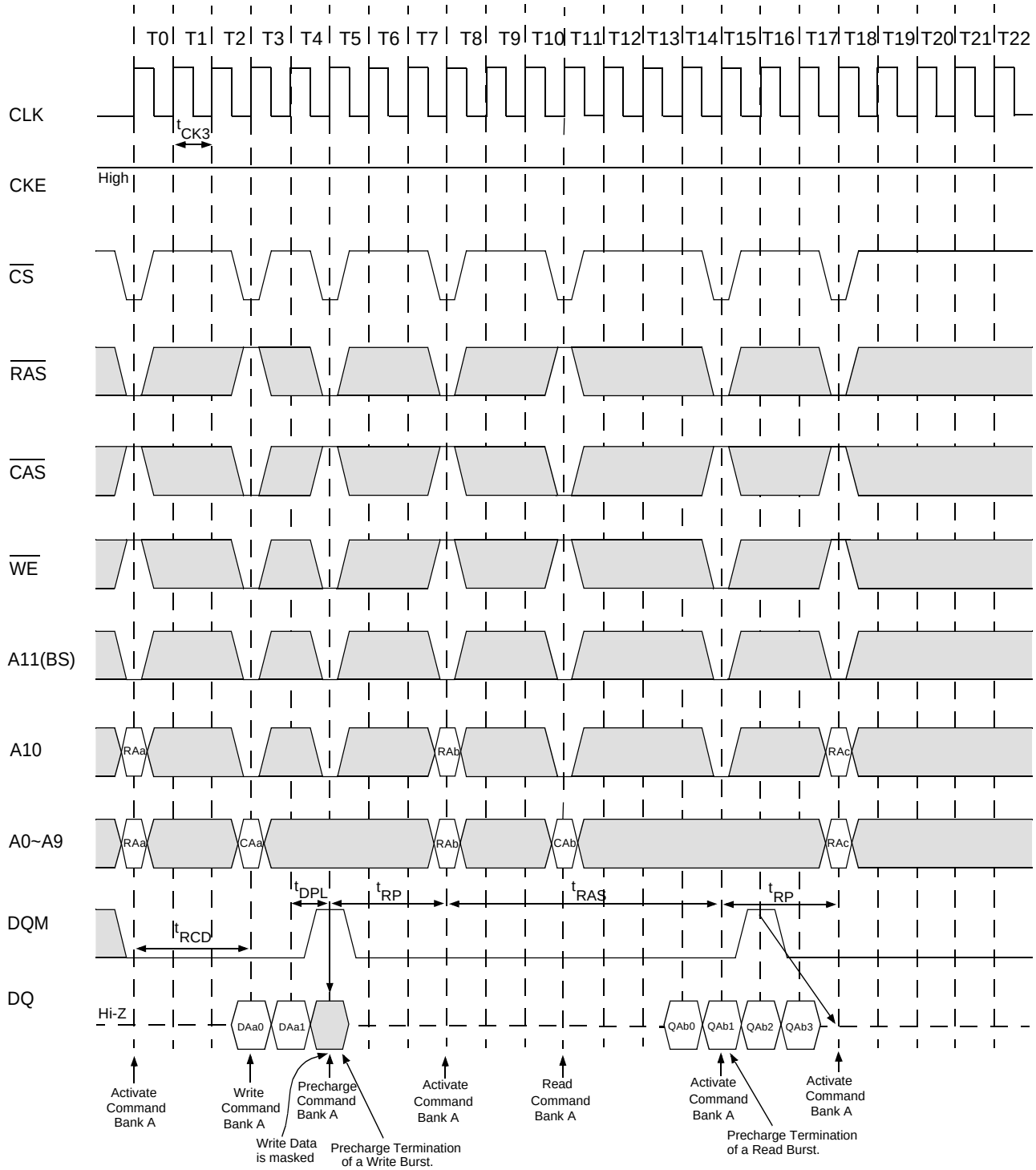
Precharge Termination of a Burst (1 of 2)

Burst Length=4,8 or Full Page, $\overline{CAS}$ Latency=2



Precharge Termination of a Burst (2 of 2)

Burst Length=4,8 or Full Page, $\overline{CAS}$ Latency=3



Ordering information

Part Number	Frequency@CL3	Package
VG3617161DT-6 VG3617161DT-7 VG3617161DT-8 VG3617161DT-10	166MHz 143MHz 125MHz 100MHz	400mil 50-Pin Plastic TSOP

VG3617161DT- 6

- VG → VIS Memory Product
- 36 → Technology/Design Rule
- 17161 → Device Type/Configuration
- B → Mask/Design Version
- T → Package Type, T: TSOP
- 6 → Cycle time, 6: 6ns, 7: 7ns, 8: 8ns, 10: 10ns

Packaging Information

400mil, 50-Pin Plastic TSOP

DIM	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.20	---	---	0.047
A1	0.05	---	0.15	0.002	---	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.30	---	0.45	0.012	---	0.018
b1	0.30	---	0.40	0.012	---	0.016
c	0.12	---	0.21	0.005	---	0.008
c1	0.11	---	0.16	0.0045	---	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
ZD	0.875 REF.			0.0344 REF.		
e	0.80 BASIC			0.0315 BASIC		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
R	0.11	---	0.25	0.004	---	0.010
R1	0.11	---	---	0.004	---	---

NOTE:
1. CONTROLLING DIMENSION : MILLIMETERS
2. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION.
   MOLD PROTRUSION SHALL NOT EXCEED 0.15mm(0.006") PER SIDE.
   DIMENSION E1 DOES NOT INCLUDE INTERLEAD PROTRUSION.
   INTERLEAD PROTRUSION SHALL NOT EXCEED 0.25mm(0.01") PER SIDE.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSIONS/INTRUSION.
   ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD TO BE WIDER THAN THE MAX b DIMENSION BY MORE THAN 0.13mm.
   DAMBAR INTRUSION SHALL NOT CAUSE THE LEAD TO BE NARROWER THAN THE MIN b DIMENSION BY MORE THAN 0.07mm.