

17-27GHz Variable Gain Amplifier *Preliminary*

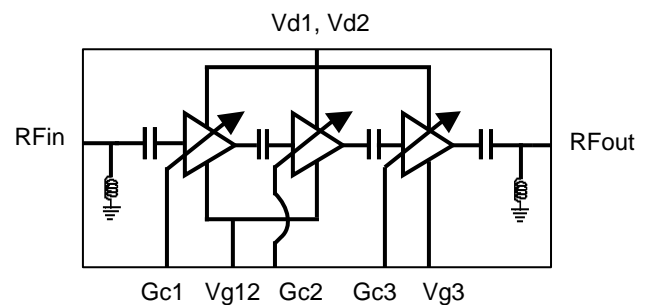
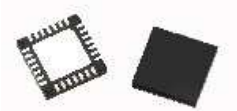
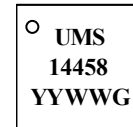
GaAs Monolithic Microwave IC in SMD package

Description

The P014458-QGG is a variable gain broadband three-stage monolithic amplifier. It is designed for a wide range of applications, typically commercial communication systems.

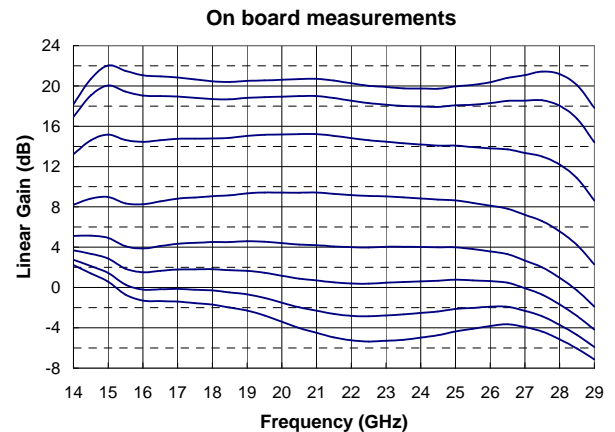
The circuit is manufactured with a power pHEMT process, 0.15 μ m gate length, via holes through the substrate and air bridges.

It is available in lead-free SMD package.



Main Features

- Broadband performance 17-27GHz
- 20dB gain
- 28dBm output IP3 @ gain max
- 24dB gain control range
- 28L-QFN5x5
- ESD protected (see page 13)



Main Characteristics

Tamb. = 25°C, Vd = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		27	GHz
G	Small signal gain		20		dB
Gc	Gain control range		24		dB
OIP3	Output Intercept Point order 3 @ gain max.		28		dBm

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

Electrical CharacteristicsTamb. = 25°C, Vd_{1,2} = 4.5V, GcX with X=1,2,3*Preliminary*

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		27	GHz
G	Nominal gain @ gain max.		20		dB
NF	Noise Figure @ gain max.		7.5		dB
	Noise Figure @ gain min.		24		dB
RLin	Input Return Loss (Fop<21GHz) (any GcX)		-9		dB
	Input Return Loss (Fop>21GHz) (any GcX)		-12		dB
RLout	Output Return Loss (Fop<21GHz) (any GcX)		-9		dB
	Output Return Loss (Fop>21GHz) (any GcX)		-12		dB
OIP3	Output Intercept Point order 3 @ gain max.		28		dBm
	Output Intercept Point order 3 @ gain min.		19		dBm
P1dB	Output Power at 1dB gain compression @ gain max.		22		dBm
Gc	Gain control range (Fop<20GHz)		22		dB
	Gain control range (Fop>20GHz)		24		dB
Vd _{1,2}	DC drain voltage		4.5		V
Id	Drain bias current (*)		250		mA
Idc	Drain current at 1dB gain compression		300		mA
Vg _{12,3}	Gate bias voltage		-1.2		V
GcX	DC gain control voltage	-2		+0,6	V

(*) Id not affected by GcX.

These values are representative of on board measurements as defined on the drawing 97263 (see page 15).

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Absolute Maximum Ratings (*)

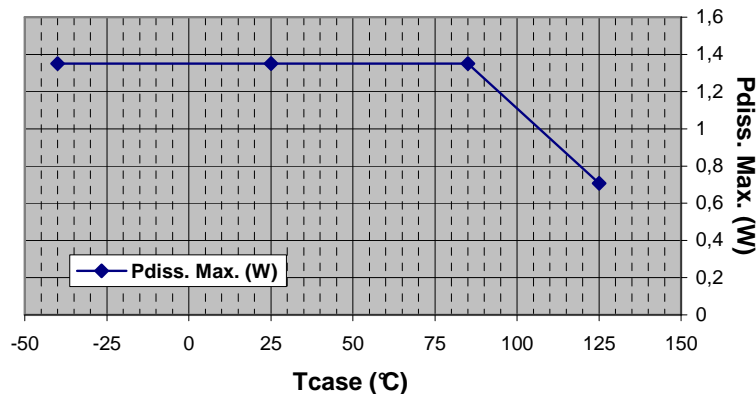
Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd _{1,2}	Drain bias voltage	5	V
Id	Power supply quiescent current	300	mA
Vg	Gate bias voltage	-2 to 0	V
GcX	DC gain control voltage	-2.5 to +1	V
Pin	RF input power @ gain max.	8	dBm
Top	Operating temperature range	-40 to +85	°C
Tj	Junction temperature	175	°C
Tstg	Storage temperature range	-55 to +125	°C

(*) Operation of this device above anyone of these parameters may cause permanent damage.

DEVICE THERMAL SPECIFICATION : VGA-P014458-QGG

Max. junction temperature (Tj max)	:	170 °C
Max. continuous dissipated power @ Tcase= 85 °C	:	1,35 W
=> P _{diss} derating above Tcase= 85 °C	:	16 mW/°C
Device thermal resistance (Rth)	:	62 °C/W
Min. package back side operating temperature	:	-40 °C
Max. package back side operating temperature	:	85 °C
Min. storage temperature	:	-55 °C
Max. storage temperature	:	125 °C



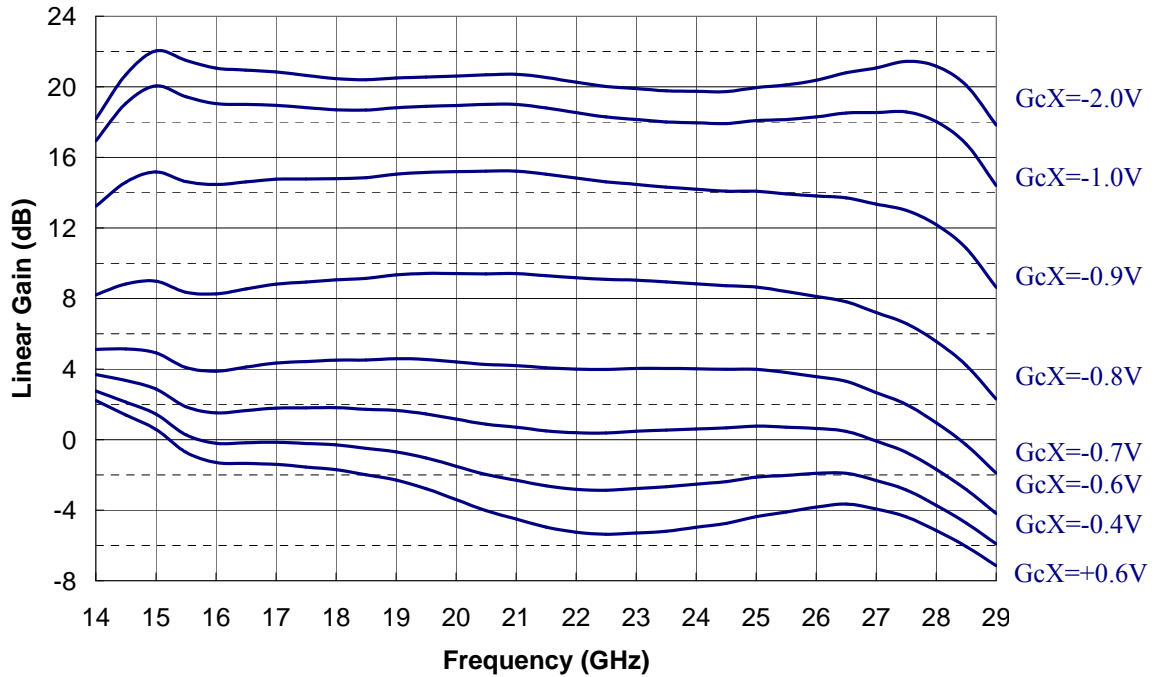
Typical Measured Performance

Preliminary

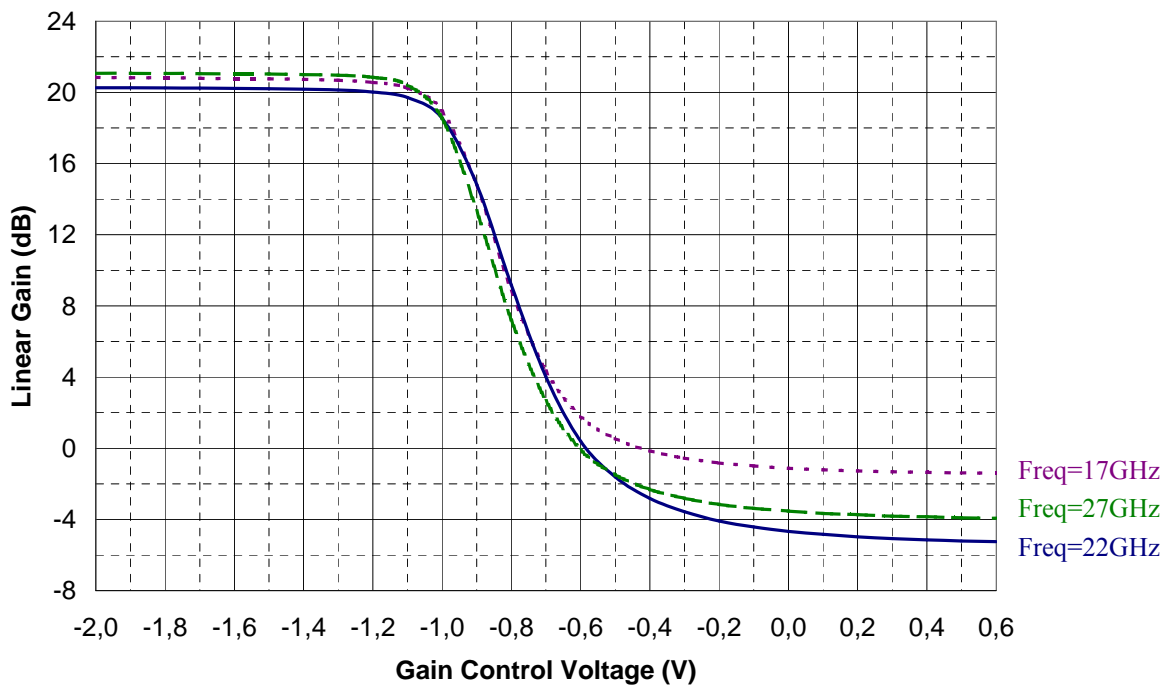
Tamb. = +25°C, Vd_{1,2} = +4.5V, Vg_{12,3} tuned for Id = 250mA

Measurements in the package access planes, using the proposed land pattern & board 97263, as defined page 15.

Linear Gain versus Frequency

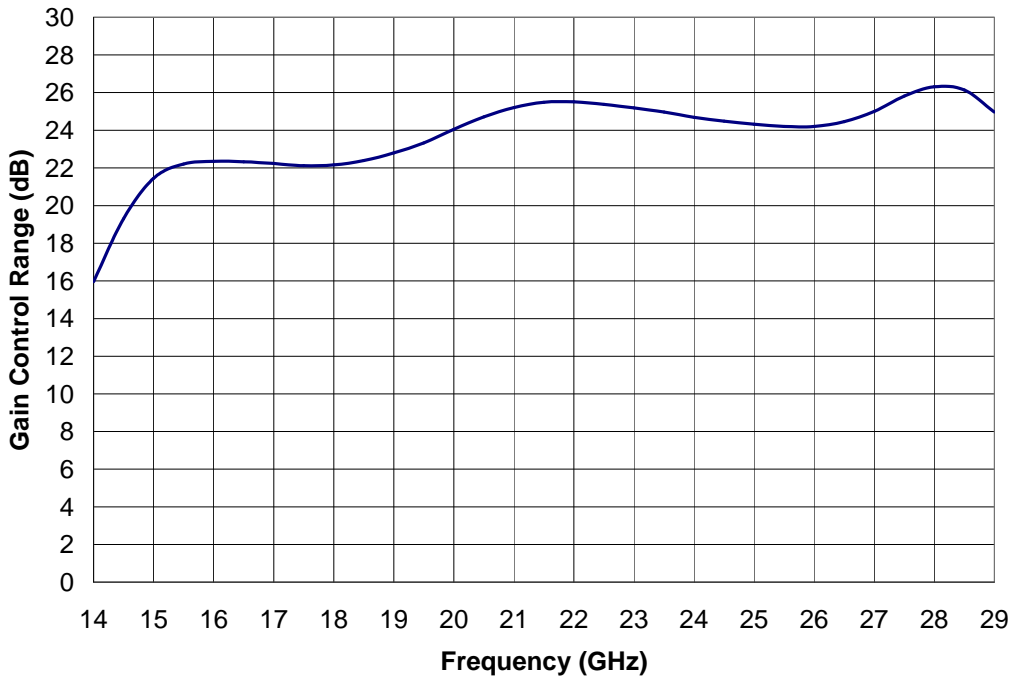


Linear Gain versus Gain Control Voltage

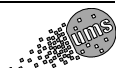
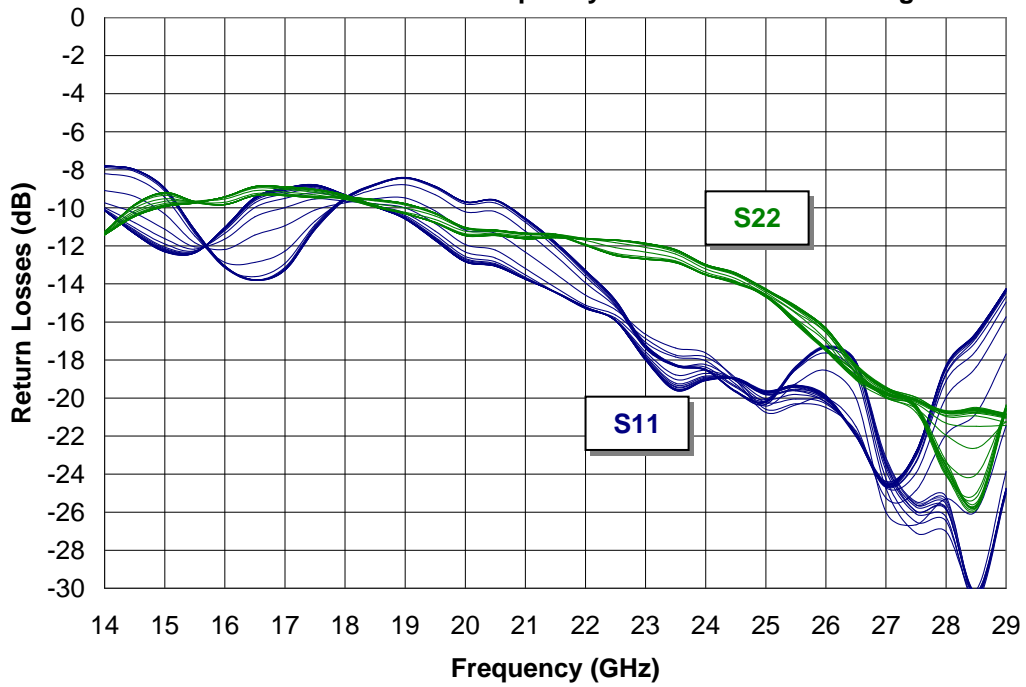


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Gain Control Range versus Frequency



Return Losses versus Frequency and Gain Control Voltage



Typical Package Sij parameters for GcX = -2.0V

Preliminary

Tamb. = +25°C, Vd_{1,2} = +4.5V, Id = 250mA

Freq (GHz)	dB(S11)	Ph(S11) (°)	dB(S12)	Ph(S12) (°)	dB(S2 1)	Ph(S21) (°)	dB(S22)	Ph(S22) (°)
2,0	-1,6	105	-62,6	-93	-35,2	-166	-10,7	74
3,0	-3,2	55	-64,1	-151	-26,3	-30	-6,2	152
4,0	-6,8	-11	-84,6	64	-35,7	-141	-1,8	109
5,0	-11,6	-104	-75,6	162	-29,5	51	-1,9	74
6,0	-11,1	173	-69,7	66	-16,8	-70	-2,7	40
7,0	-9,6	125	-62,7	56	-11,8	-167	-4,0	7
8,0	-8,0	93	-62,1	5	-6,5	121	-6,5	-26
9,0	-7,6	58	-63,1	-28	-3,1	50	-10,3	-50
10,0	-8,0	23	-64,2	-90	-0,5	-16	-14,5	-61
11,0	-7,4	-10	-64,7	-128	3,5	-72	-14,9	-57
12,0	-7,8	-47	-64,2	176	7,0	-133	-14,5	-64
13,0	-7,1	-78	-70,6	-173	12,6	167	-13,2	-71
14,0	-7,8	-109	-57,9	163	18,2	92	-11,3	-78
15,0	-9,0	-134	-50,7	110	22,0	-5	-9,2	-100
16,0	-13,1	-152	-51,1	57	21,1	-99	-9,8	-119
17,0	-13,3	-132	-52,8	36	20,8	-173	-9,4	-132
17,5	-11,2	-128	-52,4	28	20,7	152	-9,5	-139
18,0	-9,6	-133	-53,6	19	20,5	118	-9,5	-144
18,5	-8,8	-146	-53,7	12	20,4	84	-9,6	-151
19,0	-8,4	-158	-53,0	0	20,5	49	-9,8	-159
19,5	-8,9	-169	-55,7	-2	20,6	13	-10,3	-165
20,0	-9,7	179	-54,9	-9	20,6	-24	-11,0	-172
20,5	-9,6	174	-58,8	-29	20,7	-58	-11,2	-176
21,0	-10,6	161	-60,3	16	20,7	-94	-11,3	-179
21,5	-11,8	150	-56,0	32	20,5	-131	-11,4	174
22,0	-13,3	137	-54,6	3	20,3	-167	-12,0	168
22,5	-14,9	134	-54,3	1	20,0	157	-12,5	162
23,0	-17,2	139	-55,6	18	19,9	122	-12,7	154
23,5	-18,3	134	-54,2	17	19,8	86	-12,9	145
24,0	-18,5	130	-52,0	33	19,8	47	-13,5	132
24,5	-19,7	132	-48,1	23	19,7	13	-13,9	121
25,0	-20,3	119	-46,1	15	20,0	-25	-14,6	102
25,5	-18,4	102	-45,0	-7	20,1	-64	-16,1	86
26,0	-17,3	81	-43,5	-7	20,4	-104	-17,4	75
26,5	-18,1	52	-43,4	-21	20,8	-148	-18,9	53
27,0	-23,1	32	-43,1	-35	21,1	167	-19,8	23
28,0	-25,6	23	-39,4	-54	21,2	60	-23,3	-37
29,0	-24,7	36	-40,6	-72	17,8	-61	-20,5	-44
30,0	-15,8	15	-40,1	-91	9,8	-178	-18,3	-103
31,0	-9,0	-28	-38,5	-111	0,8	86	-15,5	-122
32,0	-6,3	-90	-36,1	-131	-10,4	-5	-13,1	-149
33,0	-3,7	-134	-36,4	-167	-20,6	-85	-10,5	-167
34,0	-2,6	-169	-40,1	157	-29,4	-161	-7,8	178
35,0	-1,4	164	-42,7	139	-37,1	146	-5,5	160
36,0	-1,7	138	-46,8	119	-43,1	97	-4,1	142
37,0	0,4	127	-55,8	-165	-52,9	152	-2,3	128
38,0	-0,1	109	-46,0	143	-43,0	117	-1,1	112
39,0	-0,1	95	-48,7	135	-48,2	144	-0,5	99
40,0	-1,1	82	-50,9	90	-50,0	57	-0,6	87

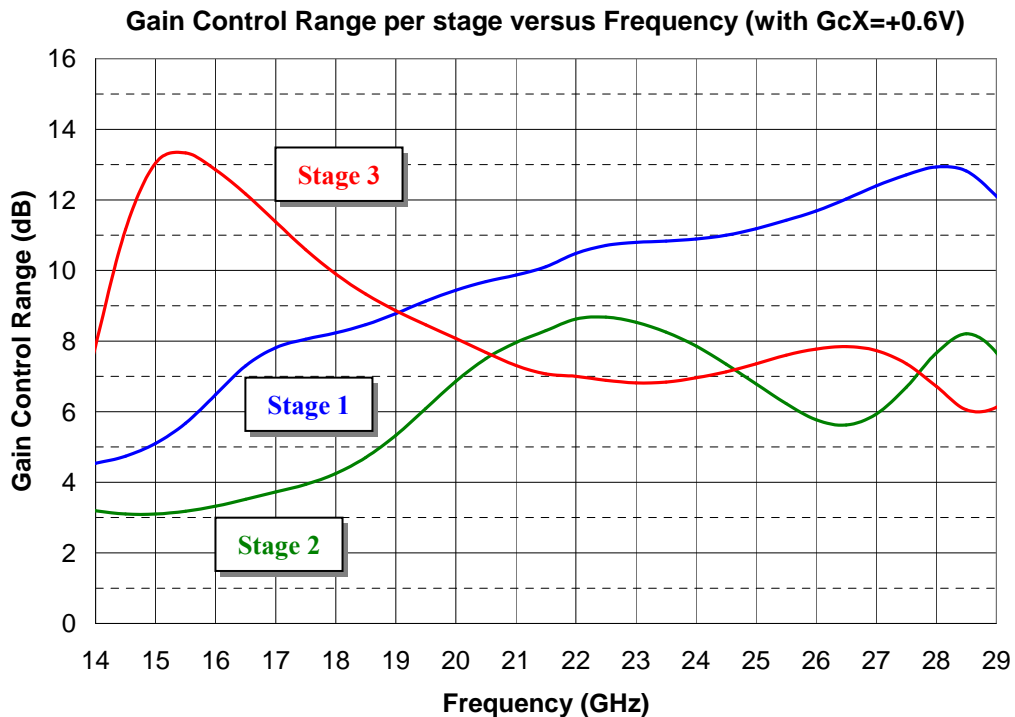
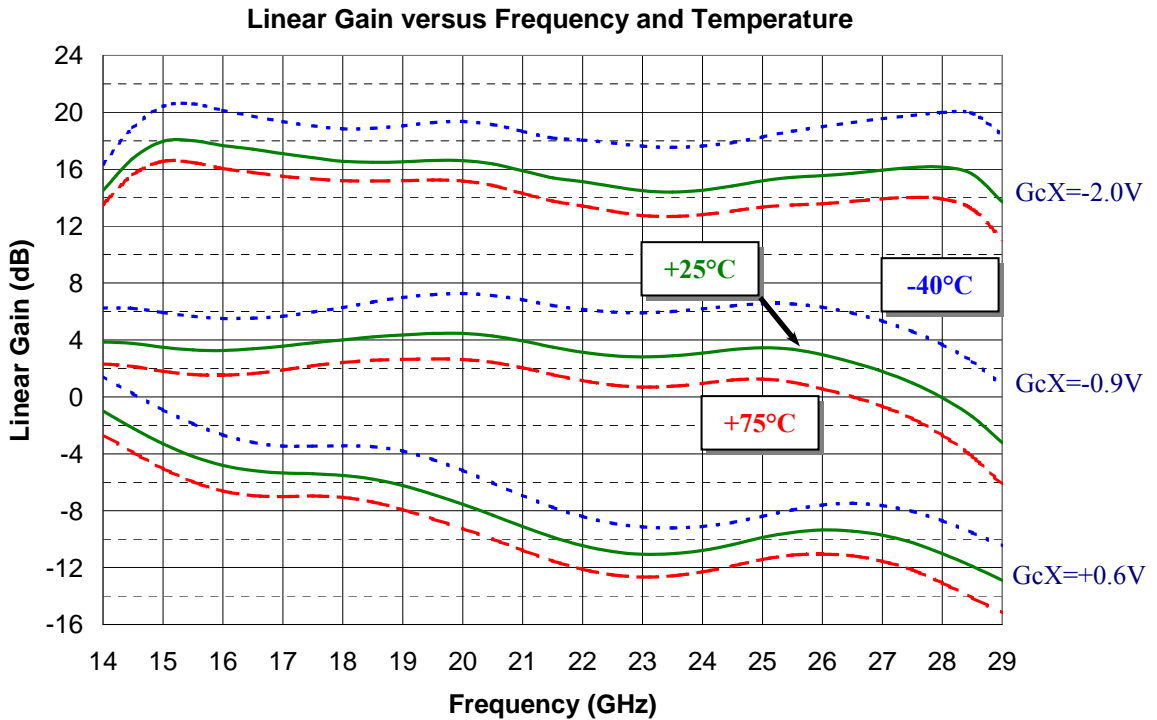
Refer to the "definition of the Sij reference planes" section below.

Typical Measured Performance

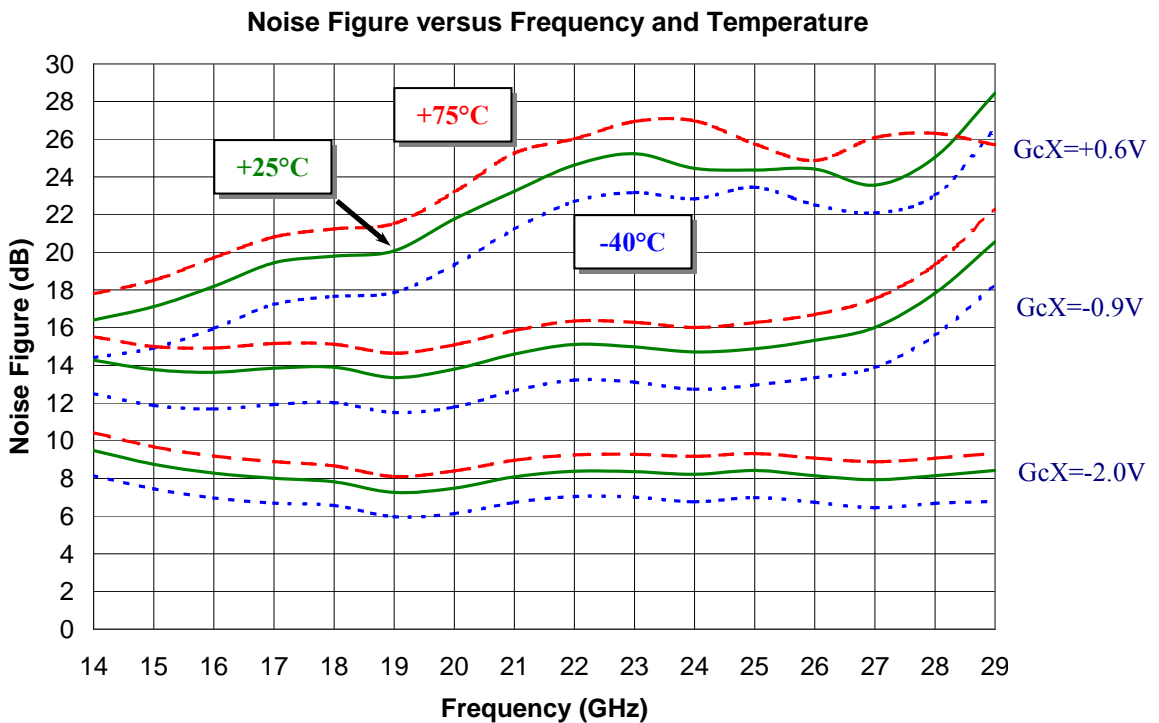
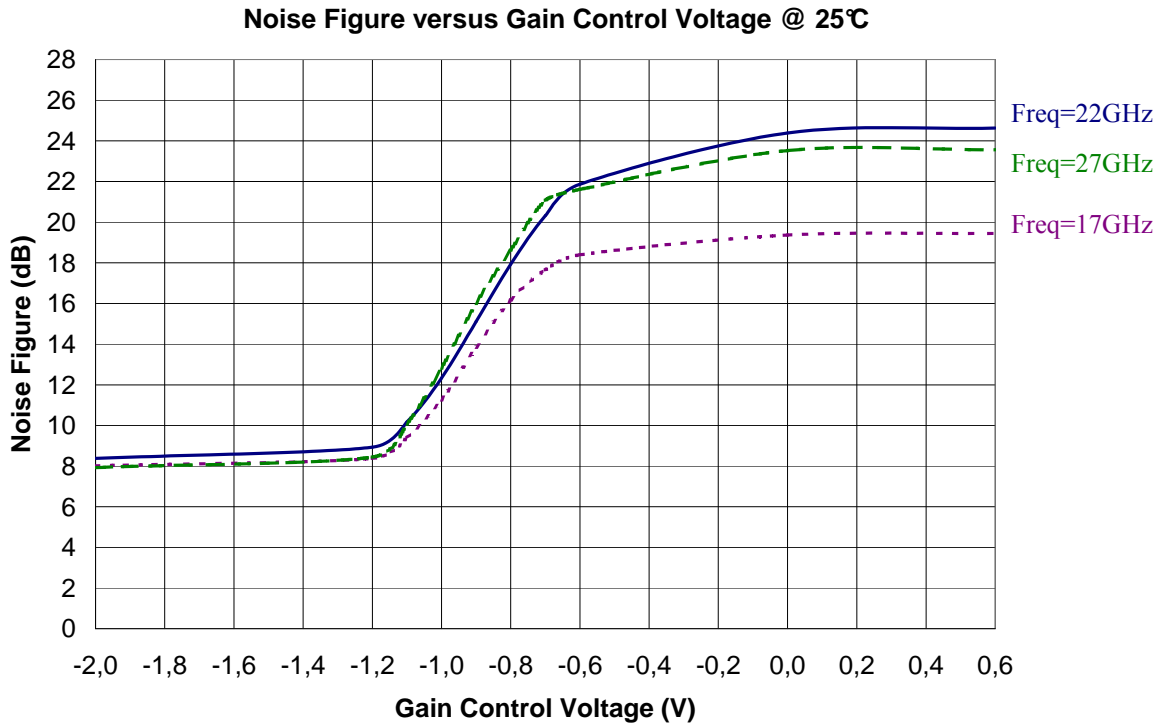
Preliminary

Tamb. = +25°C, Vd_{1,2} = +4.5V, Vg_{12,3} tuned for Id = 250mA

Measurements in the plan of the connectors (losses not deembedded), using the proposed land pattern & board 97263, as defined page 15.

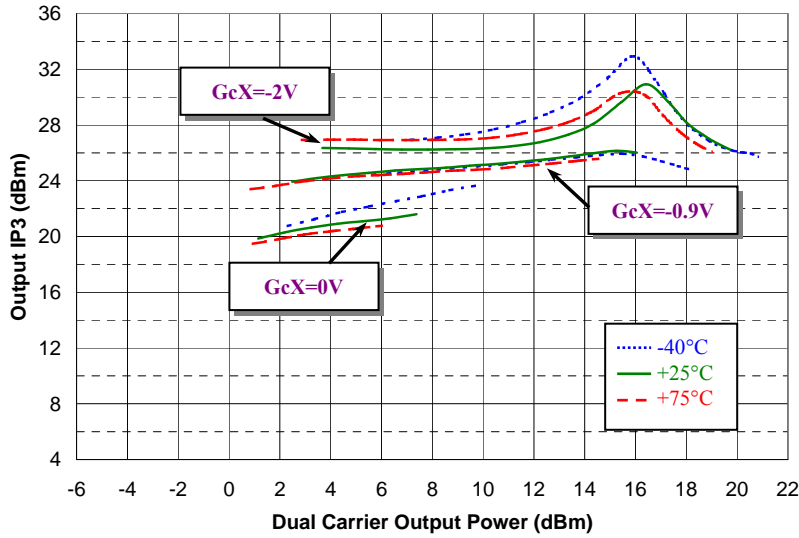


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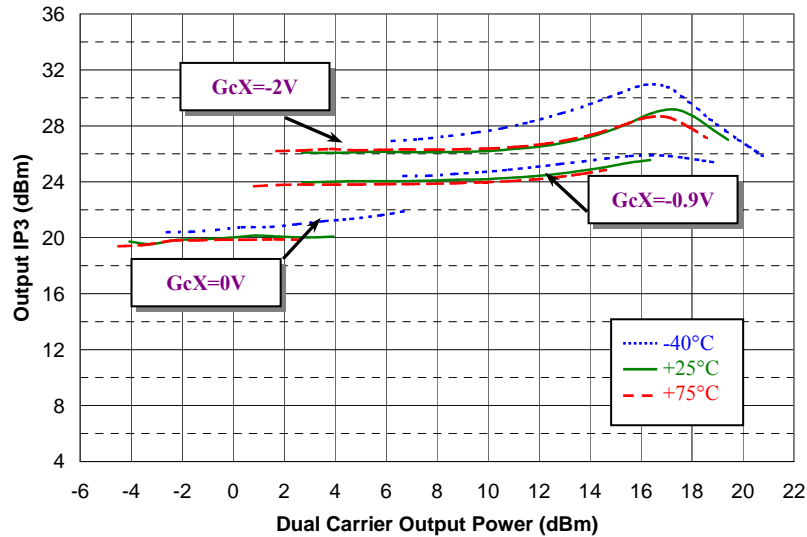


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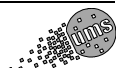
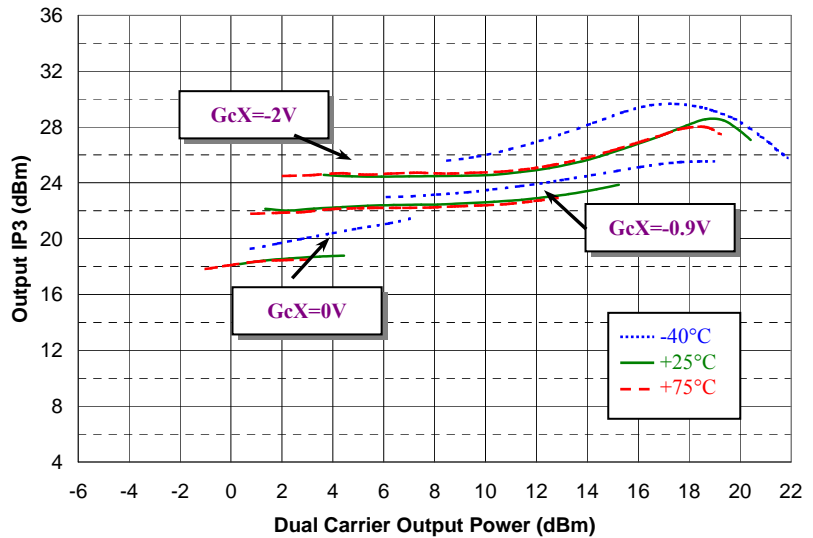
Output IP3 versus Dual Carrier Output Power and Temperature @ 17GHz



Output IP3 versus Dual Carrier Output Power and Temperature @ 21GHz

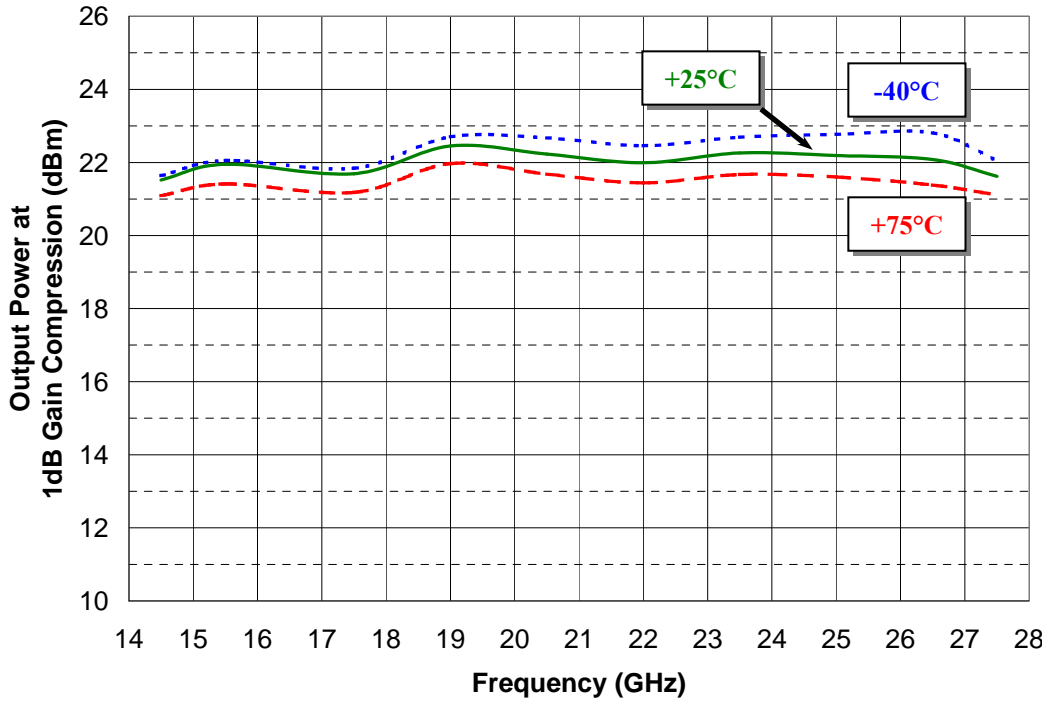


Output IP3 versus Dual Carrier Output Power and Temperature @ 27GHz



Preliminary

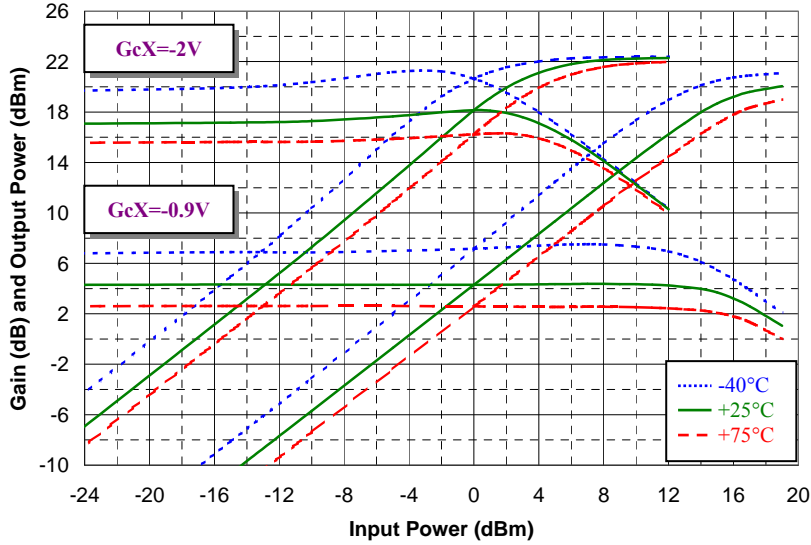
Output Power at 1dB Gain Compression versus Frequency and Temperature for GcX=-2V



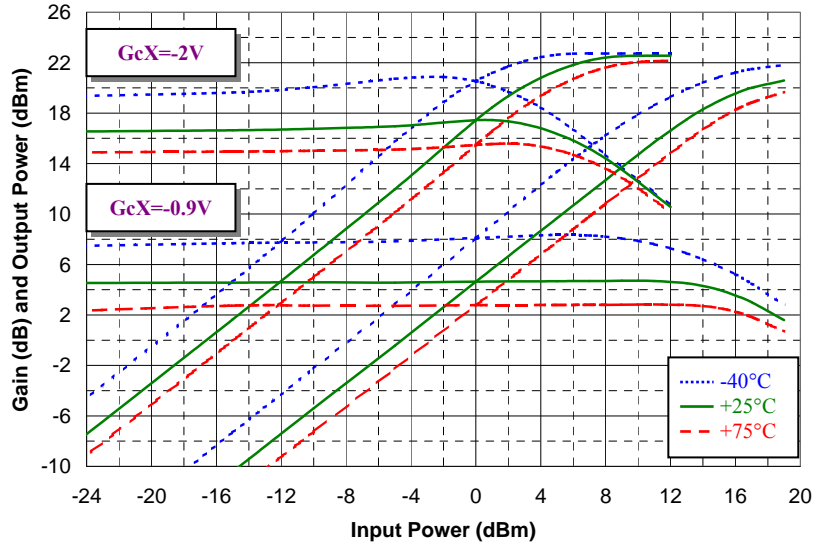
17-27GHz Variable Gain Amplifier VGA-P014458-QGG

Preliminary

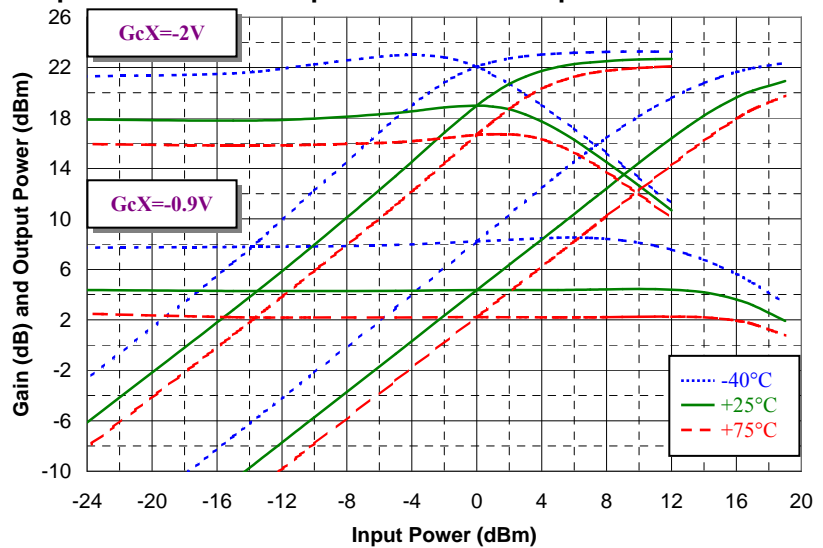
Gain and Output Power versus Input Power and Temperature @ 17.5GHz



Gain and Output Power versus Input Power and Temperature @ 22GHz

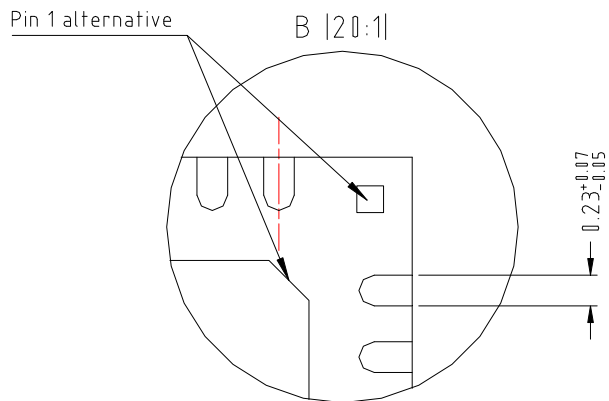
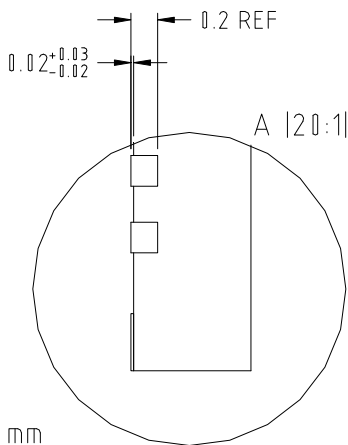
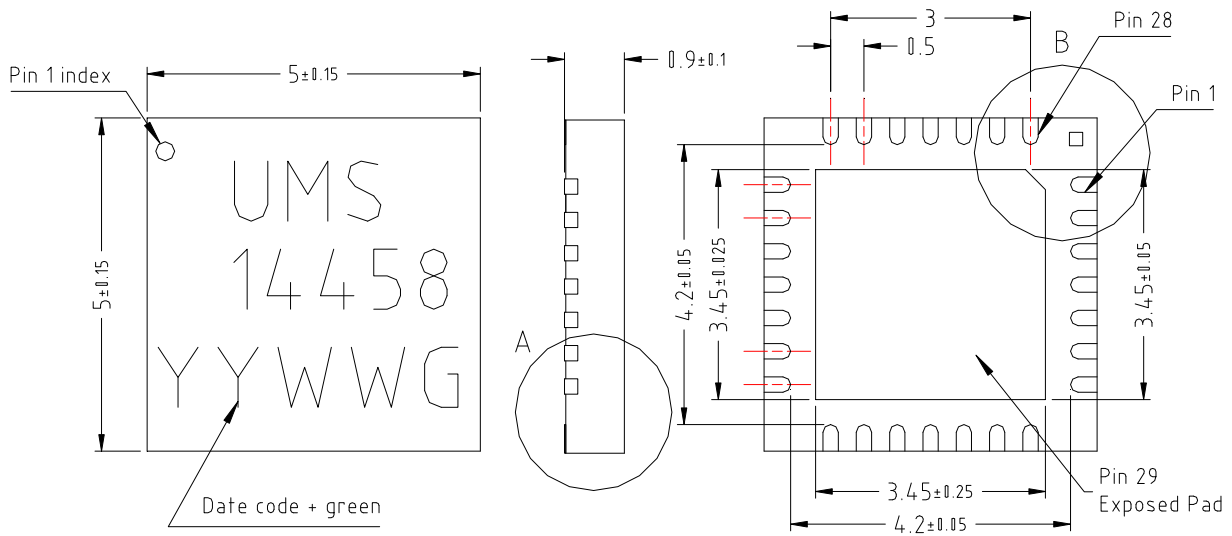


Gain and Output Power versus Input Power and Temperature @ 26.5GHz



Package outline

Preliminary



Units : mm

From the standard : JEDEC MO-220 [VHHD-3]

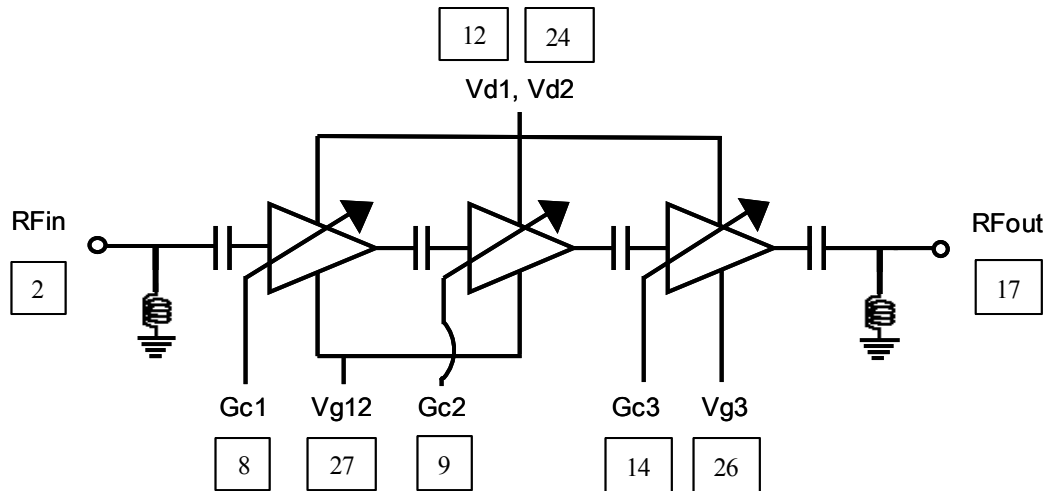
Matt tin, Lead free |Green|

1- Gnd	9- Gc2	17- RF OUT	25- Nc
2- RF IN	10- Nc	18- Gnd	26- Vg3
3- Gnd	11- Nc	19- Gnd	27- Vg12
4- Gnd	12- Vd1	20- Nc	28- Nc
5- Nc	13- Nc	21- Gnd	29- Gnd
6- Gnd	14- Gc3	22- Nc	
7- Gnd	15- Gnd	23- Nc	
8- Gc1	16- Gnd	24- Vd2	

Preliminary

Note

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



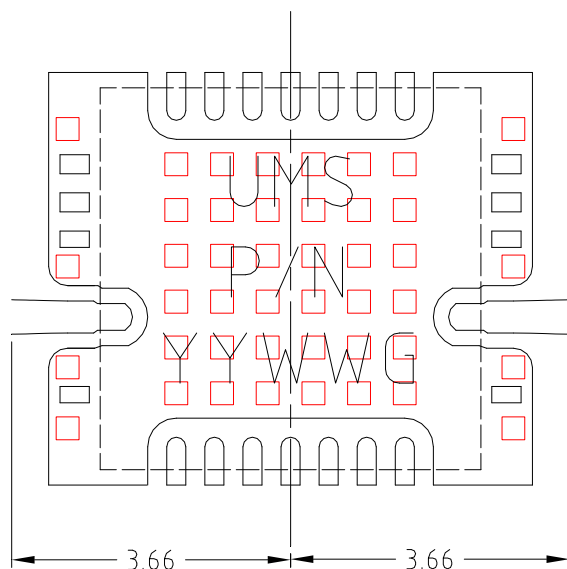
ESD protections are also implemented on gate accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

Definition of the Sij reference planes

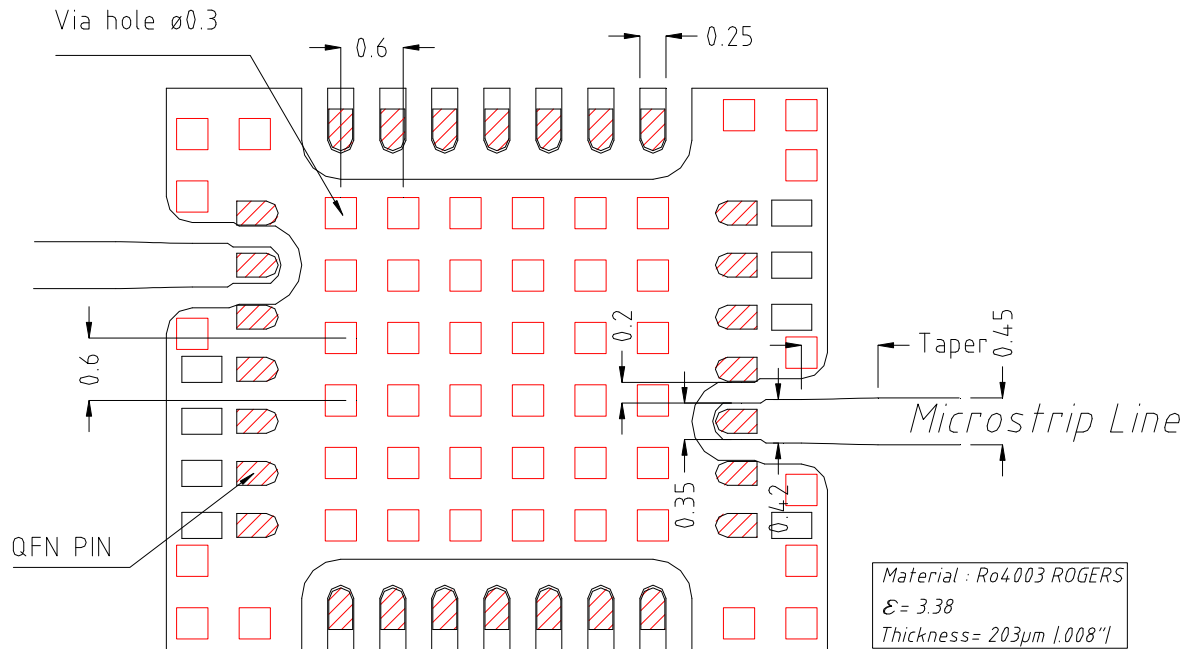
The reference planes are defined from the footprint of the recommended characterization board shown to the right.

The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.66mm offset (input wise and output wise respectively) from this axis. Then, the given Sij incorporates this land pattern.



Preliminary

Recommended footprint for 28L-QFN5X5



SMD mounting procedure

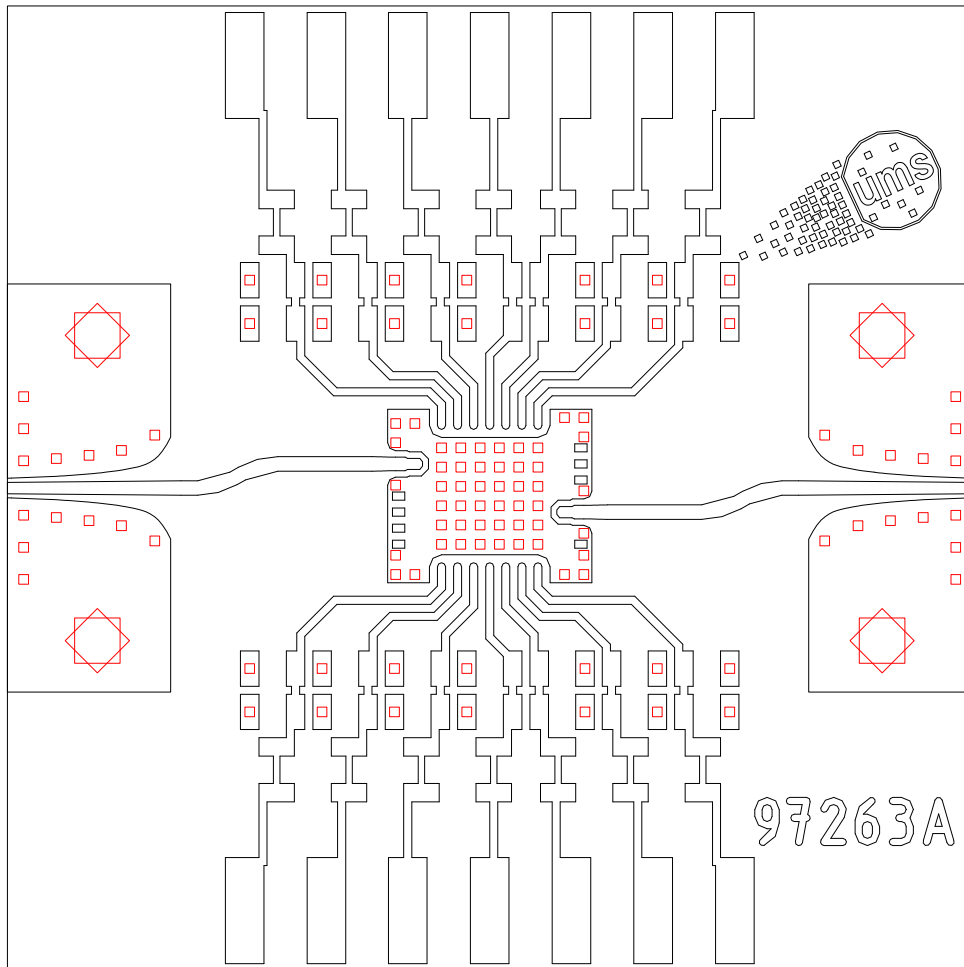
The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawing above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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Proposed Assembly board "97263" for the 28L-QFN5x5 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Decoupling capacitors of 10nF \pm 10% are recommended for all DC accesses.

Preliminary

Ordering Information

QFN 5x5 RoHS compliant package: VGA-P014458-QGG/XY
Stick: XY = 20 Tape & reel: XY = 21

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