DATEL

Model VI-7660
Monolithic Voltage Converter

FEATURES

- **Easy +5V dc supply conversion to ±5V supplies**
- **Simple voltage multiplication (V_{OUT} = (−)nV_{IN})**
- **99.9% Typical voltage conversion efficiency (RL = ∞)**
- **98% Typical power efficiency**
- **Wide operating voltage range of 1.5V dc to 10.0V dc**
- **Requires only 2 non-critical passive components**

GENERAL DESCRIPTION

The VI-7660 is a monolithic CMOS power supply circuit which offers unique performance advantages over previously available devices. The VI-7660 performs the complete supply voltage conversion from positive to negative for an input range of +1.5V dc to +10.0V dc, resulting in complementary output voltages of −1.5 to −10.0V with the addition of only two non-critical external capacitors needed for the charge pump and charge reservoir functions. Note that an additional diode is required for V_{SUPPLY} > 6.5V dc.

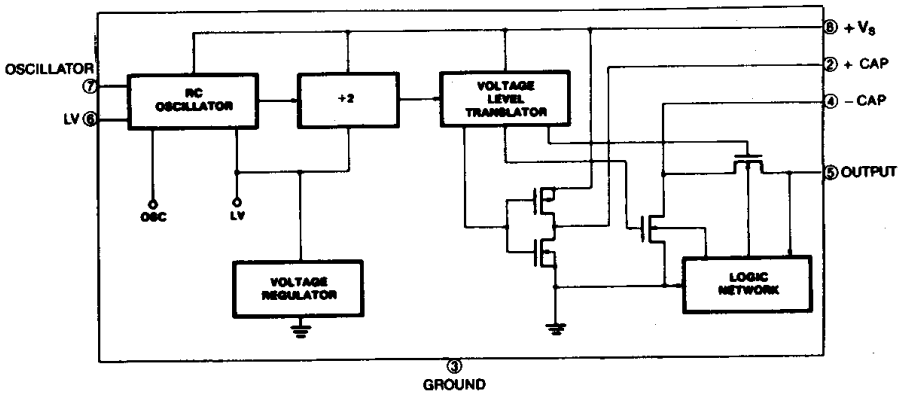
Contained on chip are a series dc power supply regulator, RC oscillator, voltage level translator, four output power MOS switches, and a unique logic element which senses the most negative voltage in the device and ensures that the output N-channel switches are not forward biased. This assures latch-up free operation.

The oscillator, when unloaded, oscillates at a nominal frequency of 10 kHz for an input supply voltage of 5.0 volts. This frequency can be lowered by the addition of an external capacitor to the OSC terminal, or the oscillator may be overdriven by an external clock.

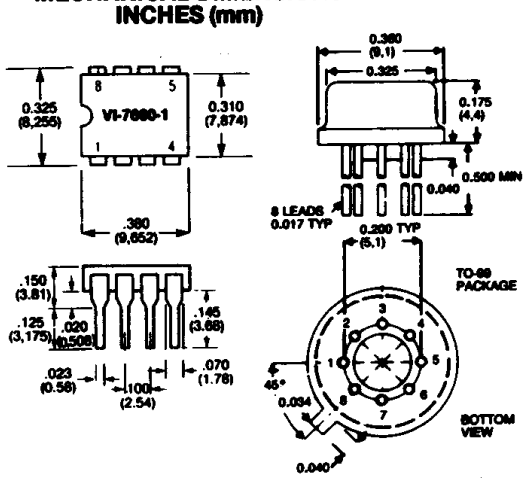
The LV terminal may be tied to GROUND to bypass the internal series regulator and improve low voltage operation. At medium to high voltages (+3.5 to +10.0 volts), the LV pin is left floating to prevent device latch-up.

Typical applications for the VI-7660 will be data acquisition and microprocessor based systems where there is a +5V dc supply available for the digital functions and an additional −5V dc supply is required for the analog functions. The VI-7660 is also ideally suited for providing low current, −5V dc body bias supply for dynamic RAMs.

The VI-7660 operates over the commercial 0°C to +70°C temperature range. It is available packaged in either an 8-pin TO-99 can or an 8-pin plastic DIP.



MECHANICAL DIMENSIONS INCHES (mm)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION
1	N.C.
2	+ CAP
3	GROUND
4	− CAP
5	OUTPUT
6	LV
7	OSCILLATOR
8	+ Vs (Input)

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ABSOLUTE MAXIMUM RATINGS	
Power Supply Voltage	10.5V
Input Voltage[1] LV, OSC (Pins 6, 7)	
$V_s > 5.5V$	$-0.3V$ to $(V_s + 0.3V)$
$V_s < 5.5V$	$(+V_s - 5.5V)$ to $(+V_s + 0.3V)$
Input Current LV (Pin 6)	20 µA
Output Short Circuit Duration[2]	Continuous
Power Dissipation; VI-7660-1[3]	300 mW
VI-7660-2	500 mW

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, +5V Supply, Cosc = 0, unless otherwise noted.

INPUT CHARACTERISTICS	
Supply Current, Max[4]	500 µA
Supply Voltage Range High, min.[5]	3.0V
max.	6.5V
Supply Voltage Range Low, min.[6]	1.5V
max.	3.5V
Supply Voltage Range High, min.[6]	3.0V
max.	10.0V
Supply Voltage Range Low, min.[7]	1.5V
max.	3.5V
PERFORMANCE	
Output Source Resistance, max.[8]	100 Ω
Oscillator Frequency	10 kHz
Voltage Conversion Efficiency, min.	97%
Power Efficiency, min.[9]	95%
Oscillator Impedance, $+V_s = 2V$	1 MΩ
$+V_s = 5V$	100 kΩ
PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Soldering Temperature, (10 sec)	300°C

FOOTNOTES:

1. Do not connect any terminal to voltages greater than $+V_s$ or less than ground or destructive latch-up may occur. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the device.
2. For $+V_s$ greater than or equal to 5.5V.
3. Derate linearly above 50°C by 5.5 mW/°C.
4. $R_L = \infty$
5. 0°C to +70°C, R_L = 10 kΩ, LV open and D_x out of circuit.
6. 0°C to +70°C, R_L = 10 kΩ, LV open and D_x in circuit.
7. 0°C to +70°C, R_L = 10 kΩ, LV to ground, D_x in circuit.
8. 0°C to +70°C, R_L = 10 kΩ, LV to ground, D_x out of circuit.
9. Iout = 20 mA. T_A = 25°C. 120Ω max., over 0°C to +70°C. 400Ω max over 0°C to +70°C, $+V_s$ = 2V, Iout = 3 mA, LV to ground.
10. R_L = 5 kΩ.

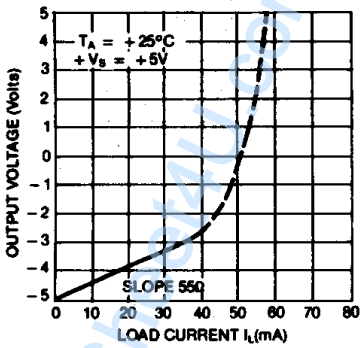
TECHNICAL NOTES

1. For improved low voltage operation, the "LV" terminal (Pin 6) should be connected to ground (this disables the regulator). For supply voltages greater than 3.5V, the "LV" terminal must be left open to insure latch-up proof operation. Never exceed the maximum rated supply voltage ($+V_s$).
2. The output (Pin 5) should not be shorted to the supply voltage pin (Pin 8) for supply voltages above 5.5V for extended periods of time. However, transient conditions, including start-up are acceptable.
3. If using polarized capacitors for charge pumping and charge reservoir functions, the positive terminal of C1 must be connected to Pin 2 of the VI-7660 and the positive terminal of C2 must be connected to ground. (See typical connection diagrams, page 4.)
4. To operate with voltages up to 10V over temperature without the danger of latch-up, a general purpose diode (D_x) must be added in series with the devices output. The affect of the diode (D_x) is the reduction of output voltage by one diode drop (0.6V).

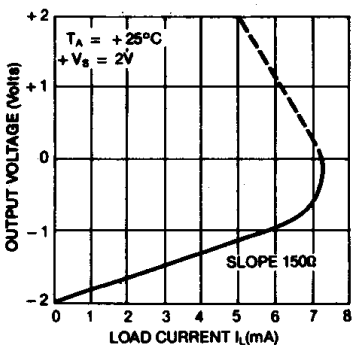
   D_x must be used in high-voltage elevated temperature applications. The device will function properly in the specified temperature range with only the 2 external capacitors, provided the supply voltage does not exceed 6.5V at 70°C. Exceeding this maximum could result in destructive latch-up of the device. (Refer to the OPERATING VOLTAGE VS TEMPERATURE graph and the typical connection diagrams.)
5. The oscillator operates (unloaded) at a nominal frequency of 10 kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the OSCILLATOR terminal (Pin 7) or the oscillator may be overdriven by an external clock. For large values of the OSCILLATOR CAPACITOR, (>1000 pF), C_1 and C_2 should be increased to 100 µF.

PERFORMANCE

OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



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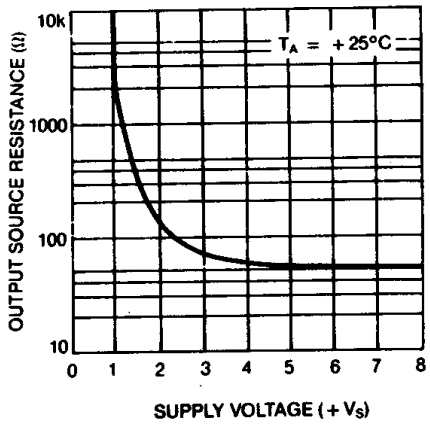
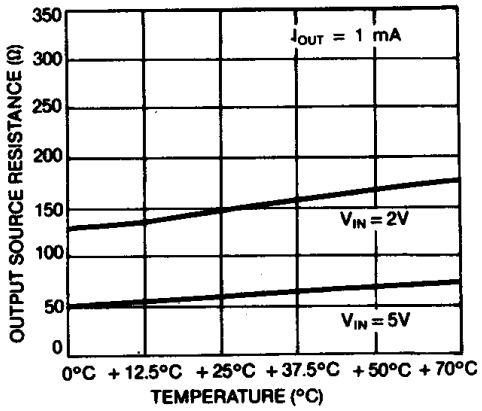
PERFORMANCE

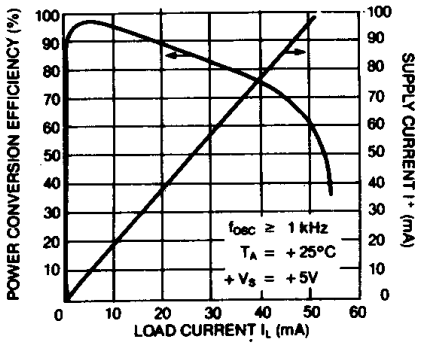
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE



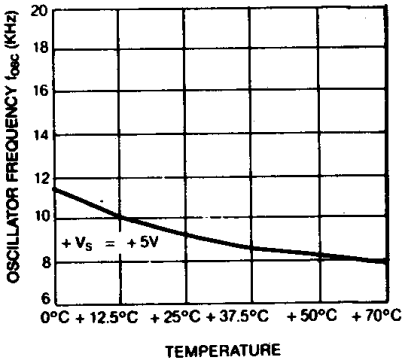
OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE



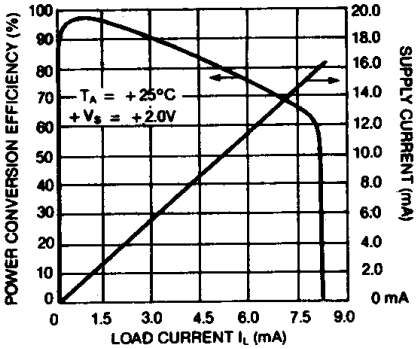
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



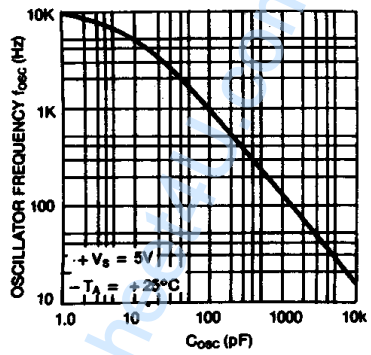
UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE



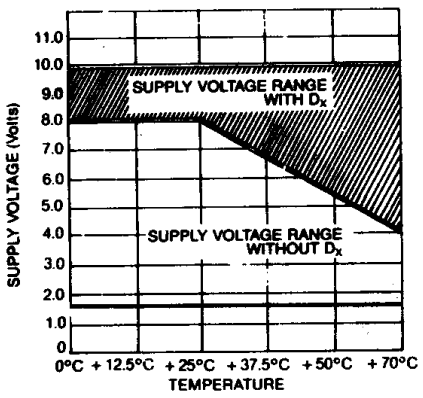
SUPPLY CURRENT & POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT



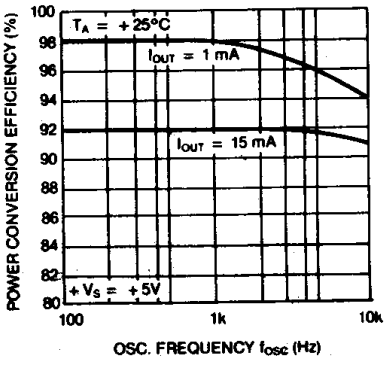
FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSC. CAPACITANCE



OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE



POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSC. FREQUENCY



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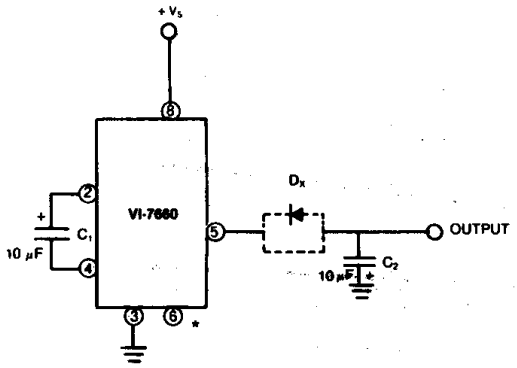
TYPICAL CONNECTION AND APPLICATION

NEGATIVE VOLTAGE CONVERTER



D_X must be included for proper operation at high voltages (>6.5V) and/or elevated temperatures.
*Ground if $+V_S < 3.5V$

This application shows the typical connections to provide a negative supply where a positive supply is available. The output characteristics of this circuit are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of −10 mA and a supply voltage of +5V, the output voltage will be −4.3V. The output equations are as follows:

V_{OUT} without D_X

$$V_{OUT} = -V_S \text{ for } +V_S = 1.5V \text{ to } 6.5V$$

V_{OUT} with D_X

$$V_{OUT} = -V_S + V_{FDX} \text{ for } +V_S = 6.5V \text{ to } 10.0V$$

Where: V_{FDX} = Forward Voltage across D_X

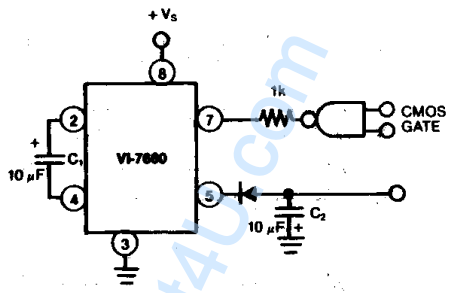
The dynamic output impedance due to the capacitor impedance is approximately $1/\omega C$ where:

$$C = C_1 = C_2$$

Giving $\frac{1}{\omega C} = \frac{1}{2\Pi f_{osc} \times 10^{-5}} = 3\Omega$

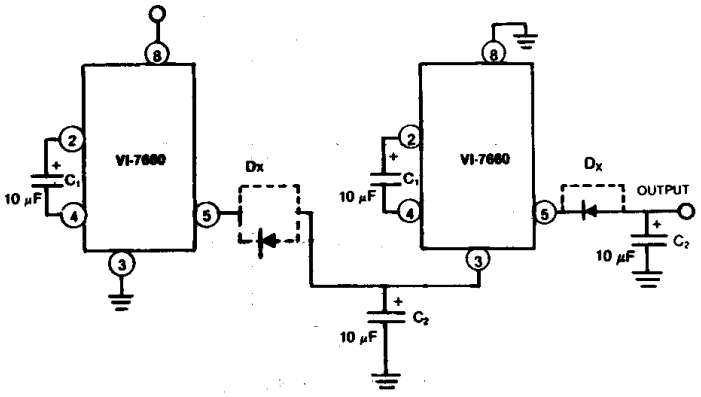
For C = 10 µF and f_{osc} = 5 kHz (½ of oscillator frequency)

EXTERNAL CLOCKING



The oscillator frequency may be increased by overdriving the oscillator from an external clock. The 1 kΩ resistor is used to prevent latch-up when using CMOS logic. If TTL is used to over drive the oscillator, a 10 kΩ pullup resistor to $+V_S$ is required.

CASCADING VI-7660's (ARITHMETIC CASCADING)

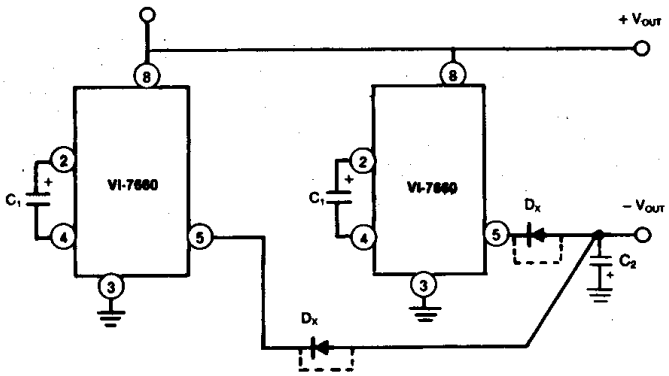


VI-7660's may be cascaded for increased output voltage. The practical limit is 10 devices for light loads due to the finite efficiency of each device. The output equation is as follows:

$$V_{OUT} = -n\,(V_S)$$

where "n" is the number of devices cascaded. The output resistance is the sum of each VI-7660's R_{OUT}.

PARALLELING VI-7660's

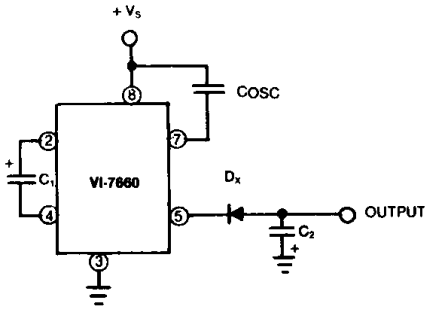


VI-7660's may be paralleled to reduce output resistance. The reservoir capacitor, C_2, serves all devices; however, each device requires its own pump capacitor (C_1).

$$\text{Output Resistance} = \frac{R_{OUT} \text{ (of VI-7660)}}{\text{n (number of devices)}}$$

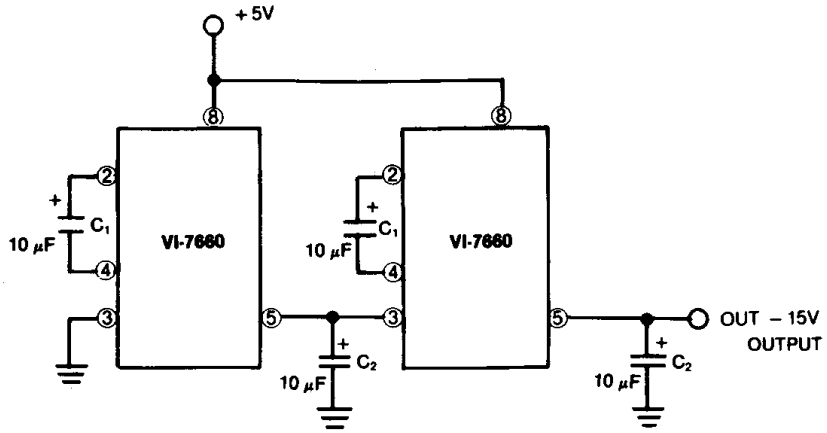
APPLICATIONS

DECREASING OSCILLATOR FREQUENCY



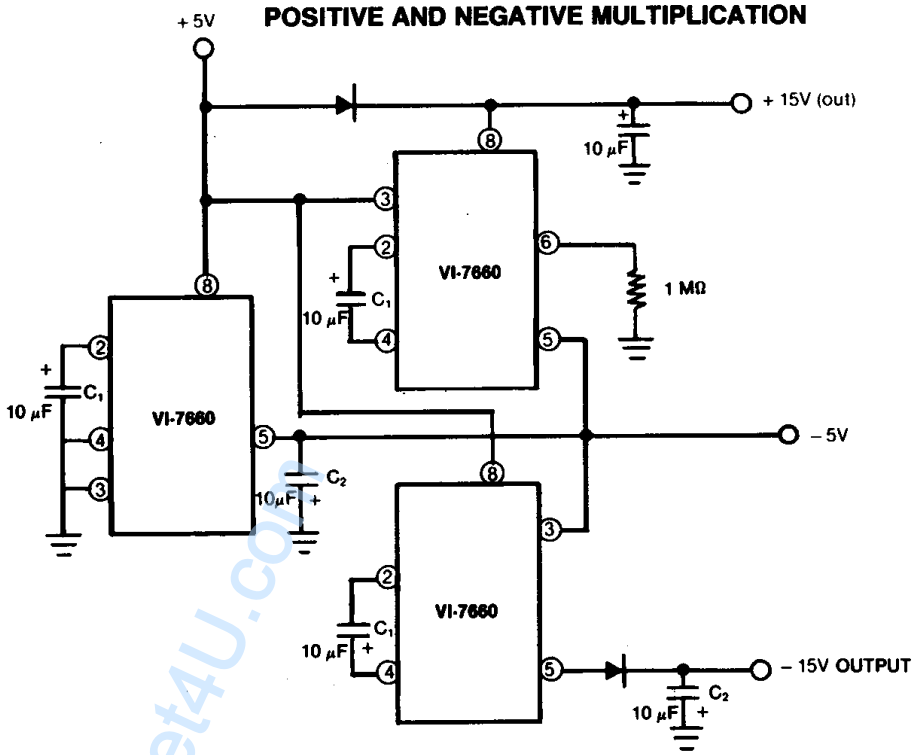
Conversion efficiency can be maximized by lowering the oscillator frequency. This is achieved by connecting an additional capacitor C_{OSC} as shown. Lowering the frequency will cause an increase in the impedance of C_1 and C_2. This can be overcome by increasing the values of C_1 and C_2 by the same factor that the frequency has been decreased.

POSITIVE MULTIPLICATION



This circuit will generate –15V dc from +5V dc using two VI-7660's. The two devices are connected in cascade fashion with Pin 3 of device #2 connected to V_{IN} rather than ground. The geometric increase performed by this circuit is good until the input voltage limit is reached, at which point, arithmetic cascading should be utilized. Cascading is recommended for use in light load applications.

POSITIVE AND NEGATIVE MULTIPLICATION



This application shows a combination of positive and negative multipliers. This circuit is an extension of the above application providing ±15V dc supplies from a +5V dc input. The 1 MΩ resistor on Pin 6 of device number 1 is used to avoid startup problems by forcing the internal regulator on.