VIB0101THJ

BCM™ Bus Converter

FEATURES

- 48 Vdc – 12 Vdc 120 W Bus Converter
- High efficiency (>95%) reduces system power consumption
- High power density (801 W/in^3) reduces power system footprint by >50%
- "Half Chip" V•I Chip package enables surface mount, low impedance interconnect to system board
- Contains built-in protection features: undervoltage, overvoltage lockout, over current protection, short circuit protection, overtemperature protection.
- Provides enable/disable control, internal temperature monitoring
- ZVS/ZCS Resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

TYPICAL APPLICATION

- High End Computing Systems
- Automated Test Equipment
- Telecom Base Stations
- High Density Power Supplies
- Communication Systems

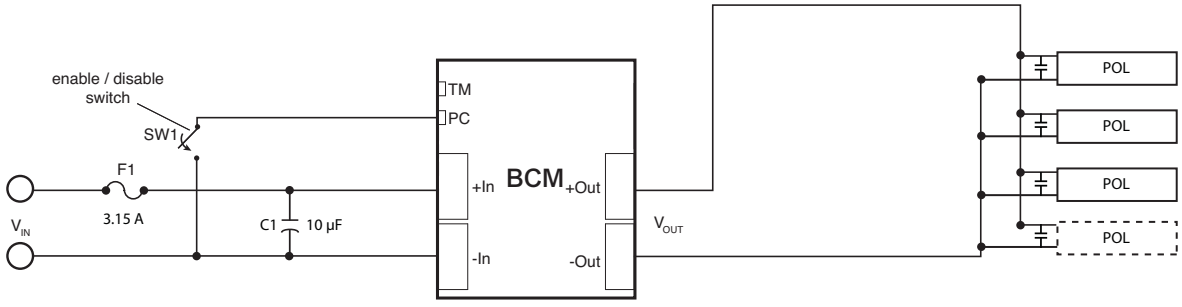
DESCRIPTION

The V•I Chip™ Bus Converter is a high efficiency (>95%) Sine Amplitude Converter™ (SAC™) operating from a 38 to 55 Vdc primary bus to deliver an isolated 12 V nominal, unregulated secondary. The SAC offers a low AC impedance beyond the bandwidth of most downstream regulators, meaning that input capacitance normally located at the input of a 12 V regulator can be located at the input to the SAC. Since the K factor of the VIB0101THJ is 1/4, that capacitance value can be reduced by a factor of 16x, resulting in savings of board area, materials and total system cost.

The VIB0101THJ is provided in a V•I Chip package compatible with standard pick-and-place and surface mount assembly processes. The V•I Chip package provides flexible thermal management through its low junction-to-case and junction-to-board thermal resistance. With high conversion efficiency the VIB0101THJ increases overall system efficiency and lowers operating costs compared to conventional approaches.

V_{IN} = 38 – 55 V	P_{OUT} = 120 $W_{(NOM)}$
V_{OUT} = 9.5 – 13.75 V (NO LOAD)	K = 1/4

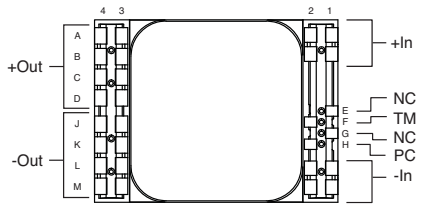
TYPICAL APPLICATION



ABSOLUTE MAXIMUM RATINGS

+IN to –IN . . . . . -1.0 Vdc – +60 Vdc
PC to –IN . . . . . -0.3 Vdc – +20 Vdc
TM to –IN . . . . . -0.3 Vdc – +7.0 Vdc
+IN/-IN to +OUT/-OUT . . . . . 2250 V (Hi Pot)
+IN/-IN to +OUT/-OUT . . . . . 60 V (working)
+OUT to –OUT . . . . . -1.0 Vdc - +16 Vdc
Temperature during reflow . . . . . 245°C (MSL 6)

PACKAGE ORDERING INFORMATION



Bottom View

Signal Name	Designation
+In	A1-B1, A2-B2
–In	L1-M1, L2-M2
NC	E1
TM	F2
NC	G1
PC	H2
+Out	A3-D3, A4-D4
–Out	J3-M3, J4-M4

PART NUMBER	DESCRIPTION
VIB0101THJ	-40°C – 125°C T_J, J lead

CONTROL PIN SPECIFICATIONS

See section 5.0 for further application details and guidelines.

PC (V•I Chip BCM Primary Control)

The PC pin can enable and disable the BCM. When held below V_{PC-DIS} the BCM shall be disabled. When allowed to float with an impedance to –IN of greater than 60 kΩ the module will start. When connected to another BCM PC pin (either directly, or isolated through a diode), the BCMs will start simultaneously when enabled. The PC pin is capable of being either driven high by an external logic signal or internal pull up to 5 V (operating).

TM (V•I Chip BCM Temperature Monitor)

The TM pin monitors the internal temperature of the BCM within an accuracy of +5/-5 °C. It has a room temperature setpoint of ~3.0 V and an approximate gain of 10 mV/°C. It can source up to 100 uA and may also be used as a "Power Good" flag to verify that the BCM is operating.

1.0 ELECTRICAL CHARACTERISTICS

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°** unless otherwise noted

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Voltage range	V_{IN}		**38**	**48**	**55**	Vdc
dV/dt	dV_{IN}/dt				**1**	V/µs
Quiescent power	P_Q	PC connected to -IN		68	**150**	mW
No load power dissipation	P_{NL}	V_{IN} = 48 V		1.7	**3.0**	W
		V_{IN} = 38 to 55 V			**3.5**	
Inrush Current Peak	I_{INR-P}	V_{IN} = 48 V C_{OUT} = 500 µF, I_{OUT} = 10.55 A		5.5	**12**	A
DC Input Current	I_{IN-DC}				**3.5**	A
K Factor $\left(\frac{V_{OUT}}{V_{IN}}\right)$	K			1/4		
Output Power (Average)	P_{OUT}	V_{IN} = 38 – 55 Vdc; See Figure 14			**97**	W
		V_{IN} = 46 – 55 Vdc; See Figure 14			**120**	
Output Power (Peak)	P_{OUT-P}	V_{IN} = 46 – 55 Vdc Average P_{OUT} < = 120 W, Tpeak < 10 ms			**150**	W
Output Voltage	V_{OUT}	Section 3.0	**8.5**		**14**	V
Output Current (Average)	I_{OUT}	Pout < =120 W			11.3	A
Efficiency (Ambient)	η	V_{IN} = 48 V, P_{OUT} = 120 W	93	94.6		%
		V_{IN} = 38 V to 55 V, P_{OUT} = 100 W	90.5			
Efficiency (Hot)	η	VIN = 48 V, T_J = 100° C,P_{OUT} = 120 W	92.6	93.7		%
Minimum Efficiency (Over Load Range)	η	24 W < P_{OUT} < P_{OUT} Max	**89**			%
Output Resistance (Ambient)	R_{OUT}	T_J = 25° C	35.4	44.1	55.8	mΩ
Output Resistance (Hot)	R_{OUT}	T_J = 125° C	46.1	56.1	69.1	mΩ
Output Resistance (Cold)	R_{OUT}	T_J = -40° C	27.2	35.0	45.7	mΩ
Load Capacitance	C_{OUT}				**500**	uF
Switching Frequency	F_{SW}		**1.60**	1.75	**1.90**	MHz
Ripple Frequency	F_{SW-RP}		**3.20**	3.50	**3.80**	MHz
Output Voltage Ripple	V_{OUT-PP}	C_{OUT} = 0µF, I_{OUT} = 10.55 A, V_{IN} = 48 V, Section 8.0		140	**355**	mV
V_{IN} to V_{OUT} (Application of V_{IN})	$T_{ON}1$	V_{IN} = 48 V, C_{PC} = 0; See Figure 16		570	800	ms
PC						
PC Voltage (Operating)	V_{PC}		**4.7**	5.0	**5.3**	V
PC Voltage (Enable)	V_{PC-EN}		**2.0**	2.5	**3.0**	V
PC Voltage (Disable)	V_{PC-DIS}				**1.95**	V
PC Source Current (Startup)	I_{PC-EN}		**50**	100	**300**	uA
PC Source Current (Operating)	I_{PC-OP}				**2**	mA
PC Internal Resistance	R_{PC-SNK}	Internal pull down resistor	**50**	150	**400**	kΩ
PC Capacitance (Internal)	C_{PC_INT}	Section 5.0			588	pF
PC Capacitance (External)	C_{PC_EXT}	External capacitance delays PC enable time			1000	pF
External PC Resistance	R_{PC}	Connected to –V_{IN}	**60**			kΩ
PC External Toggle Rate	F_{PC-TOG}				**1**	Hz
PC to V_{OUT} with PC Released	Ton2	V_{IN} = 48 V, Pre-applied; See Figure 16		60	100	µs
PC to V_{OUT}, Disable PC	T_{PC-DIS}	V_{IN} = 48 V, Pre-applied; See Figure 16		4	10	µs

1.0 ELECTRICAL CHARACTERISTICS (CONT.)

Specifications apply over all line and load conditions unless otherwise noted; **Boldface** specifications apply over the temperature range of **-40°C < T_J < 125°C (T-Grade)**; All other specifications are at **T_J = 25°** unless otherwise noted

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
TM						
TM accuracy	Actm		**-5**		**+5**	°C
TM Gain	A_{TM}			10		mV/°C
TM Source Current	I_{TM}				**100**	uA
TM Internal Resistance	R_{TM-SNK}		**25**	40	**50**	kΩ
External TM Capacitance	C_{TM}				**50**	pF
TM Voltage Ripple	V_{TM-PP}	C_{TM} = 0uF, V_{IN} = 55 V, P_{OUT} = 120 W	**75**	180	**250**	mV
PROTECTION						
Negative going OVLO	$V_{IN\ OVLO-}$		**55.1**	57.8	**59.4**	V
Positive going OVLO	$V_{IN\ OVLO+}$		**55.5**	58.1	**59.4**	V
Negative going UVLO	$V_{IN\ UVLO-}$		**29.1**	30.8	**35.4**	V
Positive going UVLO	$V_{IN\ UVLO+}$		**30.7**	32.6	**37.3**	V
Output Overcurrent Trip	I_{OCP}	V_{IN} = 48 V, 25°C	**12**	20	**25**	A
Short Circuit Protection Trip Current	I_{SSP}		**15**		40	A
Short Circuit Protection Response Time	T_{SSP}		**0.8**	1.0	**1.2**	us
Thermal Shutdown Junction setpoint	T_{J-OTP}		**125**	130	**135**	°C
GENERAL SPECIFICATION						
Isolation Voltage (Hi-Pot)	V_{HIPOT}		**2250**			V
Working Voltage (IN – OUT)	Vworking				**60**	V
Isolation Capacitance	C_{IN-OUT}	Unpowered unit	**1350**	1750	**2150**	pF
Isolation Resistance	R_{IN-OUT}		**10**			MΩ
MTBF		MIL HDBK 217F, 25° C, GB		7.1		Mhrs
Agency Approvals/Standards		cTUVus				
		CE Mark				
		ROHS 6 of 6				

1.1 APPLICATION CHARACTERISTICS

All specifications are at **T_J = 25°C** unless otherwise noted. See associated figures for general trend data.

ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	TYP	UNIT
No Load Power	P_{NL}	V_{IN} = 48 V, PC enabled; See Figure 1	1.75	W
Inrush Current Peak	I_{INR-P}	C_{OUT} = 500 µF, P_{OUT} = 120 W	6	A
Efficiency (Ambient)	η	V_{IN} = 48 V, P_{OUT} = 120 W C_{OUT} = 500 µF	95	%
Efficiency (Hot – 100°C)	η	V_{IN} = 48 V, P_{OUT} = 120 W C_{OUT} = 500 µF	94	%
Output Resistance (-40°C)	R_{OUT_C}	V_{IN} = 48 V	35	mΩ
Output Resistance (25°C)	R_{OUT_R}	V_{IN} = 48 V	44	mΩ
Output Resistance (100°C)	R_{OUT_H}	V_{IN}= 48 V	56	mΩ
Output Voltage Ripple	V_{OUT-PP}	C_{OUT} = 0uF, P_{OUT} = 120 W @ V_{IN} = 48, V_{IN} = 48 V	160	mV
V_{OUT} Transient (Positive)	$V_{OUT-TRAN+}$	I_{OUT_STEP} = 0 TO 10.55 A, I_{SLEW} >10 A/us; See Figure 12	1.4	V
V_{OUT} Transient (Negative)	$V_{OUT-TRAN-}$	I_{OUT_STEP} = 10.55 A to 0 A, I_{SLEW} > 10 A/us; See Figure 11	1.3	V
Undervoltage Lockout Response Time	T_{UVLO}		2.4	us
Output Overcurrent Response Time	T_{OCP}	12 < I_{OCP} < 25 A	4.4	ms
Overvoltage Lockout Response Time	T_{OVLO}		2.4	µs

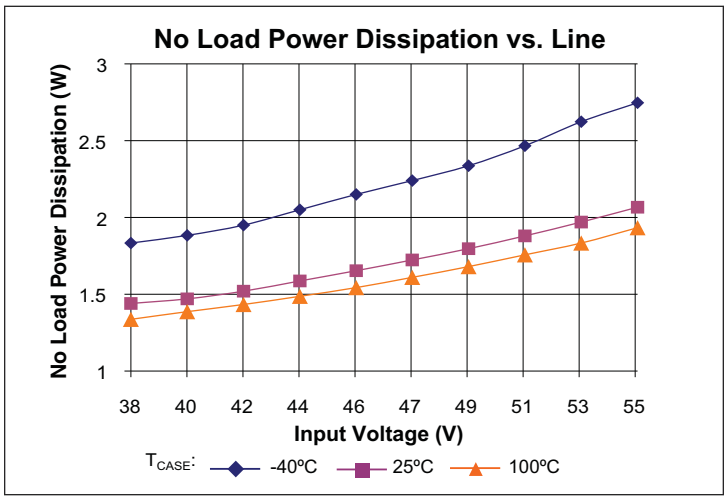


Figure 1 – *No load power dissipation vs. V_{IN}; T_{CASE}*

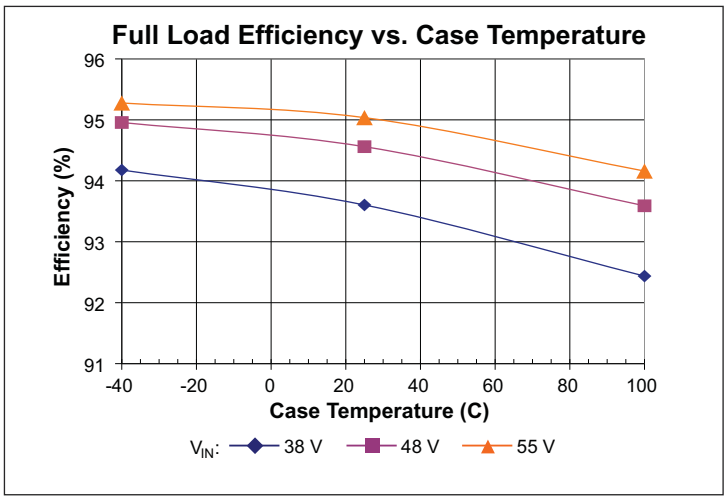


Figure 2 – *Full load efficiency vs. temperature; V_{IN}*

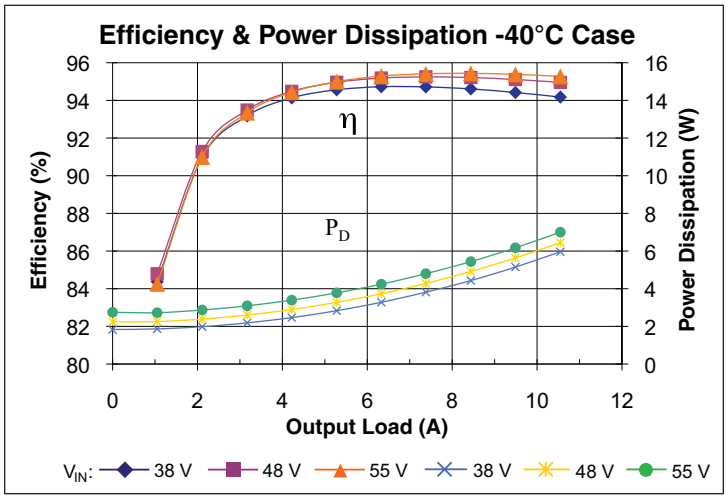


Figure 3 – *Efficiency and power dissipation at -40°C (case); V_{IN}*

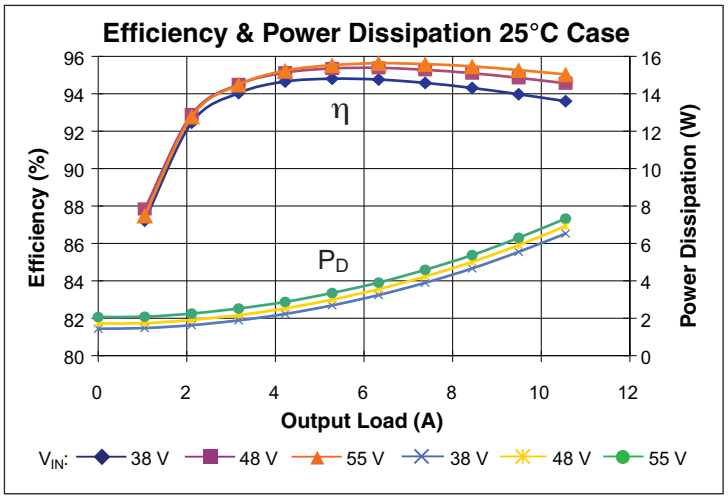


Figure 4 – *Efficiency and power dissipation at 25°C (case); V_{IN}*

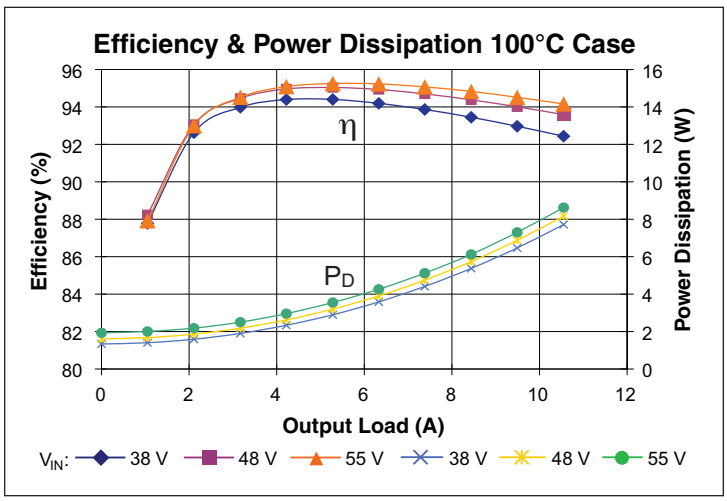


Figure 5 – *Efficiency and power dissipation at 100°C (case); V_{IN}*

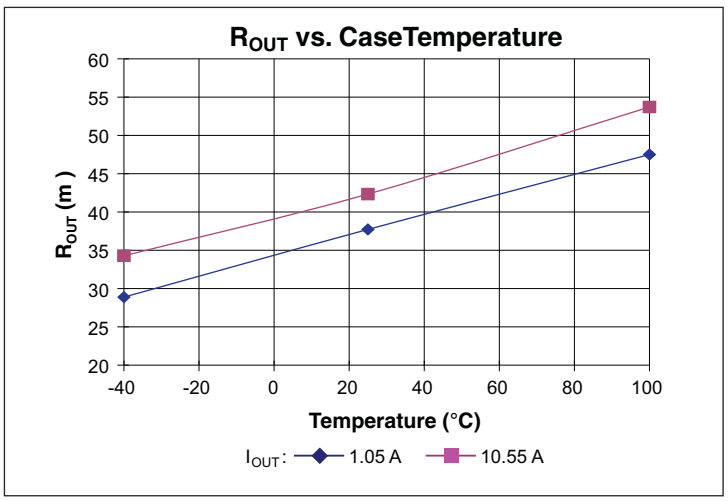


Figure 6 – *R_{OUT} vs. temperature vs. I_{OUT}*

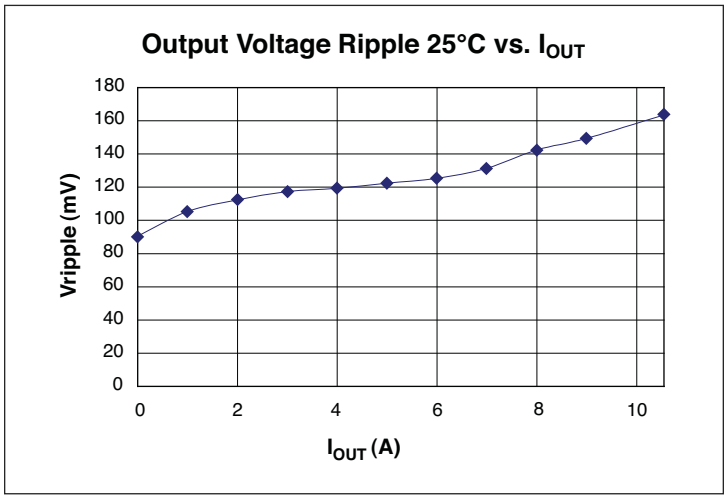


Figure 7 – *Vripple vs. I_{OUT} ; 48 Vin, no external capacitance*

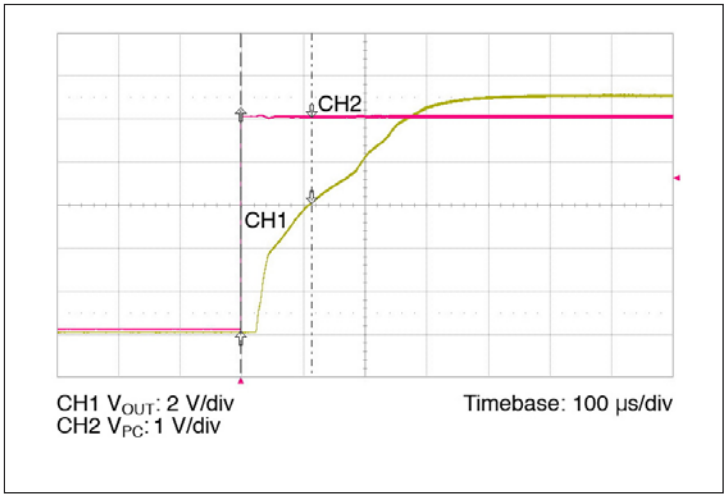


Figure 8 – *PC to V_{OUT} startup waveform*

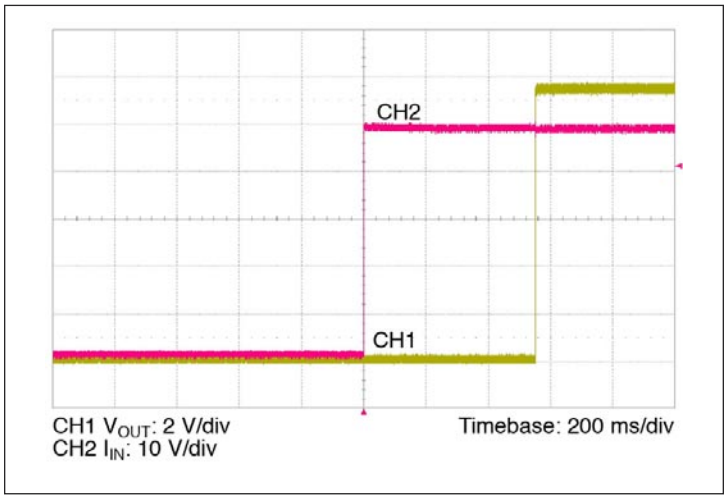


Figure 9 – *V_{IN} to V_{OUT} startup waveform*

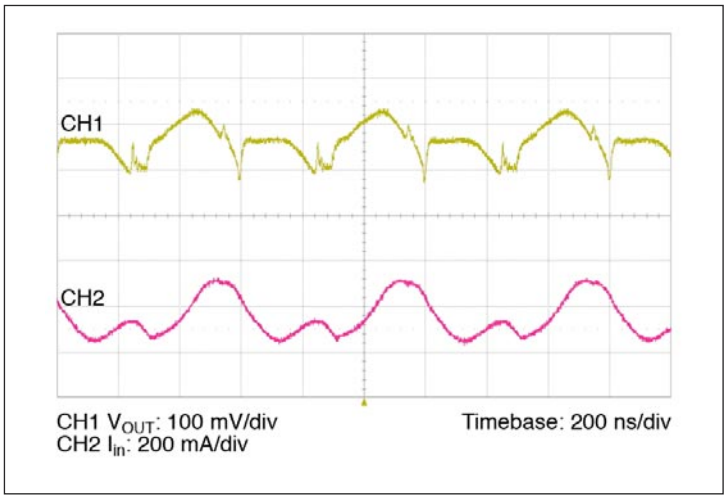


Figure 10 – *Output voltage and input current ripple, 48 Vin, 120 W no c_{OUT}*

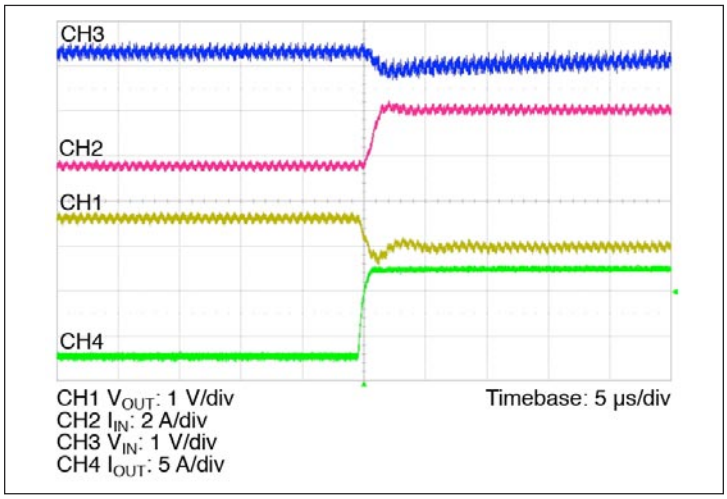


Figure 11 – *Positive load transient (0 – 11.3 A)*

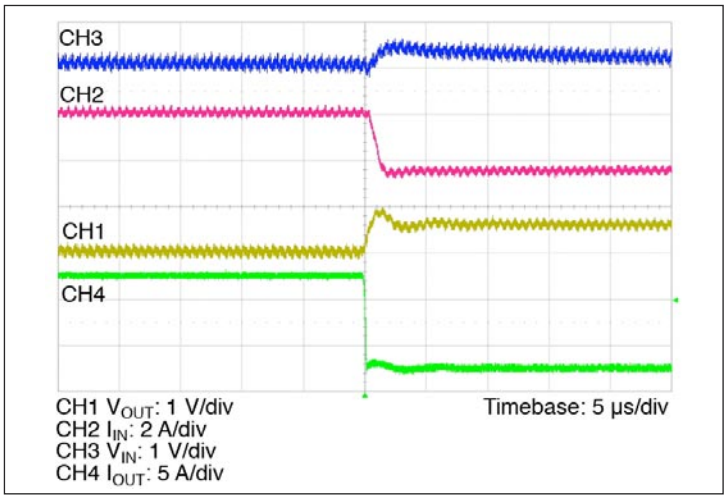


Figure 12 – *Negative load transient (11.3 A – 0 A)*

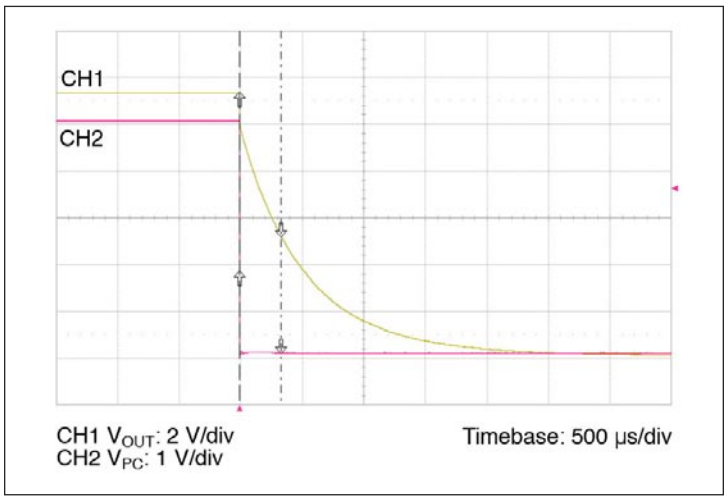


Figure 13 – *PC disable waveform, 48 V_{IN}, 500 µF C_{OUT} full load*

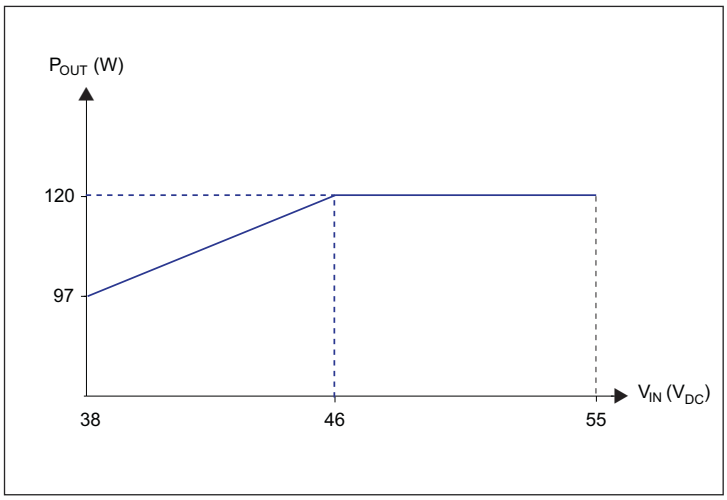


Figure 14 – *P_{OUT} derating vs. V_{IN}*

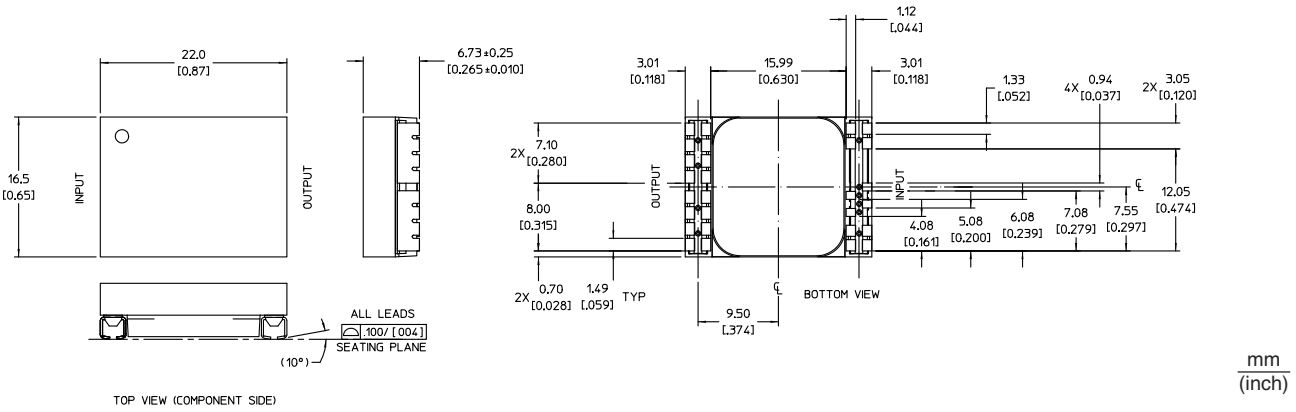
2.0 PACKAGE/MECHANICAL SPECIFICATIONS

All specifications are at **T_J=25°C** unless otherwise noted. See associated figures for general trend data.

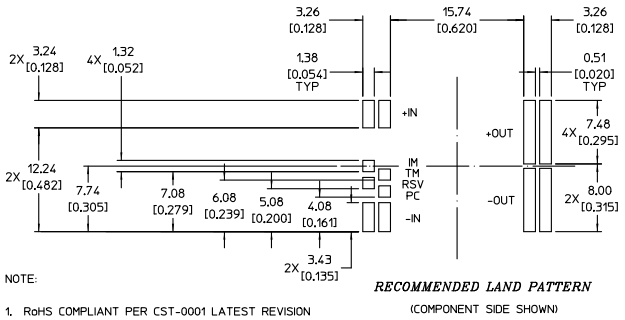
ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
Length	L		21.7 / 0.854	22.0 / 0.866	22.3 / 0.878	mm/in
Width	W		16.37 / 0.644	16.50 / 0.650	16.63 / 0.655	mm/in
Height	H		6.48 / 0.255	6.73 / 0.265	6.98 / 0.275	mm/in
Volume	Vol	No Heatsink		2.44 / 0.150		cm^3/in^3
Footprint	F	No Heatsink		3.6 / 0.56		cm^2/in^2
Power Density	PD	No Heatsink		801		W/in^3
				49		W/cm^3
Weight	W			0.28/8		oz/g
Lead Finish		Nickel (0.51-2.03 µm) Palladium (0.02-0.15 µm) Gold (0.003-0.05 µm)				
Operating Temperature	T_J		-40		125	°C
Storage Temperature	T_{ST}		-40		125	°C
Thermal Impedance	$Ø_{JC}$	Junction to Case			2.7	°C/W
Thermal Capacity				5		Ws/°C
Peak Compressive Force Applied to Case (Z-axis)		Supported by J-leads only		2.5	3.0	lbs
ESD Rating	ESD_{HBM}	Human Body Model[a]	1500			V_{DC}
	ESD_{MM}	Machine Model[b]	400			V_{DC}
Peak Temperature During Reflow		MSL 5			225	°C
		MSL 6			245	°C
Peak Time Above 183°C					150	s
Peak Heating Rate During Reflow				1.5	3	°C/s
Peak Cooling Rate Post Reflow				1.5	6	°C/s

[a] JEDEC JESD 22-A114C.01
[b] JEDED JESD 22-A115-A

2.1 MECHANICAL DRAWING



2.2 RECOMMENDED LAND PATTERN



2.3 RECOMMENDED LAND PATTERN FOR PUSH PIN HEATSINK

Notes:
1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.

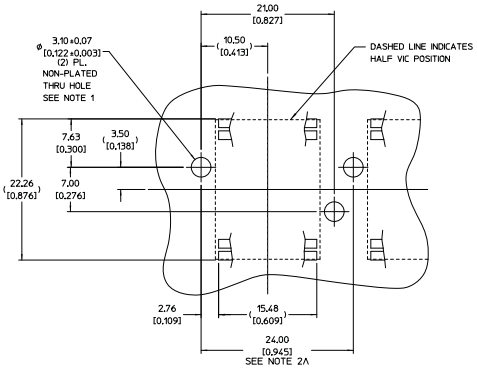
2. (A) minimum recommended pitch is 24.00 (0.945) this provides 7.50 (0.295) component edge–to–edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
(B) Minimum recommended pith is 25.50 (1.004). This provides 9.00 (0.354) component edge–to–edge spacing, and 2.00 (0.079) clearance between Vicor heat sinks.

3. V•I Chip land pattern shown for reference only, actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all half size V•I Chip Products.

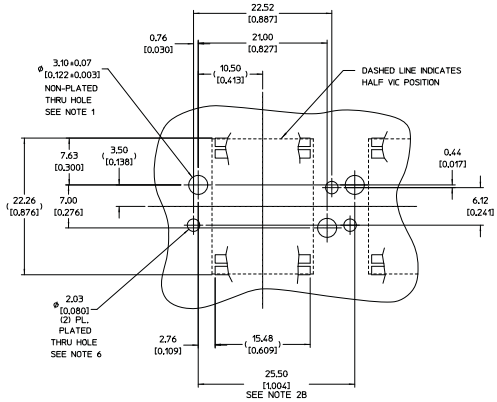
4. RoHS complient per CST–0001 latest revision.

5. Unless otherwise specified:
Dimensions are mm (inches)
tolerances are:
x.x (x.xx) = ±0.3 (0.01)
x.xx (x.xxx) = ±0.13 (0.005)

6. Plated through holes for grounding clips (33855) shown for reference, Heatsink orientation and device pitch will dictate final grounding solution.



(NO GROUNDING CLIPS)



(WITH GROUNDING CLIPS)

3.0 POWER, VOLTAGE, EFFICIENCY RELATIONSHIPS

Because of the high frequency, fully resonant SAC topology, power dissipation and overall conversion efficiency of BCM converters can be estimated as shown below.

Key relationships to be considered are the following:

1. Transfer Function

   a. No load condition

   $V_{OUT} = V_{IN} \bullet K$ Eq. 1

   Where K (transformer turns ratio) is constant for each part number

   b. Loaded condition

   $V_{OUT} = Vin \bullet K - I_{OUT} \bullet R_{OUT}$ Eq. 2

2. Dissipated Power
   The two main terms of power losses in the BCM module are:

   - No load power dissipation (P_{NL}) defined as the power used to power up the module with an enabled power train at no load.
   - Resistive loss (R_{OUT}) refers to the power loss across the BCM modeled as pure resistive impedance.

   $P_{DISSIPATED} \approx P_{NL} + P_{R_{OUT}}$ Eq. 3

Therefore, with reference to the diagram shown in Figure 15

$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{R_{OUT}}$ Eq. 4

Notice that R_{OUT} is temperature and input voltage dependent and P_{NL} is temperature dependent (See Figure 15).

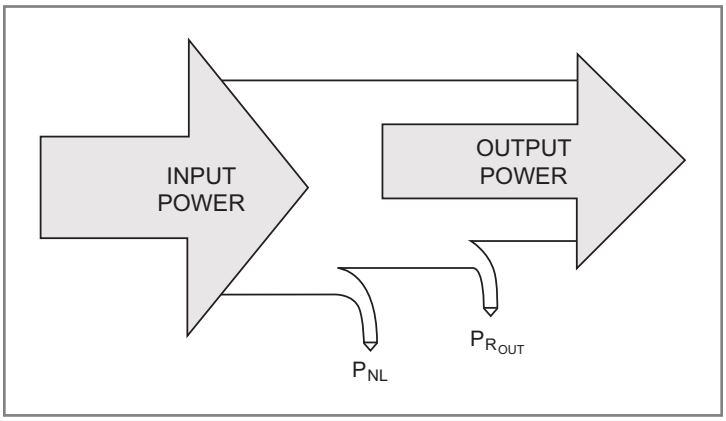


Figure 15 – *Power transfer diagram*

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{R_{OUT}}}{P_{IN}} = \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}} = 1 - \left(\frac{P_{NL} + (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}} \right) \quad \text{Eq. 5}$$

4.0 OPERATING

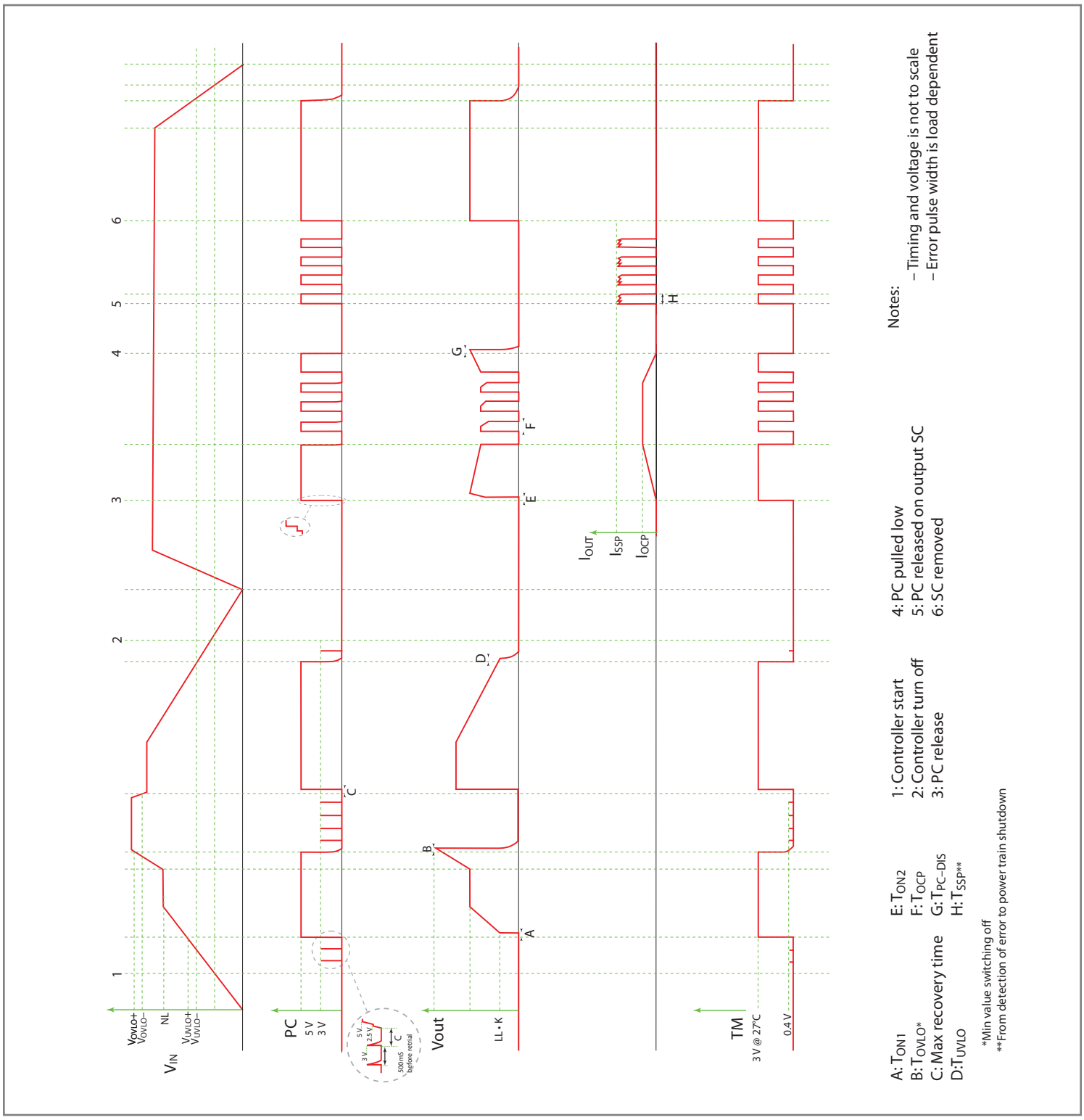


Figure 16 – *Timing diagram*

5.0 USING THE CONTROL SIGNALS TM AND PC

The PC control pin can be used to accomplish the following functions:

- **Delayed start:** At start-up, PC pin will source a constant 100 uA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start.
- **Synchronized start up:** In a parallel module array, PC pins shall be connected in order to ensure synchronous start of all the units. While every controller has a calibrated 2.5 V reference on PC comparator, many factors might cause different timing in turning on the 100 uA current source on each module, i.e.:
  - Different V_{IN} slew rate
  - Statistical component value distribution

  By connecting all PC pins, the charging transient will be shared and all the modules will be enabled synchronously.
- **Auxiliary voltage source:** Once enabled in regular operational conditions (no fault), each BCM PC provides a regulated 5 V, 2 mA voltage source.
- **Output disable:** PC pin can be actively pulled down in order to disable module operations. Pull down impedance shall be lower than 1 kΩ and toggle rate lower than 1 Hz.
- **Fault detection flag:** The PC 5 V voltage source is internally turned off as soon as a fault is detected. After a minimum disable time, the module tries to re-start, and PC voltage is re-enabled. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of PC signal.

  It is important to notice that PC doesn't have current sink capability (only 150 kΩ typical pull down is present), therefore, in an array, PC line will not be capable of disabling all the modules if a fault occurs on one of them.

The temperature monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- **Monitor the control IC temperature:** The temperature in Kelvin is equal to the voltage on the TM pin scaled by x100. (i.e. 3.0 V = 300 K = 27°C). It is important to remember that V•I chips are multi-chip modules, whose temperature distribution greatly vary for each part number as well with input/output conditions, thermal management and environmental conditions. Therefore, TM cannot be used to thermally protect the system.
- **Fault detection flag:** The TM voltage source is internally turned off as soon as a fault is detected. After a minimum disable time, the module tries to re-start, and TM voltage is re-enabled.

6.0 FUSE SELECTION

V•I Chips are not internally fused in order to provide flexibility in configuring power systems. Input line fusing of V•I Chips is recommended at system level, in order to provide thermal protection in case of catastrophic failure.

The fuse shall be selected by closely matching system requirements with the following characteristics:

- Current rating (usually greater than maximum BCM current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t
- Recommended fuse: 3.15 A Little Fuse Nano^2 Fuse

7.0 CURRENT SHARING

The SAC topology bases its performance on efficient transfer of energy through a transformer, without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array (with same K factor), the BCM module will inherently share the load current with parallel units, according to the equivalent impedance divider that the system implements from the power source to the point of load.

It is important to notice that, when successfully started, BCMs are capable of bidirectional operations (reverse power transfer is enabled if the BCM input falls within its operating range and the BCM is otherwise enabled). In parallel arrays, because of the resistive behavior, circulating currents are never experienced, because of energy conservation law.

General recommendations to achieve matched array impedances are (see also AN016 for further details):

- to dedicate common copper planes within the PCB to deliver and return the current to the modules
- to make the PCB layout as symmetric as possible
- to apply same input/output filters (if present) to each unit

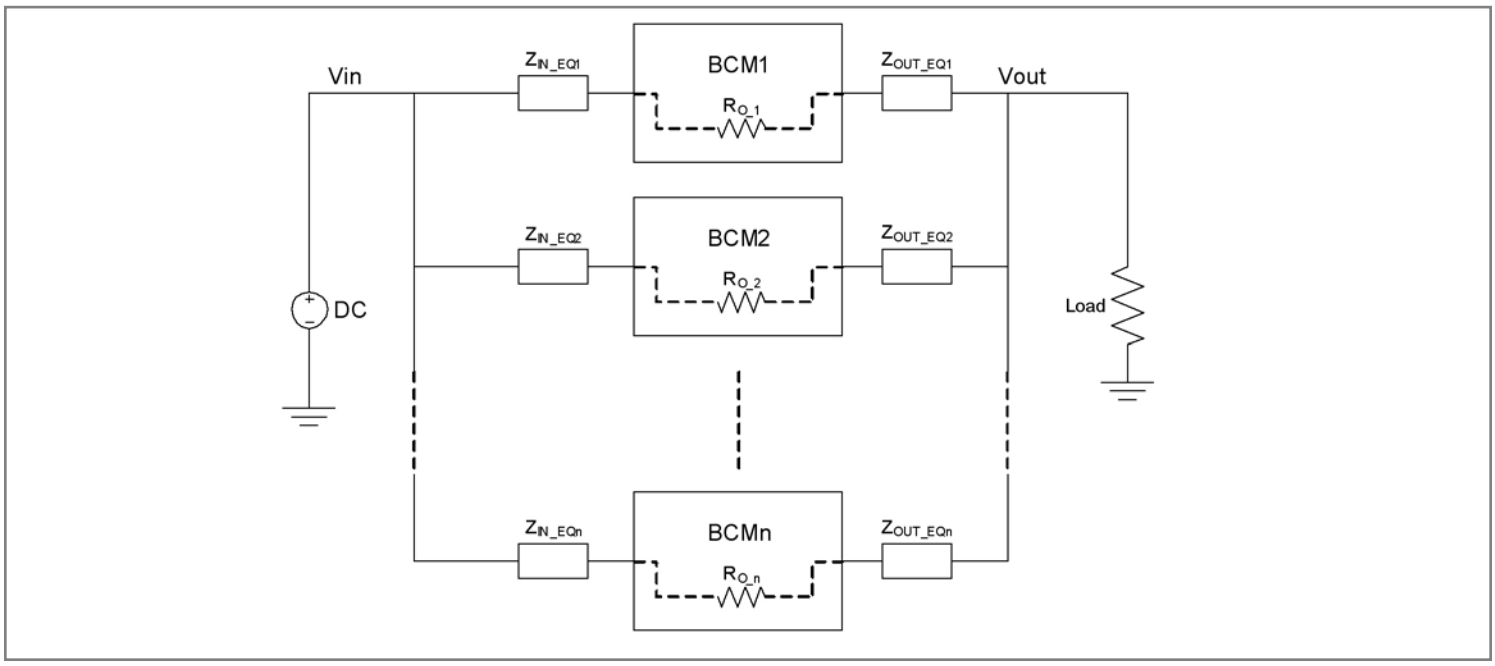


Figure 17 – *BCM Array*

8.0 INPUT AND OUTPUT FILTER DESIGN

A major advantage of SAC systems versus conventional PWM converters is that the transformers do not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current, and efficiently transfers charge through the isolation transformer. A small amount of capacitance, embedded in the input and output stages of the module, is sufficient for full functionality and is key to achieve power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance:

   To take full advantage of the BCM dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. The connection of the V•I Chip to its power source should be implemented with minimal distribution inductance. If the interconnect inductance exceeds 100 nH, the input should be bypassed with a RC damper to retain low source impedance and stable operation. With an interconnect inductance of 200 nH, the RC damper may be as high as 47 µF in series with 0.3 Ω. A single electrolytic or equivalent low-Q capacitor may be used in place of the series RC bypass.

2. Further reduce input and/or output voltage ripple without sacrificing dynamic response:

   Given the wide bandwidth of the BCM, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the BCM multiplied by its K factor. This is illustrated in Figures 11 and 12.

3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures:

   The V•I Chip input/output voltage ranges shall not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it. A criterion for protection is the maximum amount of energy that the input or output switches can tolerate if avalanched.

Total load capacitance at the output of the BCM shall not exceed the specified maximum. Owing to the wide bandwidth and low output impedance of the BCM, low frequency bypass capacitance and significant energy storage may be more densely and efficiently provided by adding capacitance at the input of the BCM. At frequencies <500 kHz the BCM appears as an impedance of R_{OUT} between the source and load. Within this frequency range capacitance at the input appears as effective capacitance on the output per the relationship defined in Eq. 6.

$$C_{OUT} = \frac{C_{IN}}{K^2} \qquad \text{Eq. 6}$$

This enables a reduction in the size and number of capacitors used in a typical system.

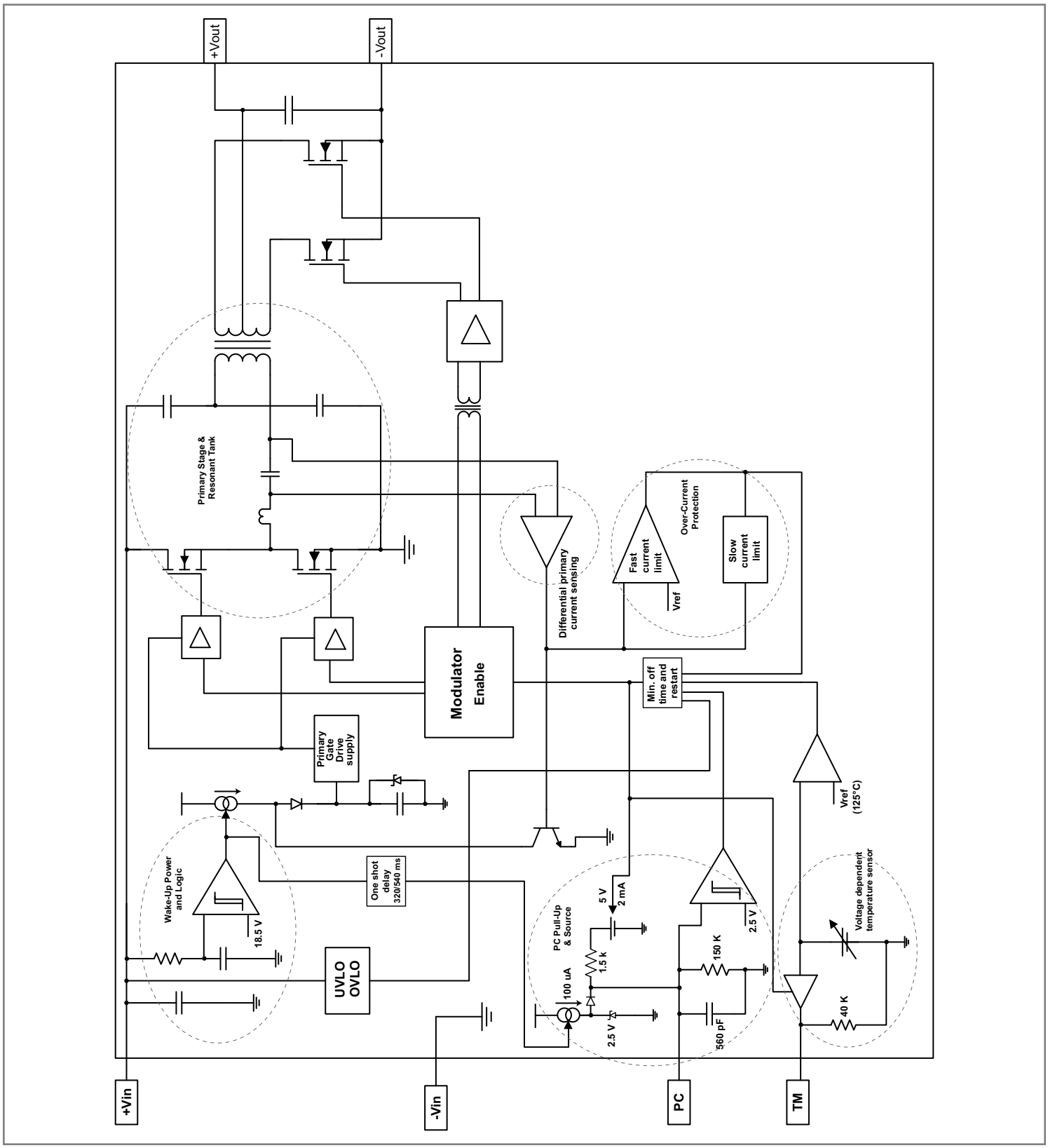


Figure 1 – *BCM behavioral block diagram*

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