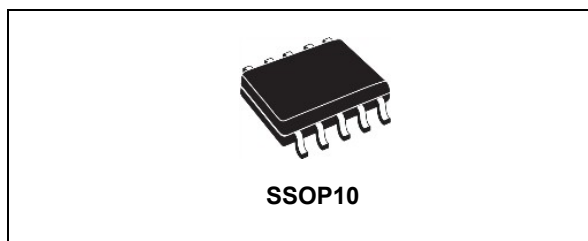


Energy saving off-line high voltage converter

Datasheet - production data



Features

- 800 V avalanche-rugged power MOSFET allowing ultra wide V_{AC} input range to be covered
- Embedded HV startup and sense-FET
- Current mode PWM controller
- Drain current limit protection
 - 480 mA (VIPER114)
 - 590 mA (VIPER115)
- Wide supply voltage range: 4.5 V to 30 V
- Minimized system input power consumption:
 - Less than 10 mW at 230 V_{AC} in no-load condition
 - Less than 400 mW at 230 V_{AC} with 250 mW load
- Jittered switching frequency reduces the EMI filter cost:
 - 30 kHz ± 7% (type X)
 - 60 kHz ± 7% (type L)
- Embedded E/A with 1.2 V reference
- Protections with automatic restart: overload/short-circuit (OLP), line or output OVP, max. duty cycle counter, VCC clamp
- Pulse-skip protection to prevent flux- runaway
- Embedded thermal shutdown
- Built-in soft-start for improved system reliability

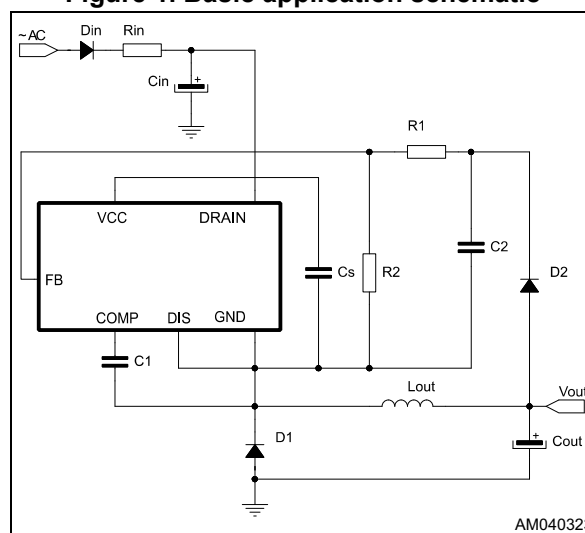
Applications

- Low power SMPS for home appliances, home automation, industrial, consumer, lighting
- Low power adapters

Description

The device is a high voltage converter smartly integrating an 800 V avalanche-rugged power MOSFET with PWM current mode control. The power MOSFET with 800 V breakdown voltage allows the extended input voltage range to be applied, as well as the size of the DRAIN snubber circuit to be reduced. This IC meets the most stringent energy-saving standards as it has very low consumption and operates in pulse frequency modulation under light load. The design of flyback, buck and buck boost converters is supported. The integrated HV startup, sense-FET, error amplifier and oscillator with jitter allow a complete application to be designed with the minimum number of components.

Figure 1. Basic application schematic



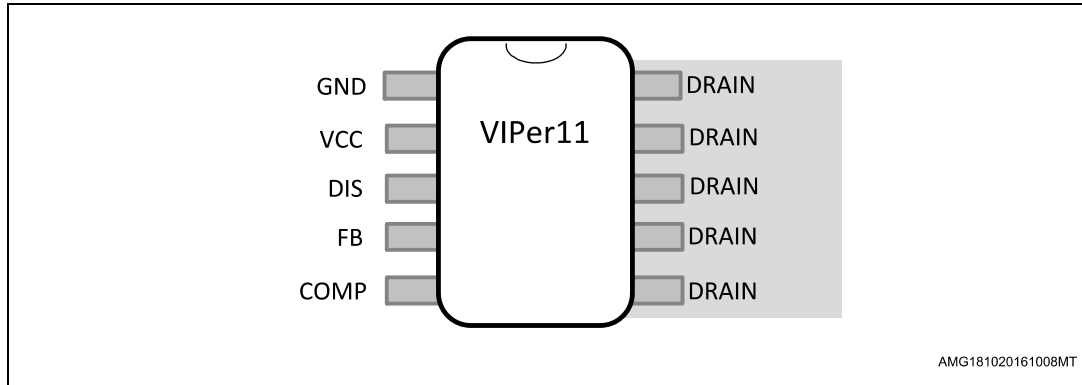
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1 Pin setting

Figure 2. Connection diagram



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Table 1. Pin description

SSOP10	Name	Function
1	GND	Ground and MOSFET source. Connection of source of the internal MOSFET and the return of the bias current of the device. All groundings of bias components must be tied to a trace going to this pin and kept separate from the pulsed current return.
2	VCC	Controller supply. An external storage capacitor has to be connected across this pin and GND. The pin, internally connected to the high voltage current source, provides the VCC capacitor charging current at startup. A small bypass capacitor (0.1 μ F typ.) in parallel, placed as close as possible to the IC, is also recommended, for noise filtering purpose.
3	DIS	Disable. If its voltage exceeds the internal threshold V_{DIS_th} (1.2 V typ.) for more than t_{DEB} time (1 ms, typ.), the PWM is disabled. An input overvoltage protection can be built by connecting a voltage divider between DIS pin and the rectified mains. In case of non-isolated topologies, with the same principle an output overvoltage protection can be implemented. If the disable function is not required, DIS pin must be soldered to GND, which excludes the function.
4	FB	Direct feedback. It is the inverting input of the internal transconductance E/A, which is internally referenced to 1.2 V with respect to GND. In case of non-isolated converter, the output voltage information is directly fed into the pin through a voltage divider. In case of primary regulation, the FB voltage divider is connected to the VCC. The E/A is disabled soldering FB to GND.
5	COMP	Compensation. It is the output of the internal E/A. A compensation network is placed between this pin and GND to achieve stability and good dynamic performance of the control loop. In case of secondary feedback, the internal E/A must be disabled and the COMP directly driven by the optocoupler to control the DRAIN peak current setpoint.
6 to 10	DRAIN	MOSFET drain. The internal high voltage current source sinks current from this pin to charge the VCC capacitor at startup and during steady-state operation. These pins are mechanically connected to the internal metal PAD of the MOSFET in order to facilitate heat dissipation. On the PCB a copper area must be placed under these pins in order to decrease the total junction-to-ambient thermal resistance thus facilitating the power dissipation.

2 Electrical and thermal ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter ^{(1), (2)}	Min.	Max.	Unit
V _{DS}	6 to 10	Drain-to-source (ground) voltage	-0.3	800	V
I _{DRAIN}	6 to 10	Pulsed drain current (pulse-width limited by SOA)	-	2	A
V _{CC}	2	VCC voltage	-0.3	Internally limited	V
I _{CC}	2	VCC internal Zener current (pulsed)	-	45 ⁽³⁾	mA
V _{DIS}	3	DIS voltage	-0.3	5 ⁽⁴⁾	V
V _{FB}	4	FB voltage	-0.3	5 ⁽⁴⁾	V
V _{COMP}	5	COMP voltage	-0.3	5 ⁽⁴⁾	V
P _{TOT}	-	Power dissipation at T _{amb} < 50 °C	-	1 ⁽⁵⁾	W
T _J	-	Junction temperature operating range	-40	150	°C
T _{STG}	-	Storage temperature	-55	150	°C

1. Stresses beyond those listed absolute maximum ratings may cause permanent damage to the device.
2. Exposure to absolute-maximum-rated conditions for extended periods may affect the device reliability.
3. Pulse-width limited by maximum power dissipation, P_{TOT}.
4. The AMR value is intended when V_{CC} ≥ 5 V, otherwise the value V_{CC} + 0.3 V has to be considered.
5. When mounted on a standard single side FR4 board with 100 mm² (0.1552 inch) of Cu (35 μm thick).

Table 3. Thermal data

Symbol	Parameter	Max. value	Unit
		SSOP10	
R _{thJP}	Thermal resistance junction-pin	35	°C/W
R _{thJA} ⁽¹⁾	Thermal resistance junction-ambient (dissipated power 1 W)	145	
	Thermal resistance junction-ambient (dissipated power 1 W) ⁽²⁾	90	

1. Derived by characterization.
2. When mounted on a standard single side FR4 board with 100 mm² (0.1552 inch) of Cu (35 μm thick).

Figure 3. $R_{thJA} / (R_{thJA} \text{ at } A = 100 \text{ mm}^2)$

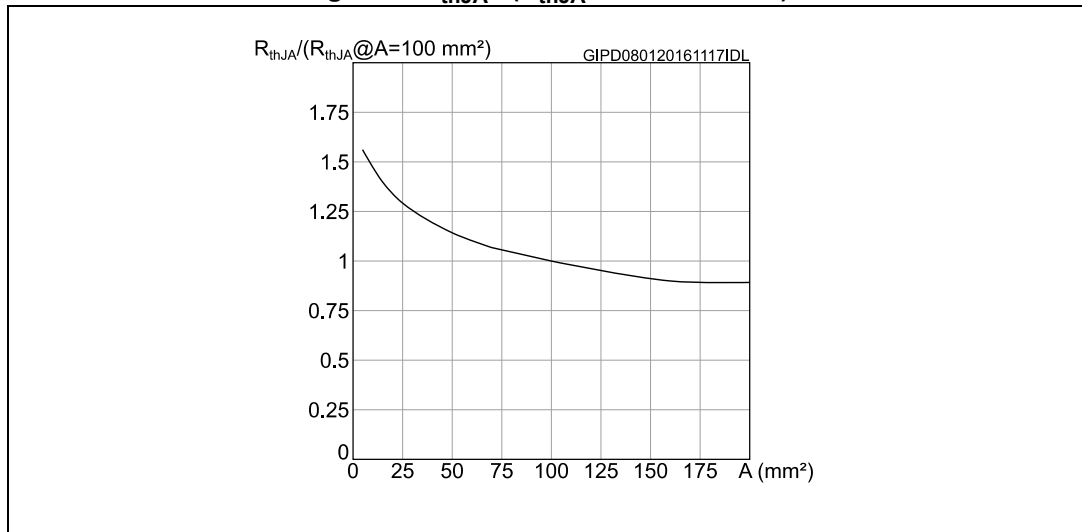


Table 4. Avalanche characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{AR}	Avalanche current	Repetitive and non-repetitive. Pulse-width limited by T_{Jmax}	-	-	0.8	A
E_{AS}	Single pulse avalanche energy ⁽¹⁾	$I_{AS} = I_{AR}$ $V_{DS} = 100 \text{ V}$ Starting $T_J = 25 \text{ }^\circ\text{C}$	-	-	1	mJ

1. Parameter derived by characterization.

Electrical characteristics

$T_J = -40$ to $125 \text{ }^\circ\text{C}$, $V_{CC} = 9 \text{ V}$ (unless otherwise specified).

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BVDSS}	Breakdown voltage	$I_{DRAIN} = 1 \text{ mA}$ $V_{COMP} = \text{GND}$ $T_J = 25 \text{ }^\circ\text{C}$	800	-	-	V
I_{DSS}	Drain-source leakage current	$V_{DS} = 400 \text{ V}$ $V_{COMP} = \text{GND}$ $T_J = 25 \text{ }^\circ\text{C}$	-	-	1	μA
I_{OFF}	OFF-state drain current	$V_{DRAIN} = \text{max. rating}$ $V_{COMP} = \text{GND}$ $T_J = 25 \text{ }^\circ\text{C}$	-	-	45	

Table 5. Power section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$R_{DS(on)}$	Static drain-source ON-resistance	$I_{DRAIN} = 295 \text{ mA}$ $T_J = 25 \text{ }^\circ\text{C}$	-	-	17	Ω
		$I_{DRAIN} = 295 \text{ mA}$ $T_J = 125 \text{ }^\circ\text{C}$	-	-	34	
C_{OSS} EQ	Equivalent output capacitance	$V_{GS} = 0$ $V_{DS} = 0 \text{ to } 640 \text{ V}$ $T_J = 25 \text{ }^\circ\text{C}$	-	10	-	pF

Table 6. Supply section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
High voltage start-up current source						
V_{BVDSS_SU}	Breakdown voltage of start-up MOSFET	$T_J = 25 \text{ }^\circ\text{C}$	800	-	-	V
V_{HV_START}	Drain-source start-up voltage	-	-	-	26	V
R_G	Start-up resistor	$V_{FB} > V_{FB_REF}$ $V_{DRAIN} = 400 \text{ V}$ $V_{DRAIN} = 600 \text{ V}$	28	34	40	M Ω
I_{CH1}	VCC charging current at startup	$V_{DRAIN} = 100 \text{ V}$ $V_{CC} = 0 \text{ V}$	0.7	1	1.3	mA
I_{CH2}	VCC charging current at startup	$V_{FB} > V_{FB_REF}$ $V_{DRAIN} = 100 \text{ V}$ $V_{CC} = 6 \text{ V}$	2	3	4	
$I_{CH3}^{(1)}$	Max. VCC charging current in self-supply	$V_{FB} > V_{FB_REF}$ $V_{DRAIN} = 100 \text{ V}$ $V_{CC} = 6 \text{ V}$	6.5	7.5	8.5	
IC supply and consumptions						
V_{CC}	Operating voltage range	$V_{GND} = 0 \text{ V}$	4.5	-	30	V
$V_{CCclamp}$	Clamp voltage	$I_{CC} = I_{clamp_max}$	30	32.5	35	V
I_{clamp_max}	Clamp shutdown current	(2)	30	35	40	mA
t_{clamp_max}	Clamp time before shutdown	-	400	500	600	μs
V_{CCon}	VCC start-up threshold	$V_{FB} = 1.2 \text{ V}$ $V_{DRAIN} = 400 \text{ V}$	15	16	17	V
V_{CSon}	HV current source turn-on threshold	V_{CC} falling	4	4.25	4.5	V
V_{CCoff}	UVLO	$V_{FB} = 1.2 \text{ V}$ $V_{DRAIN} = 400 \text{ V}$	3.75	4	4.25	V
I_q	Quiescent current	Not switching $V_{FB} > V_{FB_REF}$	-	0.3	0.45	mA

Table 6. Supply section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I _{CC}	Operating supply current, switching	V _{DS} = 150 V V _{COMP} = 1.2 V F _{OSC} = 30 kHz	-	1	1.2	mA
		V _{DS} = 150 V V _{COMP} = 1.2 V F _{OSC} = 60 kHz	-	1.25	1.5	

1. Current supplied during the main MOSFET OFF time only.
2. Parameter assured by design and characterization.

Table 7. Controller section

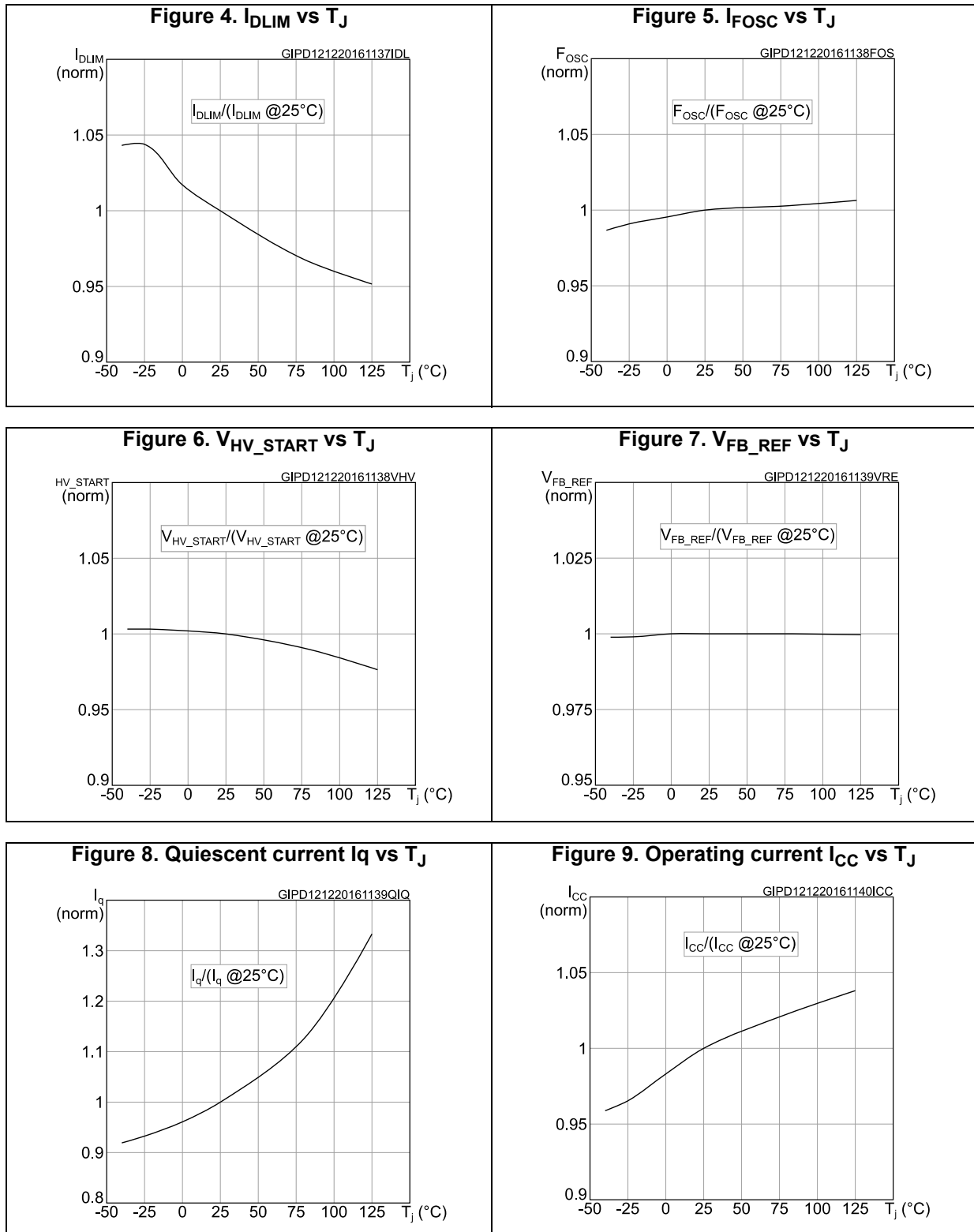
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E/A						
V _{FB_REF}	Reference voltage	-	1.175	1.2	1.225	V
V _{FB_DIS}	E/A disable voltage	-	150	180	210	mV
I _{FB_PULL UP}	Pull-up current	-	0.9	1	1.1	μA
G _M	Transconductance	V _{COMP} = 1.5 V V _{FB} > V _{FB_REF}	350	500	650	μA/V
I _{COMP1}	Max. source current	V _{COMP} = 1.5 V V _{FB} = 0.5 V	75	100	125	μA
I _{COMP2}	Max. sink current	V _{FB} = 2 V V _{COMP} = 1.5 V	75	100	125	μA
R _{COMP(DYN)}	Dynamic resistance	V _{COMP} = 2.7 V V _{FB} = GND	55	65	75	kΩ
V _{COMPH}	Current limitation threshold	-	-	3	-	V
V _{COMPL}	PFM threshold	-	-	0.8	-	V
OLP and timing						
I _{DLIM}	Drain current limitation	T _J = 25 °C VIPER114*	456	480	504	mA
		T _J = 25 °C VIPER115*	560	590	620	
I ² f	Power coefficient	I _{DLIM_TYP} ² × F _{OSC_TYP}	0.9 · I ² f	I ² f	1.1 · I ² f	A ² ·kHz
I _{DLIM_PFM}	Drain current limitation at light load	T _J = 25 °C V _{COMP} = V _{COMPL} ⁽¹⁾ VIPER114*	90	115	140	mA
		T _J = 25 °C V _{COMP} = V _{COMPL} ⁽¹⁾ VIPER115*	105	130	155	

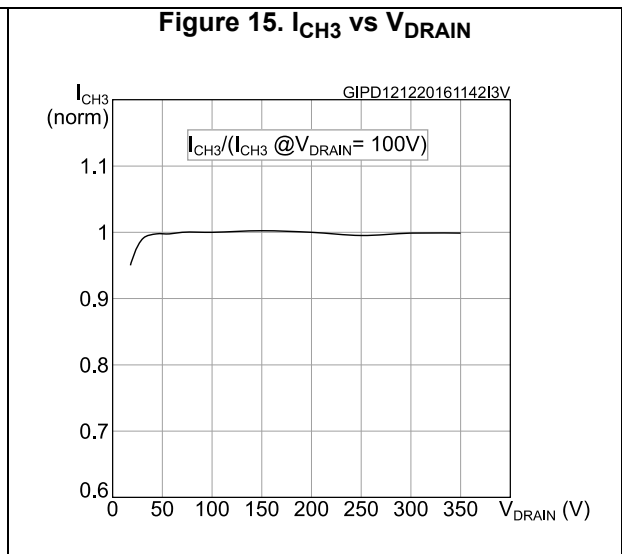
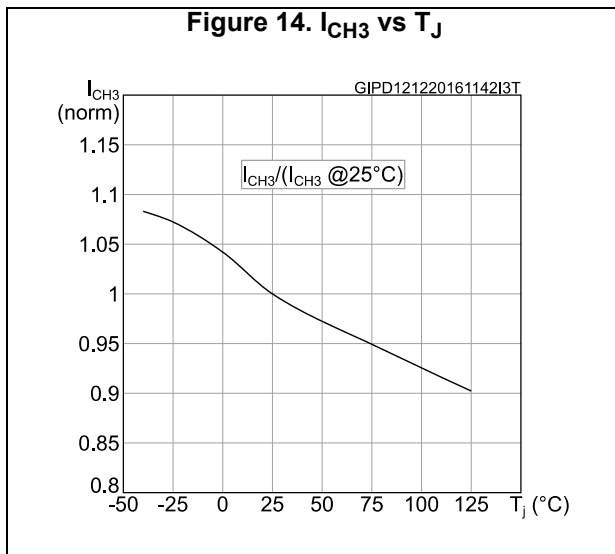
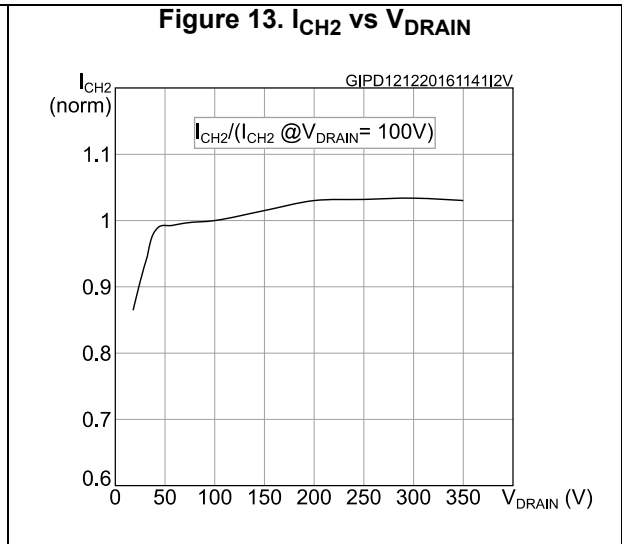
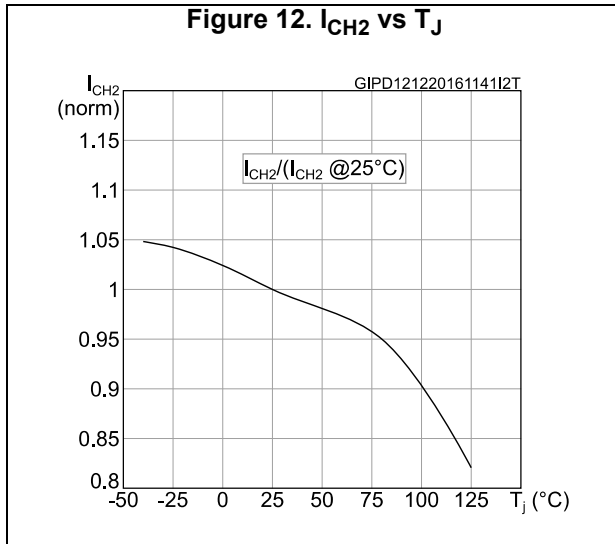
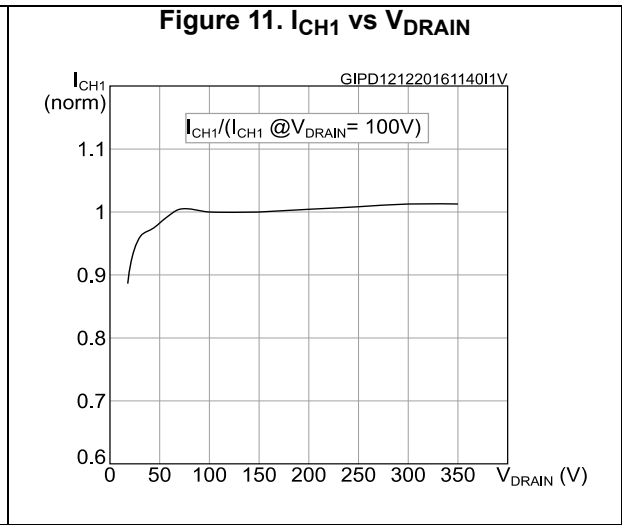
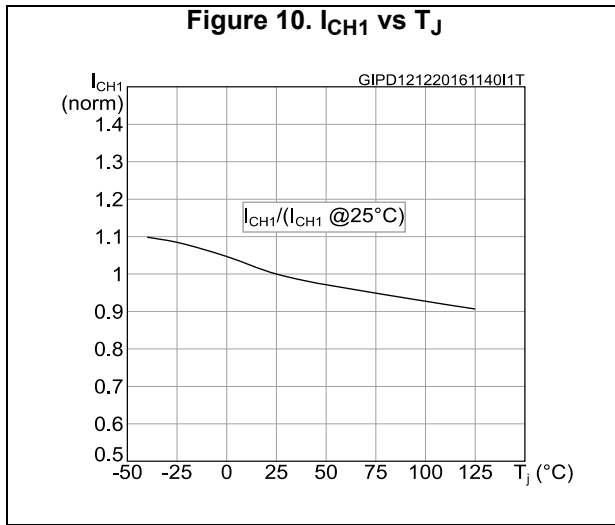
Table 7. Controller section (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{DISth}	Disable threshold voltage	$V_{CC} = 9\text{ V}$ $V_{COMP} = 1\text{ V}$ $V_{FB} = V_{FB_REF}$	1.15	1.2	1.25	V
t_{DIS}	Debounce time before DIS protection tripping	-	0.8	1	1.2	ms
$t_{DIS_RESTART}$	Restart time after DIS protection tripping	-	400	500	600	ms
t_{OVL}	Overload delay time	-	45	50	55	ms
t_{OVL_MAX}	Max. overload delay time	VIPER11*X $F_{OSC} = F_{OSC\ MIN}$	90	100	110	ms
		VIPER11*L $F_{OSC} = F_{OSC\ MIN}$	180	200	220	
		VIPER11*H $F_{OSC} = F_{OSC\ MIN}$	360	400	440	
t_{SS}	Soft-start time	-	6	8	10	ms
t_{ON_MIN}	Minimum turn-on time	$V_{CC} = 9\text{ V}$ $V_{COMP} = 1\text{ V}$ $V_{FB} = V_{FB_REF}$	250	300	350	ns
$t_{RESTART}$	Restart time after fault	-	0.8	1	1.2	s
Oscillator						
F_{OSC}	Switching frequency	$T_J = 25\text{ °C}$ VIPER11*X	27	30	33	kHz
		$T_J = 25\text{ °C}$ VIPER11*L	54	60	66	
F_{OSC_MIN}	Minimum switching frequency	$T_J = 25\text{ °C}^{(2)}$	13.5	15	16.5	kHz
F_D	Modulation depth	⁽³⁾	-	± 7 FOSC	-	%
F_M	Modulation frequency	⁽³⁾	-	260	-	Hz
D_{MAX}	Max. duty cycle	⁽³⁾	70		80	%
Thermal shutdown						
T_{SD}	Thermal shutdown temperature	⁽³⁾	150	160		°C

1. See [Section 4.10: Pulse frequency modulation on page 19](#).
2. See [Section 4.7: Pulse-skipping on page 18](#).
3. Parameter assured by design and characterization.

3 Typical electrical characteristics





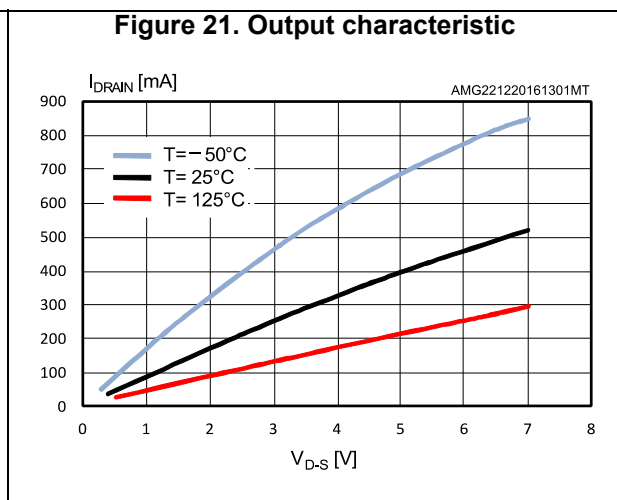
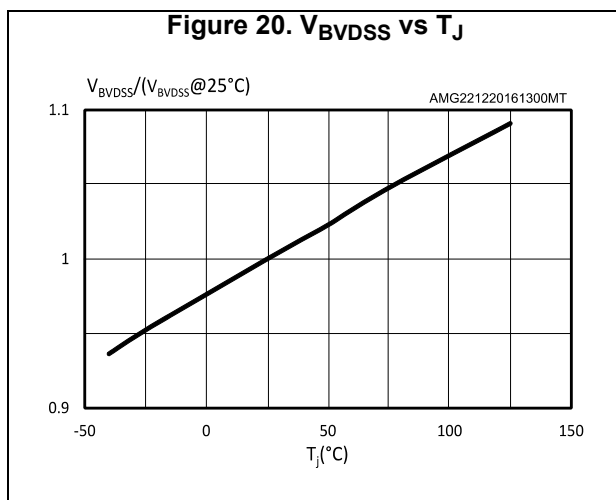
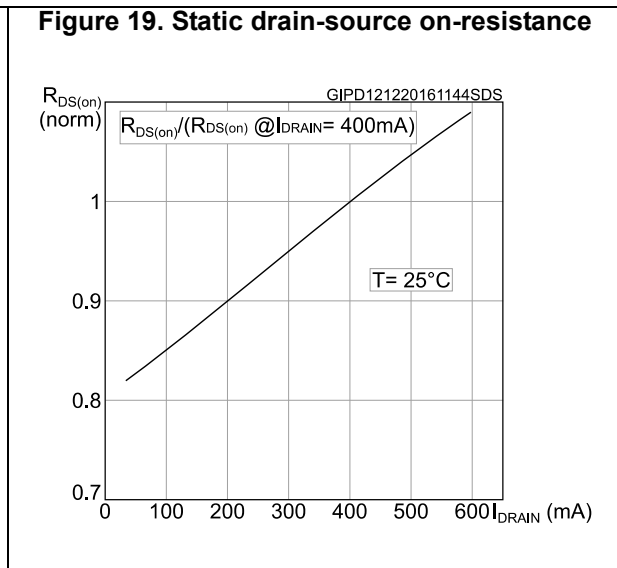
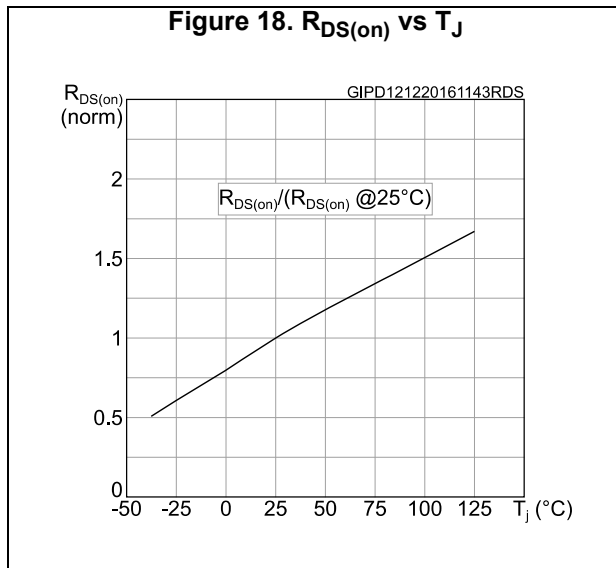
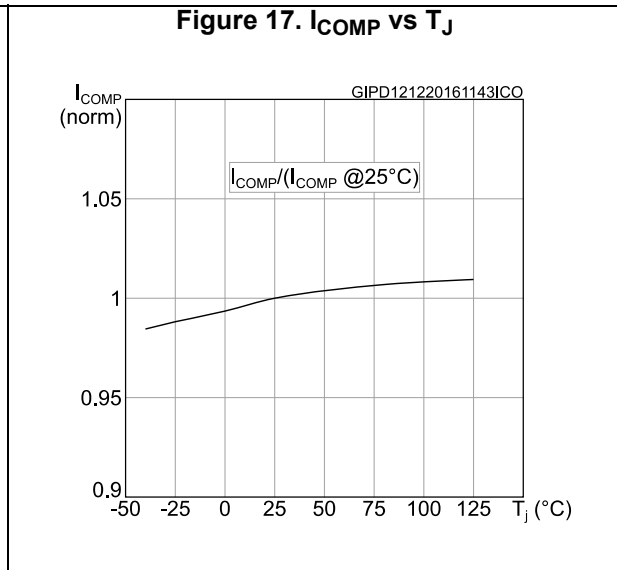
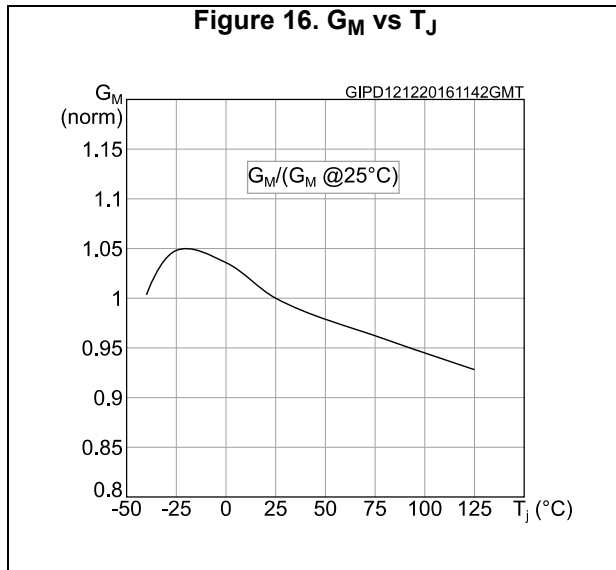
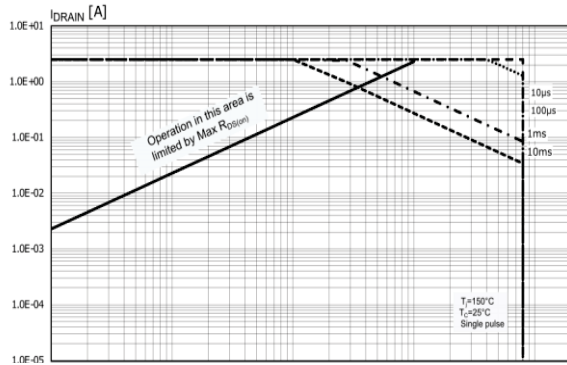
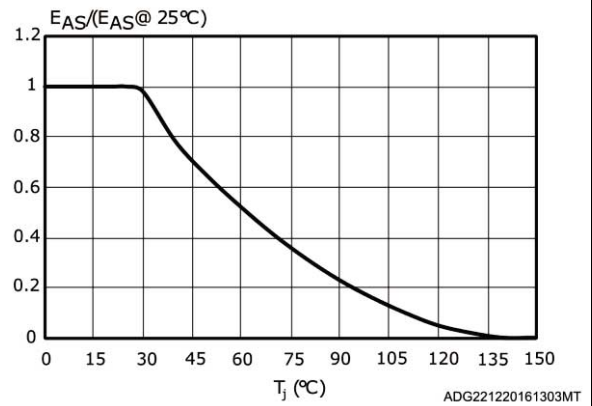


Figure 22. SOA SSOP10 package



* When mounted on a standard single side FR4 board with 50 mm² (0.077 sq in) of Cu (35 µm thick).

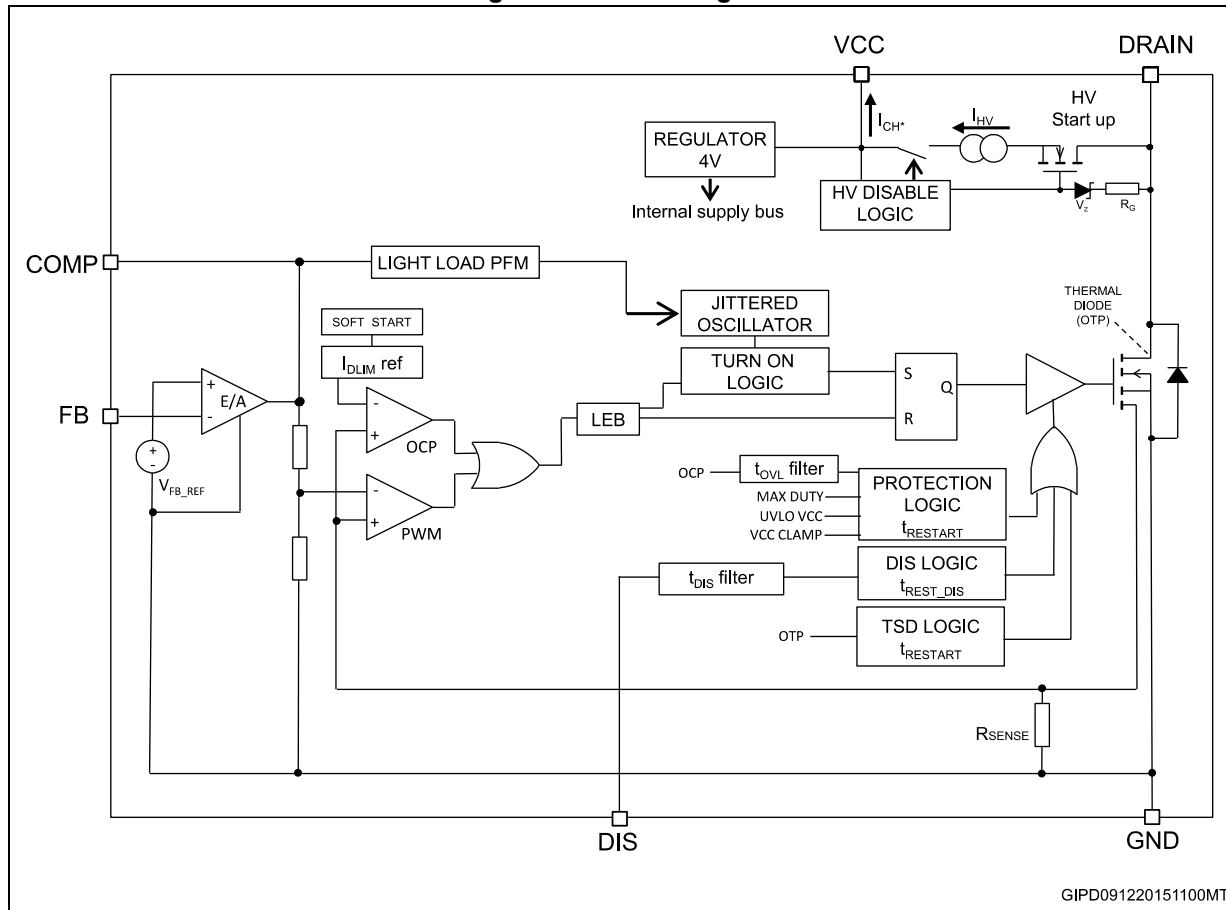
Figure 23. Maximum avalanche energy vs T_J



4 General description

4.1 Block diagram

Figure 24. Block diagram



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4.2 Typical power capability

Table 8. Typical power

Vin: 230 V _{AC}		Vin: 85-265 V _{AC}	
Adapter ⁽¹⁾	Open frame ⁽²⁾	Adapter	Open frame
10 W	12 W	6 W	7 W

1. Typical continuous power in non-ventilated enclosed adapter measured at 50 °C ambient.
2. Maximum practical continuous power in an open frame design at 50 °C ambient, with adequate heat-sinking.

4.3 Primary MOSFET

The primary switch is implemented with an avalanche-rugged N-channel MOSFET with minimum breakdown voltage 800 V, V_{BVDSS} , and maximum on-resistance of 20Ω , $R_{DS(on)}$. The sense-FET is embedded and it allows a virtually lossless current sensing. The MOSFET is embedded and it allows the HV voltage start-up operation.

The MOSFET gate driver controls the gate current during both turn-on and turn-off in order to minimize EMI. Under UVLO conditions the embedded pull-down circuit holds the gate low in order to ensure that the MOSFET cannot be turned on accidentally.

4.4 High voltage startup

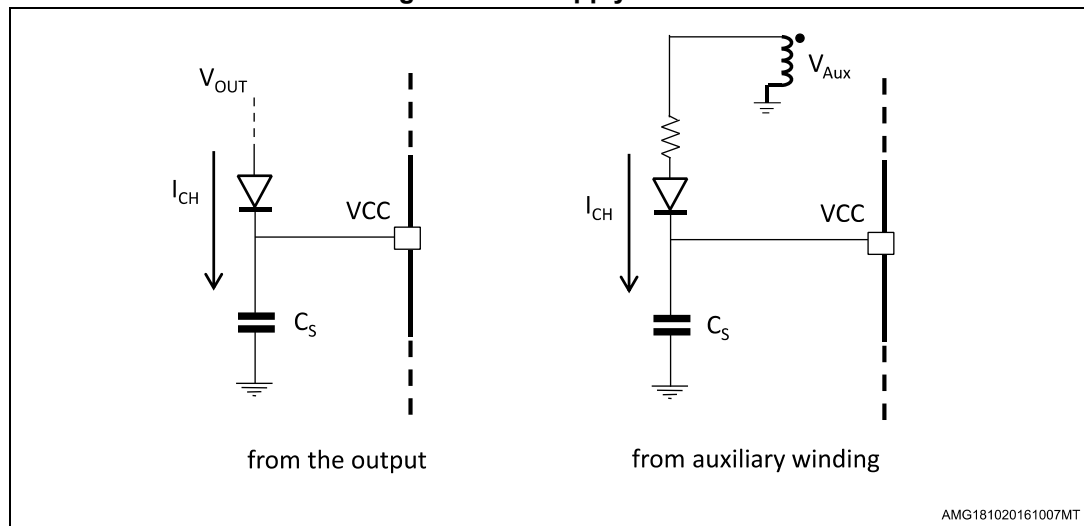
The embedded high voltage startup includes both the 800 V start-up FET, whose gate is biased through the resistor R_G , and the switchable HV current source, delivering the current I_{HV} . The major portion of I_{HV} , (I_{CH}), charges the capacitor connected to VCC. A minor portion is sunk by the controller block.

At startup, as the voltage across the DRAIN pin exceeds the V_{HV_START} threshold, the HV current source is turned on, charging linearly the C_S capacitor. At the very beginning of the startup, when C_S is fully discharged, the charging current is low, I_{CH1} , in order to avoid IC damaging in case V_{CC} is accidentally shorted to GND. As V_{CC} exceeds 1 V, I_{CH} is increased to I_{CH2} in order to speed up the charging of C_S .

As V_{CC} reaches the start-up threshold V_{CCon} the chip starts operating, the primary MOSFET is enabled to switch, the HV current source is disabled and the device is powered by the energy stored in the C_S capacitor.

In steady-state the IC can be supplied from the output (in case of non-isolated topologies) or through an auxiliary winding (in case of isolated topologies), as shown in [Figure 25](#).

Figure 25. IC supply modes



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In external supply the HV current source is always kept off by maintaining the V_{CC} above V_{CCson} . In this case the residual consumption is given by the power dissipated on R_G , calculated as follows:

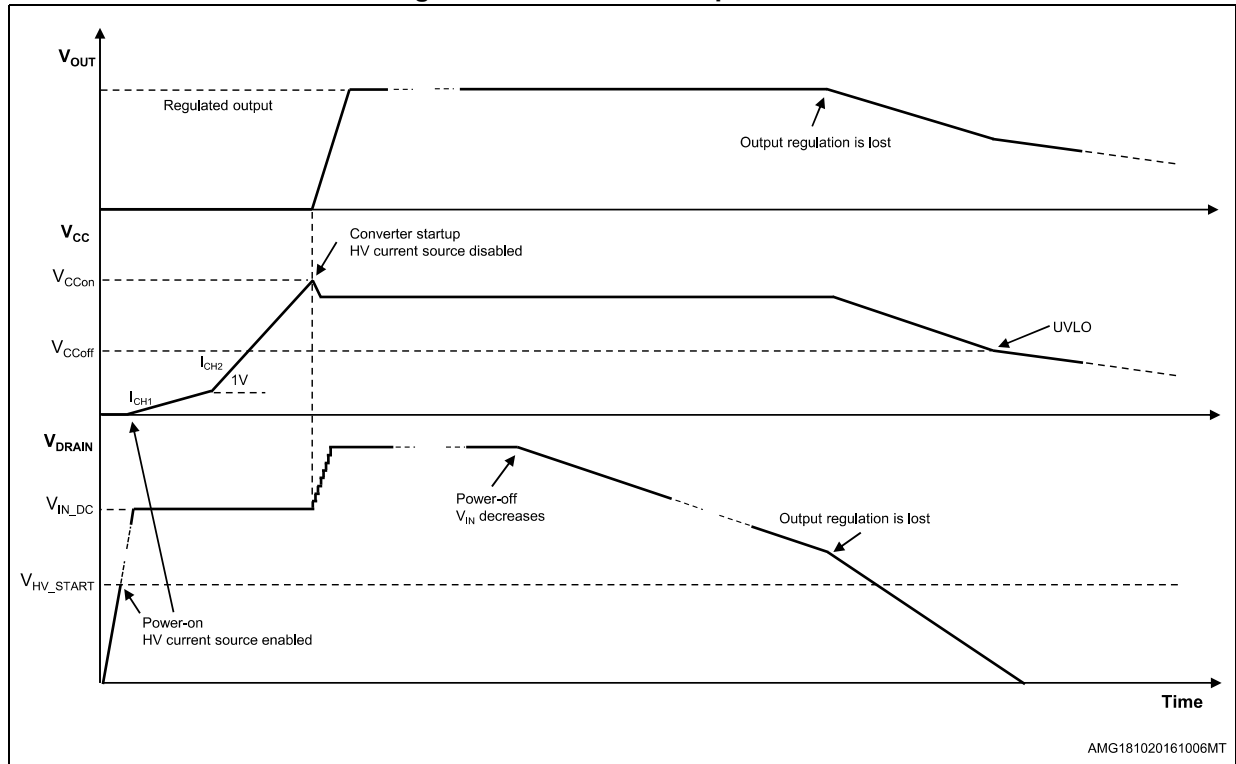
Equation 1

$$P = \frac{V_{INDC}^2}{R_G}$$

At the nominal input voltage, 230 V_{AC}, the typical consumption ($R_G = 34 \text{ M}\Omega$) is 3.2 mW and the worst-case consumption ($R_G = 28 \text{ M}\Omega$) is 3.9 mW.

When the IC is disconnected from the mains, or there is a mains interruption, for some time the converter keeps on working, powered by the energy stored in the input bulk capacitor. When it is discharged below a critical value, the converter is no longer able to keep the output voltage regulated. During the power down, when the DRAIN voltage becomes too low, the HV current source (I_{HV}) remains off and the IC is stopped as soon as the V_{CC} drops below the UVLO threshold, V_{CCoff} .

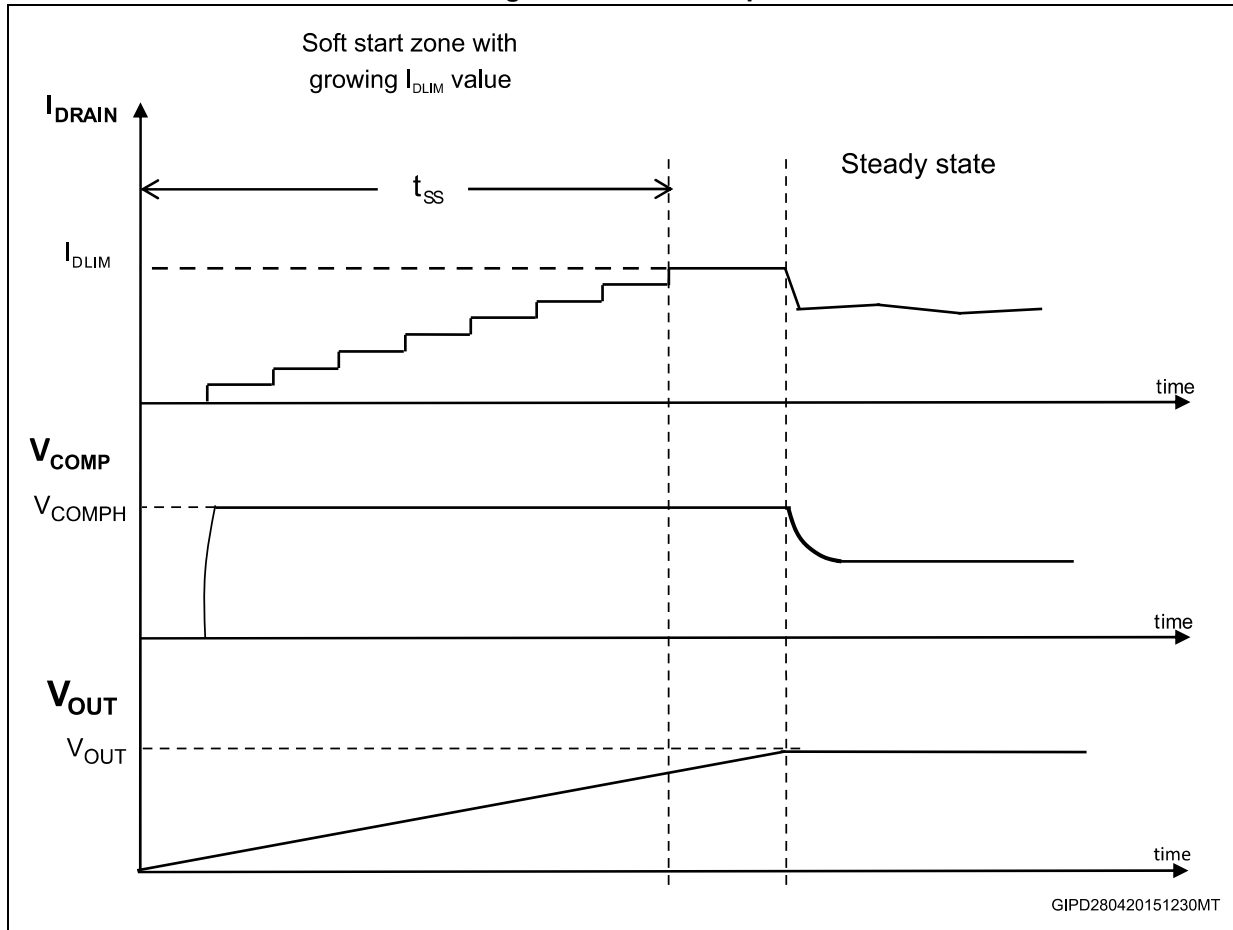
Figure 26. Power-ON and power-OFF



4.5 Soft-start

The internal soft-start function of the device progressively increases the cycle-by-cycle current limitation set point from zero up to I_{DLIM} in 8 steps. The soft-start time, t_{SS} , is internally set at 8 ms. This function is activated at any attempt of converter startup and at any restart after a fault event. The feature protects the system at the startup when the output load occurs like a short-circuit and the converter works at its maximum drain current limitation.

Figure 27. Soft startup



4.6 Oscillator

The IC embeds a fixed frequency oscillator with jittering feature. The switching frequency is modulated by approximately $\pm 7\%$ kHz F_{OSC} at 260 Hz rate. The purpose of the jittering is to get a spread-spectrum action that distributes the energy of each harmonic of the switching frequency over a number of frequency bands, having the same energy on the whole but smaller amplitudes. This helps to reduce the conducted emissions, especially when measured with the average detection method or, which is the same, to pass the EMI tests with an input filter of smaller size than that needed in absence of jittering feature.

Two options with different switching frequencies, F_{OSC} , are available: 30 (X type) and 60 kHz (L type).

4.7 Pulse-skipping

The IC embeds a pulse-skip circuit that operates in the following ways:

- Each time the DRAIN peak current exceeds I_{DLIM} level within t_{ON_MIN} , the switching cycle is skipped. The cycles can be skipped until the minimum switching frequency is reached, F_{OSC_MIN} (15 kHz).
- Each time the DRAIN peak current does not exceed I_{DLIM} within t_{ON_MIN} , a switching cycle is restored. The cycles can be restored until the nominal switching frequency is reached, F_{OSC} (30 or 60 kHz).

If the converter is operated at F_{OSC_MIN} , the IC is turned off after the time t_{OVL_MAX} (100 ms or 200 ms or 400 ms typ., depending on F_{OSC}) and then automatically restarted with soft-start phase, after the time $t_{RESTART}$ (1 s, typ.).

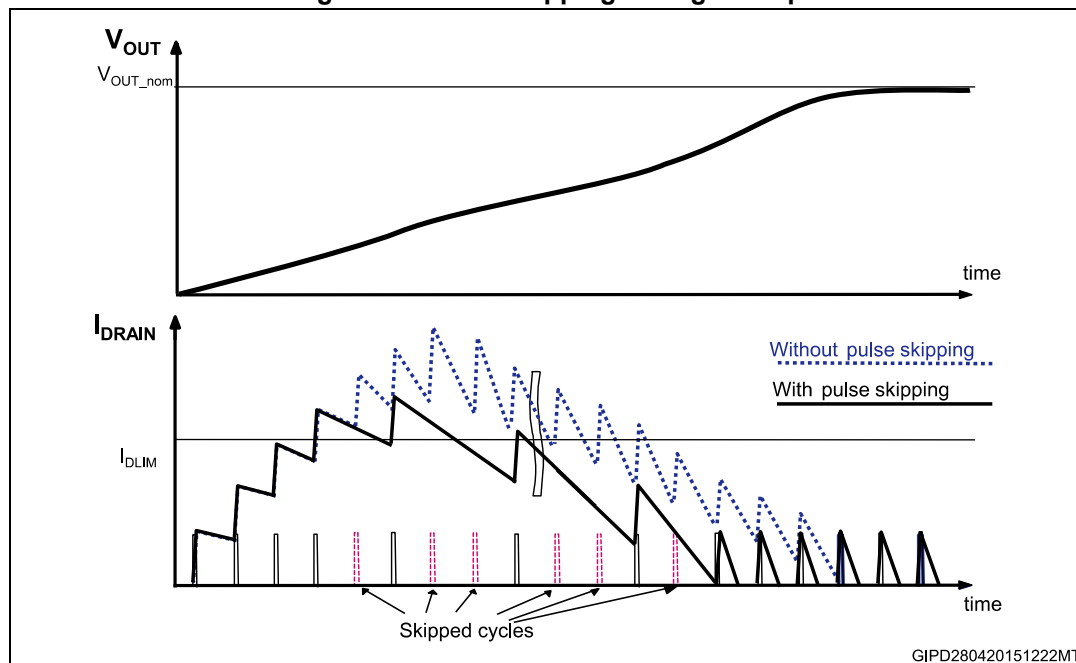
The protection is intended to avoid the so called “flux-runaway” condition often present at converter startup and due to the fact that the primary MOSFET, which is turned on by the internal oscillator, cannot be turned off before than the minimum on-time.

During the on-time, the inductor is charged by the input voltage and if it cannot be discharged by the same amount during the off-time, in every switching cycle there is an increase of the average inductor current, that can reach dangerously high values until the output capacitor is not charged enough to ensure the inductor discharge rate needed for the volt-second balance. This condition may happen at converter startup, because of the low output voltage.

In [Figure 28](#) the effect of pulse-skipping feature on the DRAIN peak current shape is shown (solid line), compared with the DRAIN peak current shape when pulse-skipping feature is not implemented (dashed line).

Providing more time for cycle-by-cycle inductor discharge when needed, this feature is effective by keeping low the maximum DRAIN peak current avoiding the flux-runaway condition.

Figure 28. Pulse-skipping during startup



4.8 Direct feedback

The IC embeds a transconductance type error amplifier (E/A) whose inverting input, ground reference and output are FB and COMP, respectively. The internal reference voltage of the E/A is V_{FB_REF} (1.2 V typical value referred to GND). In non-isolated topologies this tightly regulates positive output voltages through a simple voltage divider applied to the output voltage terminal, FB and GND.

The E/A output is scaled down and fed into the PWM comparator, where it is compared to the voltage across the sense resistor in series to the sense-FET, thus setting the cycle-by-cycle drain current limitation.

An R-C network connected on the output of the E/A (COMP) is usually used to stabilize the overall control loop.

The FB is provided with an internal pull-up to prevent a wrong IC behavior when the pin is accidentally left floating.

The E/A is disabled if the FB voltage is lower than V_{FB_DIS} (200 mV, typ.).

4.9 Secondary feedback

When a secondary feedback is required, the internal E/A has to be disabled shorting FB to GND ($V_{FB} < V_{FB_DIS}$). With this setting, COMP is internally connected to a pre-regulated voltage through the pull-up resistor $R_{COMP(DYN)}$ and the voltage across COMP is set by the current sunk.

This allows the output voltage value to be set through an external error amplifier (TL431 or similar) placed on the secondary side, whose error signal is used to set the DRAIN peak current setpoint corresponding to the output power demand. If isolation is required, the error signal must be transferred through an optocoupler, with the phototransistor collector connected across COMP and GND.

4.10 Pulse frequency modulation

If the output load is decreased, the feedback loop reacts lowering the V_{COMP} voltage, which reduces the DRAIN peak current setpoint, down to the minimum value of I_{DLIM_PFM} when the V_{COMPL} threshold is reached.

If the load is furtherly decreased, the DRAIN peak current value is maintained at I_{DLIM_PFM} and some PWM cycles are skipped. This kind of operation is referred to as “pulse frequency modulation” (PFM), the number of the skipped cycles depends on the balance between the output power demand and the power transferred from the input. The result is an equivalent switching frequency which can go down to some hundreds Hz, thus reducing all the frequency-related losses.

This kind of operation, together with the extremely low IC quiescent current, allows very low input power consumption in no-load and light load, while the low DRAIN peak current value, I_{DLIM_PFM} , prevents any audible noise which could arise from low switching frequency values. When the load is increased, V_{COMP} increases and PFM is exited. V_{COMP} reaches its maximum at V_{COMPH} and corresponding to that value, the DRAIN current limitation (I_{DLIM}) is reached.

4.11 Overload protection

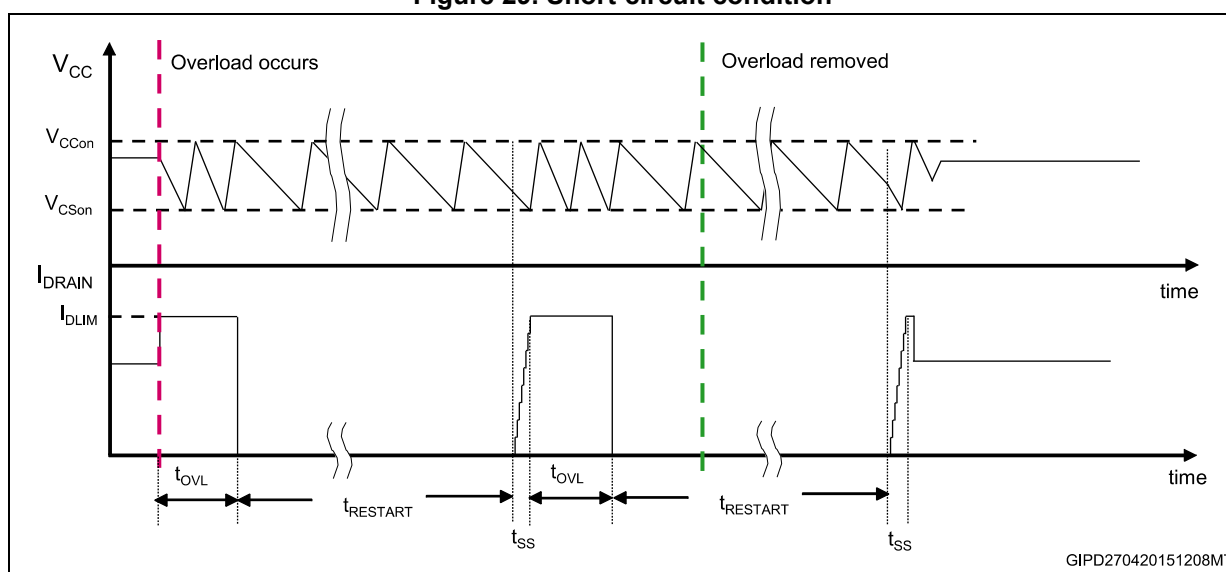
To manage the overload condition, the IC embeds the following main blocks: the OCP comparator to turn off the power MOSFET when the drain current reaches its limit (I_{DLIM}), the up and down OCP counter to define the turn-off delay time in case of continuous overload ($t_{OVL} = 50\text{ ms typ.}$) and the timer to define the restart time after protection tripping ($t_{RESTART} = 1\text{ s typ.}$).

In case of short-circuit or overload, the control level on the inverting input of the PWM comparator is greater than the reference level fed into the inverting input of the OCP comparator. As a result, the cycle-by-cycle turn-off of the power switch is triggered by the OCP comparator instead of PWM comparator. Every cycle where this condition is met, the OCP counter is incremented and if the fault condition lasts longer than t_{OVL} (corresponding to the counter end-of-count), the protection is tripped, the PWM is disabled for $t_{RESTART}$, then it resumes switching with soft-start and, if the fault is still present, it is disabled again after t_{OVL} . The OLP management prevents IC from operating indefinitely at I_{DLIM} and the low repetition rate of the restart attempts of the converter avoids IC overheating in case of repeated fault events.

After the fault removal, the IC resumes working normally. If the fault is removed earlier than the protection tripping (before t_{OVL}), the t_{OVL} -counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped. If the fault is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period has elapsed before resuming switching.

In fault condition the V_{CC} ranges between V_{CCson} and V_{CCcon} levels, due to the periodical activation of the HV current source recharging the V_{CC} capacitor.

Figure 29. Short-circuit condition



4.12 Max. duty cycle counter protection

The IC embeds a max. duty cycle counter, which disables the PWM if the MOSFET is turned off by max. duty cycle (70% min., 80% max.) for ten consecutive switching cycles. After protection tripping, the PWM is stopped for t_{RESTART} and then activated again with soft-start phase until the fault condition is removed.

In some cases (i.e. breaking of the loop) even if V_{COMP} is saturated high, the OLP cannot be triggered because at every switching cycle the PWM is turned off by maximum duty cycle before than DRAIN peak current reaches the IDLIM setpoint. As a result, the output voltage V_{OUT} can increase without control by keeping a value much higher than the nominal one with the risk for the output capacitor, the output diode and the IC itself. The max. duty cycle counter protection avoids this kind of failures.

4.13 VCC clamp protection

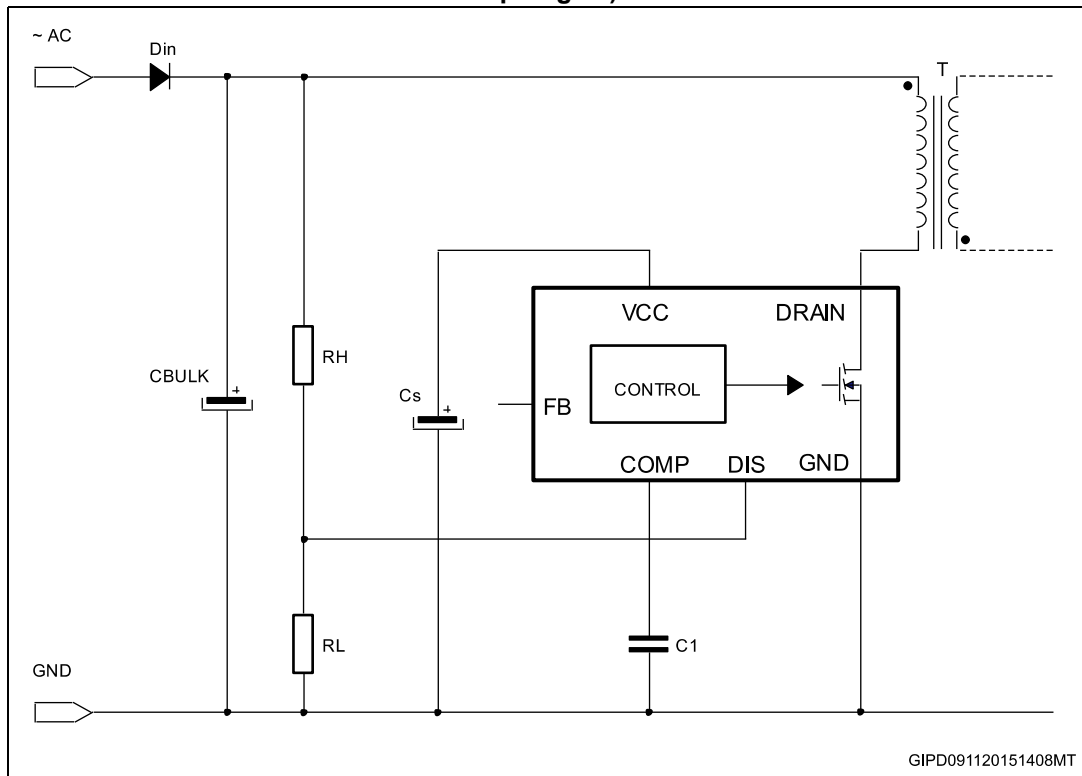
This protection can occur when the IC is supplied by auxiliary winding or diode from the output voltage, when an output overvoltage produces an increase of V_{CC} .

If V_{CC} reaches the clamp level V_{CCclamp} (30 V, min. referred to GND) the current injected into the pin is monitored and if it exceeds the internal threshold $I_{\text{clamp_max}}$ (30 mA, typ.) for more than $t_{\text{clamp_max}}$ (500 μs , typ.), the PWM is disabled for t_{RESTART} (1 s, typ.) and then activated again in soft-start phase. The protection is disabled during the soft-start time.

4.14 Disable function

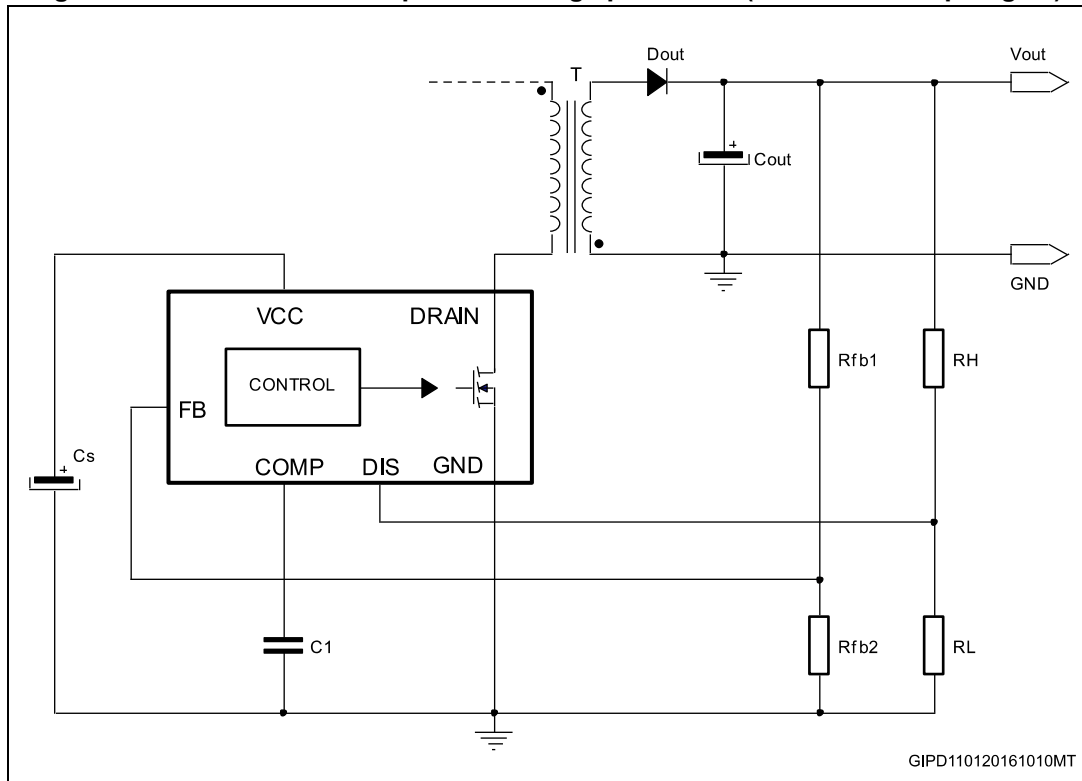
When the voltage across the pin is externally pulled above V_{DIS_th} (1.2 V typ.) for more than t_{DEB} (for instance by a voltage divider connected to some higher voltages), the PWM is disabled. If the voltage divider on the DIS pin is connected to the rectified mains, as shown in [Figure 30](#), an input overvoltage protection can be built.

Figure 30. Connection for input overvoltage protection (isolated or non-isolated topologies)



In case of non-isolated topologies, by following the same principle an output overvoltage protection can be built, as shown in [Figure 31](#).

Figure 31. Connection for output overvoltage protection (non-isolated topologies)



If V_{OVP} is the desired input/output overvoltage threshold, the resistors R_H and R_L of the voltage divider are to be selected according to the following formula:

Equation 2

$$R_H = (V_{OVP} / V_{DIS_th} - 1) \times R_L$$

The power dissipation associated to the DIS network is:

Equation 3

$$P_{DIS}(V_{IN}) = P_{RH} + P_{RL} = \frac{(V_{IN} - V_{DIS})^2}{R_H} + \frac{V_{DIS}^2}{R_L}$$

in case of connection for the input overvoltage detection and

Equation 4

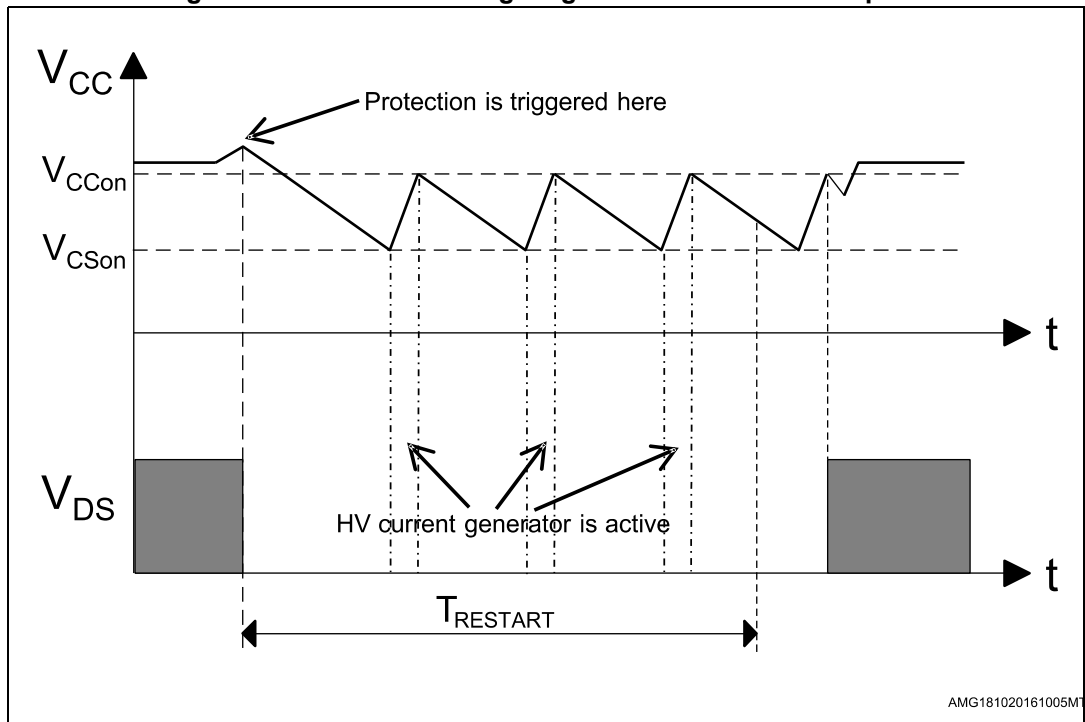
$$P_{DIS}(V_{OUT}) = P_{RH} + P_{RL} = \frac{(V_{OUT} - V_{DIS})^2}{R_H} + \frac{V_{DIS}^2}{R_L}$$

in case of connection for the output overvoltage detection.

4.15 Auto-restart

When a fault occurs and a protection trips the PWM is disabled for $t_{RESTART}$ (1 s typ). During this time interval, the HV generator is activated periodically, maintaining the VCC pin voltage between V_{CSon} and V_{CCon} . The PWM is enabled at the first V_{CC} recycle to V_{CCon} after $T_{RESTART}$, as shown in [Figure 32](#). If the fault is still present, the protection is tripped in the same way, otherwise normal operation is restored.

Figure 32. Protection timing diagram with auto-restart option

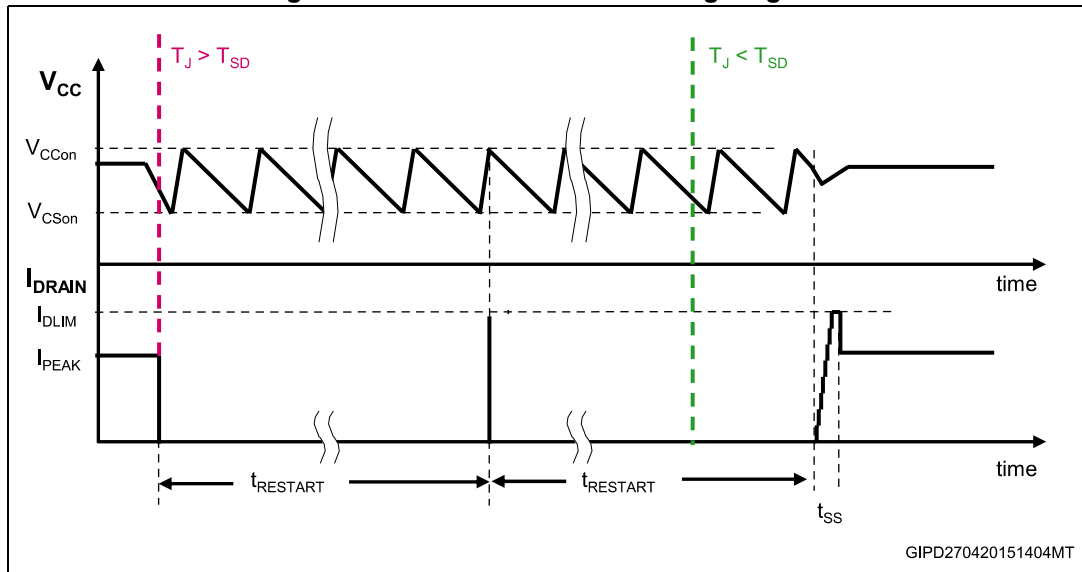


4.16 Thermal shutdown

If the junction temperature becomes higher than the internal threshold TSD (160 °C, typ.), the PWM is disabled. After $t_{RESTART}$ time, a single switching cycle is performed, during which the temperature sensor embedded in the power MOSFET section is checked. If a junction temperature above TSD is still measured, the PWM is maintained disabled for $t_{RESTART}$ time, otherwise it resumes switching with soft-start phase.

During $t_{RESTART}$ V_{CC} is maintained between V_{CCon} and V_{CSon} levels by the HV current source periodical activation. Such a behavior is summarized in below figure:

Figure 33. Thermal shutdown timing diagram



5 Application information

5.1 Typical schematics

Figure 34. Flyback converter (non-isolated)

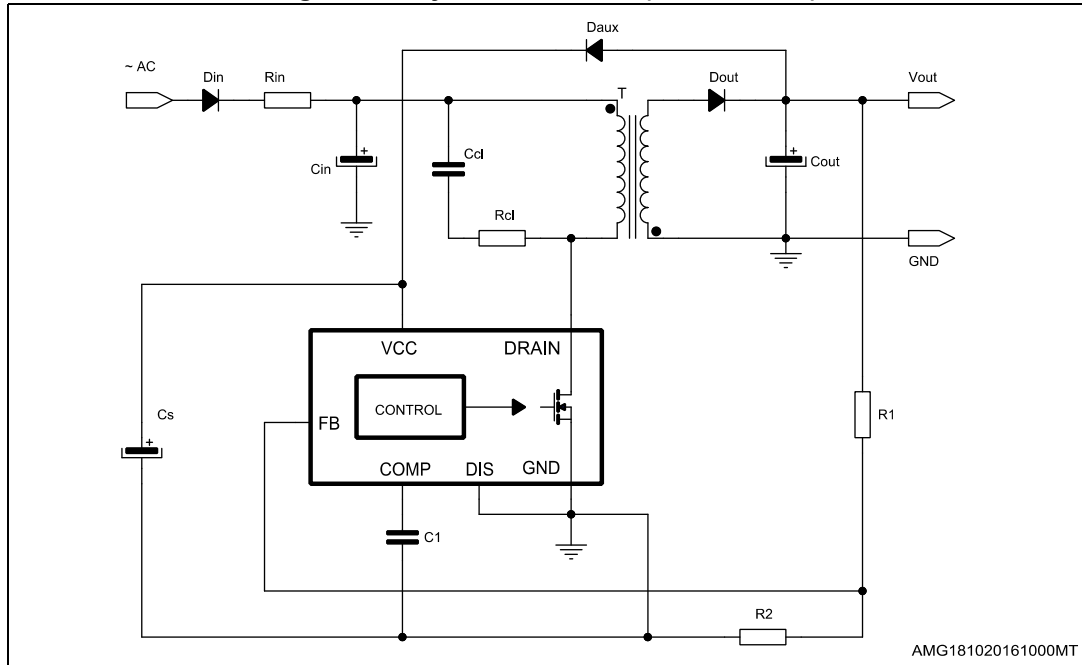


Figure 35. Flyback converter with line OVP (non-isolated)

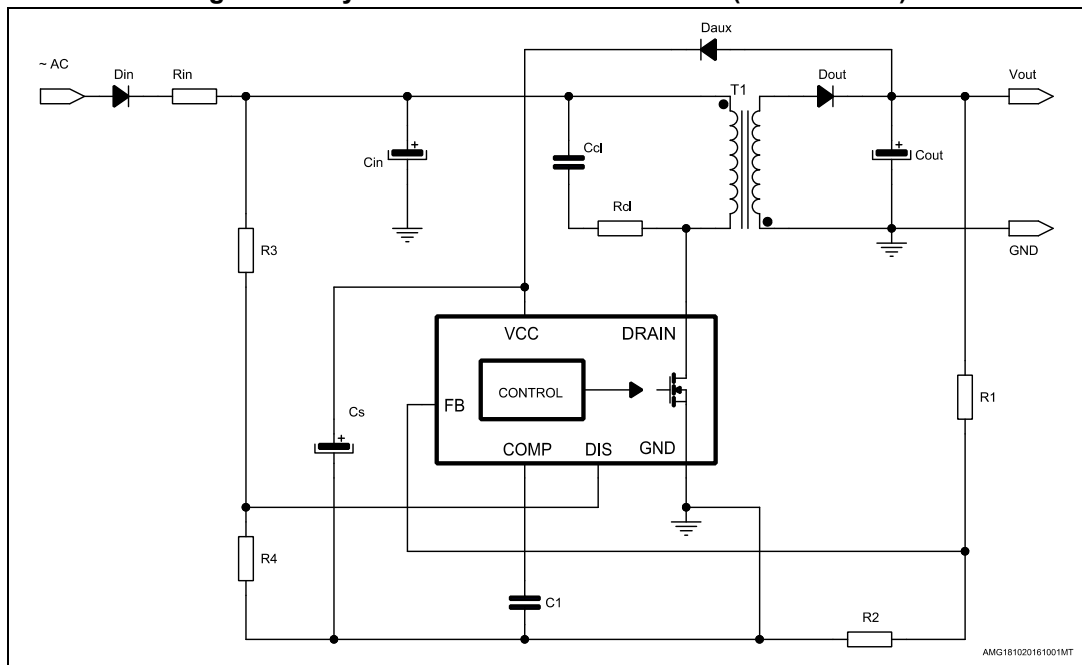


Figure 36. Flyback converter (isolated)

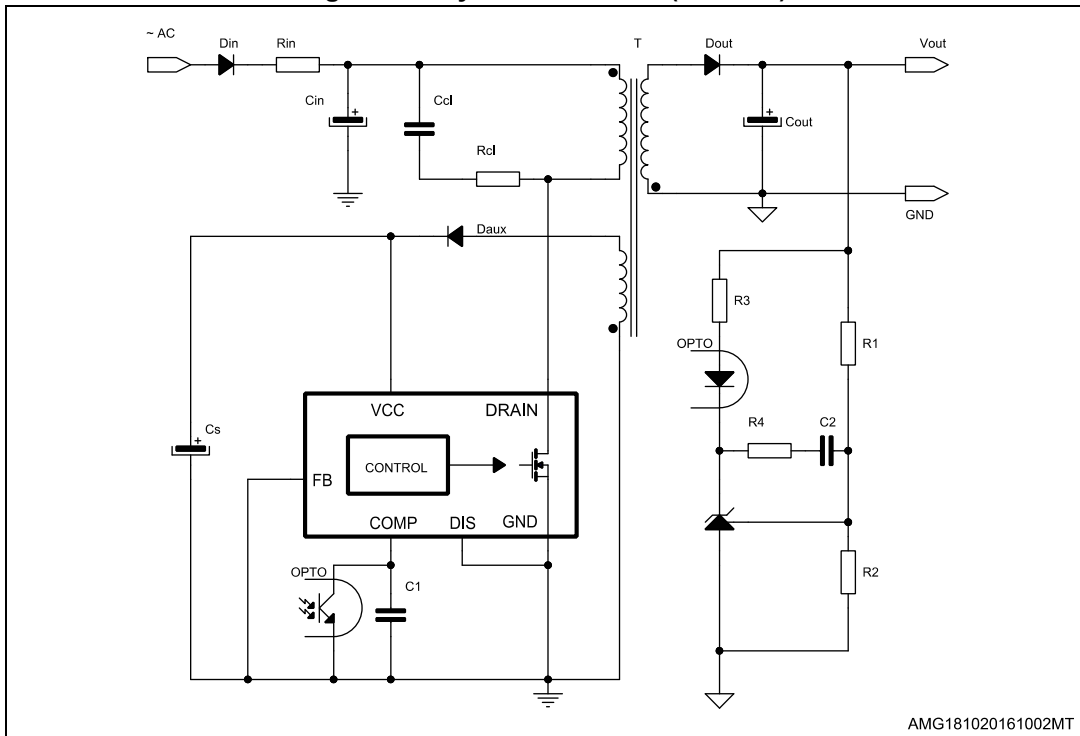


Figure 37. Primary side regulation isolated flyback converter

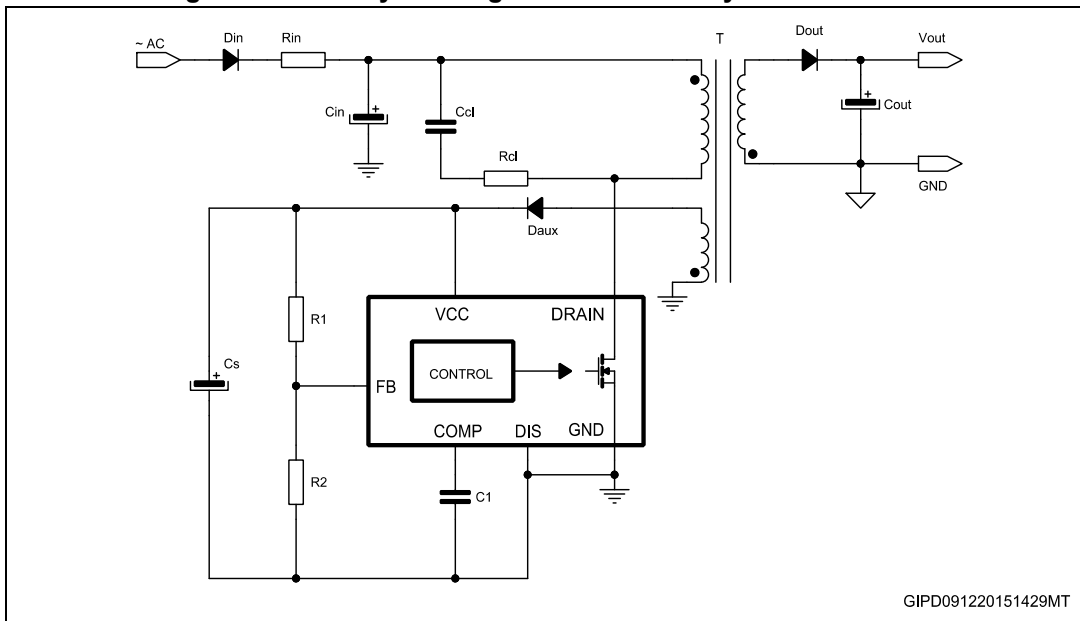


Figure 38. Buck converter (positive output)

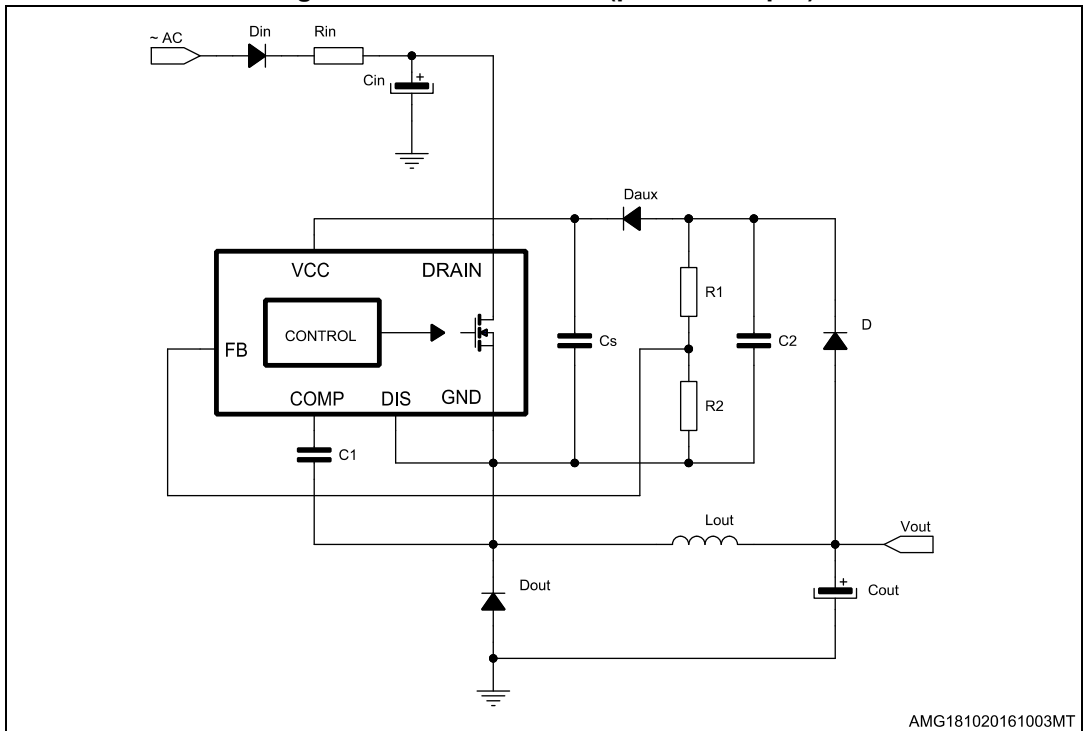
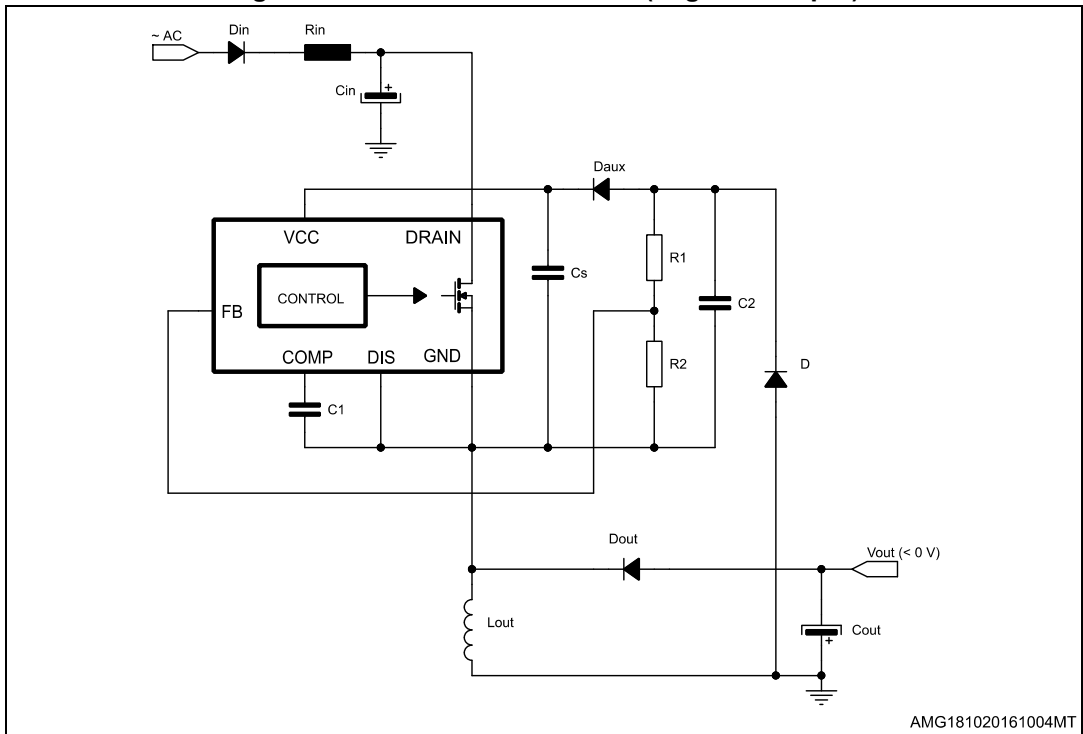


Figure 39. Buck-boost converter (negative output)



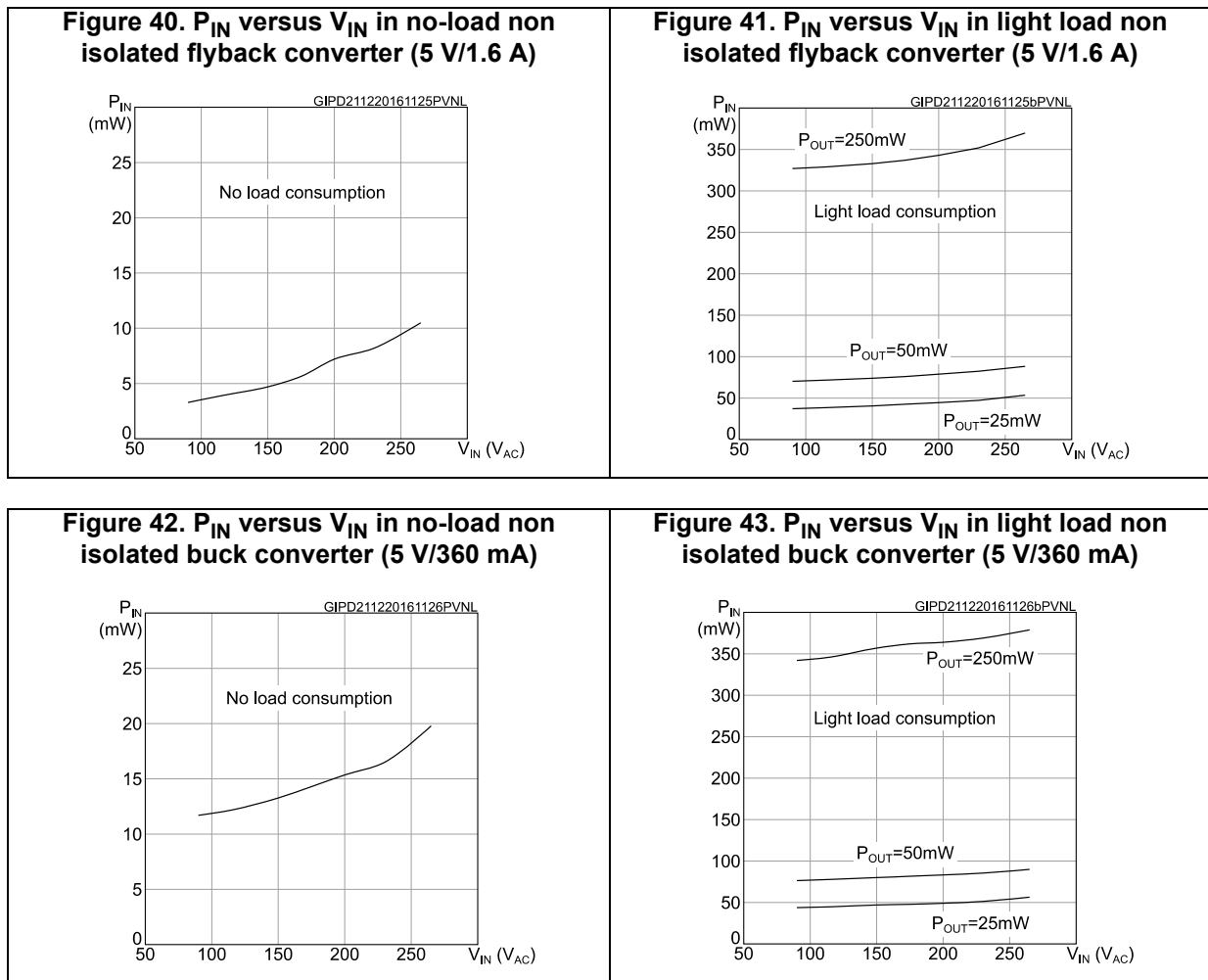
5.2 Energy saving performance

The device allows designing applications to be compliant with the most stringent energy saving regulations. In order to show the typical performance is achievable, the active mode average efficiency and the efficiency at 10% of the rated output power of a 5 V/1.6 A non isolated flyback and 5 V/360 mA buck converters adopting VIPer11, have been measured and are reported in [Table 9](#). In addition, no-load and light load consumptions are shown from [Figure 40](#) to [Figure 43](#).

Table 9. Power supply efficiency, $V_{OUT} = 5 V$

Parameter	V_{IN}	10 % output load efficiency [%]	Active mode average efficiency [%]	Pin at no-load [mW]
Flyback non iso. 5 V/1.6 A	115 V_{AC}	78.3	78.5	3.9
	230 V_{AC}	71.4	79.4	8.2
Buck 5 V/360 mA ⁽¹⁾	115 V_{AC}	73.9	71.6	12.1
	230 V_{AC}	69.1	69.8	16.2

1. 5 mW bleeder connected at the output.



5.3 Layout guidelines and design recommendations

A proper printed circuit board layout ensures the correct operation of any switch-mode converter and this is true for the VIPer as well. The main reasons to have a proper PCB layout are:

- Providing clean signals to the IC, ensuring good immunity against external and switching noises.
- Reducing the electromagnetic interferences, both radiated and conducted, to pass the EMC tests more easily.

If the VIPer is used to design a SMPS, the following basic rules should be considered:

- **Separating signal from power tracks.** Generally, traces carrying signal currents should run far from others carrying pulsed currents or with fast swinging voltages. Signal ground traces should be connected to the IC signal ground, GND, using a single “star point”, placed close to the IC. Power ground traces should be connected to the IC power ground, GND. The compensation network should be connected to the COMP, maintaining the trace to GND as short as possible. In case of two-layer PCB, it is a good practice to route signal traces on one PCB side and power traces on the other side.
- **Filtering sensitive pins.** Some crucial points of the circuit need or may need filtering. A small high-frequency bypass capacitor to GND might be useful to get a clean bias voltage for the signal part of the IC and protect the IC itself during EFT/ESD tests. A low ESL ceramic capacitor (a few hundreds pF up to 0.1 μ F) should be connected across VCC and GND, placed as close as possible to the IC. With flyback topologies, when the auxiliary winding is used, it is suggested to connect the VCC capacitor on the auxiliary return and then to the main GND using a single track.
- **Keeping power loops as confined as possible.** The area circumscribed by current loops where high pulsed current flow should be minimized to reduce its parasitic self-inductance and the radiated electromagnetic field. As a consequence, the electromagnetic interferences produced by the power supply during the switching are highly reduced. In a flyback converter the most critical loops are: the one including the input bulk capacitor, the power switch, the power transformer, the one including the snubber, the one including the secondary winding, the output rectifier and the output capacitor. In a buck converter the most critical loop is the one including the input bulk capacitor, the power switch, the power inductor, the output capacitor and the free-wheeling diode.
- **Reducing line lengths.** Any wire acts as an antenna. With the very short rise times exhibited by EFT pulses, any antenna can receive high voltage spikes. By reducing line lengths, the level of received radiated energy is reduced, and the resulting spikes from electrostatic discharges are lower. This also keeps both resistive and inductive effects to a minimum. In particular, all traces carrying high currents, especially if pulsed (tracks of the power loops) should be as short and wide as possible.
- **Optimizing track routing.** As levels of pickup from static discharges are likely greater near the edges of the board, it is wise to keep any sensitive lines away from these areas. Input and output lines often need to reach the PCB edge at some stage, but they can be routed away from the edge as soon as possible where applicable. Since vias are to be considered inductive elements, it is recommended to minimize their number in the signal path and avoid them in the power path.
- **Improving thermal dissipation.** An adequate copper area has to be provided under the DRAIN pins as heatsink, while it is not recommended to place large copper areas on the GND.

Figure 44. Recommended routing for flyback converter

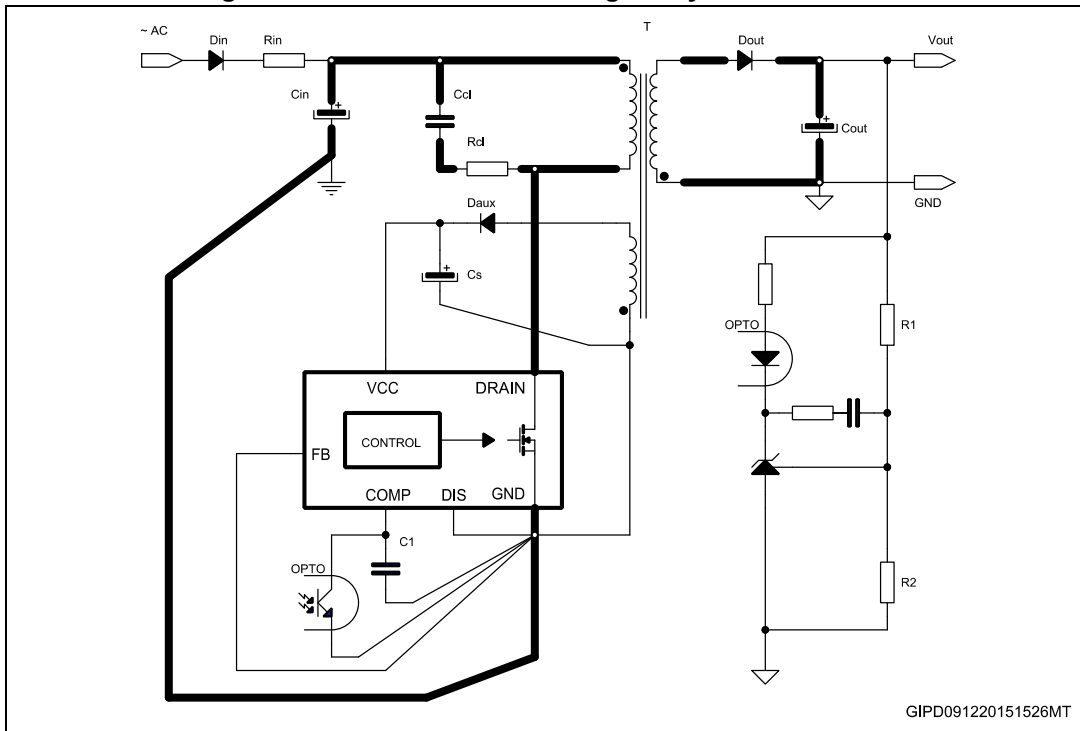
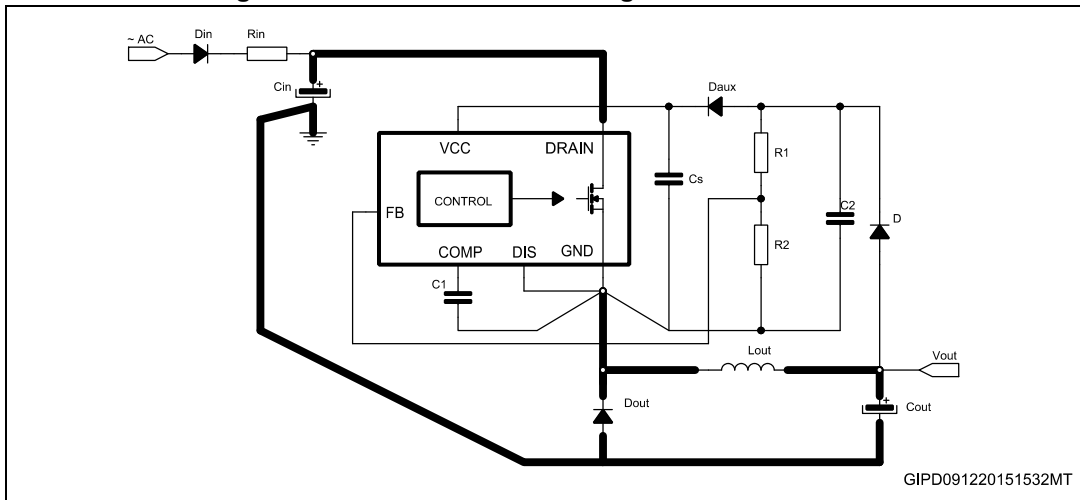


Figure 45. Recommended routing for buck converter



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

6.1 SSOP10 package information

Figure 46. SSOP10 package outline

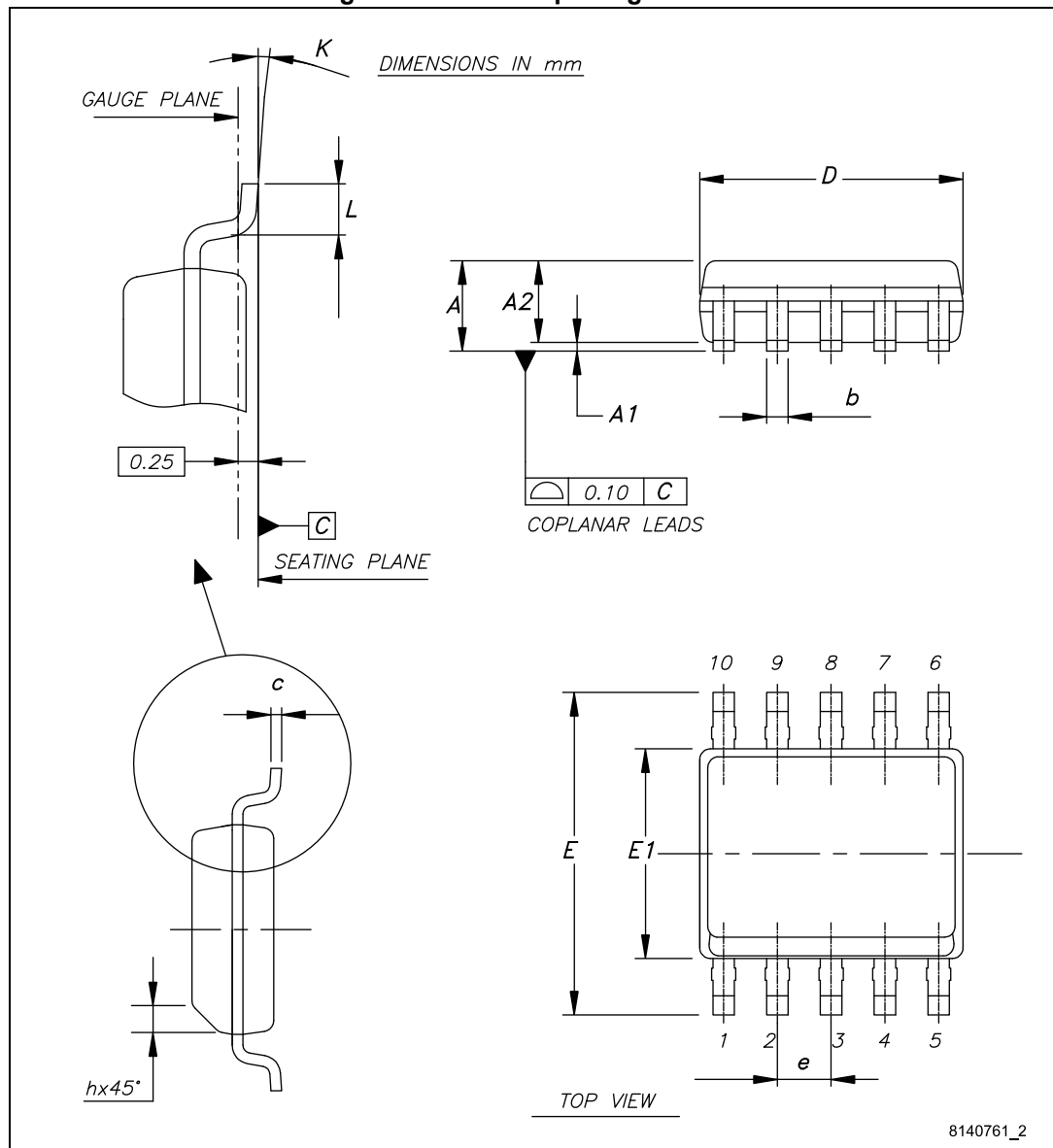
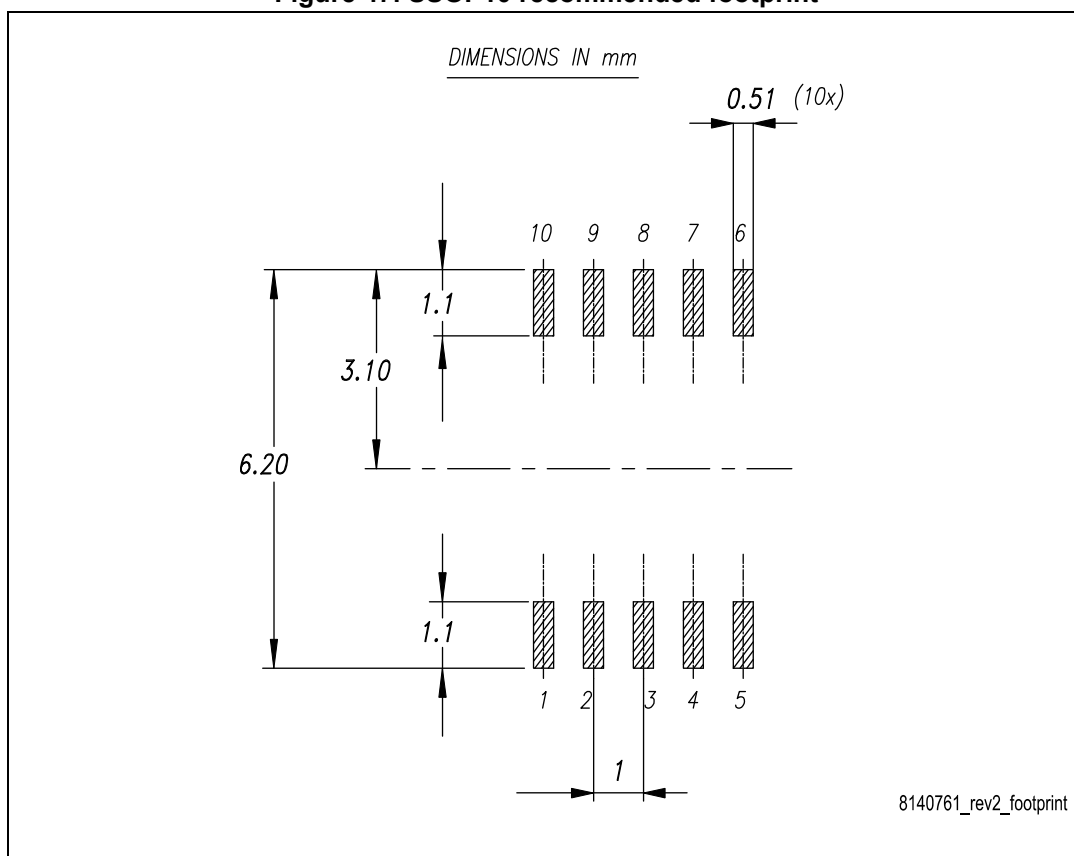


Table 10. SSOP10 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
A2	1.25	-	-
b	0.31	-	0.51
c	0.17	-	0.25
D	4.80	4.90	5
E	5.80	6	6.20
E1	3.80	3.90	4
e	-	1	-
h	0.25	-	0.50
L	0.40	-	0.90
K	0°	-	8°

Figure 47. SSOP10 recommended footprint



7 Ordering information

Table 11. Order code

Order code	I _{DLIM} (OCP)	FOSC ± jitter	Package
VIPER115XSTR	590 mA	30 kHz ± 7%	SSOP10 tape and reel
VIPER114LSTR	480 mA	60 kHz ± 7%	
VIPER115LSTR	590 mA		

8 Revision history

Table 12. Document revision history

Date	Revision	Changes
11-Apr-2018	1	Initial release.
19-Apr-2018	2	Document status changed from preliminary to production data.
14-Dec-2018	3	Updated Table 7 , amended Section 4.15 .

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