Features

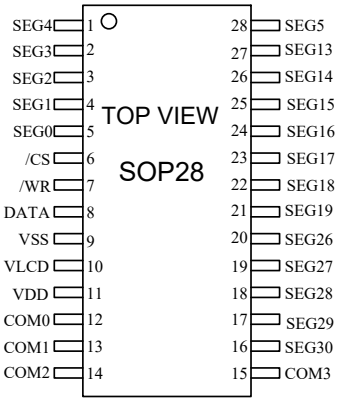
- Operating voltage:2.4-5.2V
- Built-in 256kHz RC oscillator（default）
- Selection of 1/2 or 1/3 bias
- Selection of 1/2 or 1/3 or 1/4 duty
- Built-in 18×4 bit display RAM
- STANDBY mode（by Cmd LCD OFF,SYS DIS）
- 3 wire serial interface
- Software configuration LCD parameters
- Data mode and command mode instructions
- Write address auto increment
- VLCD pin for adjusting LCD operating voltage（≤VDD）
- Package:
  SOP28(300mil)(18.0mm x 7.5mm PP=1.27mm)

1 General Description

VK1072C is a RAM Mapping 18x4 LCD Driver，It can support LCD screens with a maximum of 72 pattern(18SEGx4COM), it is also supports LCD screens of 2COM or 3COM.Only 3 lines are required to communication interface with the VK1072C,it is used to configure display parameters and transfer display data, and can also enter the standby mode through Power down command.

5 Pinouts and pin description

2.1 VK1072C SOP28 Pin Assignment

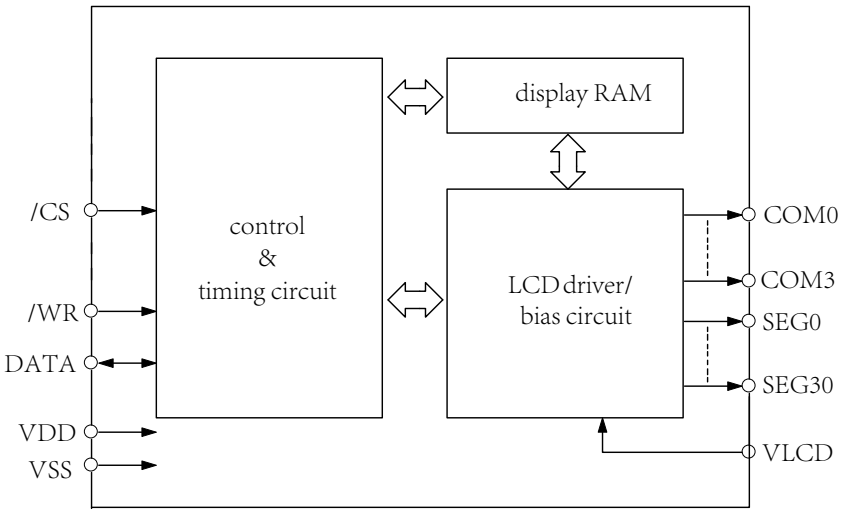


2.2 VK1072C SOP28 Pin Description

No.	Name	I/O	Function
1-5 16-28	SEG4-SEG0 SEG30-SEG13 SEG5	O	LCD SEG outputs
6	/CS	I	Chip selection input with pull-up resistor 1-disabe，0-enable.
7	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
8	DATA	I/O	Serial data input/output with pull-high resistor.
9	VSS	VSS	Negative power supply
10	VLCD	I	LCD power input
11	VDD	VDD	Positive power supply
12-15	COM0-COM3	O	LCD COM outputs

3 Functional Description

3.1 Block diagram



3.2 Display RAM

The static display memory (RAM) is organized into 18×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the WRITE commands.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0		
SEG0					0	地址 6 位（A5----A0）
SEG1					1	
SEG2					2	
SEG3					3	
⋮					⋮	
SEG30					30	
	D3	D2	D1	D0	Data\Addr	

Note:

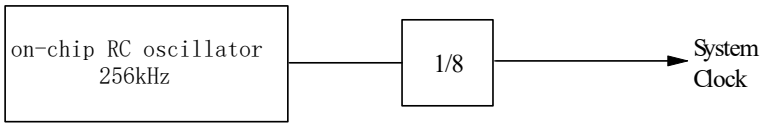
1. When the SEG is not continuous, the display RAM address is also not continuous.
2. When writing multiple data continuously, the display data address is automatically incremented by 1.When SEG is not continuous, write 0 to the empty display RAM address data, until the address automatically adds 1 to the display RAM address where the next SEG is located.

3.3 System Oscillator

The VK1072C system clock is used to generate the time base and LCD driving clock. The source of the clock is from an on-chip RC oscillator (256kHz). After the SYS DIS command is executed, the system clock will stop and the LCD bias generator will turn off,the LCD display will become blank, and the time base lose its function as well.

The LCD OFF command is used to turn the LCD bias generator off. After the LCD OFF command, using the SYS DIS command reduces power consumption, serving as a standby command.

System Oscillator Configuration：



3.4 LCD Driver

The VK1072C is a 72 (18×4) pattern LCD driver. It can be configured as 1/2 or 1/3 bias and 2COM or 3COM or 4COM by the software configuration.

3.4.1 Communication Interfacing

3 lines are required to interface with the VK1072C.

The /CS pin is used to initialize the serial interface circuit and to terminate the communication with HOST.

The DATA pin is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The /WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into the VK1072C on the rising edge of the WR signal.

3.4.2 Command Format

VK1072C can be configured by the Software setting. There are two mode commands to configure the LCD parameters and to transfer the LCD display data,The command mode ID is 100,The data mode WRITE operation ID is 101.

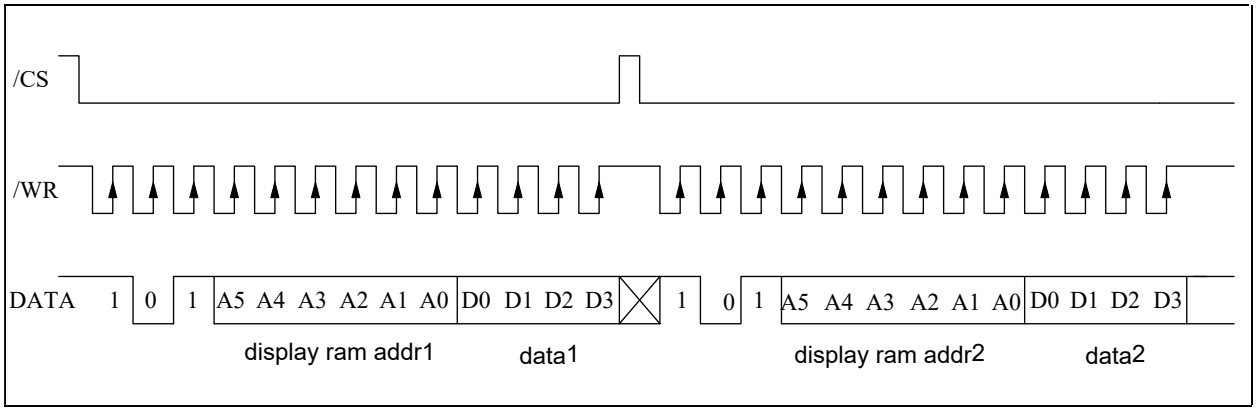
The following are the data mode IDs and the command mode ID:

Operation	MODE	ID
WRITE	DATA	101
COMMAND	COMMAND	100

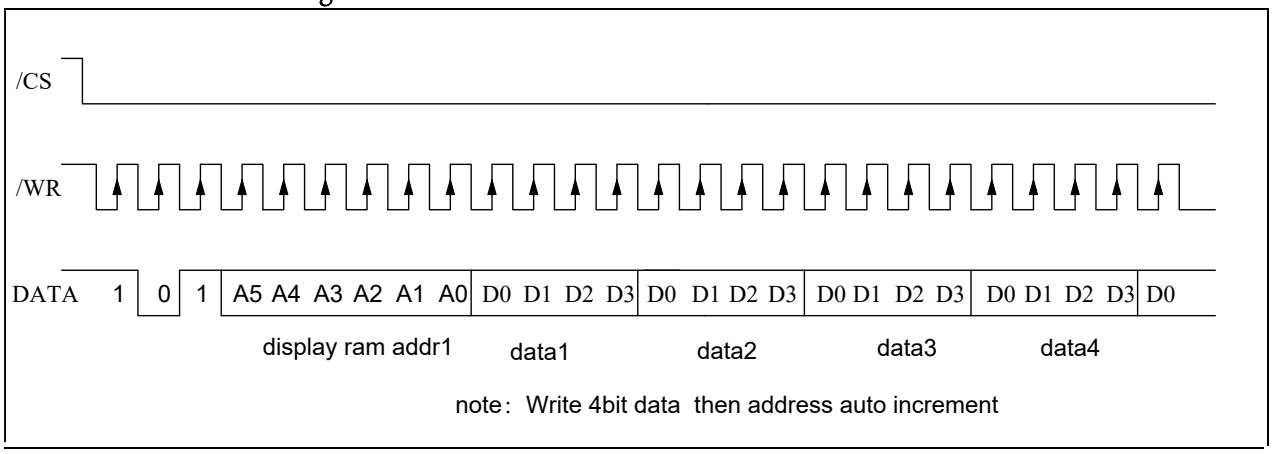
3.4.3 CMD/Data Timing Diagrams

3.4.3.1 WRITE Mode

Command Code : 101

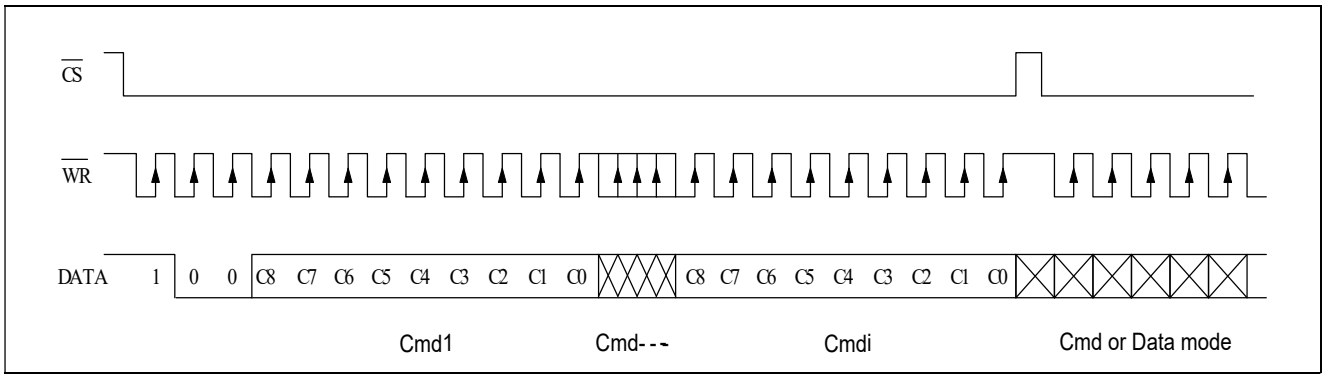


Successive Address Writing



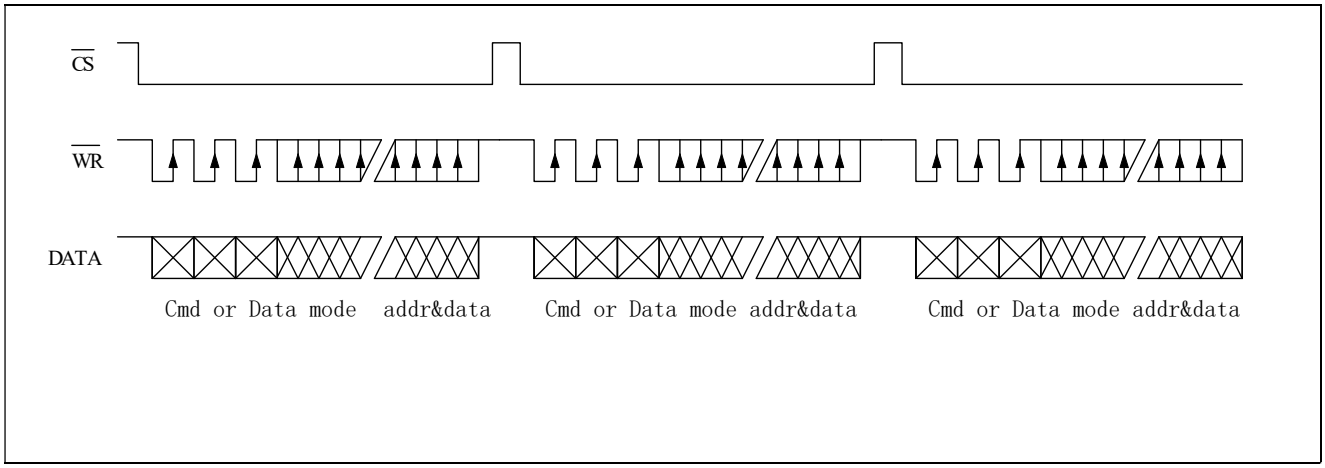
3.4.3.2 Command Mode

Command Code : 100



3.4.3.3 Data and Command Mode

Data and Command Mode



4 Command Summary

Name	ID	Command Code	D/C	Function	Def.
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
SYS DIS	100	0000-0000-X	C	Turn off system oscillator	YES
SYS EN	100	0000-0001-X	C	Turn on system oscillator	
LCD OFF	100	0000-0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000-0011-X	C	Turn on LCD bias generator	
RC 256k	100	0001-10XX-X	C	on-chip RC oscillator	YES
BIAS 1/2	100	0010-abX0-X	C	LCD 1/2 2bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
BIAS 1/3	100	0010-abX1-X	C	LCD 1/3 2bias option ab=00：2 COMS ab=01：3 COMS ab=10：4 COMS	
TEST	100	1110-0000-X	C	Test mode	
NORMAL	100	1110-0011-X	C	Normal mode YES	YES

Note: X: 0 or1

A5-A0: DIspaly RAM addresses

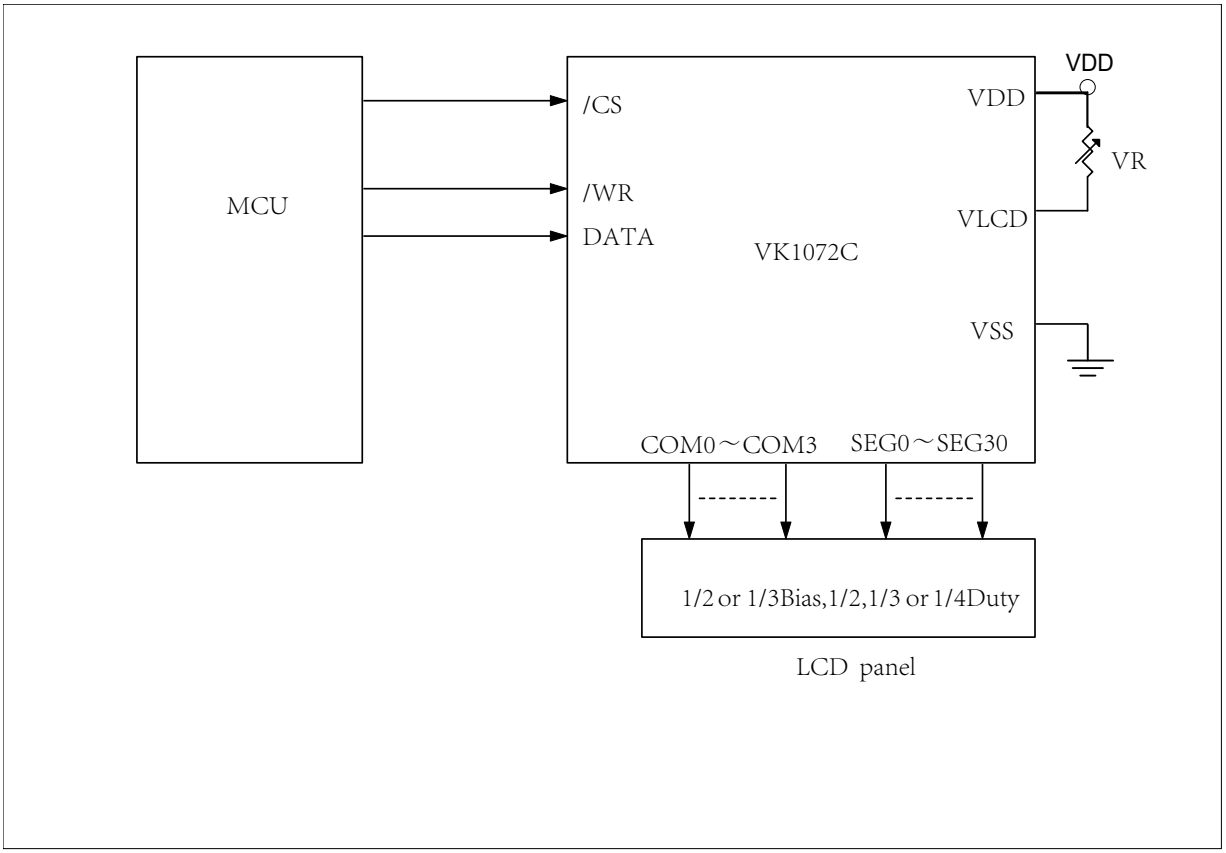
D3-D0: 4bit DIspaly RAM data

D/C： Data/Command mode

Def.:Power on reset default

101 and 100 is Command ID

5 Application Circuits



Note: Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

6 Electrical characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	VSS-0.3～VDD+0.3	V
Storage Temperature	TSTG	-50～+125	℃
Operating Temperature	TOTG	-40～+85	℃

6.2 DC Characteristics

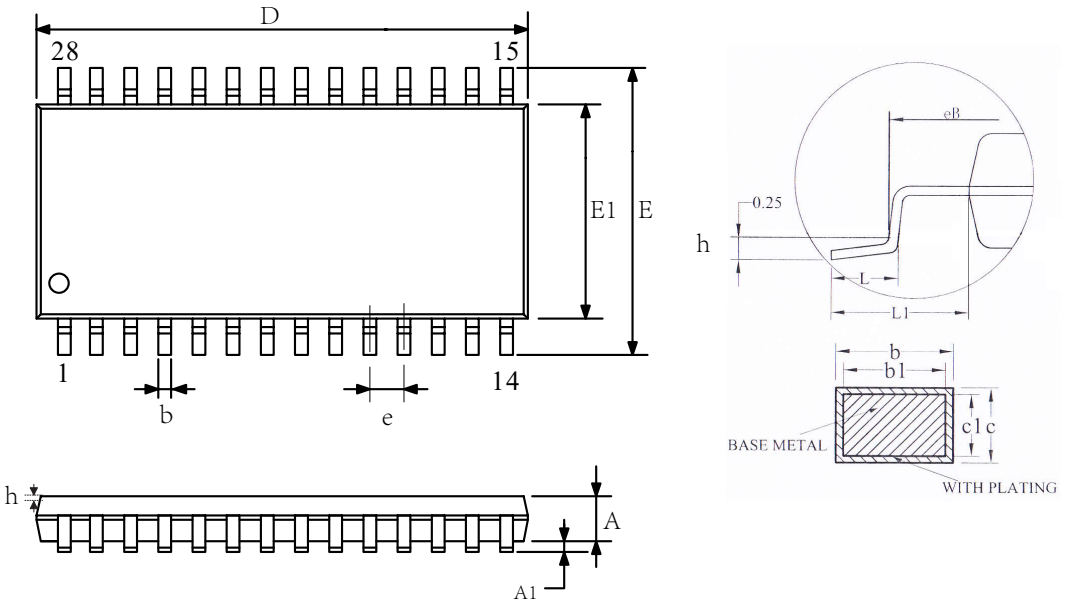
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Standby current	I_{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Input Low Voltage	V_{IL}	0	—	0.6	V	3V	DATA, /WR, /CS
		0	—	1.0		5V	
Input High Voltage	V_{IH}	2.4	—	3.0	V	3V	DATA, /WR, /CS
		4.0	—	5.0		5V	
DATA	I_{OL1}	0.5	1.2	—	mA	3V	V_{OL}=0.3V
		1.3	2.6	—		5V	V_{OL}=0.5V
DATA	I_{OH1}	-0.4	-0.8	—	mA	3V	V_{OH}=2.7V
		-0.9	-1.8	—		5V	V_{OH}=4.5V
LCD COM Sink Current	I_{OL2}	80	150	—	μA	3V	V_{OL}=0.3V
		150	250	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH2}	-80	-120	—	μA	3V	V_{OH}=2.7V
		-120	-200	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL3}	60	120	—	μA	3V	V_{OL}=0.3V
		120	200	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH3}	-40	-70	—	μA	3V	V_{OH}=2.7V
		-70	-100	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{UP}	40	80	150	kΩ	3V	DATA, /WR, /CS
		30	60	100		5V	

6.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	—	256	—	kHz	3V	On-chip RC oscillator
		—	256	—		5V	On-chip RC oscillator
LCD Clock	f_{LCD1}	—	f_{SYS1}/1024	—			On-chip RC oscillator
LCD Common Period	t_{COM}	—	n/ f_{LCD}	—	sec	—	N： Number of COM
Serial Data Clock （/WR）	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		6.67	—	—			Read mode
		1.67	—	—	μs	5V	Write mode
		3.34	—	—			Read mode
Rise/Fall Time Serial Data Clock Width	t_r， t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

7 Package Information

7.1 SOP28 (300mil) (18mm x 7.5mm PP=1.27mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	2.65
A1	0.10	--	0.30
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.25	--	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.30	--	0.50
L	0.70	--	1.00
L1	1.40REF		

8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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