Features

- Operating voltage 3.0-5.5V
- Built-in RC oscillator
- Max. 12 SEG and 8 GRID(Number of SEG pins in different packages)
- SEG pins connect to LED Anode , GRID pins connect to LED Cathode
- I2C bus interface,I2C slave address can be configured through IO pins
- 16-level brightness control
- Max. 10 × 3 key scan
  Key display multiplexing requires hardware circuit
  Supporting combination keys requires circuit
- Read/Write address auto increment
- Dispaly mode 12x8
- Power-On Reset(POR)
- Versatile blinking modes
- Standby mode
- High driving current, suitable for highlighted applications

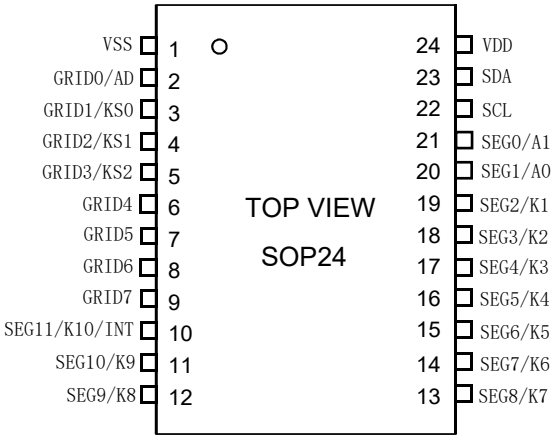
- Package:
  SOP24(300mil)(15.40mm x 7.50mm PP=1.27mm)·

1 General Description

The VK16K33B is a memory mapping and multi-function LED controller driver. The max. Display segment numbers in the device is 96 patterns (12 SEG x 8 GRID) with a 10×3 (MAX.) matrix key scan circuit. The software configuration features of the VK16K33B makes it suitable for multiple LED applications including LED modules and display subsystems. The device communicates with host microcontrollers via a two-line bidirectional I2C bus,it is used to configure display parameters and transfer display data, and can also enter the standby mode through System Set Command .

2 Pinouts and pin description

2.1 VK16K33B SOP24 Pin Assignment



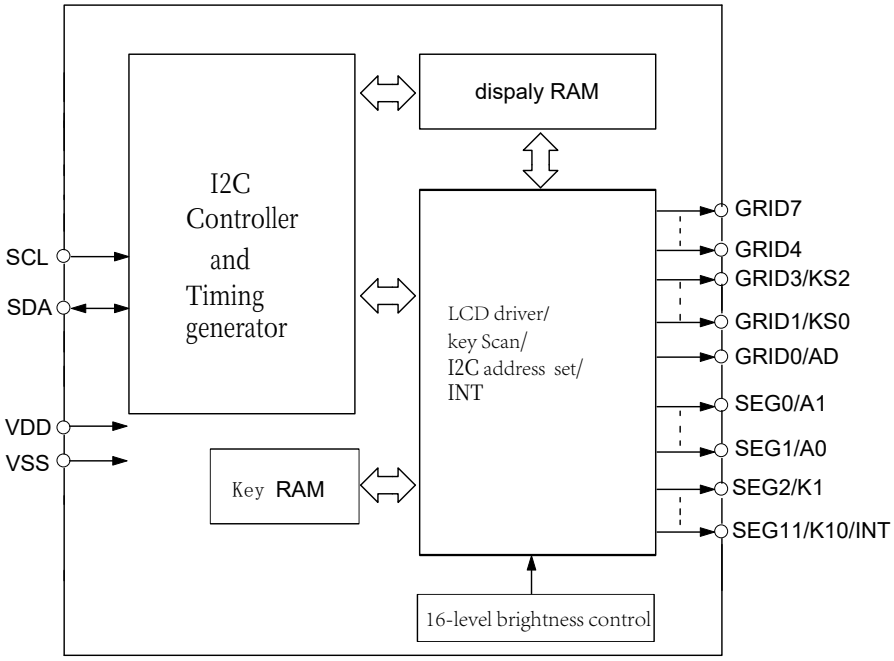
2.2 VK16K33B SOP24 Pin Description

No.	Name	I/O	Function
1	VSS	VSS	Negative power supply
2	GRID0/AD	O	LED GRID outputs（N-MOS open drain） I2C slave address source output pin, active high during power on and key scan *1
3-5	GRID1/KS0- GRID3/KS2	O	LED GRID outputs（N-MOS open drain）； Key source output pin, active high during key scan operation
6~9	GRID4 ~GRID7	O	LED GRID outputs（N-MOS open drain）
11-19	SEG10/K9- SEG2/K1	I/O	LED SEG outputs（P-MOS open drain）； Key data input pin, internal pull-low during key scan operation
20-21	SEG1/A0- SEG0/A1	I/O	LED SEG outputs（P-MOS open drain） I2C slave address setting pin, 4 address 0xe0-0xe3 can be set, and bit0 is the read / write bit. *1
22	SCL	O	Serial Clock Input for I2C interface
23	SDA	I/O	Serial Data Input/Output for I2C interface
24	VDD	VDD	Positive power supply
10	SEG11/K10 /INT	I/O	I. when bit0 of SEG / INT register is set to “0”,this pin is LED SEG output（P-MOS open drain）and Key data input during key scan operation. II. when bit0 of SEG / INT register is set to “1”,this pin is Interrupt signal (INT) output pin bit1 of SEG/INT register is set to “0”,INT pin output active-low bit1 of SEG/INT register is set to “1”,INT pin output active-high

*1 I2C slave address is updated during power on reset or key scanning cycle.

3 Functional Description

3.1 Block diagram



3.2 Power-On Reset

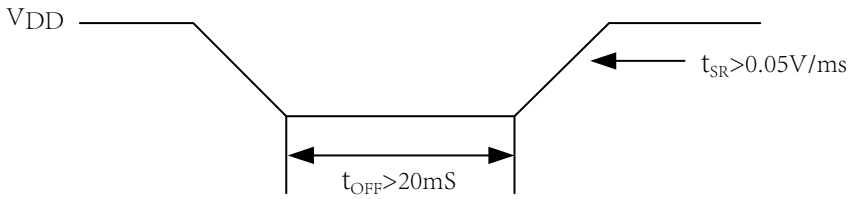
When the power is applied, the device is initialized by an internal power-on reset circuit. Data transfers on the I2C bus should be avoided for 1 ms following power-on.

The status of the internal circuits after initialization is as follows:

- System Oscillator is off state
- GRID0~GRID3 outputs are set to VDD.
- GRID4~GRID7 outputs are set to high impedance.
- all SEG pins are set to input.
- LED Display Off.
- Key scan stopped.
- SEG/INT pin is set to SEG.
- brightness is set to 16/16 duty。

if VDD drops below the minimum voltage of operating voltage specification during operation, the power-on reset timing conditions must be also satisfied. This means that VDD must fall to 0V and remain at 0V for a minimum time of 20ms before rising to the normal operating voltage.

Power-on Reset Timing



3.3 Standby Mode & Wake-up

Standby Mode

In the standby mode, the VK16K33B can not accept input commands nor write data to the display RAM except using the system setup command.

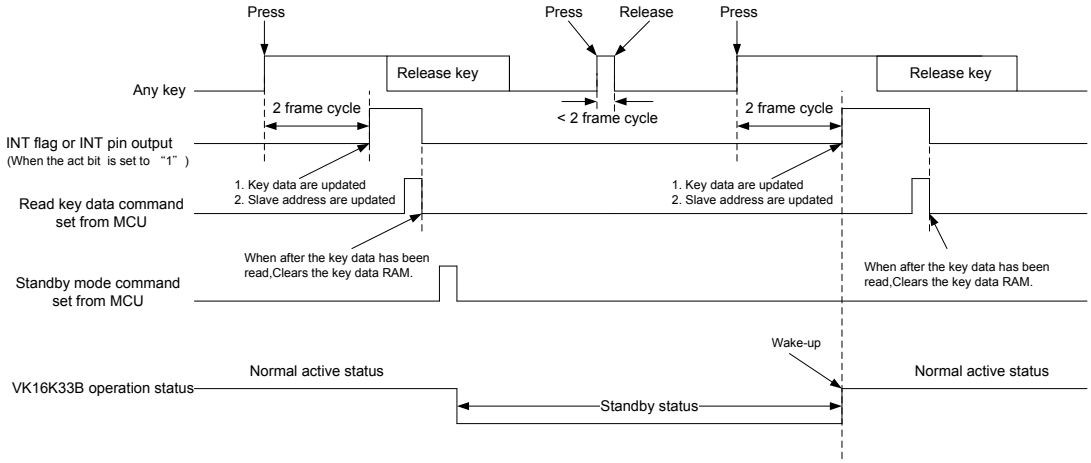
If the standby mode is selected with the bit0 of the System Set Command set to "0", the status of the standby model is as follows:

- System Oscillator is off state
- GRID0~GRID3 outputs are set to VDD.
- GRID4~GRID7 outputs are set to high impedance.
- all SEG pins are set to input.
- LED Display Off.
- Key scan stopped.
- All key data and INT flags are cleared until the standby mode is canceled.
- If any key is pressed or the bit0 of the System Set Command is set to "1", the standby mode will be canceled and will cause the device to wake-up.
- If the bit0 of the SEG/INT register is set to "0", all SEG pins are changed to input pins.
- If the bit0 of the SEG/INT register is set to "1": all SEG pins are changed to input pins except for the INT pin (output).
- The INT pin output remain at a high level when the bit 1of the SEG/INT register is set to "0".
- The INT pin output remain at a low level when the bit1 of the SEG/INT register is set to "1".

Wake-up

- Wake-up by any key or by set the bit0 of the System Set Command to "1". A key scan will then be performed.
- The System Oscillator restarts for normal operation.
- The previous display data output will be updated by Each Mode command set.

The relationship between the Wake-up and any key press is shown as follows:



3.4 Display RAM

The static display memory (RAM) is organized into 16×8 bits and stores the displayed data.The contents of the RAM are directly mapped to the contents of the LCD driver. Display address is 0x00-0x0F,the RAM size is 16 bytes.If you want to lighted on or off an LED, only set or clear the corresponding display RAM bit to 1 or 0,For example, if LED1 driven by SEG0 pin and GRID1 pin is on or off, only set bit0 to 1 or 0 of the corresponding display RAM (0x00).The ram bit corresponding to the unused SEG pin is cleared to 0.

The following is a mapping from the RAM to the LED pattern:

SEG / GRID					SEG11	SEG10	SEG9	SEG8	Addr	SEG7	SEG6	SEG5	SEG4	SEG3	SEG2	SEG1	SEG0	Addr	SEG / GRID
GRID0									0x01								LED1	0x00	GRID0
GRID1									0x03									0x02	GRID1
GRID2									0x05									0x04	GRID2
GRID3									0x07									0x06	GRID3
⋮									⋮									⋮	⋮
GRID7									0x0F									0x0E	GRID7
	D7	D6	D5	D4	D3	D2	D1	D0		D7	D6	D5	D4	D3	D2	D1	D0		

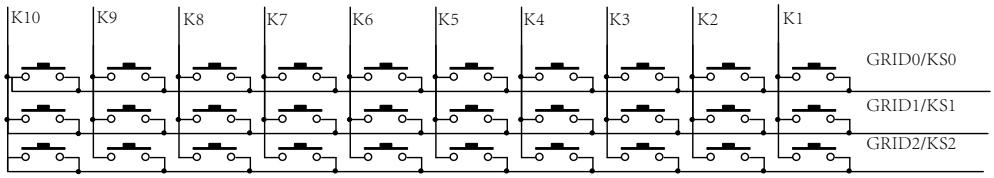
Note:

At the initial system power on, the value stored in the chip display RAM may be random. It is recommended to clear the display RAM after power on, write 0x00 to the all display RAM (0x00-0x0f).

SEG pins connect to LED Anode, GRID pins connect to LED Cathode, Reverse connection is not allowed.

3.5 Keyscan

3.5.1 Key data reading



The key scanning is automatically completed by the hardware, only needs to read the key value through I2C. When a key is pressed, INT interrupt is generated. This interrupt flag can be read through I2C or output throughINT pin (open drain output).The keyscan cycle loops continuously over time, with all 30 keys(10x3) experiencing a full keyscanning debounce over 20ms.A key press is debounced and an interrupt issued if at least one key that was not pressed in a previous cycle is found to be pressed during both sampling periods.The keyscan circuit detects any combination of keys pressed during each debounce cycle (n-key rollover).

When after all the key data has been read that clears the key data RAM and the int flag bit is set to “0”, If the SEG / intINT pin is set to INT output, the INT pin returns to the level when no key is pressed.

INT flag Register:

INT Register address	INTflag								Function
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	key press flag
0x60	INT flag	INT flag	INT flag	INT flag	INT flag	INT flag	INT flag	INT flag	bit7-bit0 set 1when key press,when all key read clear 0.

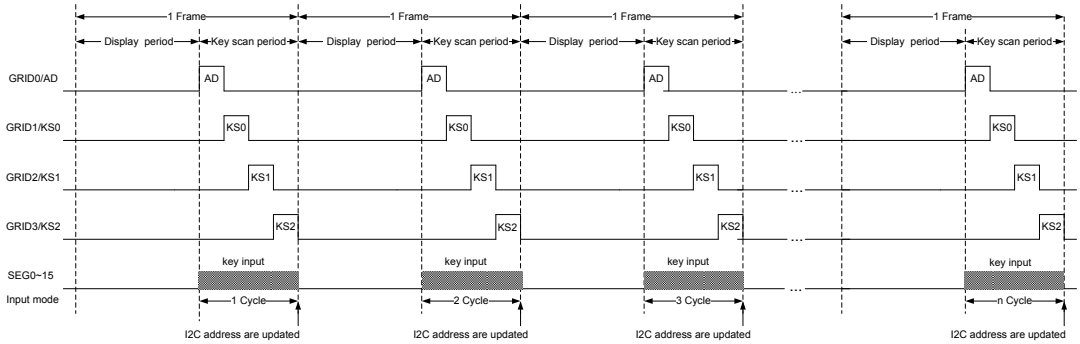
The following shows the mapping from the RAM to the key data output:

key RAM addr	key data							
	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0x40	KS0/K8	KS0/K7	KS0/K6	KS0/K5	KS0/K4	KS0/K3	KS0/K2	KS0/K1
0x41	0	0	0	0	0	0	KS0/K10	KS0/K9
0x42	KS1/K8	KS1/K7	KS1/K6	KS1/K5	KS1/K4	KS1/K3	KS1/K2	KS1/K1
0x43	0	0	0	0	0	0	KS1/K10	KS1/K9
0x44	KS2/K8	KS2/K7	KS2/K6	KS2/K5	KS2/K4	KS2K3	KS2/K2	KS2/K1
0x45	0	0	0	0	0	0	KS2/K10	KS2/K9

Note: It is recommended that the key data RAM is read only and should be started form address 0x40 only, the key data RAM of address 0X40~0X45 should be read continuously and in one operation.

3.5.2 Keyscan Timing

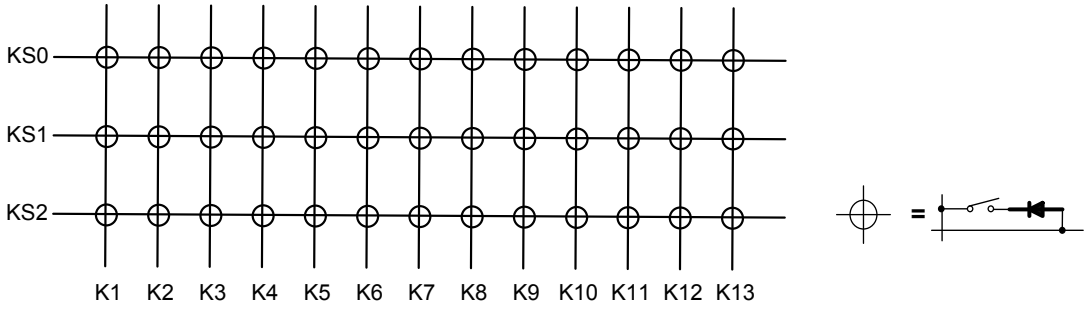
keyscan timing as shown:



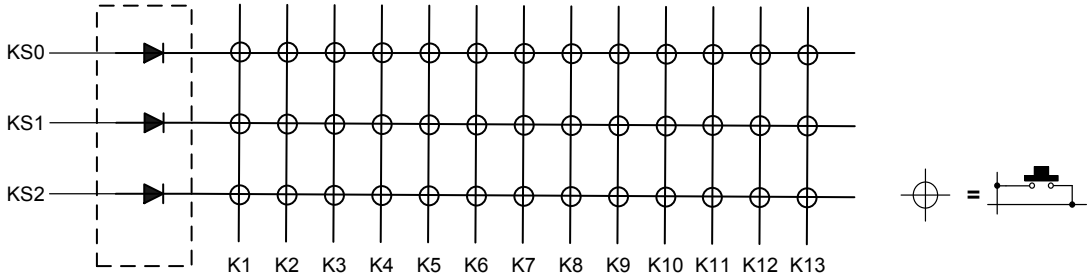
Note: The Slave addresses are updated on the keyscan timing

3.5.3 Key Combination

When pressing three or more times is assumed,each combination key is required to connect diodes in series,shown as below :



When pressing twice is assumed,KS0-KS2 is required to connect diodes in series,shown as below:



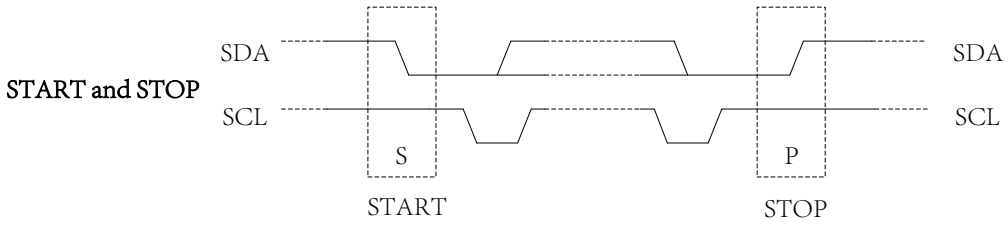
Note： In this circuit, pressing three or more times may cause the OFF switches to be determined as being ON.

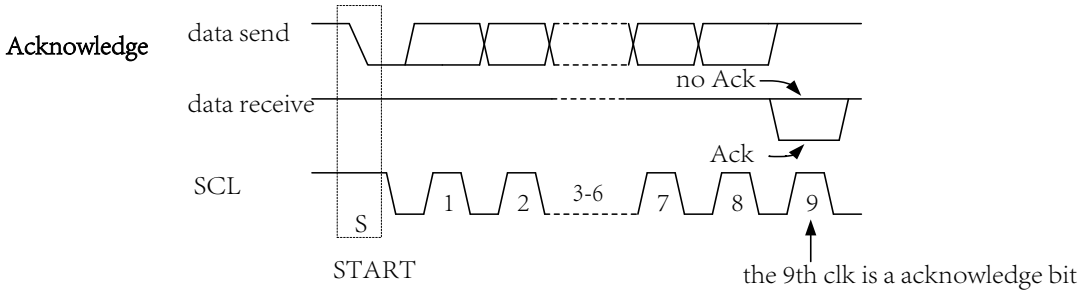
3.6 Communication Command

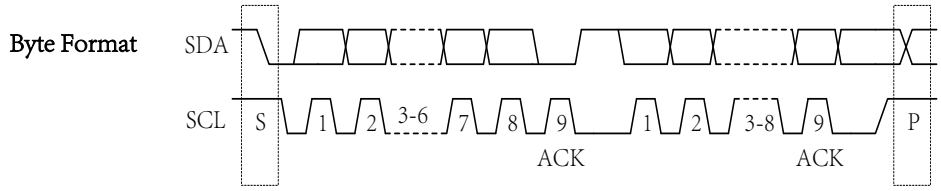
3.6.1 I2C Serial Interface

The device supports I2C serial interface.

The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7k. When the bus is free, both lines are high.



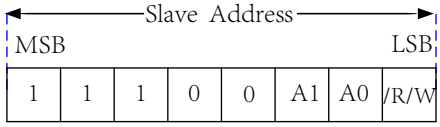




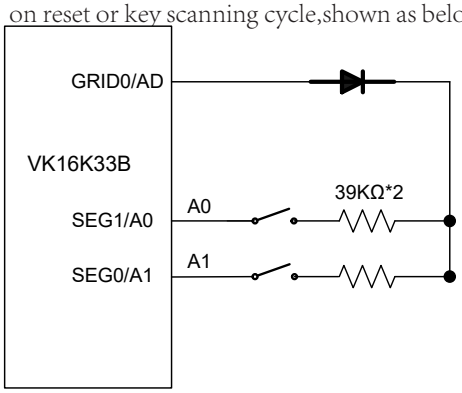
3.6.. I2C Address set

Slave Address

（0xE0-0xEE）bit0-R/W



I2C slave address is selected through A2-A0 pins, and I2C slave address is updated during power on reset or key scanning cycle,shown as below：

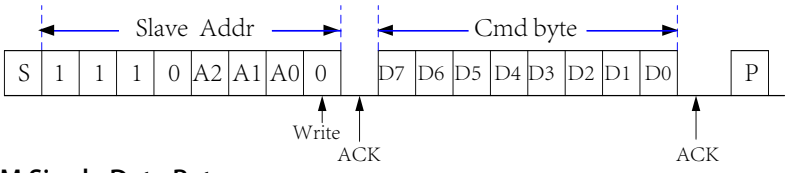


Note：A1-A0 float is 0，connect is 1，when all float the device address is 0xE0

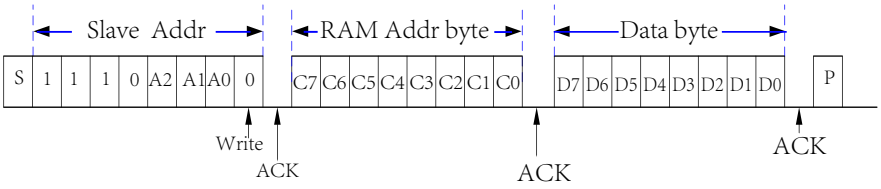
3.6.3 I2C Command Format

3.6.3.1 Write Operation

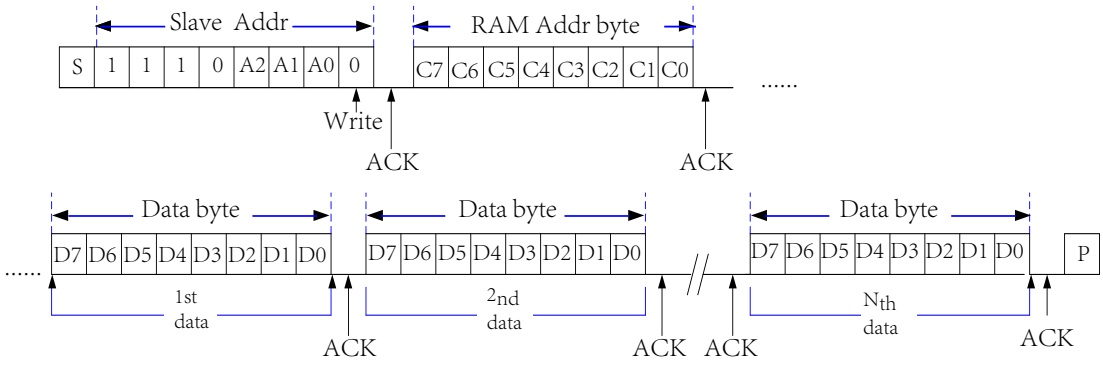
Write Command



Display RAM Single Data Byte

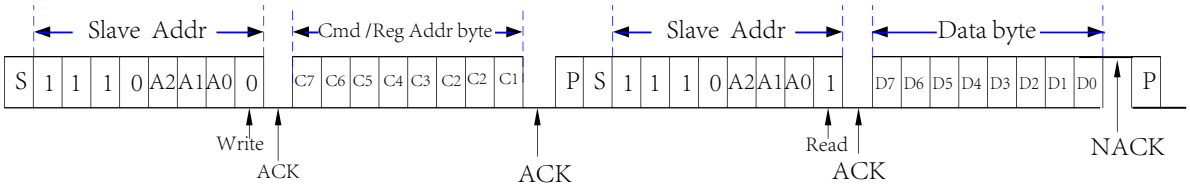


Display RAM Page Write Operation

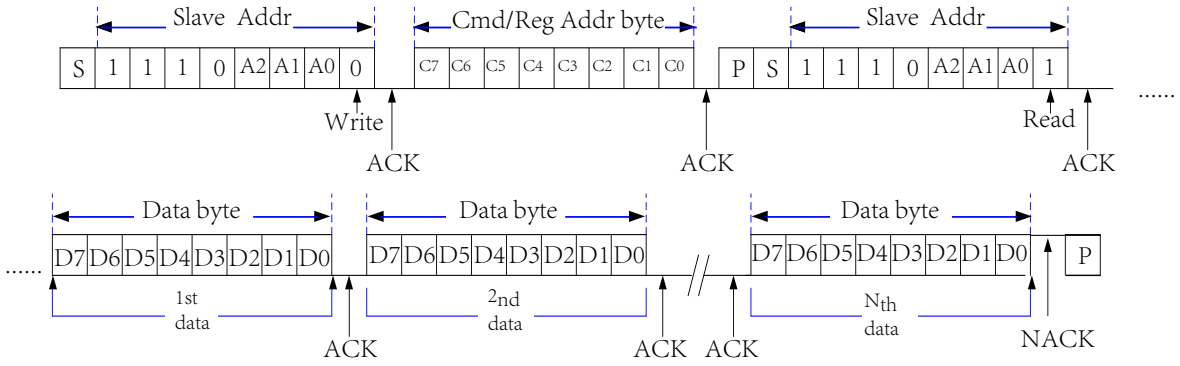


3.6.2.2 Read Operation

Reading a data byte is not applicable to reading the key value.



Read n bytes data. The address pointer will auto-increase after received ACK. When reading the key, read 6 data continuously from start address 0x40.



3.6.6 Command Summary

3.6.4.1 System Set Command

This command is used to set the work mode: Normal mode or Standby mode.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note	Def
0	0	1	0	X	X	X	0	system oscillator ON/OFF	Standby mode(OSC off)	0x20
0	0	1	0				1		Normal mode(OSC on)	

3.6.4.2 Display Set Command

This command is used to set the LED Display on/off and Blink Frequency.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note	Def
1	0	0	0	X			0	Display On/Off	Off	0x80
1	0	0	0				1		On	
1	0	0	0		0	0		Blink Frequency	blink off	0x80
1	0	0	0		0	1			2Hz	
1	0	0	0	X	1	0			1Hz	
1	0	0	0		1	1			0.5Hz	

3.6.4.3 SEG/INT pin Set Command

This command is used to set the INT / SEG pin output function.

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note	Def
1	0	1	0	X	X	0	0	INT/SEG pin function select and INT pin out level	SEG pin	0xA0
1	0	1	0			0	1		INT pin,active low.	
1	0	1	0			1	1		INT pin,active high.	

3.6.4.3 Display Address Set Command

Set the address of the Display RAM (0x00 - 0x0f). When powered on, the address is set to 0x00(default).

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	DisplayRAM Addr
0	0	0	0	0	0	0	0	0x00
0	0	0	0	0	0	0	1	0x01
0	0	0	0	0	0	1	0	0x02
0	0	0	0	0	0	1	1	0x03
0	0	0	0	0	1	0	0	0x04
0	0	0	0	0	1	0	1	0x05
0	0	0	0	0	1	1	0	0x06
0	0	0	0	0	1	1	1	0x07
0	0	0	0	1	0	0	0	0x08
0	0	0	0	1	0	0	1	0x09
0	0	0	0	1	0	1	0	0x0A
0	0	0	0	1	0	1	1	0x0B
0	0	0	0	1	1	0	0	0x0C
0	0	0	0	1	1	0	1	0x0D
0	0	0	0	1	1	0	1	0x0E
0	0	0	0	1	1	1	1	0x0F

3.6.4.5 Display brightness Set Command

Set the Display brightness (level 16).

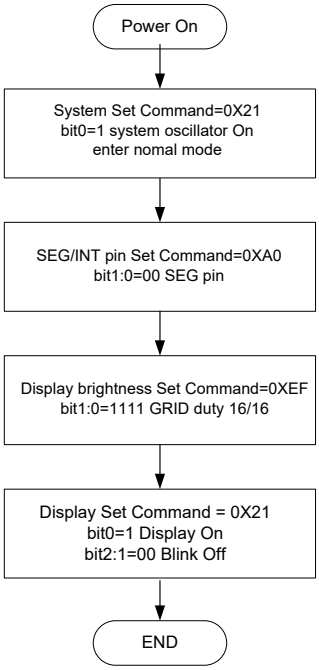
bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Function	Note
1	1	1	0	0	0	0	0	Set GRID Pulse Width	1/16 duty
1	1	1	0	0	0	0	1		2/16 duty
1	1	1	0	0	0	1	0		3/16 duty
1	1	1	0	0	0	1	1		4/16 duty
1	1	1	0	0	1	0	0		5/16 duty
1	1	1	0	0	1	0	1		6/16 duty
1	1	1	0	0	1	1	0		7/16 duty
1	1	1	0	0	1	1	1		8/16 duty
1	1	1	0	1	0	0	0		9/16 duty
1	1	1	0	1	0	0	1		10/16 duty
1	1	1	0	1	0	1	0		11/16 duty
1	1	1	0	1	0	1	1		12/16 duty
1	1	1	0	1	1	0	0		13/16 duty
1	1	1	0	1	1	0	1		14/16 duty
1	1	1	0	1	1	1	0		15/16 duty
1	1	1	0	1	1	1	1		16/16 duty

3.7 Command application

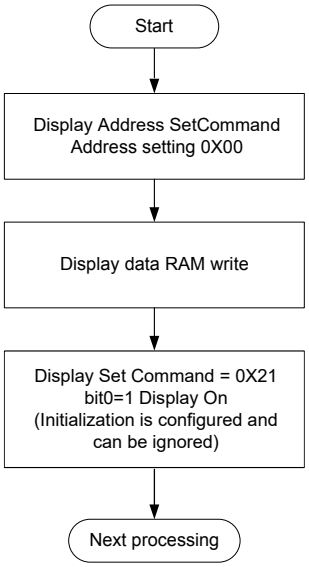
3.7.1 Initialize configuration

During power on, the power on reset sequence shall be met. After power on, the parameters shall be configured first.

Config parameters through a series of commands. The command sequence is as follows:

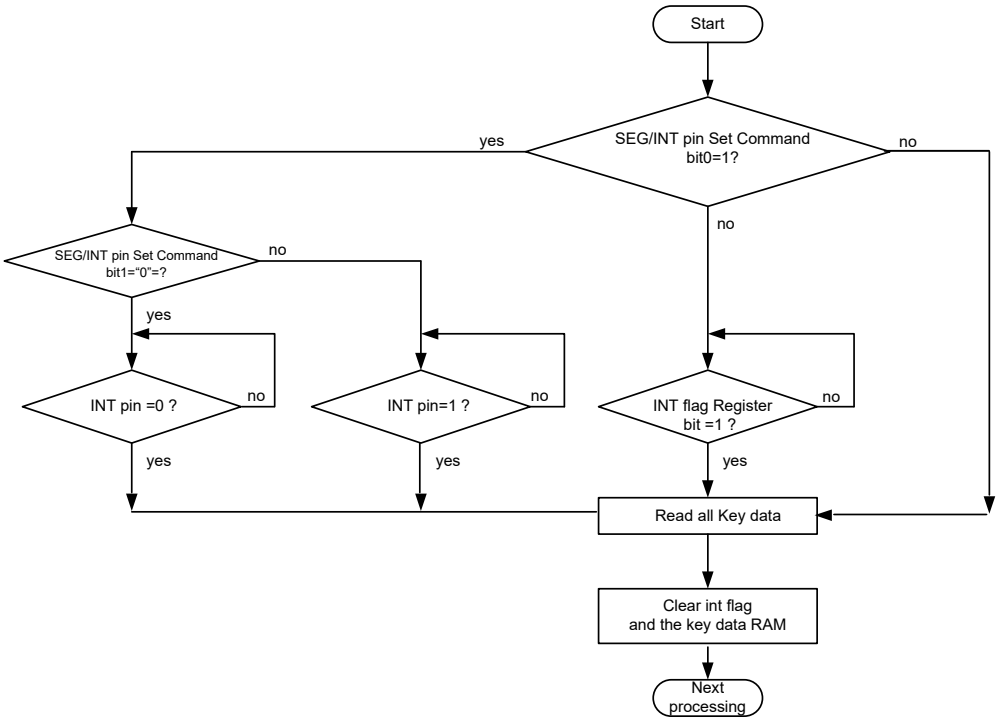


3.7.2 Display data Read Command

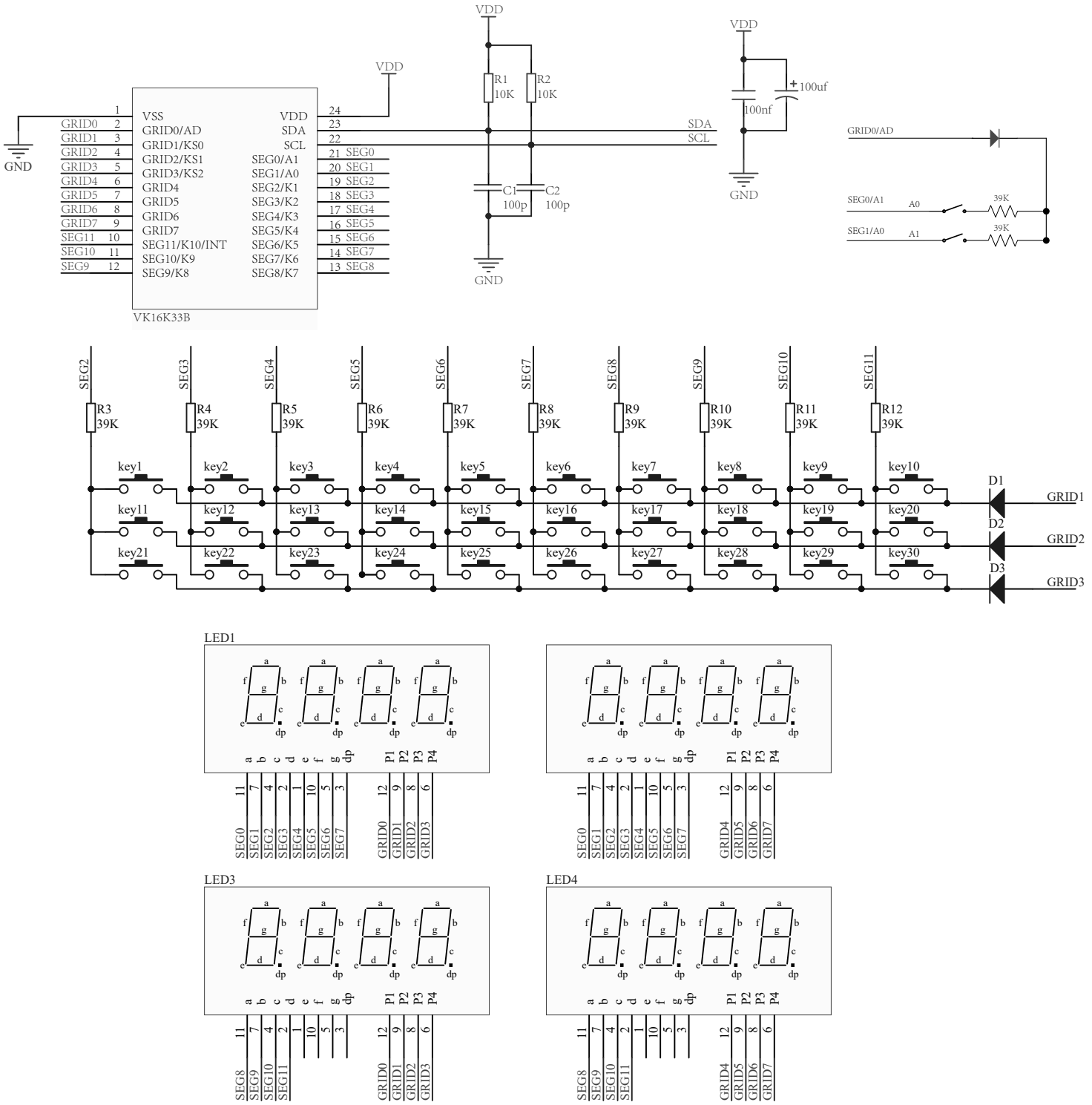


3.7.3 Key Read Command

It is recommended that the key data RAM is read only and should be started form address 0X40 only, the key data RAM of address 0X40~0X45 should be read continuously and in one operation.



4 Application Circuits



5 Electrical characteristics

5.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	VSS-0.3V to VSS+6.5	V
Input Voltage	VIN	VSS-0.3V to VDD+0.3	V
Storage Temperature	TSTG	-50～+120	℃
Operating Temperature	TOTG	-40～+85	℃

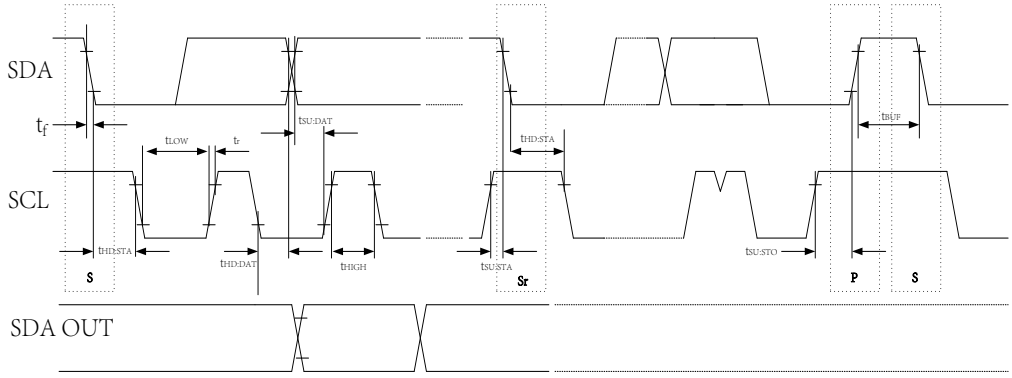
5.2 DC Characteristics

Symbol	Item	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
V_{DD}	Operating voltage	3.0	5	5.5	V	-	-
I_{DD}	Operating current	-	1	2	mA	5	No load, normal mode SEG/INT pin set 0
I_{STB}	Standby Current	-	1	10	μA	5	No load, standby mode
V_{IH}	Input High Voltage	$0.7V_{DD}$	-	V_{DD}	V	5	SDA,SCL
V_{IL}	Input Low Voltage	0	-	$0.3V_{DD}$	V	5	SDA,SCL
I_{IL}	Input leakage current	-1	-	μ1A		-	V_{IN} = V_{SS} 或 V_{DD}
R_{PL}	Input pull-down resistor	250		-	KΩ	5	SEG3/K1~SEG15/K13, SEG0/A2~SEG2/A0 Key scan period
I_{OL1}	Low level output current	6	-	-	mA	5	V_{OL}=0.4V; SDA
I_{OL2}	SEG Sink Current	6	-	-	mA	5	V_{OL}=0.4V,INT pin
I_{OH1}	SEG Source Current	-20	-25	-40	mA	5	V_{OH}=V_{DD}-2V,(SEG0~SEG15)
		-25	-30	-50	mA		V_{OH}=V_{DD}-3V,(SEG0~SEG15)
I_{TOLSEG}	High level output current tolerance	-	-	5	%	5	V_{OH}=V_{DD}-3V,(SEG0~SEG15)
I_{OL3}	GRID Sink Current	160	200	-	mA	5	V_{OL}=0.3V,(GRID0~GRID7 pin)
I_{OH2}	GRID Source Current	-20	-25	-40	mA	5	V_{OH}= V_{DD}-2V, (GRID0~GRID3 pin)

5.3 AC Characteristics

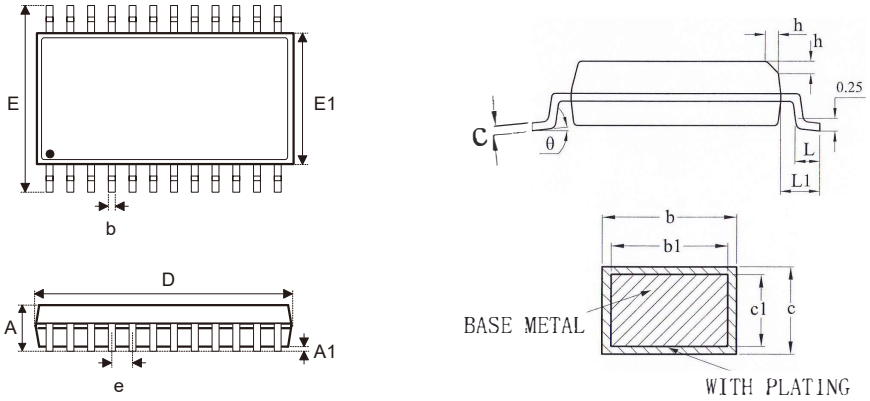
Symbol	Item	Min.	Max.	Unit	Test Conditions
					Conditions
f_{SCL}	Clock Frequency	-	400	kHZ	—
t_{BUF}	Bus Free Time	1.3	-	μs	Time in which the bus must be free before a new transmission can start
$t_{HD;STA}$	Start Condition Hold Time	0.6	-	μs	After this period, the first clock pulse is generated
t_{LOW}	SCL Low Time	1.3	-	μs	—
t_{HIGH}	SCL High Time	0.6	-	μs	—
$t_{SU;STA}$	Start Condition Setup Time	0.6	-	μs	Only relevant for repeated START condition
$t_{HD;DAT}$	Data Hold Time	0	-	μs	—
$t_{SU;DAT}$	Data Setup Time	100	-	ns	—
t_r	Rising Time	-	0.3	μs	periodically sampled
t_f	Falling Time	-	0.3	μs	periodically sampled
$t_{SU;STO}$	Stop Condition Setup Time	0.6	-	μs	—
tAA	Output Valid from Clock	-	0.9	μs	—
t_{SP}	Input Filter Time Constant (SDA and SCL pin)	-	50	ns	Noise suppression time

I²C Timing



6 Package Information

6.1 SOP24 (300mil) (15.40mm x 7.5mm PP=1.27mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	2.64
A1	0.10	0.20	0.30
b	0.39	--	0.47
b1	0.38	0.41	0.44
c	0.25	--	0.29
c1	0.24	0.25	0.26
D	15.30	15.40	15.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	--	0.75
L	0.70	--	1.00
L1	1.40REF		

7 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2019-07-11	Add Ref circuits	Yes
3	1.2	2020-02-11	Update content	Yes

Disclaimers

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