

## Features

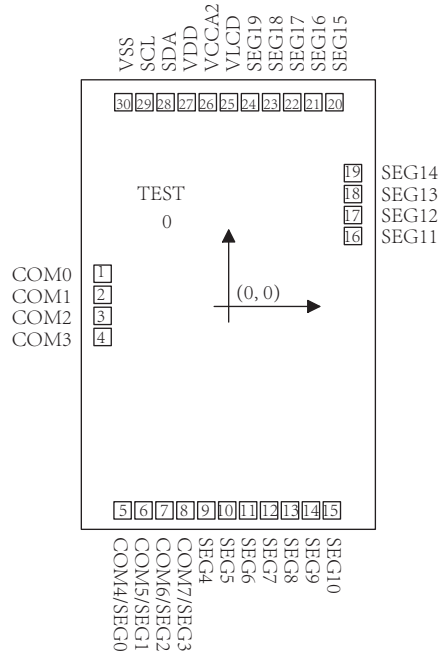
- Operating voltage:2.4-5.5V
- Built-in 32kHz RC oscillator
- Selection of 1/3 or 1/4 bias
- Selection of 1/4 or 1/8 duty
- Built-in 20x4、16x8 bit display RAM
- Selection of 80Hz or 160Hz Frame Frequency
- STANDBY mode ( by System Set Command LCD OFF, SYS oscillator OFF)
- I2C bus interface
- Display mode 20x4、16x8
- Versatile blinking modes
- Software configuration LCD parameters
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage ( VDD )
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Power-On Reset(POR)
- Low power consumption、High anti-interference
  
- Package:
  - SOP20 (300mil) (12.8mm x 7.5mm PP=1.27mm)
  - SOP24 (300mil) (15.4mm x 7.5mm PP=1.27mm)
  - SOP28 (300mil) (18.0mm x 7.5mm PP=1.27mm)
  - NSOP16 (150mil) (9.9mm x 3.9mm PP=1.27mm)
  - DICE
  - COG

## 1 General Description

VK2C21 is a RAM Mapping LCD Driver, It can support LCD screens with a maximum of 80 pattern(20SEGx4COM) or a maximum of 128 pattern(16SEGx8COM) .The device communicates with host microcontrollers via a two-line bidirectional I2C bus,it is used to configure display parameters and transfer display data,, and can also enter the standby mode through System Set Command .With the characteristics of high anti-interference and low power consumption, it is suitable for water electrical meters and industrial control instruments.

## 2 COB PAD description and Coordinates

### 2.1 COB PAD Assignment



Chip size:  $1150 \times 1715 \text{ um}^2$       Substrate: connected to VSS  
 PAD size:  $70 \times 70 \text{ um}$

VDD (Pad27) and VCCA2 (Pad26) must be bound together.

VLCD (Pad25) and SEG19 (Pad24) must be bound together.

The LCD voltage may be temperature compensated externally through the voltage supply to the VLCD pin.

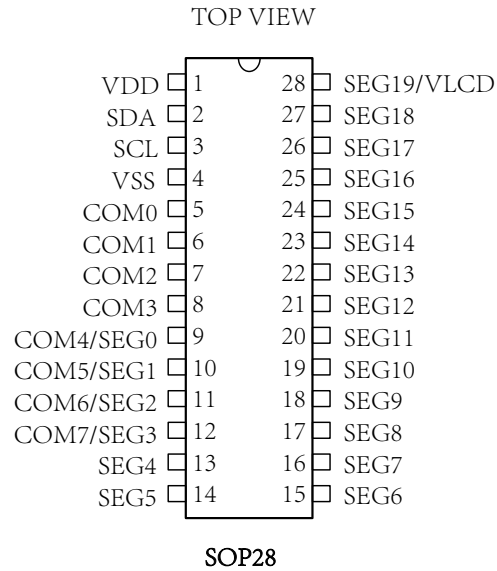
## 2.2 COB PAD Coordinates

 Unit :  $\mu\text{m}$ 

Pad No	Name	X	Y	Pad No	Name	X	Y
1	COM0	93.11	1016.655	17	SEG12	1056.89	1621.89
2	COM1	93.11	932.155	18	SEG13	1056.89	1265.89
3	COM2	93.11	847.655	19	SEG14	1056.89	1350.39
4	COM3	93.11	763.155	20	SEG15	1040.39	1621.89
5	COM4/SEG0	130.97	93.11	21	SEG16	950.39	1621.89
6	COM5/SEG1	220.97	93.11	22	SEG17	860.39	1621.89
7	COM6/SEG2	310.9	93.11	23	SEG18	756.75	1621.89
8	COM7/SEG3	400.97	93.11	24	SEG19	666.75	1621.89
9	SEG4	490.97	93.11	25	VLCD	576.75	1621.89
10	SEG5	580.97	93.11	26	VCCA2	486.75	1621.89
11	SEG6	670.97	93.11	27	VDD	396.75	1621.89
12	SEG7	760.97	93.11	28	SDA	306.75	1621.89
13	SEG8	850.97	93.11	29	SCL	199.61	1621.89
14	SEG9	940.97	93.11	30	VSS	109.61	1621.89
15	SEG10	1030.97	93.11				
16	SEG11	1056.89	1096.89	0	TEST	295.57	1211.795

### 3 Pinouts and pin description

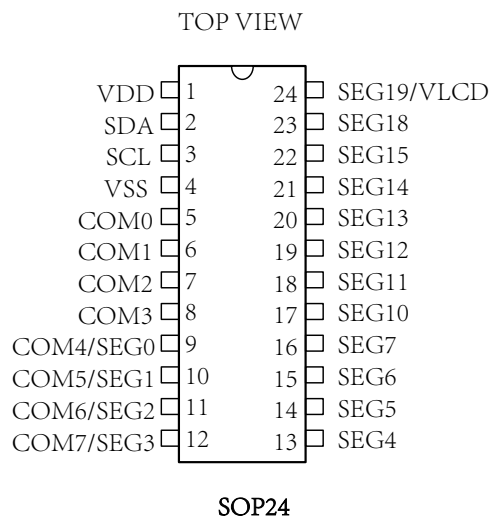
#### 3.1 VK2C21A SOP28 Pin Assignment



### 3.2 VK2C21A SOP28 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-8	COM0-COM3	O	LCD COM outputs
9-12	COM4/SEG0-COM7/SEG3	O	LCD SEG/COM outputs, software configuration 4COM or 8COM
13-27	SEG4-SEG18	O	LCD SEG outputs
28	SEG19/VLCD	I	<p>VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation.</p> <p>VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.</p>

### 3.3 VK2C21B SOP24 Pin Assignment

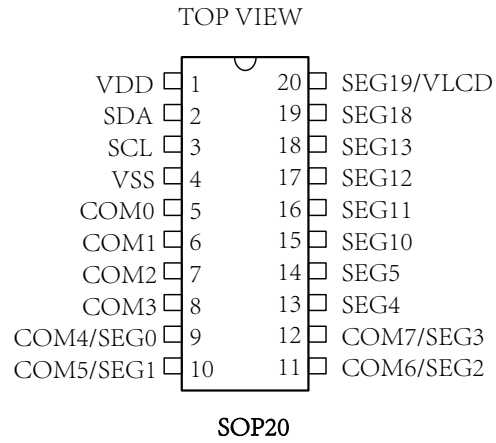


### 3.4 VK2C21B SOP24 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-8	COM0-COM3	O	LCD COM outputs
9-12	COM4/SEG0- COM7/SEG3	O	LCD SEG/COM outputs, software configuration 4COM or 8COM
13-16 17-22 23	SEG4-SEG7 SEG10-SEG15 SEG18	O	LCD SEG outputs
24	SEG19/VLCD	I	VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation.  VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.



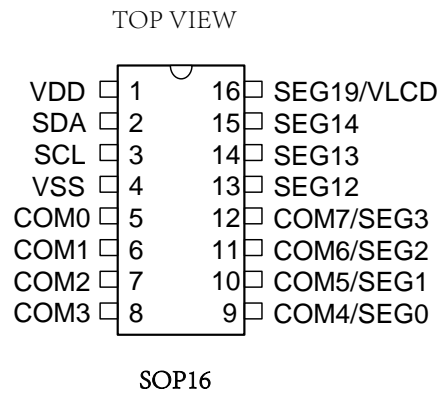
### 3.5 VK2C21C SOP20 Pin Assignment



### 3.6 VK2C21C SOP20 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	VDD
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	VSS
5-8	COM0-COM3	O	LCD COM outputs
9-12	COM4/SEG0-COM7/SEG3	O	LCD SEG/COM outputs, software configuration 4COM or 8COM
13-14 15-18 19	SEG4-SEG5 SEG10-SEG13 SEG18	O	LCD SEG outputs
20	SEG19/VLCD	I	VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation.  VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.

### 3.7 VK2C21D NSOP16 Pin Assignment

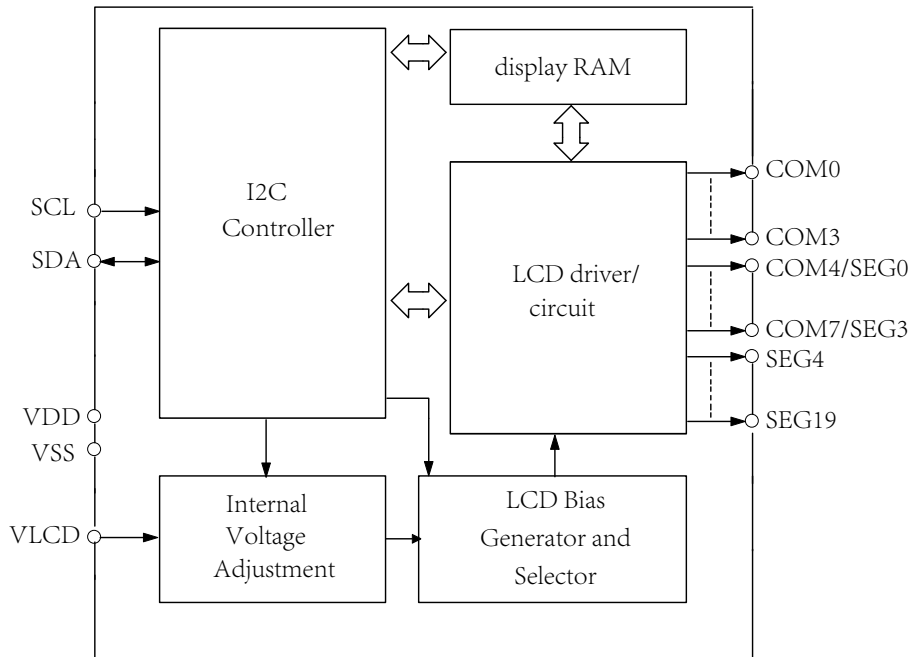


### 3.8 VK2C21D NSOP16 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	VSS
5-8	COM0-COM3	O	LCD COM outputs
9-12	COM4/SEG0-COM7/SEG3	O	LCD SEG/COM outputs, software configuration 4COM or 8COM
13-15	SEG12-SEG14	O	LCD SEG outputs
28	SEG19/VLCD	I	<p>VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation.</p> <p>VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.</p>

## 4.Functional Description

### 4.1 Block diagram



## 4.2 Display RAM

The static display memory (RAM) is organized in 20×4 or 16×8bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the I2C bus interface.

The following is a mapping from the RAM to the LCD pattern:

OUTPUT	COM3	COM2	COM1	COM0	OUTPUT	COM3	COM2	COM1	COM0	ADDRESS
SEG1					SEG0					0x00
SEG3					SEG2					0x01
SEG5					SEG4					0x02
SEG7					SEG6					0x03
SEG9					SEG8					0x04
SEG11					SEG10					0x05
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG19					SEG18					0x09
Data	bit7	bit6	bit5	bit4		bit3	bit2	bit1	bit0	

**RAM Mapping of 20×4**

OUTPUT	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	ADDRESS
SEG4									0x00
SEG5									0x01
SEG6									0x02
SEG7									0x03
SEG8									0x04
SEG9									0x05
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG19									0x0F
Data	bit7	bit6	bit5	bit4	bit3	bit22	bit1	bit0	

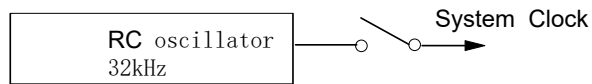
**RAM Mapping of 16×8**

### 4.3 System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The system clock frequency (f<sub>SYS</sub>) determines the LCD frame frequency.

System set command controls the internal system oscillator on/off and display on/off. During initial system power-on the system oscillator will be in the stop state.

System Oscillator Configuration:



## 4.4 LCD operating voltage

LCD voltage is obtained from VLCD pin or Internal voltage adjustment circuit.

VLCD pad and VCCA2 pad be bonded together for VLCD<5.5V,an externally voltage supply to the VLCD pin.

VDD pad and VCCA2 pad be bonded together for VLCD<VDD,VLCD connect to VDD through a resistor,Adjust the VLCD voltage by changing this external resistance.

<b>DA3~DA0</b>	<b>Bias</b>	<b>1/3</b>	<b>1/4</b>	<b>Note</b>
<b>0x00</b>		$1.000 \times VDD$	$1.000 \times VDD$	Default
<b>0x01</b>		$0.944 \times VDD$	$0.957 \times VDD$	
<b>0x02</b>		$0.894 \times VDD$	$0.918 \times VDD$	
<b>0x03</b>		$0.849 \times VDD$	$0.882 \times VDD$	
<b>0x04</b>		$0.808 \times VDD$	$0.849 \times VDD$	
<b>0x05</b>		$0.771 \times VDD$	$0.818 \times VDD$	
<b>0x06</b>		$0.738 \times VDD$	$0.789 \times VDD$	
<b>0x07</b>		$0.707 \times VDD$	$0.763 \times VDD$	
<b>0x08</b>		$0.678 \times VDD$	$0.738 \times VDD$	
<b>0x09</b>		$0.652 \times VDD$	$0.714 \times VDD$	
<b>0x0A</b>		$0.628 \times VDD$	$0.692 \times VDD$	
<b>0x0B</b>		$0.605 \times VDD$	$0.672 \times VDD$	
<b>0x0C</b>		$0.584 \times VDD$	$0.652 \times VDD$	
<b>0x0D</b>		$0.565 \times VDD$	$0.634 \times VDD$	
<b>0x0E</b>		$0.547 \times VDD$	$0.616 \times VDD$	
<b>0x0F</b>		$0.529 \times VDD$	$0.600 \times VDD$	



## 4.5 Power-On Reset

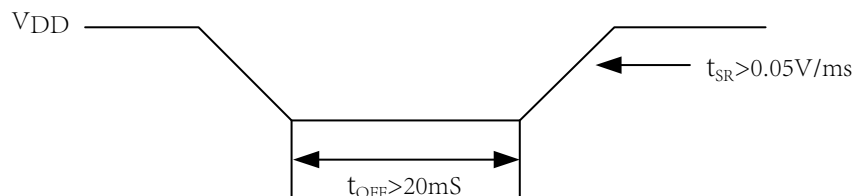
When the power is applied, the device is initialized by an internal power-on reset circuit. Data transfers on the I2C bus should be avoided for 1 ms following power-on.

The status of the internal circuits after initialization is as follows:

- All COM/SEG outputs are set to VLCD.
- 1/4 duty and 1/3 bias.
- The System Oscillator and the LCD bias generator are off state.
- LCD Display is off state.
- Internal voltage adjustment function is enabled.
- The Segment/VLCD shared pin is set as the SEG
- Detection switch for the VLCD pin is disabled
- Frame Frequency is set to 80Hz
- Blinking function is switched off

if VDD drops below the minimum voltage of operating voltage specification during operation, the power-on reset timing conditions must be also satisfied. This means that VDD must fall to 0V and remain at 0V for a minimum time of 20ms before rising to the normal operating voltage.

Power-on Reset Timing:



## 4.6 LCD Communication Command

The display modes supported by the LCD driver are 56SEG x 4COM and 52SEG x 8 COM, The unused SEG or COM outputs should be left open.

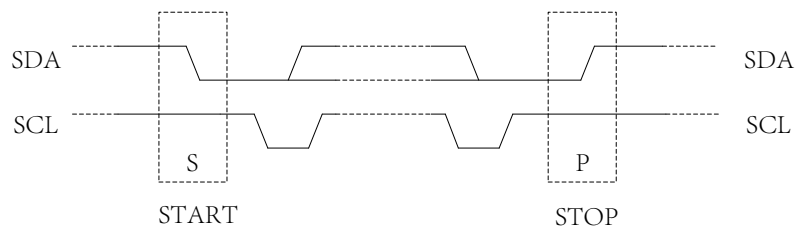
The device provides two frame frequencies selected with Mode set command known as 80Hz and 160Hz respectively.

### 4.6.1 I2C Serial Interface

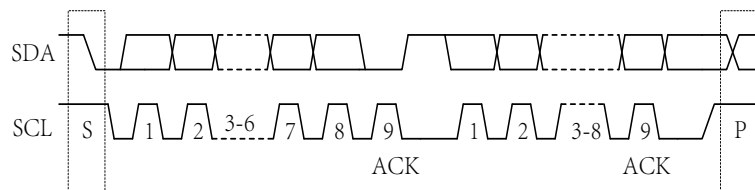
The device supports I2C serial interface.

The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7k. When the bus is free, both lines are high.

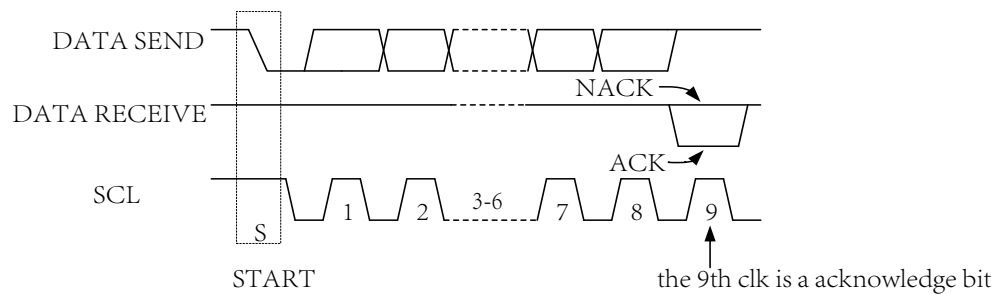
#### START and STOP



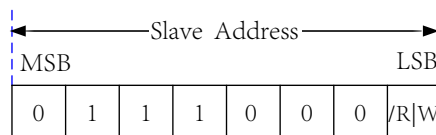
#### Byte Format



#### Acknowledge



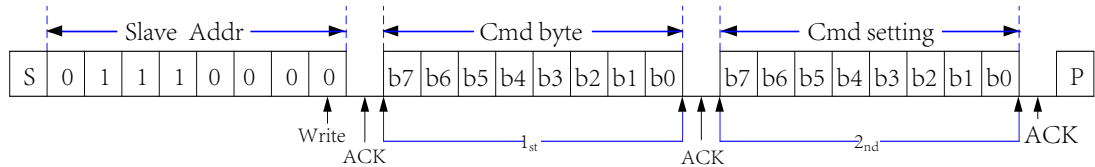
#### Slave Address (0x70) bit0-R/W



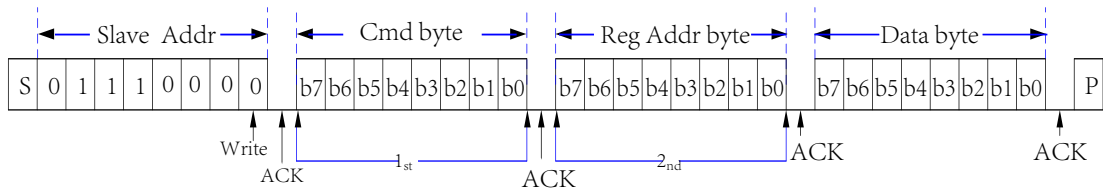
## 4.6.2 I2C Command Format

### Write Operation

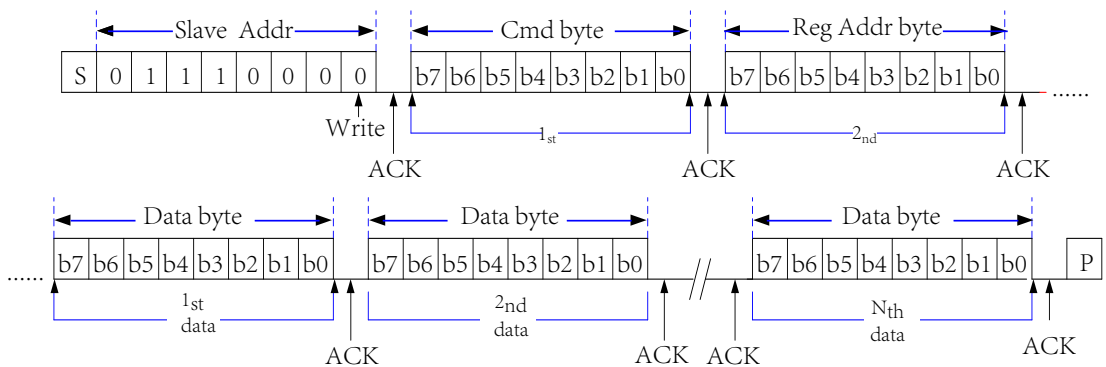
#### Byte Writes Operation



#### Display RAM Single Data Byte

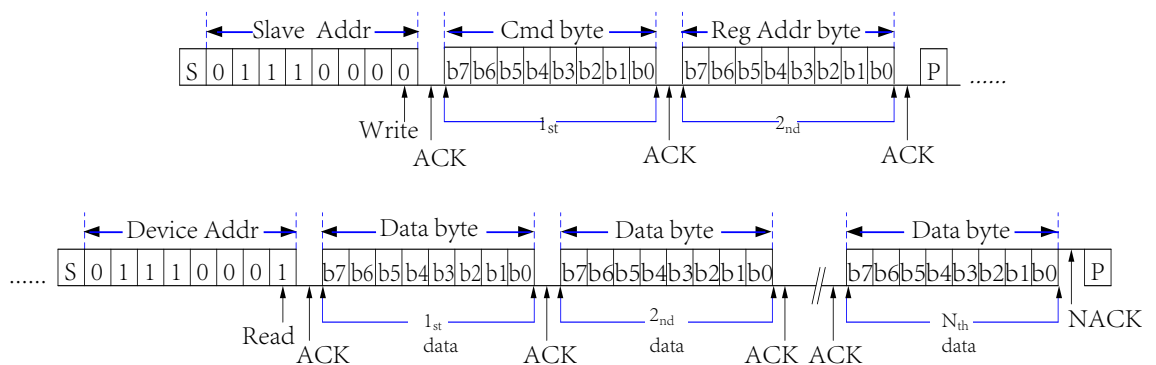


#### Display RAM Page Write Operation

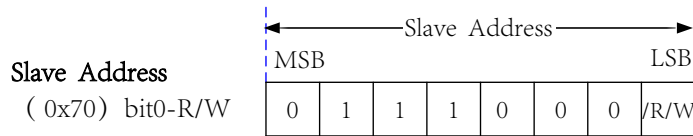


### Read Operation

#### Display RAM Page Read Operation



## 4.6.3 Command Summary



### 4.6.3.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

### 4.6.3.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
mode set cmd	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias	2nd	X	X	X	X	X	X	Duty	Bias		W	00H

Bit 1	Bit 0	Duty	Bias
Duty	Bias		
0	0	1/4 duty	1/3 bias
0	1	1/4 duty	1/4 bias
1	0	1/8 duty	1/3 bias
1	1	1/8 duty	1/4 bias

### 4.6.3.3 System Set Command

Set the internal system oscillator on/off and display on/off.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
system set cmd	1 <sup>st</sup>	1	0	0	0	0	1	0	0		W	
System oscillator and Display on/off set	2 <sup>nd</sup>	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	internal oscillator	LCD on/off
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

### 4.6.3.4 Frame Frequency Command

Selects the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
frame freq cmd	1 <sup>st</sup>	1	0	0	0	0	1	1	0		W	
frame freq set	2 <sup>nd</sup>	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame Frequency
F	
0	80Hz
1	160Hz

### 4.6.3.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq cmd	1st	1	0	0	0	1	0	0	0		W	
blinking freq set	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

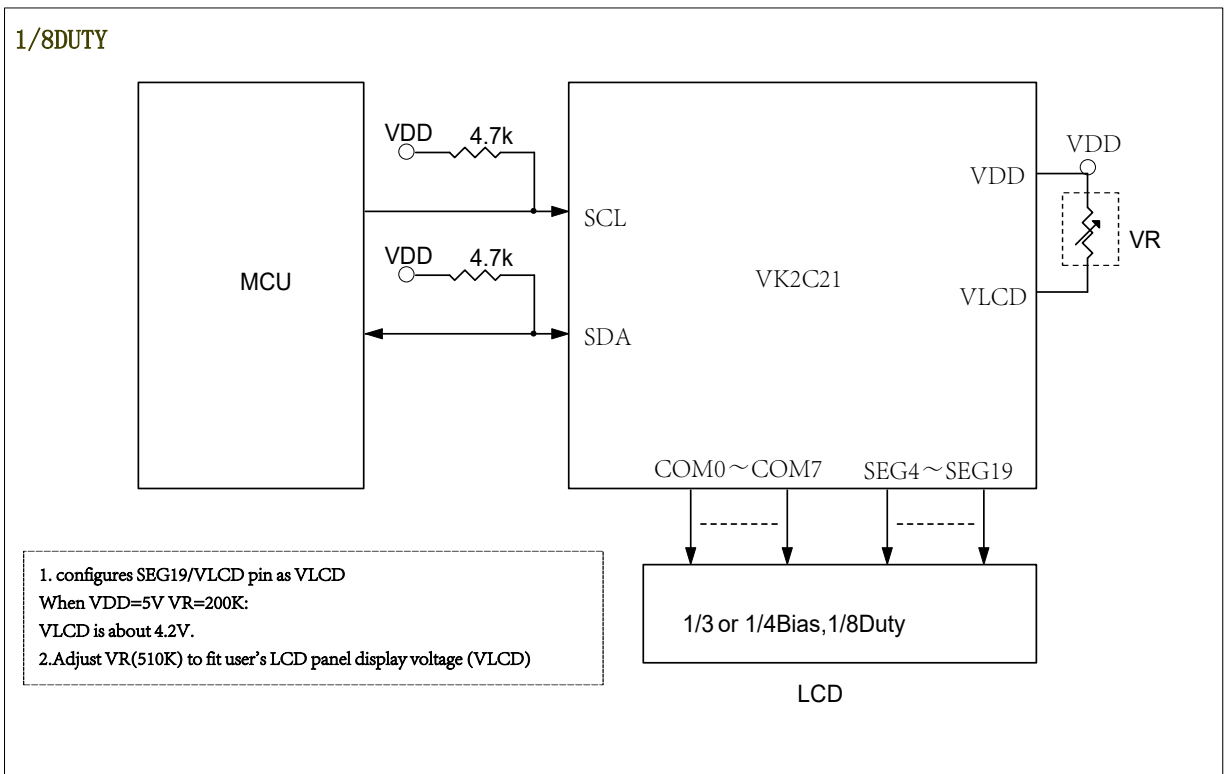
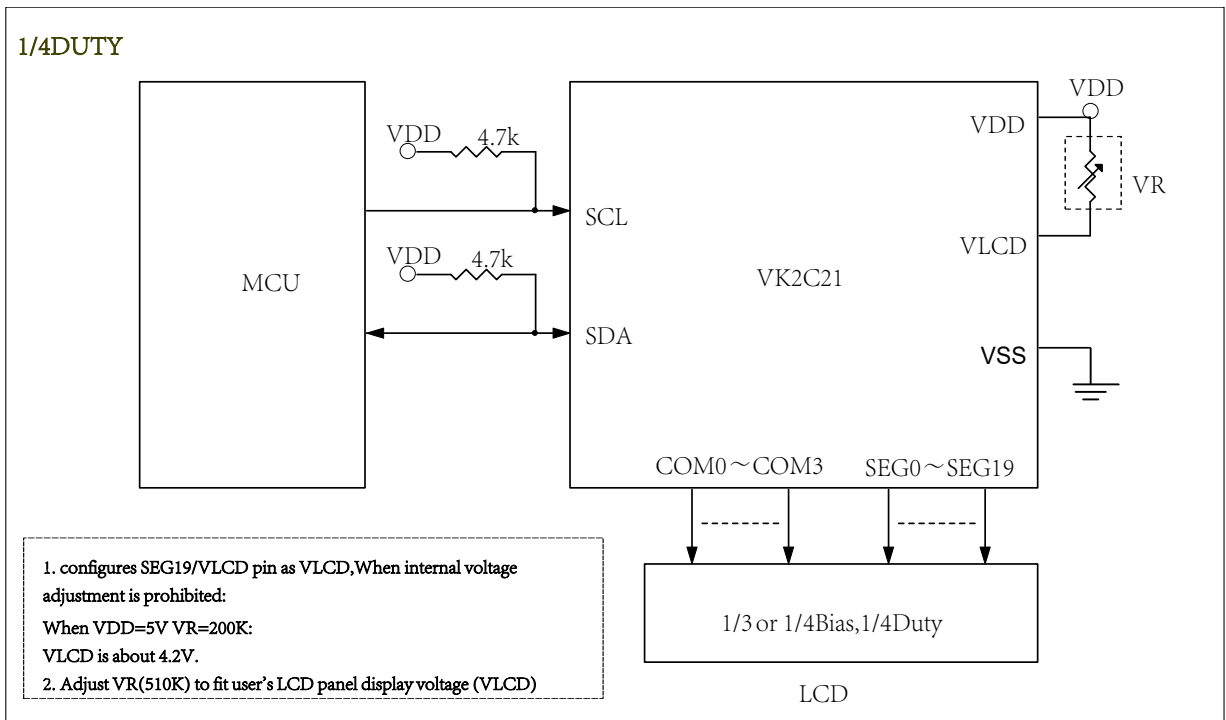
Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off(Def)
0	1	2Hz
1	0	1Hz
1	1	0.5Hz

### 4.6.3.6 Internal Voltage Set Command

The internal voltage adjustment can provide sixteen kinds of regulator voltage adjustment options.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA cmd	1 <sup>st</sup>	1	0	0	0	1	0	1	0		W	
IVA set	2 <sup>nd</sup>	X	X	DE	VE	DA3	DA2	DA1	DA0	SEG/VLCD pin can be set via the DE bit. internal voltage adjustment can be set via the VE bit. DA3~DA0 bits can be used to adjust the VLCD output voltage.	W	30H
Note:												
		<b>Bit 5</b>	<b>Bit 4</b>	<b>SEG 19/VLCD shared pin sel</b>	<b>internal voltage adjustment</b>	<b>Note</b>						
		<b>DE</b>	<b>VE</b>									
		0	0	VLCD pin	off	<ul style="list-style-type: none"> <li>• SEG/VLCD pin is set as the VLCD pin</li> <li>• Disable internal voltage adjustment function</li> <li>• An external resistor is connected in series between the VLCD pin and the VDD pin to adjust the bias voltage. At the same time, the DA3-DA0 bit must be set to a value other than "0000" to enable the internal voltage follower.</li> <li>• VLCD pin is connected to the VDD pin, the internal voltage must be disabled by set DA3~DA0 as "0000".</li> </ul>						
		0	1	VLCD pin	on	<ul style="list-style-type: none"> <li>• SEG/VLCD pin is set as the VLCD pin</li> <li>• Enable internal voltage adjustment function</li> <li>• The VLCD pin is an output pin, and the voltage of the VLCD pin is detected by the MCU.</li> </ul>						
		1	0	SEG19 pin	off	<ul style="list-style-type: none"> <li>• SEG/VLCD pin is set as the segment pin</li> <li>• Disable internal voltage adjustment function</li> <li>• The bias voltage is provided by internal VDD.</li> <li>• Regardless of the value of DA3-DA0, the internal voltage follower is prohibited.</li> </ul>						
		1	1	SEG19 pin	on	<ul style="list-style-type: none"> <li>• SEG/VLCD pin is set as the segment pin</li> <li>• Enable internal voltage adjustment function</li> </ul>						
<ul style="list-style-type: none"> <li>• Power-on:Enable internal voltage Adjustment and the SEG/VLCD pin is set as the segment pin.</li> <li>• When the DA0~DA3 bits are set to "0000", the internal voltage is disabled.</li> <li>• When the DA0~DA3 bits are set to other values except "0000", internal voltage follower is enabled.</li> </ul>												

## 5 Application Circuits





## 6 Electrical characteristics

### 6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3~6.5	V
Input Voltage	VIN	$V_{SS}-0.3\sim V_{DD}+0.3$	V
Storage Temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

### 6.2 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	I <sub>DD1</sub>	—	18	27	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD on, Internal osc on, DA0~DA3 = "0000"
		—	25	40		5V	
Operating current	I <sub>DD2</sub>	—	2	5	μA	3V	No load, VLCD=VDD, 1/3 bias, fLCD=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	I <sub>STB</sub>	—	0.1	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	0.3	2		5V	
Input Low Voltage	V <sub>IL</sub>	0	—	0.3	VDD	3V	SCL, SDA
						5V	
Input High Voltage	V <sub>IH</sub>	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	I <sub>OL</sub>	3.0	—	—	mA	3V	V <sub>OL</sub> =0.4V, SDA
		6.0	—	—		5V	
LCD COM Sink Current	I <sub>OL1</sub>	250	400	—	μA	3V	V <sub>OL</sub> =0.3V
		500	800	—		5V	V <sub>OL</sub> =0.5V
LCD COM Source Current	I <sub>OH1</sub>	-140	-230	—	μA	3V	V <sub>OH</sub> =2.7V
		-300	-500	—		5V	V <sub>OH</sub> =4.5V
LCD SEG Sink Current	I <sub>OL2</sub>	250	400	—	μA	3V	V <sub>OL</sub> =0.3V
		500	800	—		5V	V <sub>OL</sub> =0.5V
LCD SEG Source Current	I <sub>OH2</sub>	-140	-230	—	μA	3V	V <sub>OH</sub> =2.7V
		-300	-500	—		5V	V <sub>OH</sub> =4.5V

## 6.3 AC Characteristics

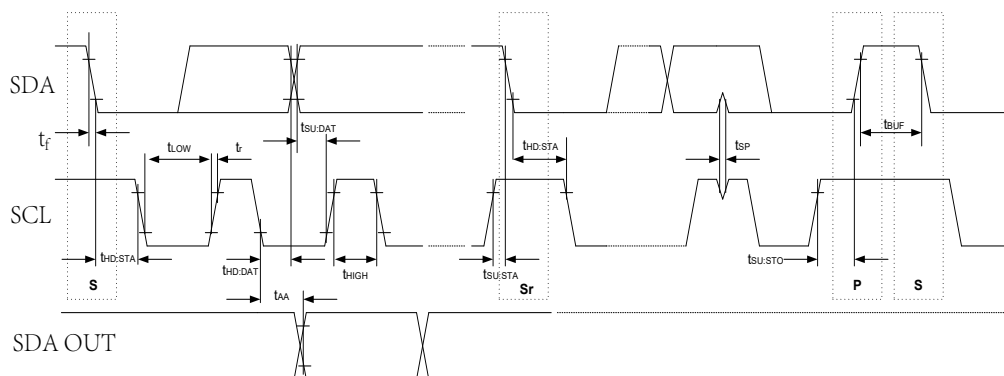
### Frame Frequency

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	$f_{LCD1}$	72	80	88	Hz	4.0V	1/4 duty, 25 °C
LCD Frame Frequency	$f_{LCD2}$	144	160	176	Hz	4.0V	1/4 duty, 25 °C
LCD Frame Frequency	$f_{LCD3}$	52	80	124	Hz	4.0V	1/4 duty, -40 ~ +85 °C
LCD Frame Frequency	$f_{LCD4}$	104	160	248	Hz	4.0V	1/4 duty, -40 ~ +85 °C

### I2C parameter

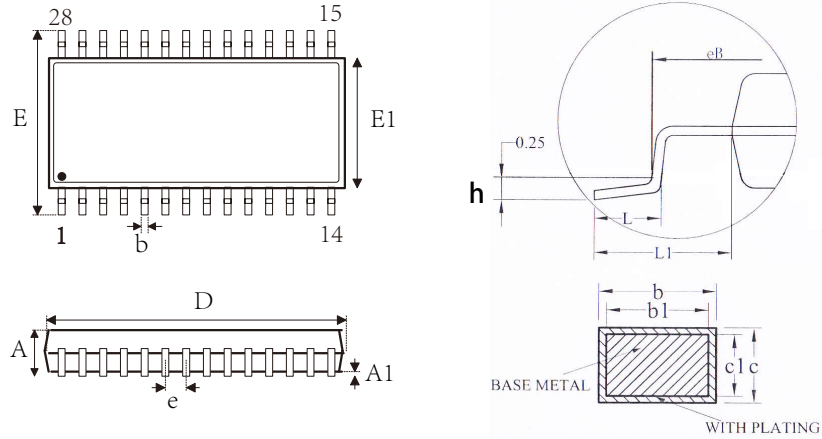
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	$f_{SCL}$	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	$t_{BUF}$	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	$t_{LOW}$	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	$t_{HIGH}$	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	$t_R$	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	$t_F$	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—	—	μs	3.0-5.5V	—
Output Valid from Clock	$t_{AA}$	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	$t_{SP}$	—	—	50	ns	3.0-5.5V	Noise suppression time

### I<sup>2</sup>C Timing



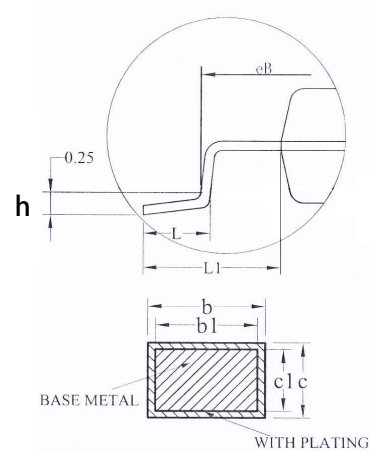
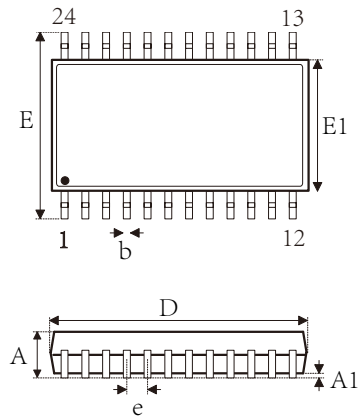
## 7 Package Information

### 7.1 SOP28 (300mil) (18.0mm x 7.5mm PP=1.27mm)

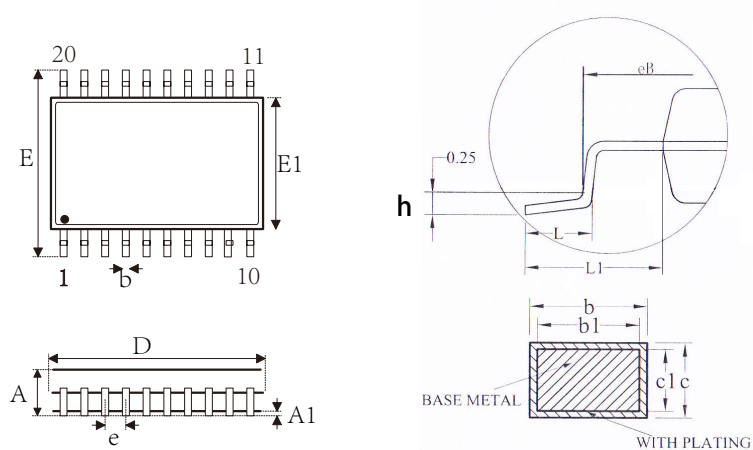


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	2.65
A1	0.10	---	0.30
b	0.39	---	0.47
b1	0.38	0.41	0.44
c	0.25	---	0.29
c1	0.24	0.25	0.26
D	17.90	18.00	18.10
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	---	0.50
L	0.70	---	1.00
L1	1.40REF		

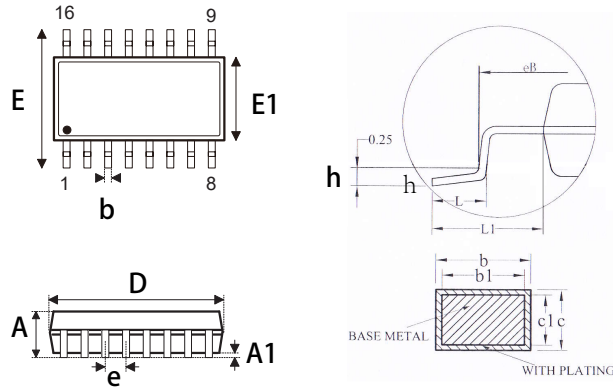
## 7.2 SOP24 (300mil) (15.4mm x 7.5mm PP=1.27mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	2.36	2.54	2.64
A1	0.10	0.20	0.30
b	0.39	---	0.47
b1	0.38	0.41	0.44
c	0.25	---	0.29
c1	0.24	0.25	0.26
D	15.30	15.40	15.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	---	0.50
L	0.70	---	1.00
L1	1.40REF		

**7.3 SOP20 (300mil) (12.8mm x 7.5mm PP=1.27mm)**


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	2.65
A1	0.10	---	0.30
b	0.35	---	0.43
b1	0.34	0.37	0.40
c	0.25	---	0.29
c1	0.24	0.25	0.26
D	12.70	12.80	12.90
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.27BSC		
h	0.25	---	0.50
L	0.70	---	1.00
L1	1.40REF		

**7.4 NSOP16 (150mil) (9.9mm x 3.9mm PP=1.27mm)**


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	---	---	1.75
A1	0.10	---	0.225
b	0.39	---	0.47
b1	0.38	0.41	0.44
c	0.20	---	0.24
c1	0.19	0.20	0.21
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	---	0.50
L	0.50	---	0.80
L1	1.05REF		

## 8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

### Disclaimers

Information in this document is believed to be accurate and reliable. However, VinKa does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information. VinKa reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof. For the latest information, please visit <https://www.szvinka.com> Or contact VinKa's staff.