Features

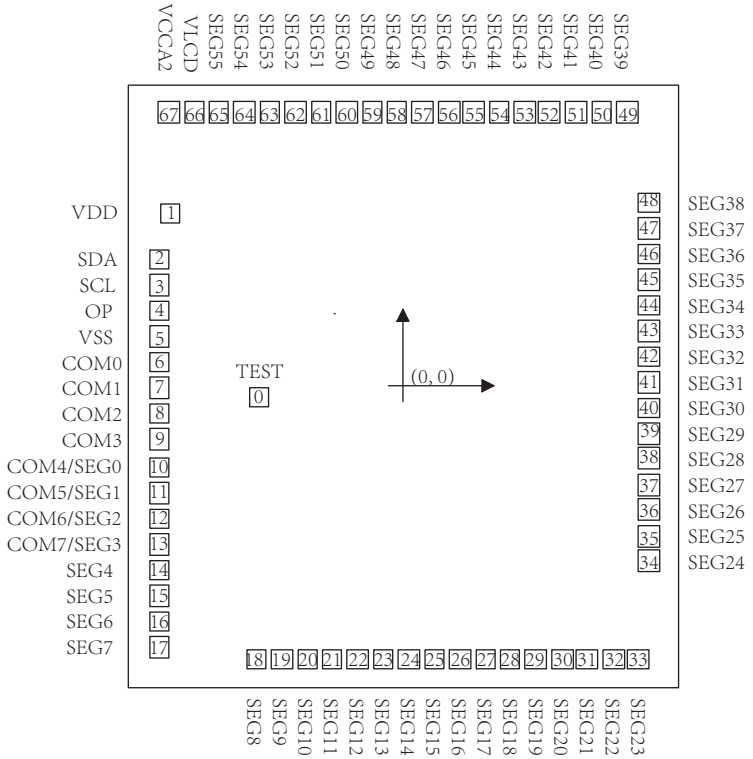
- Operating voltage:2.4-5.2V
- Built-in 32kHz RC oscillator
- Selection of 1/3 or 1/4 bias
- Selection of 1/4 or 1/8 duty
- Built-in 56x4、52x8 bit display RAM
- Selection of 80Hz or 160Hz Frame Frequency
- STANDBY mode（by System Set Command LCD OFF,SYS oscillator OFF）
- I2C bus interface
- Display mode 56x4、52x8
- Versatile blinking modes
- Software configuration LCD parameters
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage（2.4~5.5V）
- Internal 16-step voltage adjustment to adjust LCD operating voltage
- Power-On Reset(POR)
- Low power consumption、High anti-interference
- Package:
  LQFP48(7.0mm x 7.0mm PP=0.5mm)
  LQFP64(7.0mm x 7.0mm PP=0.4mm)
  DICE
  COG

1 General Description

VK2C23 is a RAM Mapping LCD Driver， It can support LCD screens with a maximum of 224 pattern(56SEGx4COM) or a maximum of 416 pattern(52SEGx8COM) .The device communicates with host microcontrollers via a two-line bidirectional I2C bus,it is used to configure display parameters and transfer display data,, and can also enter the standby mode through System Set Command .With the characteristics of high anti-interference and low power consumption, it is suitable for water electrical meters and industrial control instruments.

2 COB PAD description and Coordinates

2.1 COB PAD Assignment



Chip size: 1750×1920 um² Substrate: connected to VSS
PAD size: 70×70 um PAD spacing: 113 um

VLCD pad and VCCA2 pad be bonded together for VLCD ≤+5.5V(VLCD≥VDD)

Internal Voltage Set Command		VLCD	SEG55	Note
DE bit	VE bit			
0	0	INPUT	Null	• VLCD support internal bias voltage
0	1	INPUT	Null	• Internal Voltage is null • VLCD support internal bias voltage
1	0	INPUT	OUTPUT	• VLCD support internal bias voltage
1	1	INPUT	OUTPUT	• VLCD support internal bias voltage

VDD pad and VCCA2 pad be bonded together for VLCD ≤ VDD。

Internal Voltage Set Command		VLCD	SEG55	Note
DE bit	VE bit			
0	0	INPUT	Null	• VLCD support internal bias voltage
0	1	OUTPUT	Null	• Detect the internal bias voltage • VDD support internal bias voltage
1	0	FLOAT	OUTPUT	• VDD support internal bias voltage
1	1	FLOAT	OUTPUT	• VDD support internal bias voltage

***1** The LCD voltage may be temperature compensated externally through the voltage supply to the VLCD pin.

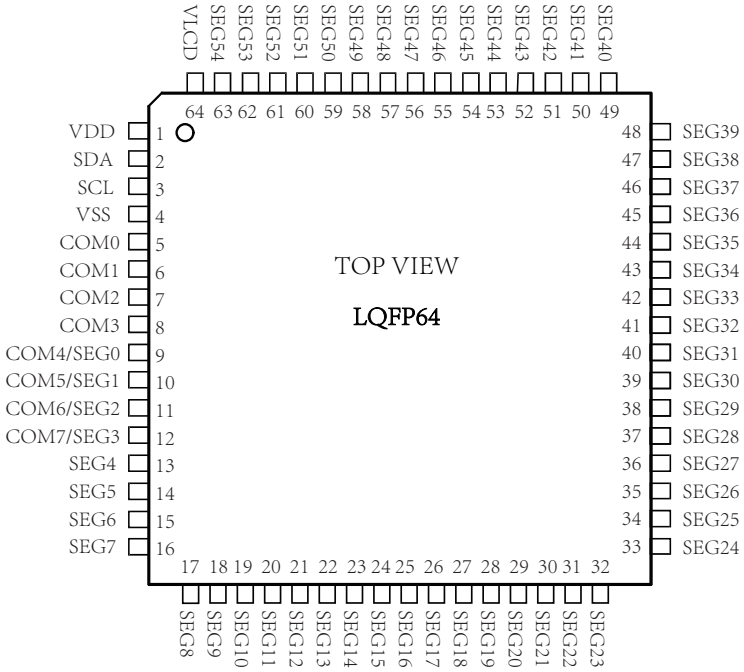
2.2 COB PAD Coordinates

Unit：μm

Pad No	Name	X	Y	Pad No	Name	X	Y
1	VDD	103.11	1887.01	35	SEG25	2021.89	488.19
2	SDA	98.11	1736.67	36	SEG26	2021.89	593.19
3	SCL	98.11	1623.17	37	SEG27	2021.89	698.19
4	OP	98.11	1518.17	38	SEG28	2021.89	803.19
5	VSS	103.11	1413.17	39	SEG29	2021.89	908.19
6	COM0	98.11	1308.17	40	SEG30	2021.89	1013.19
7	COM1	98.11	1203.17	41	SEG31	2021.89	1118.19
8	COM2	98.11	1098.17	42	SEG32	2021.89	1223.19
9	COM3	98.11	993.17	43	SEG33	2021.89	1328.19
10	COM4/SEG0	98.11	888.17	44	SEG34	2021.89	1433.19
11	COM5/SEG1	98.11	783.17	45	SEG35	2021.89	1538.19
12	COM6/SEG2	98.11	1724.57	46	SEG36	2021.89	1643.19
13	COM7/SEG3	98.11	573.17	47	SEG37	2021.89	1748.19
14	SEG4	98.11	468.17	48	SEG38	2021.89	1853.19
15	SEG5	98.11	363.17	49	SEG39	1973.75	2191.89
16	SEG6	98.11	258.17	50	SEG40	1868.75	1868.75
17	SEG7	98.11	153.17	51	SEG41	1763.75	2191.89
18	SEG8	359.57	98.11	52	SEG42	1658.75	2191.89
19	SEG9	464.57	98.11	53	SEG43	1553.75	2191.89
20	SEG10	569.57	98.11	54	SEG44	1448.75	2191.89
21	SEG11	674.57	98.11	55	SEG45	1343.75	2191.89
22	SEG12	779.57	98.11	56	SEG46	1238.75	2191.89
23	SEG13	884.57	98.11	57	SEG47	1133.75	2191.89
24	SEG14	989.57	98.11	58	SEG48	1028.75	2191.89
25	SEG15	1094.57	98.11	59	SEG49	923.75	2191.89
26	SEG16	1199.57	98.11	60	SEG50	818.75	2191.89
27	SEG17	1304.57	98.11	61	SEG51	713.75	2191.89
28	SEG18	1409.57	98.11	62	SEG52	608.75	2191.89
29	SEG19	1514.57	98.11	63	SEG53	503.75	2191.89
30	SEG20	1619.57	98.11	64	SEG54	392.75	2191.89
31	SEG21	1724.57	98.11	65	SEG55	287.75	2191.89
32	SEG22	1829.57	98.11	66	VLCD	182.75	1452.16
33	SEG23	1934.57	98.11	67	VCCA2	77.75	2191.89
34	SEG24	2021.89	383.19	0	TEST	629.32	1452.16

3 Pinouts and pin description

3.1 VK2C23A LQFP64 Pin Assignment

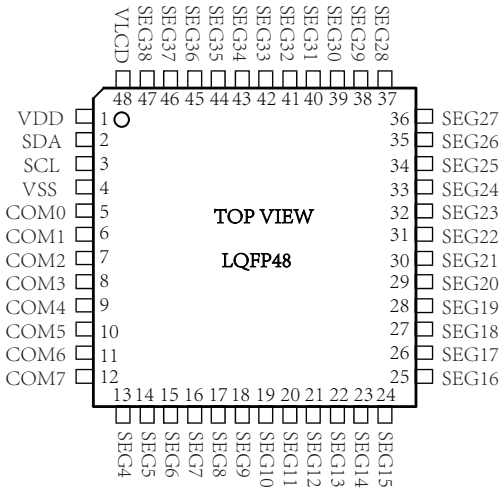


Note：VCCA2 pad is internally connected to VLCD pad
OP pad is float

3.2 VK2C23A LQFP64 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-8	COM0-COM3	O	LCD COM outputs
9-12	COM4/SEG0-COM7/SEG3	O	LCD SEG/COM outputs， software configuration 4COM or 8COM
13-63	SEG4-SEG54	O	LCD SEG outputs
64	VLCD	I	VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation. VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.

3.3 VK2C23B LQFP48 Pin Assignment



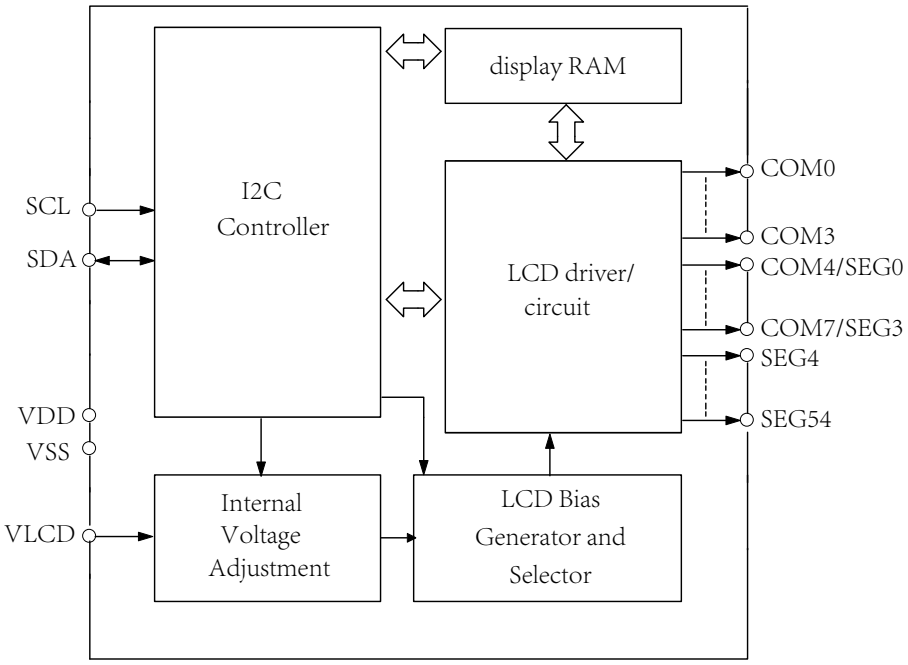
说明：不支持 LCD 1/4 duty
VCCA2 pad 内部与 VLCD pad 连接
OP pad接地

3.4 VK2C23B LQFP48 Pin Description

No.	Name	I/O	Function
1	VDD	VDD	Positive power supply
2	SDA	I/O	Serial Data Input/Output for I2C interface
3	SCL	I	Serial Clock Input for I2C interface
4	VSS	VSS	Negative power supply
5-12	COM0-COM7	O	LCD COM outputs
13-47	SEG4-SEG38	O	LCD SEG outputs
48	VLCD	I	VLCD connect to VDD ,When internal voltage regulation function is configured to be enabled,Adjust the VLCD voltage by internal voltage regulation. VLCD connect to VDD through a resistor,When internal voltage regulation function is configured to be Disabled,Adjust the VLCD voltage by changing this external resistance.

4.Functional Description

4.1 Block diagram



4.2 Display RAM

The static display memory (RAM) is organized into 56×4 or 52×8bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the I2C bus interface.

The following is a mapping from the RAM to the LCD pattern:

OUTPUT	COM3	COM2	COM1	COM0	OUTPUT	COM3	COM2	COM1	COM0	ADDRESS
SEG1					SEG0					0x00
SEG3					SEG2					0x01
SEG5					SEG4					0x02
SEG7					SEG6					0x03
SEG9					SEG8					0x04
SEG11					SEG10					0x05
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG55					SEG54					0x1B
Data	bit7	bit6	bit5	bit4		bit3	bit2	bit1	bit0	

RAM Mapping of 56×4

OUTPUT	COM7/ SEG3	COM6/ SEG2	COM5/ SEG1	COM4/ SEG0	COM3	COM2	COM1	COM0	ADDRESS
SEG4									0x00
SEG5									0x01
SEG6									0x02
SEG7									0x03
SEG8									0x04
SEG9									0x05
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
SEG55									0x33
Data	bit7	bit6	bit5	bit4	bit3	bit22	bit1	bit0	

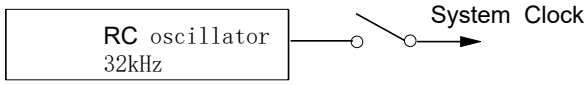
RAM Mapping of 52×8

4.3 System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator. The system clock frequency (f_{SYS}) determines the LCD frame frequency.

System set command controls the internal system oscillator on/off and display on/off. During initial system power-on the system oscillator will be in the stop state.

System Oscillator Configuration:



4.4 LCD operating voltage

LCD voltage is obtained from VLCD pin or Internal voltage adjustment circuit.

VLCD pad and VCCA2 pad be bonded together for VLCD≤5.5V,an externally voltage supply to the VLCD pin.

VDD pad and VCCA2 pad be bonded together for VLCD≤VDD,VLCD connect to VDD through a resistor,Adjust the VLCD voltage by changing this external resistance.

The relationship between the programmable 4-bit analog switch and the VLCD output voltage is shown in the table:

When VCCA2 pad is connected to VDD pad

Bias / DA3~DA0	1/3	1/4	Note
0x00	1.000×VDD	1.000×VDD	Default
0x01	0.944×VDD	0.957×VDD	
0x02	0.894×VDD	0.918×VDD	
0x03	0.849×VDD	0.882×VDD	
0x04	0.808×VDD	0.849×VDD	
0x05	0.771×VDD	0.818×VDD	
0x06	0.738×VDD	0.789×VDD	
0x07	0.707×VDD	0.763×VDD	
0x08	0.678×VDD	0.738×VDD	
0x09	0.652×VDD	0.714×VDD	
0x0A	0.628×VDD	0.692×VDD	
0x0B	0.605×VDD	0.672×VDD	
0x0C	0.584×VDD	0.652×VDD	
0x0D	0.565×VDD	0.634×VDD	
0x0E	0.547×VDD	0.616×VDD	
0x0F	0.529×VDD	0.600×VDD	

When VCCA2 pad is connected to VLCD pad

Bias / DA3~DA0	1/3	1/4	Note
0x00	1.000×VLCD	1.000×VLCD	Default
0x01	0.944×VLCD	0.957×VLCD	
0x02	0.894×VLCD	0.918×VLCD	
0x03	0.849×VLCD	0.882×VLCD	
0x04	0.808×VLCD	0.849×VLCD	
0x05	0.771×VLCD	0.818×VLCD	
0x06	0.738×VLCD	0.789×VLCD	
0x07	0.707×VLCD	0.763×VLCD	
0x08	0.678×VLCD	0.738×VLCD	
0x09	0.652×VLCD	0.714×VLCD	
0x0A	0.628×VLCD	0.692×VLCD	
0x0B	0.605×VLCD	0.672×VLCD	
0x0C	0.584×VLCD	0.652×VLCD	
0x0D	0.565×VLCD	0.634×VLCD	
0x0E	0.547×VLCD	0.616×VLCD	
0x0F	0.529×VLCD	0.600×VLCD	

4.5 Power-On Reset

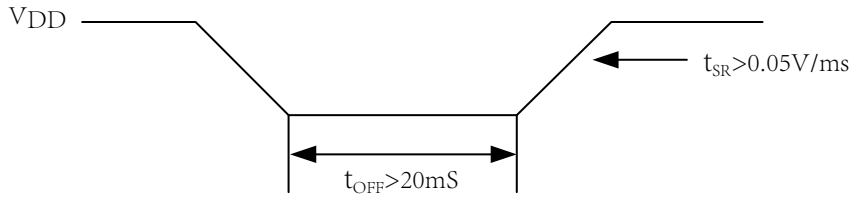
When the power is applied, the device is initialized by an internal power-on reset circuit. Data transfers on the I2C bus should be avoided for 1 ms following power-on.

The status of the internal circuits after initialization is as follows:

- when VLCD≤VDD ,all COM/SEG outputs are set to VDD.
- when VDD≤VLCD ,all COM/SEG outputs are set to VLCD.
- for LQFP64 is 1/4 duty and 1/3 bias.
- for LQFP48 is 1/8 duty and 1/3 bias.
- The System Oscillator and the LCD bias generator are off state
- LCD Display is off state.
- Internal voltage adjustment function is enabled.
- The Segment/VLCD shared pin is set as the SEG
- Detection switch for the VLCD pin is disabled
- Frame Frequency is set to 80Hz
- Blinking function is switched off

if VDD drops below the minimum voltage of operating voltage specification during operation, the power-on reset timing conditions must be also satisfied. This means that VDD must fall to 0V and remain at 0V for a minimum time of 20ms before rising to the normal operating voltage.

Power-on Reset Timing



4.6 LCD Communication Command

The display modes supported by the LCD driver are 56SEG x 4COMand 52SEG x 8 COM,The unused SEG or COM outputs should be left open.

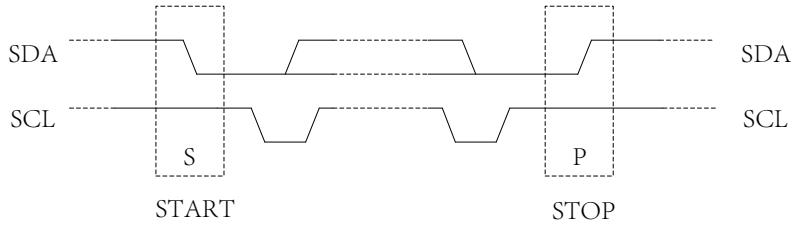
The device provides two frame frequencies selected with Mode set command known as 80Hz and 160Hz respectively.

4.6.1 I2C Serial Interface

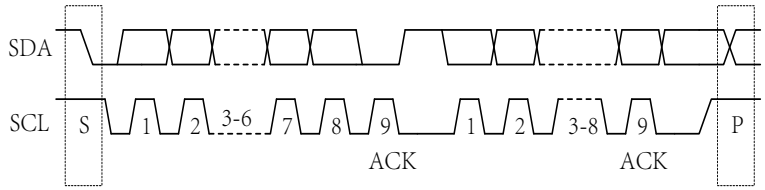
The device supports I2C serial interface.

The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7k. When the bus is free, both lines are high.

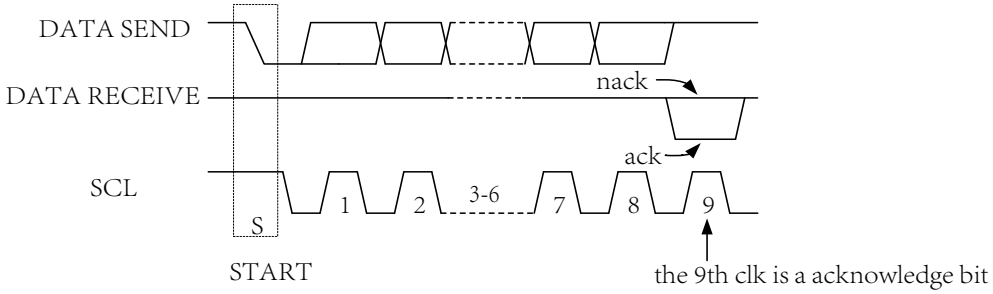
START and STOP



Byte Format

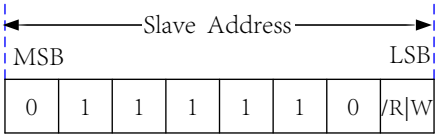


Acknowledge



Slave Address

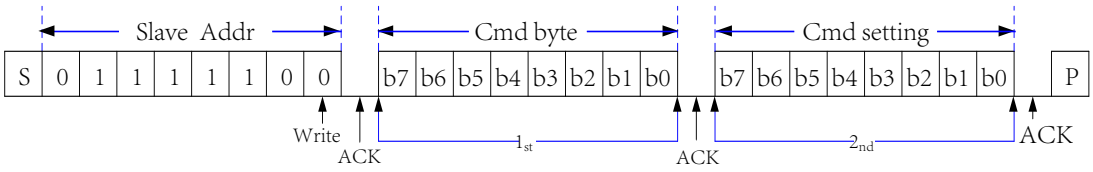
(0x7c) bit0-R/W



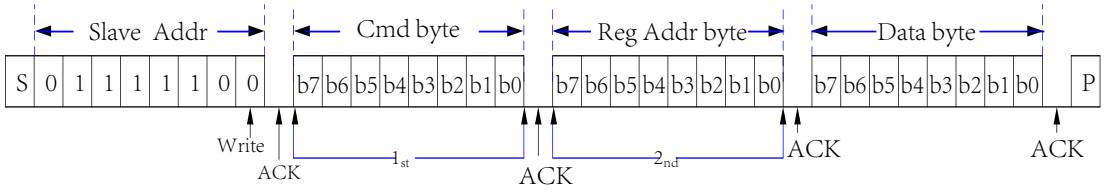
4.6.2 I2C Command Format

Write Operation

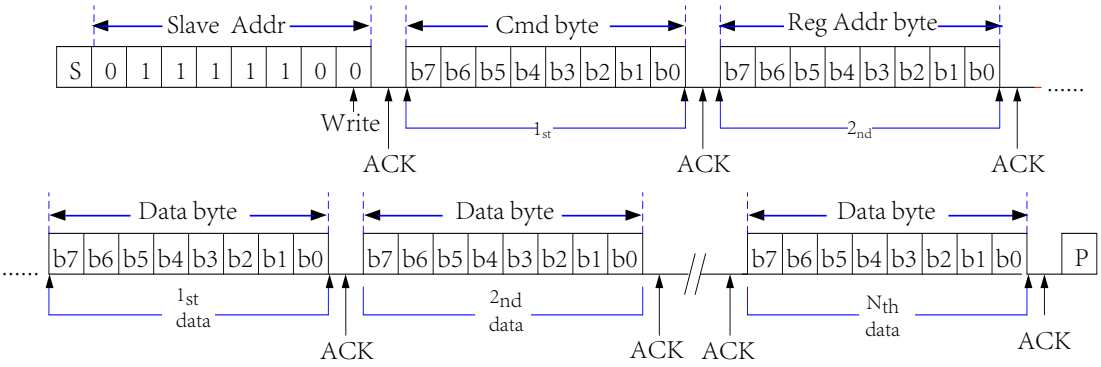
Byte Writes Operation



Display RAM Single Data Byte

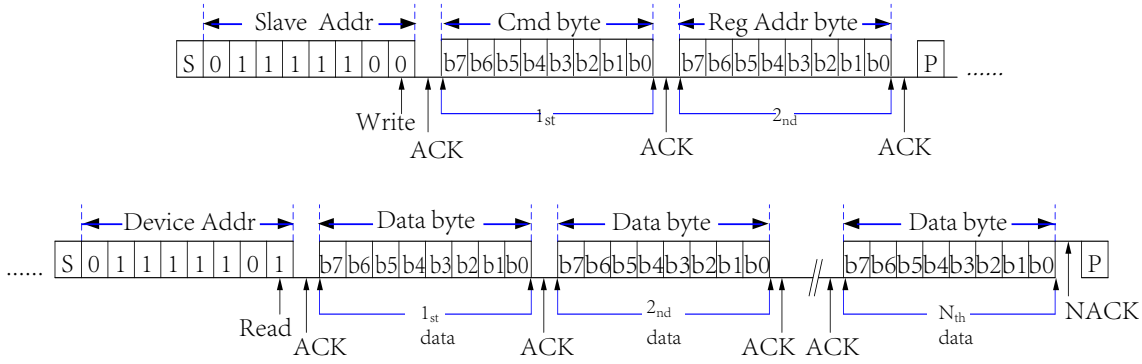


Display RAM Page Write Operation



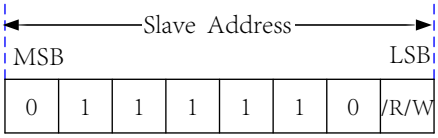
Read Operation

Display RAM Page Read Operation



4.6.3 Command Summary

Slave Address
(0x7c) bit0-R/W



4.6.3.1 Display Data Command

Send display data to display RAM

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display data command	1st	1	0	0	0	0	0	0	0		W	
Address pointer	2nd	X	X	A5	A4	A3	A2	A1	A0	Display data start address	W	00H

4.6.3.2 Mode Set Command

Set BIAS and DUTY

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
mode set cmd	1st	1	0	0	0	0	0	1	0		W	
Duty and Bias	2nd	X	X	X	X	X	X	Duty	Bias	LQFP48 only 1/8 duty	W	00H

Bit 1	Bit 0	Duty	Bias
Duty	Bias		
0	0	1/4 duty	1/3 bias
0	1	1/4 duty	1/4 bias
1	0	1/8 duty	1/3 bias
1	1	1/8 duty	1/4 bias

4.6.3.3 System Set Command

Set the internal system oscillator on/off and display on/off.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
system set cmd	1st	1	0	0	0	0	1	0	0		W	
System oscillator and Display on/off set	2nd	X	X	X	X	X	X	S	E		W	00H

Bit 1	Bit 0	internal oscillator	LCD on/off
S	E		
0	X	off	off
1	0	on	off
1	1	on	on

4.6.3.4 Frame Frequency Command

Selects the frame frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
frame freq cmd	1st	1	0	0	0	0	1	1	0		W	
frame freq set	2nd	X	X	X	X	X	X	X	F		W	00H

Bit 0	Frame Frequency
F	
0	80Hz
1	160Hz

4.6.3.5 Blinking Frequency Command

Set the blinking frequency

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq cmd	1st	1	0	0	0	1	0	0	0		W	
blinking freq set	2nd	X	X	X	X	X	X	BK1	BK0		W	00H

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off (Def)
0	1	4Hz
1	0	2Hz
1	1	1Hz

4.6.3.6 Internal Voltage Set Command

The internal voltage adjustment can provide sixteen kinds of regulator voltage adjustment options.

Function	Byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
IVA cmd	1st	1	0	0	0	1	0	1	0		W	
IVA set	2nd	X	X	DE	VE	DA3	DA2	DA1	DA0	SEG/VLCD pin can be set via the DE bit. internal voltage adjustment can be set via the VE bit. DA3~DA0 bits can be used to adjust the VLCD output voltage.	W	30H

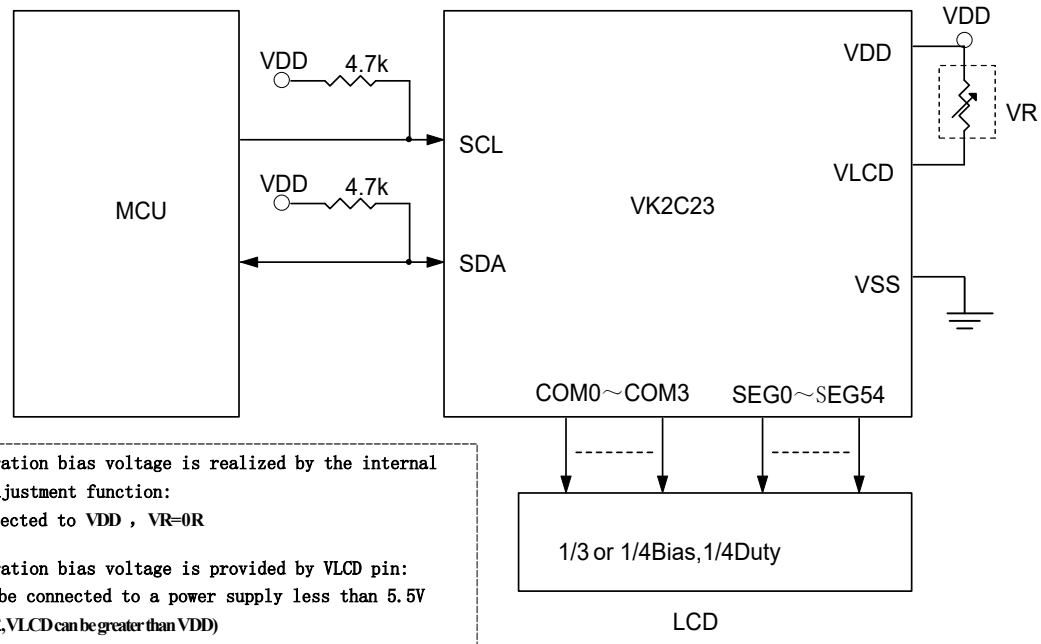
Note:

Bit 5 DE	Bit 4 VE	SEG 55/VLCD shared pin sel	internal voltage adjustment	Note
0	0	VLCD pin	off	● the bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VLCD。 ● The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VDD. ● VLCD pin is connected to the VDD pin, the internal voltage must be disabled by set DA3~DA0 as"0000".
0	1	VLCD pin	on	● When VCCA2 is connected to VLCD, internal voltage adjustment can not be used to adjust internal bias voltage. (Bias voltage is supplied by the external VLCD pin) ● When VCCA2 is connected to VDD, internal voltage adjustment can not be used to adjust internal bias voltage when VLCD pin is supplies with external voltage. (Recommend: can not be used) ● When VCCA2 is connected to VDD, internal voltage adjustment can be used to adjust internal bias voltage when VLCD pin is floating and internal voltage adjustment is enable.(Bias is supplied by internal voltage adjustment).
1	0	SEG55 pin	off	● The bias voltage is supplied by the external VLCD pin when VCCA2 is connected to VLCD. ● The bias voltage is supplied by the external VDD pin when VCCA2 is connected to VDD ● The internal voltage-follower (OP4) is disabled automatically and DA3~DA0 don't care.
1	1	SEG55 pin	on	● When VCCA2 is connected to VLCD, internal voltage adjustment can be used to adjust internal bias voltage when VLCD pin is supplies with external voltage and internal voltage adjustment is enable. (Bias voltage is supplied by the internal voltage adjustment) ● When VCCA2 is connected to VDD, internal voltage adjustment can be used to adjust internal bias voltage when internal voltage adjustment is enable.(Bias voltage is supplied by the internal voltage adjustment)

- Power-on: Enable internal voltage Adjustment and the SEG/VLCD pin is set as the segment pin.
- When the DA0~DA3 bits are set to "0000", the internal voltage is disabled.
- When the DA0~DA3 bits are set to other values except "0000", internal voltage follower is enabled.

5 Application Circuits

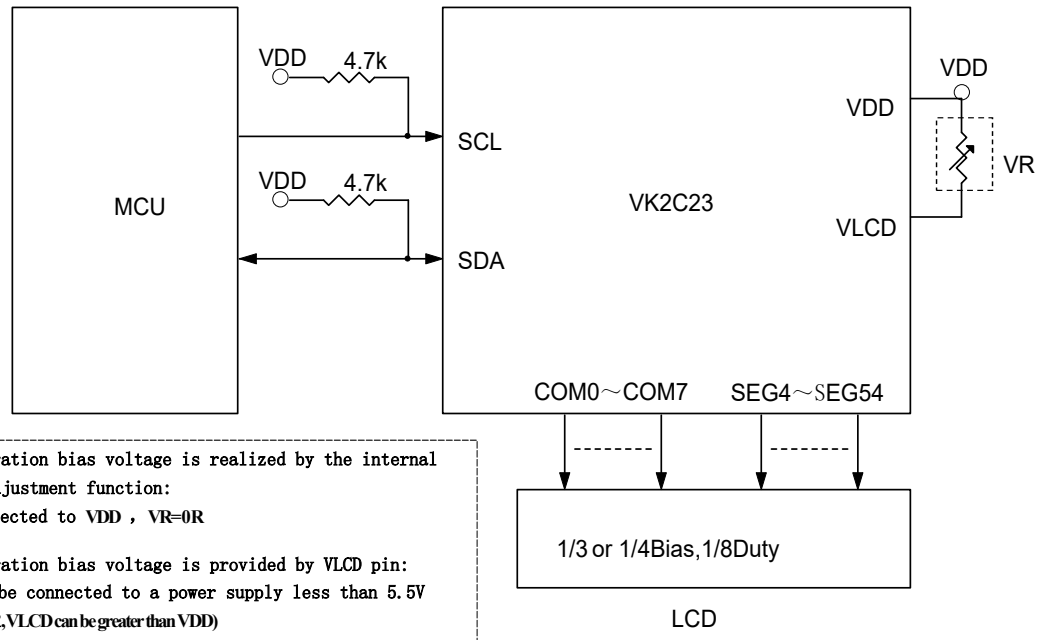
1/4DUTY



1. Configuration bias voltage is realized by the internal voltage adjustment function:
VLCD connected to VDD , VR=0R

2. configuration bias voltage is provided by VLCD pin:
(VLCD can be connected to a power supply less than 5.5V through VR,VLCD can be greater than VDD)
Note: Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

1/8DUTY



1. Configuration bias voltage is realized by the internal voltage adjustment function:
VLCD connected to VDD , VR=0R

2. configuration bias voltage is provided by VLCD pin:
(VLCD can be connected to a power supply less than 5.5V through VR,VLCD can be greater than VDD)
Note: Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

6 Electrical characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	TSTG	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

6.2 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.5	V	—	—
Operating current	I_{DD1}	—	25	40	μA	3V	No load, VLCD=VDD, 1/3 bias, f_{LCD}=80Hz, LCD on, Internal osc on, DA0~DA3 ="0000"
		—	35	50		5V	
Operating current	I_{DD2}	—	2	5	μA	3V	No load, VLCD=VDD, 1/3 bias, f_{LCD}=80Hz, LCD off, Internal osc on, DA0~DA3 = "0000"
		—	4	10		5V	
Standby Current	I_{STB}	—	—	1	μA	3V	No load, VLCD=VDD, LCD off, Internal osc off
		—	—	2		5V	
Input Low Voltage	V_{IL}	0	—	0.3	VDD	3V	SCL, SDA
						5V	
Input High Voltage	V_{IH}	0.7	—	1.0	VDD	3V	SCL, SDA
						5V	
Low Level Output Current	I_{OL}	3.0	—	—	mA	3V	V_{OL}=0.4V, SDA
		6.0	—	—		5V	
LCD COM Sink Current	I_{OL1}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH1}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL2}	250	400	—	μA	3V	V_{OL}=0.3V
		500	800	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH2}	-140	-230	—	μA	3V	V_{OH}=2.7V
		-300	-500	—		5V	V_{OH}=4.5V

6.3 AC Characteristics

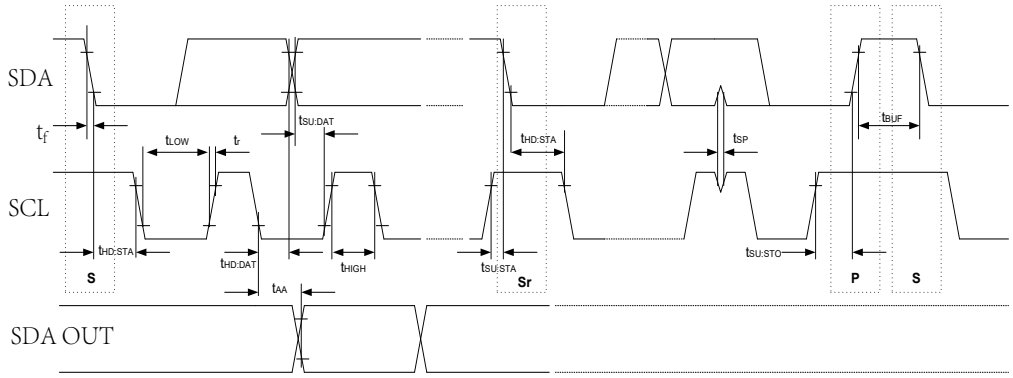
Frame Frequency

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	f_{LCD1}	72	80	88	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	f_{LCD2}	144	160	176	Hz	4.0V	1/4 duty,25℃
LCD Frame Frequency	f_{LCD3}	52	80	124	Hz	4.0V	1/4 duty,-40 ~ +85℃
LCD Frame Frequency	f_{LCD4}	104	160	248	Hz	4.0V	1/4 duty,-40 ~ +85℃

I2C parameter

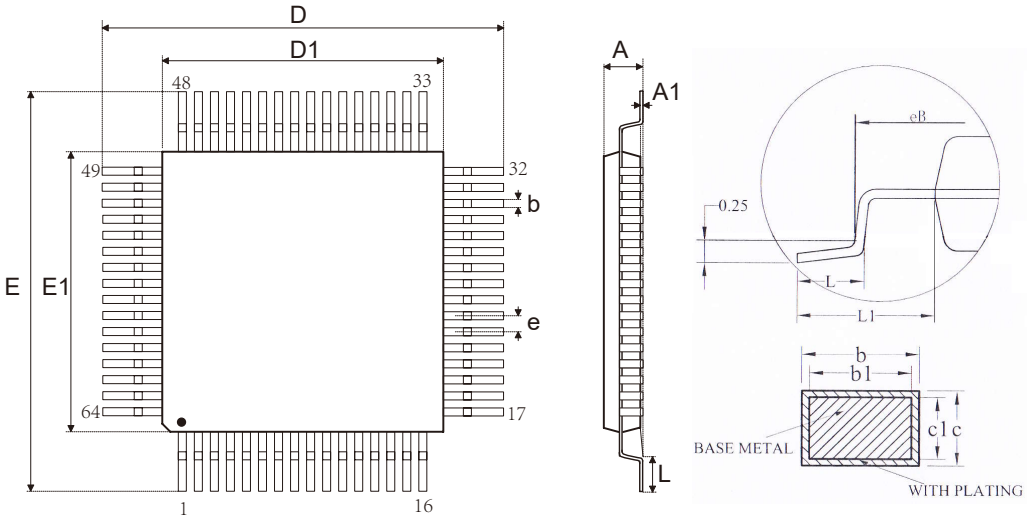
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD: STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU: STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD: DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU: DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU: STO}$	0.6	—	—	μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing



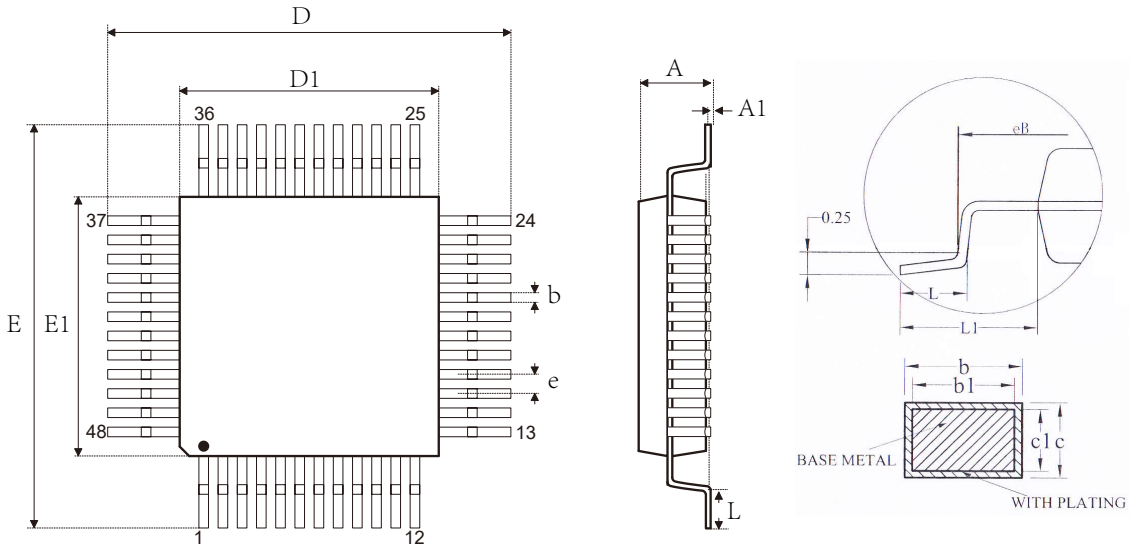
7 Package Information

7.1 LQFP64(7.0mm x 7.0mm PP=0.4mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
b	0.16	--	0.24
b1	0.15	0.18	0.21
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.40BSC		
L	0.45	--	0.75
L1	1.00REF		

7.2 LQFP48(7.0mm x 7.0mm PP=0.5mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	0.05	--	0.15
b	0.18	--	0.26
b1	0.17	0.20	0.23
c	0.13	--	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
L	0.45	--	0.75
L1	1.00REF		

8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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