

## Features

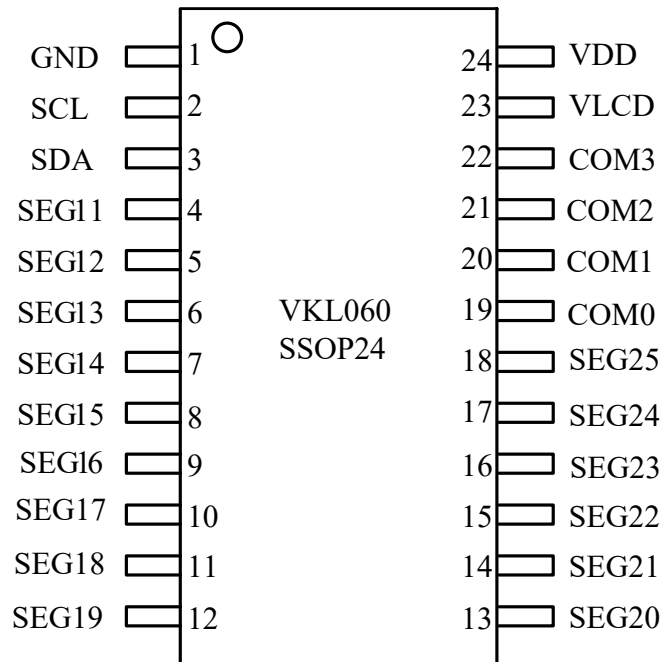
- Operating voltage: 2.5-5.5V
- Built-in 32kHz RC oscillator
- Selection of 1/2 or 1/3 bias
- 1/4duty(4COM)
- Built-in 15x4 bits display RAM
- 80Hz Frame Frequency
- STANDBY mode (by System Set Command LCD OFF)
- Four power consumption modes can be configured
- I2C bus interface
- Display mode 15x4
- Versatile blinking modes
- Software configuration LCD parameters
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage( $\leq (VDD-VLCD)$ )
- Built-in power on reset circuit (POR) — TEST2 =0 enable
- Low power consumption、 High anti-interference
- Package:  
SSOP24L(150mil) (8.65mm x 3.9mm PP=0.635mm).....

## 1 General Description

VKL060 is a RAM Mapping LCD Driver , It can support LCD screens with a maximum of 60 pattern(15SEGx4COM) .The device communicates with host microcontrollers via a two-line bidirectional I2C bus,it is used to configure display parameters and transfer display data , , and can also enter the standby mode through System Set Command .Four power consumption modes can be configured. With the characteristics of high anti-interference and low power consumption, it is suitable for water electrical meters and industrial control instruments.

## 2 Pinouts and pin description

### 2.1 VKL060 SSOP24 Pin Assignment

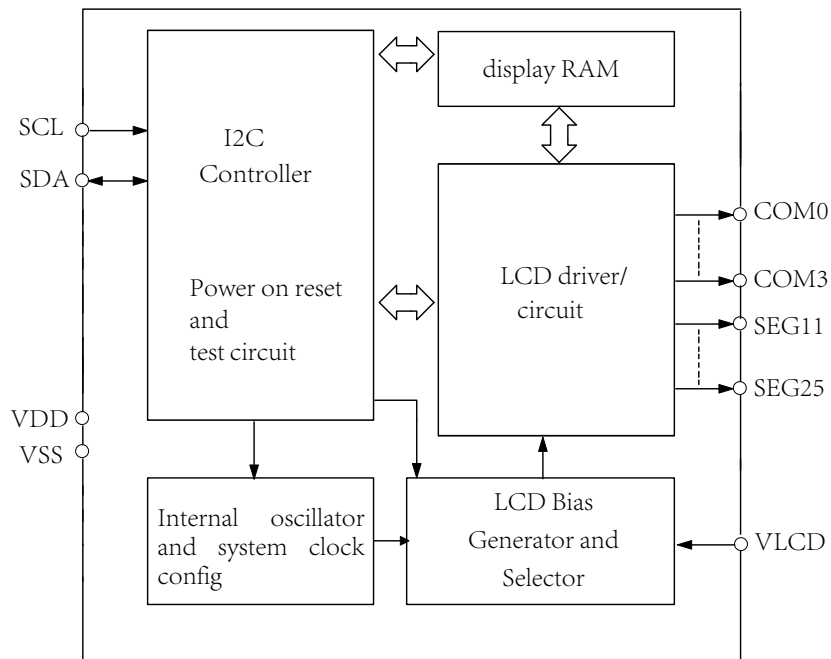


## 2.2 VKL060 SSOP24 Pin Description

No.	Name	I/O	Function
1	GND	GND	Negative power supply
2	SCL	I	Serial Clock Input for I2C interface
3	SDA	I/O	Serial Data Input/Output for I2C interface
4-18	SEG11-SEG25	O	LCD SEG outputs
19-22	COM0-COM3	O	LCD COM outputs
23	VLCD	I	LCD power input=(VDD-VLCD)
24	VDD	VDD	Positive power supply

## 3 Functional Description

### 3.1 Block diagram



## 3.2 Display RAM

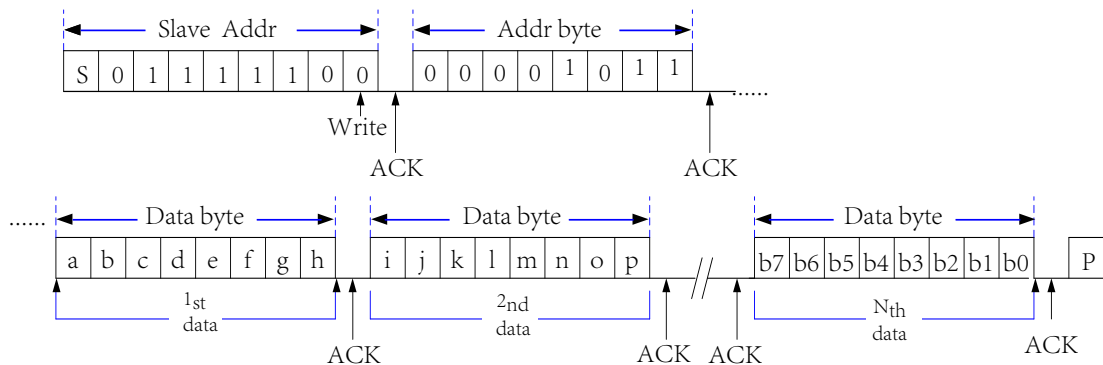
The static display memory (RAM) is organized into  $15 \times 4$  bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the I2C bus interface.

The following is a mapping from the RAM to the LCD pattern:

OUTPUT	COM3	COM2	COM1	COM0	ADDR	OUTPUT	COM3	COM2	COM1	COM0	ADDR
SEG12	h	g	f	e	0x0C	SEG11	d	c	b	a	0x0B
SEG14	p	o	n	m	0x0E	SEG13	l	k	j	i	0x0D
SEG16					0x10	SEG15					0x0F
SEG18					0x12	SEG17					0x11
SEG20					0x14	SEG19					0x13
SEG22					0x16	SEG21					0x15
SEG24					0x18	SEG23					0x17
						SEG25					0x19
Data	bit7	bit6	bit5	bit4			bit3	bit2	bit1	bit0	

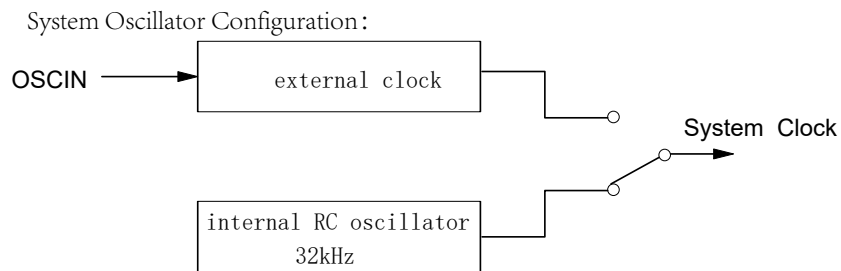
### RAM Mapping of $15 \times 4$

For example, display data seg10-seg14 shown in the table above and the data a-p written to the display RAM is as follows:



### 3.3 System Oscillator

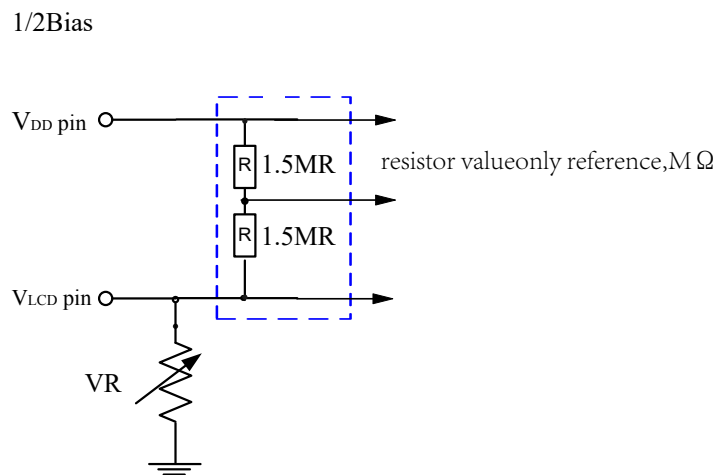
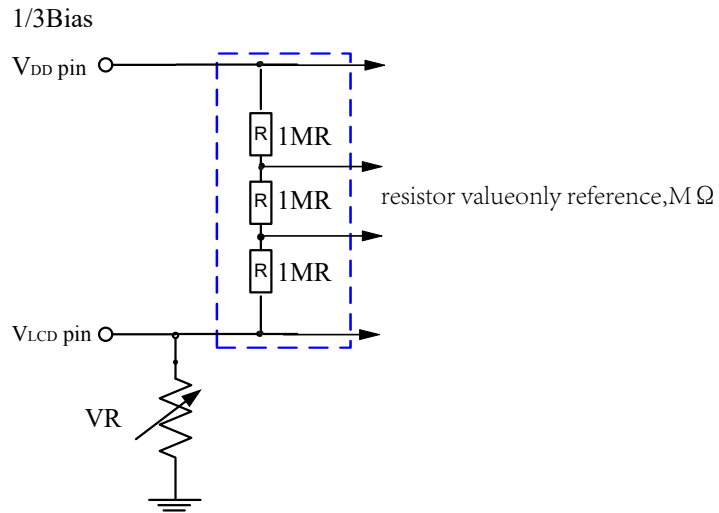
The timing for the internal logic and the LCD drive signals are generated by an internal oscillator(32kHz) or an external clock source(OSCIN). The system clock frequency ( $f_{SYS}$ ) determines the LCD frame frequency.



### 3.4 LCD operating voltage

It can be obtained through VLCD pin (connected a resistor to VSS pin), LCD operating voltage =  $V_{DD} - V_{LCD}$ , and built-in op amplifier to realize low-power driving.

VR is used to adjust the contrast, use  $1M\Omega$  resistor to adjust to the best display effect, and take the resistance value at this time.





### 3.5 Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. Data transfers on the I2C bus should be avoided for 1 ms following power-on.

The status of the internal circuits after initialization is as follows:

All COM/SEG outputs are set to VDD

1/4 duty and 1/3 bias.

The System Oscillator and the LCD bias generator are off state

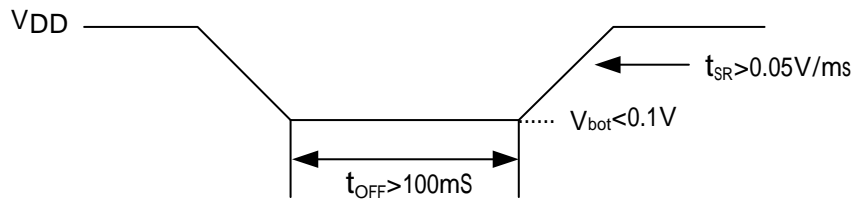
LCD Display is off state.

Blinking function is switched off .

When powered on, TEST2 pin is low-level enabling POR.

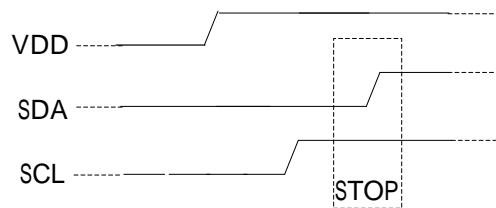
if VDD drops below the minimum voltage of operating voltage specification during operation, the power-on reset timing conditions must be also satisfied. This means that VDD must fall to 0V and remain at 0V for a minimum time of 100ms before rising to the normal operating voltage.

Power-on Reset Timing



When power on, TEST2 pin is high-level and POR is disable. In order to make the internal circuit in the reset state, it must be configured as follows:

- I. The stop condition is that when SCL = h, SDA changes from L to H
- II. Set soft reset in System set command (bit1=1)



### 3.6 LCD Communication Command

The display modes supported by the LCD driver are 15SEG x 4COM, The unused SEG or COM outputs should be left open. The frame frequency can be configured as 4 frequencies, and the default is 80Hz when powered on.

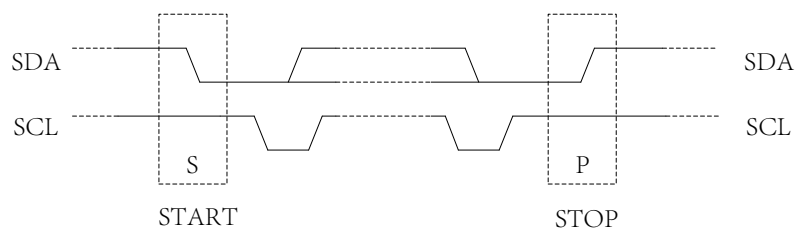
Configure display parameters and read / write display data through I2C interface.

#### 3.6.1 I2C Serial Interface

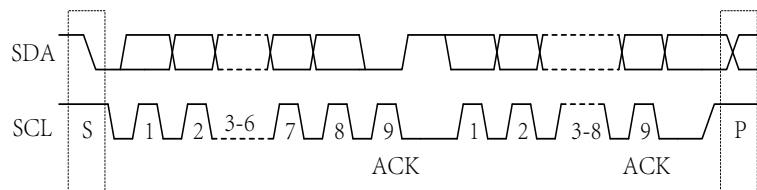
The device supports I2C serial interface.

The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7k. When the bus is free, both lines are high.

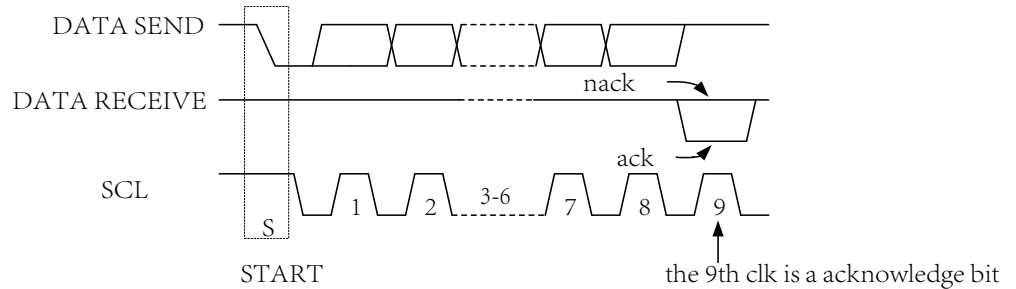
##### START and STOP



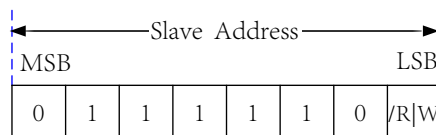
##### Byte Format



##### Acknowledge



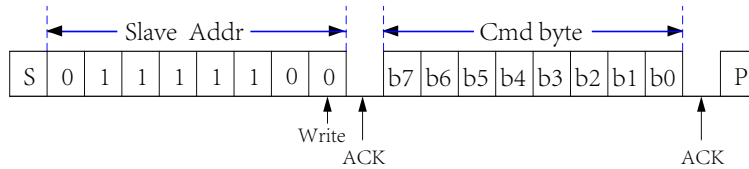
##### Slave Address (0x7c) bit0-R/W



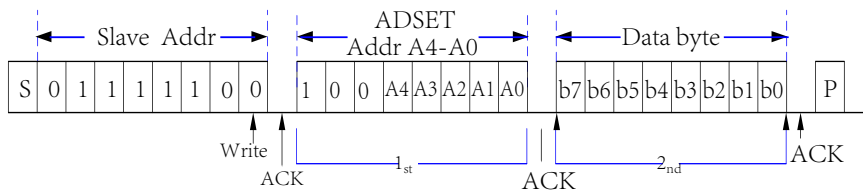
### 3.6.2 I2C Command Format

#### Write Operation

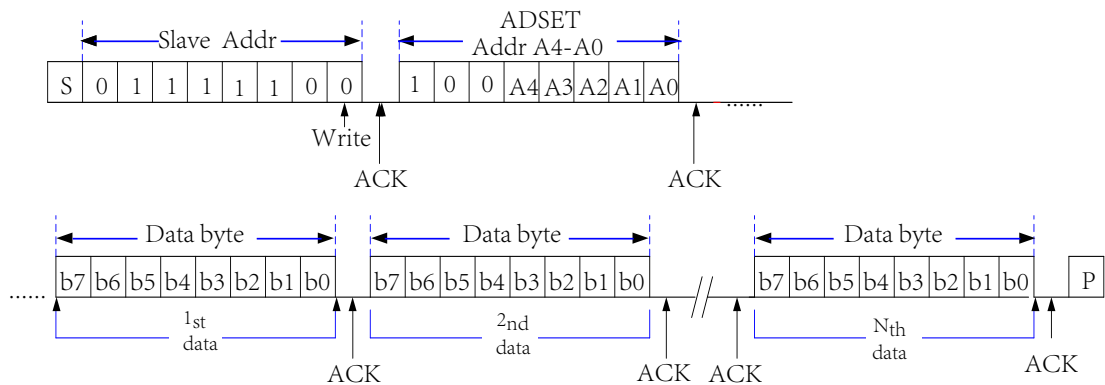
##### Write command



##### Display RAM Single Data Byte

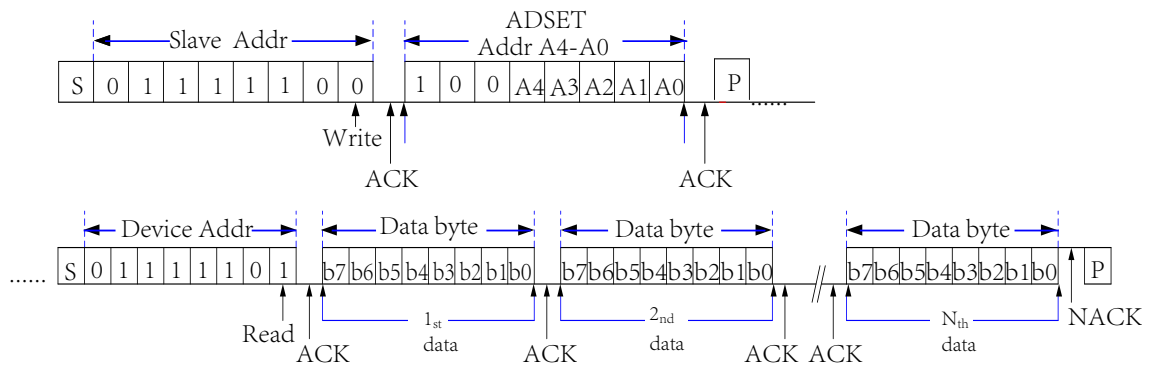


##### Display RAM Page Write Operation

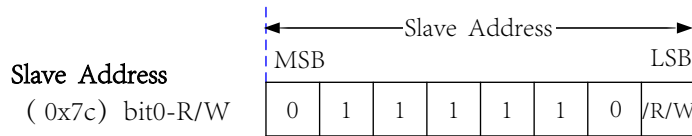


#### Read Operation

##### Display RAM Page Read Operation



### 3.6.3 Command Description



bit7 next byte is data (D) or command(C):  
 bit7=0 next byte is data, bit7=1 next byte is command

#### 3.6.3.1 Mode Set Command

Set working mode:

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	0	X	E	M0	X	X		W	

Bit 3	LCD On/Off
<b>E</b>	
0	
1	ON

Bit 2	BIAS
<b>M0</b>	
0	
1	1/2 bias

#### 3.6.3.2 System Set Command

Select the internal system oscillat or external clock and set soft reset.

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	1	0	1	0	R	CLKS		W	

Bit 1	soft reset
<b>R</b>	
0	
1	soft reset

Bit 0	System clock source
<b>CLKS</b>	
0	
1	external clock OSCIN

### 3.6.3.3 Address Set Command

Display start address set:

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	R/W	Def
Address pointer	1	C/D	0	0	A4	A3	A2	A1	A0	W	

Bit4-0 A4-A0	Display address
01011	0x0B (Def)
01100	0x0C
01101	0x0D
.....	.....
11001	0x19

### 3.6.3.4 All Pixel On /Off Command

LCD All Pixel On /Off set:

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	1	1	1	1	AP1	AP0		W	

Bit 1 AP1	Bit 0 AP0	All Pixel On /Off
0	0	Normal (Def)
0	1	All Pixel Off
1	0	All Pixel On
1	1	All Pixel Off

Note:

- 1.This command does not affect the content display of RAM
- 2.This command is valid only when the LCD ON

### 3.6.3.5 Blinking Frequency Command

Set the blinking frequency

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq set	1	C/D	1	1	1	0	0	BK1	BK0		W	

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off <b>(Def)</b>
0	1	0.5Hz
1	0	1Hz
1	1	2Hz

### 3.6.3.6 Display Control Command

Set LCD Driver Mode, Frame Frequency and 4 Power Modes

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display Control Set	1	C/D	0	1	FR1	FR0	DM	SR1	SR0		W	

Bit 4	Bit 3	Frame Frequency
FR1	FR0	
0	0	80Hz <b>(Def)</b>
0	1	71Hz
1	0	64Hz
1	1	53Hz

Bit 2	Driver Mode
DM	
0	Line Flip <b>(Def)</b>
1	Frame Flip

Bit 1	Bit 0	Power Modes	Power Diss
SR1	SR0		
0	0	low power mode1 (LP1)	x0.5
0	1	low power mode2 (LP2)	0.67
1	0	normal (NP) <b>(Def)</b>	1.0
1	1	high power mode(HP)	1.8

Operating current :

- 80Hz>71Hz>64Hz>53Hz
- Line Flip>Frame Flip
- high power>normal>low power mode2>low power mode1
- power consumption data is only for reference and is also related to the LCD used

Different display control commands have different display effects, as shown in the following table:

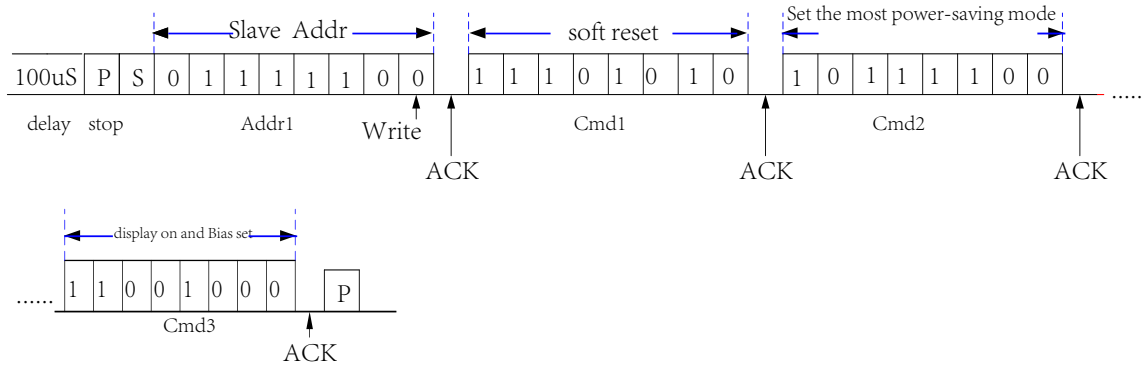
display control	tremble	Display effect/contrast
frame freq	V	---
drive mode	V	V
power mode	---	V
The impact is not absolute, but also related to the LCD used.		

## 4 Command application

### 4.1 Start Sequence

During power on, the power on reset sequence shall be met. After power on, the parameters shall be configured first.

Config parameters through a series of commands. The command sequence is as follows:

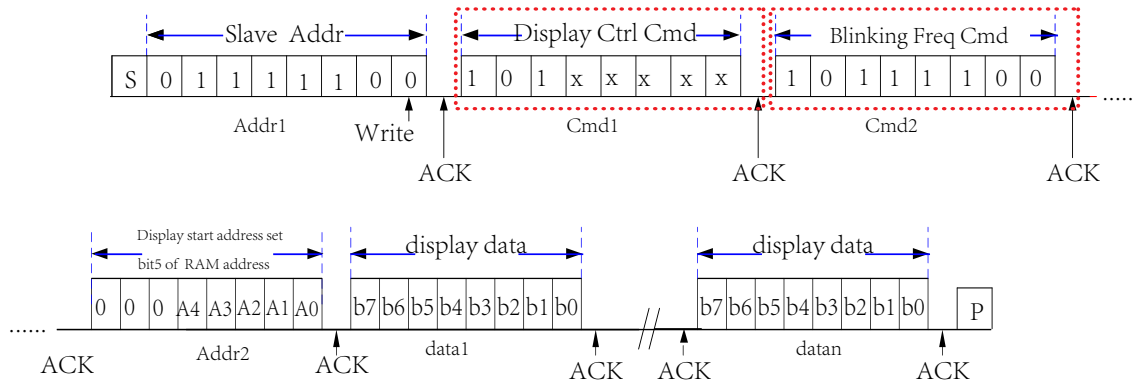


power on:	power sequence
delay:	Delay 100uS for chip initialization
STOP:	Send I2C stop signal
START:	Send I2C start signal
Addr1:	Send slave address (0x7c)
Cmd1:	System Set Cmd -SOFT reset (0xEA)
Cmd2:	Display Control Cmd -For example, set to the most power-saving mode (0xBC)
Cmd3:	Mode Set Command -display on and bias set.For example, 1/3bias,display on (0xC8)
STOP	Send I2C stop signal



## 4.2 Display Control Command

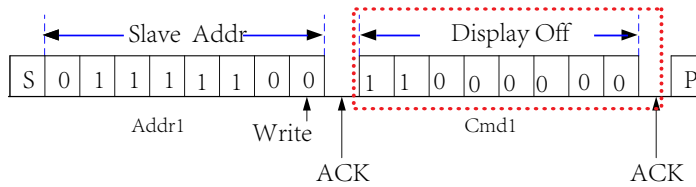
The display control has been configured during initialization and does not need blinking. Only display data need to be sent.



- START: Send I2C start signal
- Addr1: Send slave address (0x7c)
- Cmd1: Display Ctrl Cmd - do not need to send this byte when the display configuration has not changed
- Cmd2: Blinking Freq Cmd - blink does not need and this byte does not need to be sent
- Addr2: Address Set Cmd - Display start address set (0x0B)
- Data1-Datan: Send display data 0x00 to display RAM (up to 8 bytes)
- STOP: Send I2C stop signal

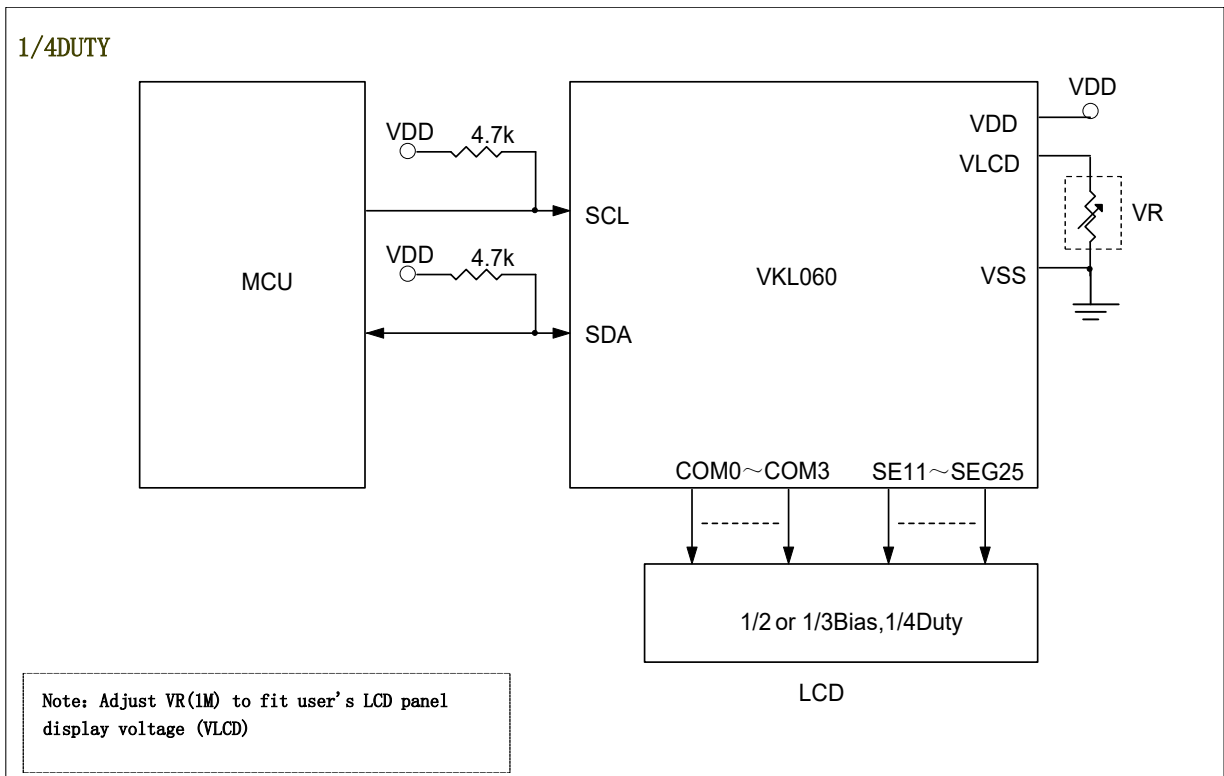
### 4.3 Display Off

Other commands can also refer to this format.



- START: Send I2C start signal
- Addr1: Send slave address (0x7c)
- Cmd1: Mode set command -Display Off (0xC0)
- STOP: Send I2C stop signal

## 5 Application Circuits



## 6 Electrical characteristics

### 6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3~6.5	V
Input Voltage	VIN	$V_{SS}-0.3 \sim V_{DD}+0.3$	V
Storage Temperature	TSTG	-50~+125	°C
Operating Temperature	TOTG	-40~+85	°C

### 6.2 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.5	—	5.5	V	—	—
Operating current	I <sub>DD1</sub>	—	7.5	20	μA	3V	VDD=3.3V, 25°C, 1/3bias, power save model (LP1), frame freq 80Hz, FRAME flip
Standby Current	I <sub>STB</sub>	—	0.5	5	μA	3V	LCD off, Internal osc off
VLCD pin voltage *1	VLCD	0	—	VDD-2.4	V	3V	VDD-VLCD>=2.5V
Input Low Voltage	V <sub>IL</sub>	0	—	0.3	VDD	3V 5V	SCL, SDA
Input High Voltage	V <sub>IH</sub>	0.7	—	1.0	VDD	3V 5V	SCL, SDA
Low Level input Current	I <sub>IL</sub>	-1	—	—	μA	3V	---
High Level input Current	I <sub>IH</sub>	—	—	1	μA	3V	---
LCD ON resistor	R <sub>ON</sub>	—	3	—	kΩ	3V	I <sub>load</sub> =±10uA

\*1 LCD voltage=VDD-VLCD

## 6.3 AC Characteristics

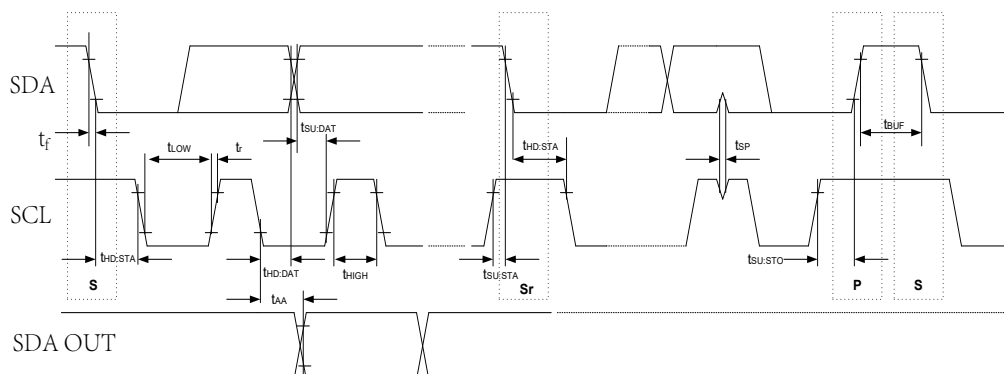
### Frame Frequency

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	$f_{LCD1}$	56	80	104	Hz	3.3V	80Hz, -40 ~ +85 °C
LCD Frame Frequency	$f_{LCD2}$	49	71	93	Hz	3.3V	71Hz, -40 ~ +85 °C
LCD Frame Frequency	$f_{LCD3}$	44	64	84	Hz	3.3V	64Hz, -40 ~ +85 °C
LCD Frame Frequency	$f_{LCD4}$	37	53	69	Hz	3.3V	53Hz, -40 ~ +85 °C

### I2C parameter

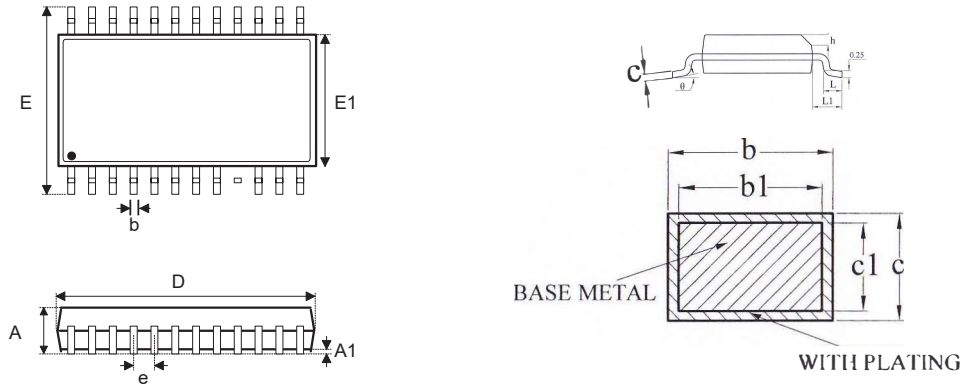
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	$f_{SCL}$	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	$t_{BUF}$	1.3	—	—	$\mu$ s	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	$\mu$ s	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	$t_{LOW}$	1.3	—	—	$\mu$ s	3.0-5.5V	—
SCL High Time	$t_{HIGH}$	0.6	—	—	$\mu$ s	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	$\mu$ s	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	$t_R$	—	—	0.3	$\mu$ s	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	$t_F$	—	—	0.3	$\mu$ s	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—	—	$\mu$ s	3.0-5.5V	—
Output Valid from Clock	$t_{AA}$	—	—	0.9	$\mu$ s	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin)	$t_{SP}$	—	—	50	ns	3.0-5.5V	Noise suppression time

### I<sup>2</sup>C Timing



## 7 Package Information

### 7.1 SSOP24L(150mil)(8.65mm × 3.90mm PP=0.635mm)



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
b	0.23	—	0.31
b1	0.22	0.25	0.28
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

## 8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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