Features

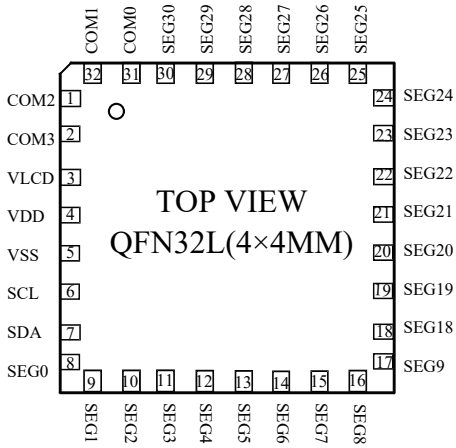
- Operating voltage:2.5-5.5V
- Built-in 32kHz RC oscillator
- Selection of 1/2 or 1/3 bias
- 1/4duty(4COM)
- 80Hz Frame Frequency
- STANDBY mode （by System Set Command LCD OFF）
- Four power consumption modes can be configured
- I2C bus interface
- Display mode 23x4
- Versatile blinking modes
- Software configuration LCD parameters
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage(≤(VDD-VLCD))
- Built-in power on reset circuit (POR) - TEST2 =0 enable
- Low power consumption、 High anti-interference
- Package:
  QFN32 (4.0mm x 4.0mm PP=0.4mm)

1 General Description

VKL092Q is a RAM Mapping LCD Driver， It can support LCD screens with a maximum of 92 pattern(23SEGx4COM) .The device communicates with host microcontrollers via a two-line bidirectional I2C bus,it is used to configure display parameters and transfer display data, , and can also enter the standby mode through System Set Command .Four power consumption modes can be configured.With the characteristics of high anti-interference and low power consumption, it is suitable for water electrical meters and industrial control instruments.

2 Pinouts and pin description

2.1 VKL092Q QFN32L Pin Assignment

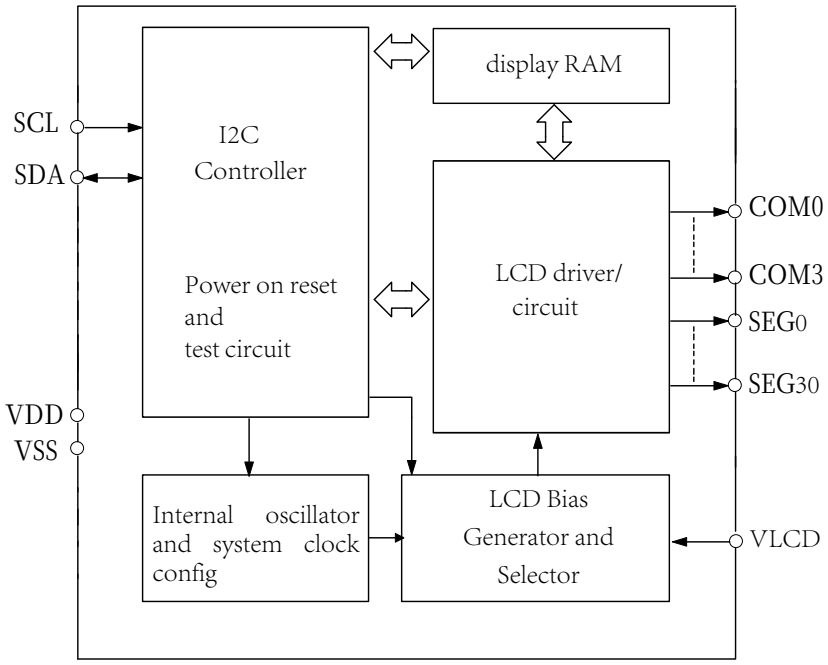


2.2 VKL092L QFN32L Pin Description

No.	Name	I/O	Function
31,32 1,2	COM0-COM3	O	LCD COM outputs
3	VLCD	I	LCD power input=(VDD-VLCD)
4	VDD	VDD	Positive power supply
5	GND	GND	Negative power supply
6	SCL	I	Serial Clock Input for I2C interface
7	SDA	I/O	Serial Data Input/Output for I2C interface
8-30	SEG0-SEG30	O	LCD SEG outputs

3 Functional Description

3.1 Block diagram



3.2 Display RAM

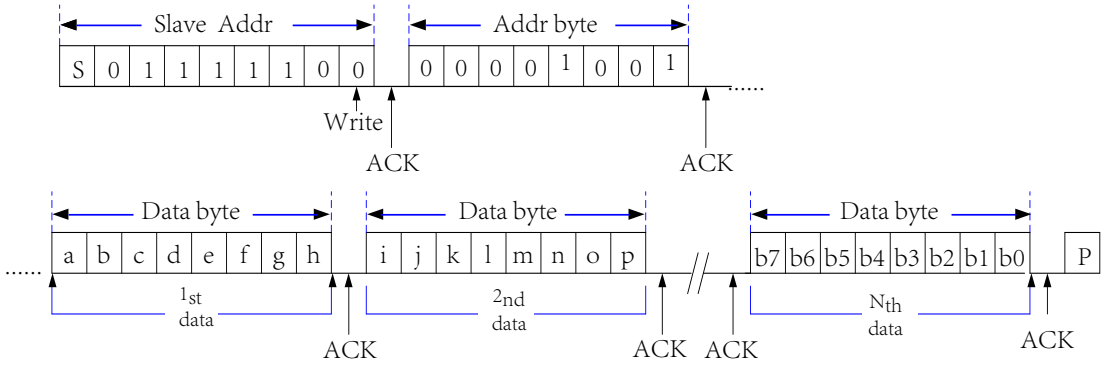
The static display memory (RAM) is organized into 32×4 bits and stores the displayed data. The contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the I2C bus interface.

The following is a mapping from the RAM to the LCD pattern:

	COM3	COM2	COM1	COM0	ADD		COM3	COM2	COM1	COM0	ADD
SEG1	h	g	f	e	0x01	SEG0	d	c	b	a	0x00
SEG3	p	o	n	m	0x03	SEG2	l	k	j	i	0x02
SEG5					0x05	SEG4					0x04
SEG7					0x07	SEG6					0x06
SEG9					0x09	SEG8					0x08
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
						SEG30					0x1E
显示数据	bit7	bit6	bit5	bit4			bit3	bit2	bit1	bit0	

RAM Mapping

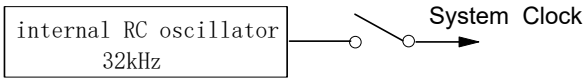
For example, display data seg9-seg12 shown in the table above and the data a-p written to the display RAM is as follows:



3.3 System Oscillator

The timing for the internal logic and the LCD drive signals are generated by an internal oscillator(32kHz) or an external clock source(OSCIN). The system clock frequency (fSYS) determines the LCD frame frequency.

System Oscillator Configuration：



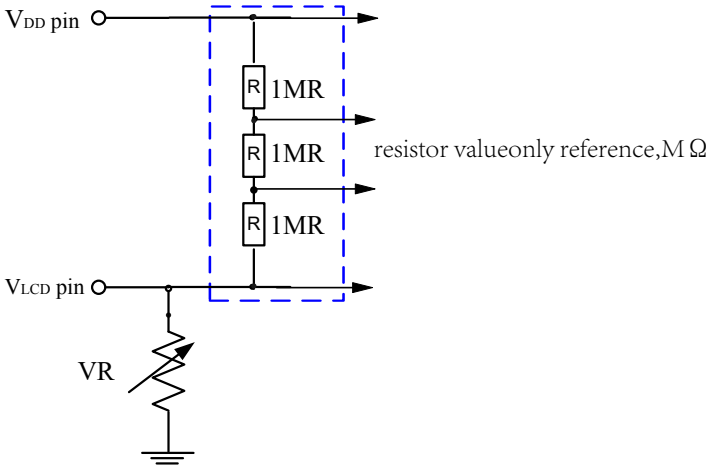
3.4 LCD operating voltage

It can be obtained through VLCD pin (connected a resistor to VSS pin), LCD operating voltage = VDD-VLCD, and built-in op amplifier to realize low-power driving.

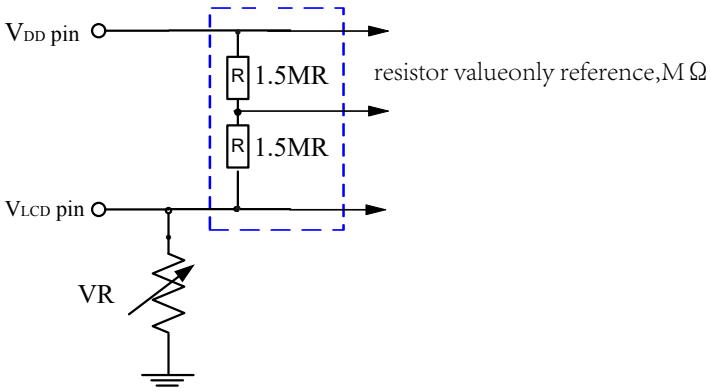
VR is used to adjust the contrast, use 1MΩ resistor to adjust to the best

VR is used to adjust the contrast, use 1MΩ resistor to adjust to the best display effect, and take the resistance value at this time.

1/3Bias



1/2Bias



3.5 Power-On Reset

When the power is applied, the device is initialized by an internal power-on reset circuit. Data transfers on the I2C bus should be avoided for 1 ms following power-on.

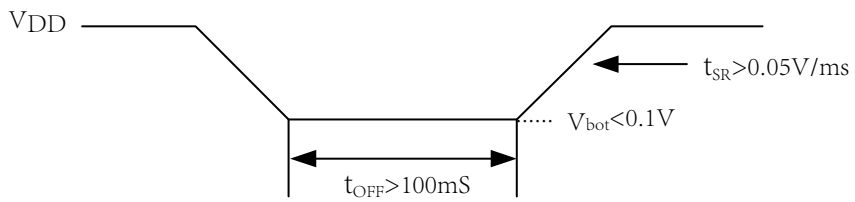
The status of the internal circuits after initialization is as follows:

- All COM/SEG outputs are set to VDD
- 1/4 duty and 1/3 bias.
- The System Oscillator and the LCD bias generator are off state
- LCD Display is off state.
- Blinking function is switched off

When powered on, TEST2 pin is low-level enabling POR.

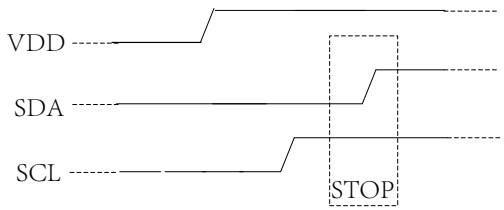
if VDD drops below the minimum voltage of operating voltage specification during operation, the power-on reset timing conditions must be also satisfied. This means that VDD must fall to 0V and remain at 0V for a minimum time of 100ms before rising to the normal operating voltage.

Power-on Reset Timing



When power on, TEST2 pin is high-level and POR is disable. In order to make the internal circuit in the reset state, it must be configured as follows:

I. The stop condition is that when SCL = h, SDA changes from L to H
II. Set soft reset in System set command （bit1=1）



3.6 LCD Communication Command

The display modes supported by the LCD driver are 23SEG x 4COM,The unused SEG or COM outputs should be left open.The frame frequency can be configured as 4 frequencies, and the default is 80Hz when powered on.

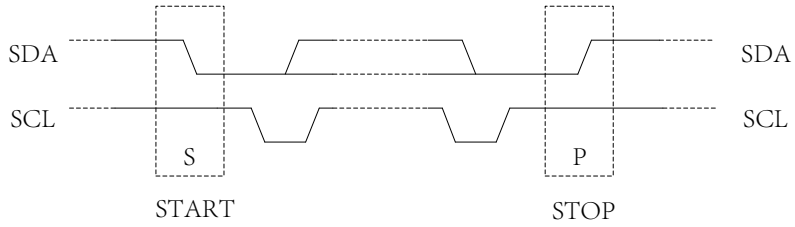
Configure display parameters and read / write display data through I2C interface.

3.6.1 I2C Serial Interface

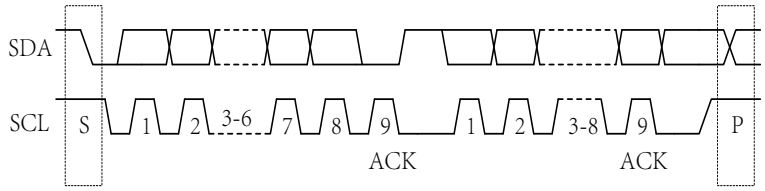
The device supports I2C serial interface.

The two lines are a serial data line, SDA, and a serial clock line, SCL. Both lines are connected to the positive supply via pull-up resistors with a typical value of 4.7k. When the bus is free, both lines are high.

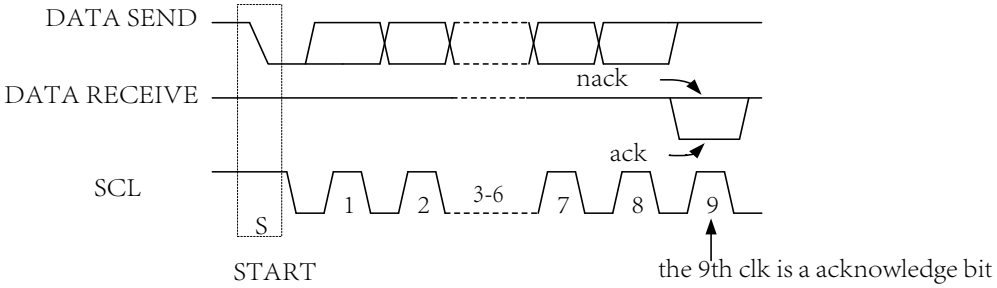
START and STOP



Byte Format

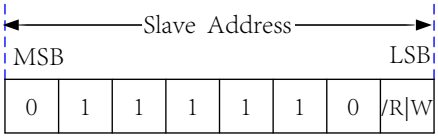


Acknowledge



Slave Address

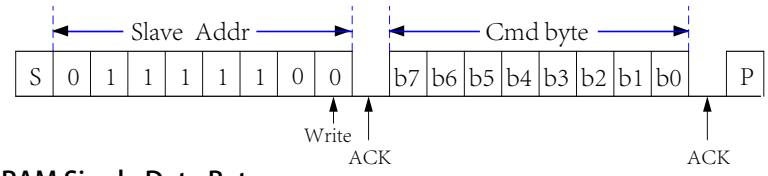
(0x7c) bit0-R/W



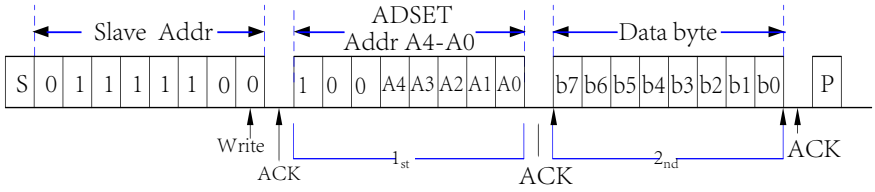
3.6.2 I2C Command Format

Write Operation

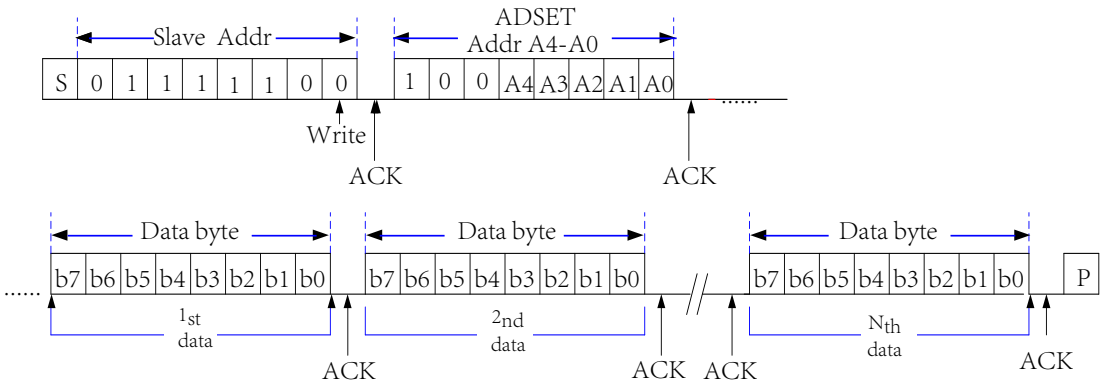
Write command



Display RAM Single Data Byte

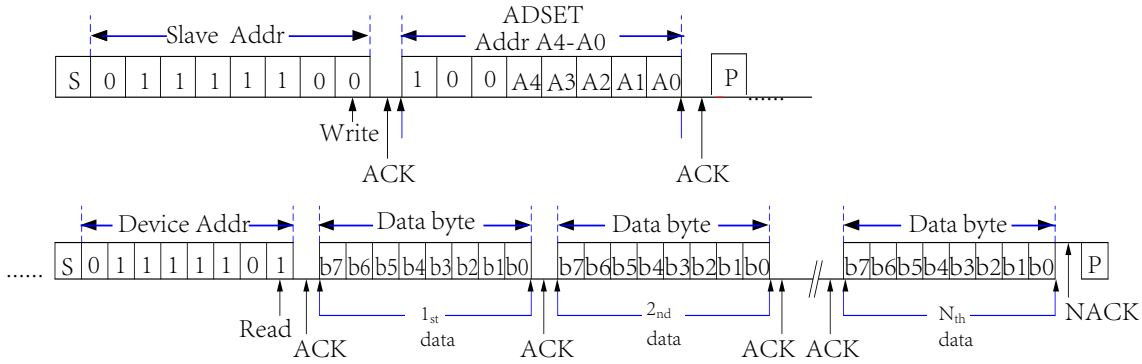


Display RAM Single Data Byte



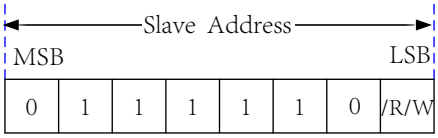
Read Operation

Display RAM Page Read Operation



3.6.3 Command Description

Slave Address
(0x7c) bit0-R/W



bit7 next byte is data (D) or command(C):
bit7=0 next byte is data,bit7=1 next byte is command

3.6.3.1 Mode Set Command

Set working mode:

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	0	X	E	M0	X	X		W	

Bit 3 E	LCD On/Off
0	OFF (Def)
1	ON

Bit 2 M0	BIAS
0	1/3 bias (Def)
1	1/2 bias

3.6.3.2 System Set Command

Select the internal system oscillator external clock and set soft reset.

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	1	0	1	0	R	CLKS		W	

Bit 1 R	soft reset
0	--- (Def)
1	soft reset

Bit0 CLKS	System clock source
0	internal oscillator(Def)
1	external cloclk OSCIN

3.6.3.3 Address Set Command

Display start address set:

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
address pointer	1	C/D	0	0	A4	A3	A2	A1	A0		W	

Bit4-0 A4-A0	Display address
01001	0x09 (Def)
01010	0x0A
01011	0x0B
.....	.....
11011	0x1B

3.6.3.4 All Pixel On /Off Command

LCD All Pixel On /Off set:

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Address pointer	1	C/D	1	1	1	1	1	AP1	AP0		W	

Bit 1 AP1	Bit 0 AP0	All Pixel On /Off
0	0	Normal (Def)
0	1	All Pixel Off
1	0	All Pixel On
1	1	All Pixel Off

Note:
1.This command does not affect the content display of RAM
2.This command is valid only when the LCD ON

3.6.3.5 Blinking Frequency Command

Set the blinking frequency

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
blinking freq set	1	C/D	1	1	1	0	0	BK1	BK0		W	

Bit 1	Bit 0	blinking freq
BK1	BK0	
0	0	blinking off (Def)
0	1	0.5Hz
1	0	1Hz
1	1	2Hz

3.6.3.6 Display Control Command

Set LCD Driver Mode, Frame Frequency and 4 Power Modes

function	byte	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Note	R/W	Def
Display Control set	1	C/D	0	1	FR1	FR0	DM	SR1	SR0		W	

Bit 4	Bit 3	Frame Frequency
FR1	FR0	
0	0	80Hz (Def)
0	1	71Hz
1	0	64Hz
1	1	53Hz

Bit2	Driver Mode
DM	
0	Line Flip (Def)
1	Frame Flip

Bit 1	Bit 0	Power Modes	Power Diss
SR1	SR0		
0	0	low power mode1 (LP1)	x0.5
0	1	low power mode2 (LP2)	0.67
1	0	normal (NP) (Def)	1.0
1	1	high power mode (HP)	1.8

Operating current:

1. 80Hz>71Hz>64Hz>53Hz
2. Line Flip>Frame Flip
3. high power>normal>low power mode2>low power mode1
4. power consumption data is only for reference and is also related to the LCD used

Different display control commands have different display effects, as shown in the following table:

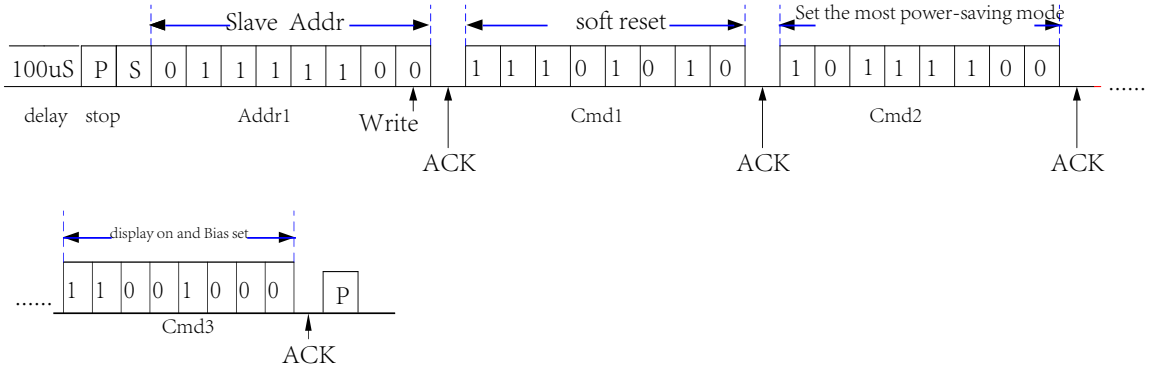
display control	tremble	Display effect/ contrast
frame freq	V	---
drive mode	V	V
power mode	---	V
The impact is not absolute, but also related to the LCD used.		

4 Command application

4.1 Start Sequence

During power on, the power on reset sequence shall be met. After power on, the parameters shall be configured first.

Config parameters through a series of commands. The command sequence is as follows:



power on: power sequence

delay: Delay 100uS for chip initialization

STOP: Send I2C stop signal

START: Send I2C start signal

Addr1: Send slave address (0x7c)

Cmd1: System Set Cmd -SOFT reset (0xEA)

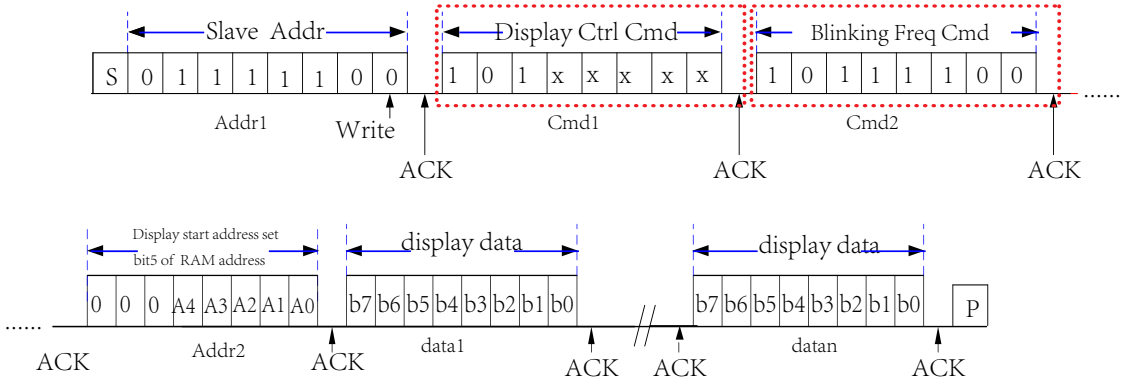
Cmd2: Display Control Cmd -For example, set to the most power-saving mode (0xBC)

Cmd3: Mode Set Command -display on and bias set.For example, 1/3bias,display on (0xC8)

STOP Send I2C stop signal

4.2 Display Control Command

The display control has been configured during initialization and does not need blinking. Only display data need to be sent.



START: Send I2C start signal

Addr1: Send slave address (0x7c)

Cmd1: Display Ctrl Cmd - do not need to send this byte when the display configuration has not changed

Cmd2: Blinking Freq Cmd - blink does not need and this byte does not need to be sent

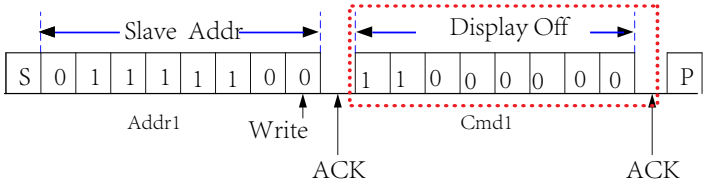
Addr2-Addr3: Address Set Cmd - Display start address set (0x09)

Data1-Datan: Send the display data to the set start address of the RAM and its subsequent address (up to 10 bytes)

STOP Send I2C stop signal

4.3 Display Off

Other commands can also refer to this format.



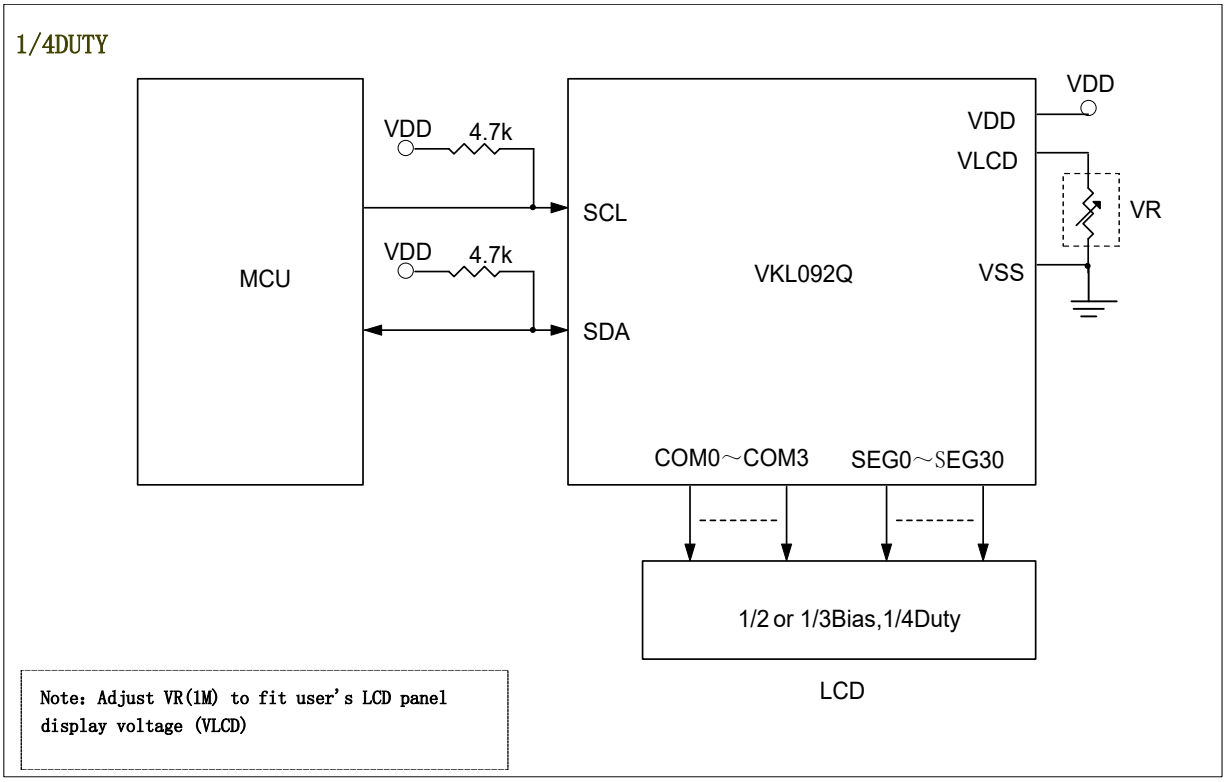
START: Send I2C start signal

Addr1: Send slave address (0x7c)

Cmd1: Mode set command -Display Off (0xC0)

STOP: Send I2C stop signal

5 Application Circuits



6 Hohfwulfdo fkdudfwhulvwlfv

6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～6.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	TSTG	-50～+125	℃
Operating Temperature	T_{OTG}	-40～+85	℃

6.2 DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.5	—	5.5	V	—	—
Operating current	I_{DD1}	—	7.5	20	μA	3V	VDD=3.3V,25℃,1/3bias, power save mode1(LP1)， frame freq 80Hz， FRAME flip
Standby Current	I_{STB}	—	0.5	5	μA	3V	LCD off, Internal osc off
VLCD pin voltage *1	VLCD	0	—	VDD-2.4	V	3V	VDD-VLCD>=2.5V
Input Low Voltage	V_{IL}	0	—	0.3	VDD	3V 5V	SCL, SDA
Input High Voltage	V_{IH}	0.7	—	1.0	VDD	3V 5V	SCL, SDA
Low Level input Current	I_{IL}	-1	—	—	μA	3V	---
High Level input Current	I_{IH}	—	—	1	μA	3V	---
LCD ON resistor	RON	—	3	—	kΩ	3V	I_{load}=±10uA

*1 LCD voltage=VDD-VLCD

6.3 AC Characteristics

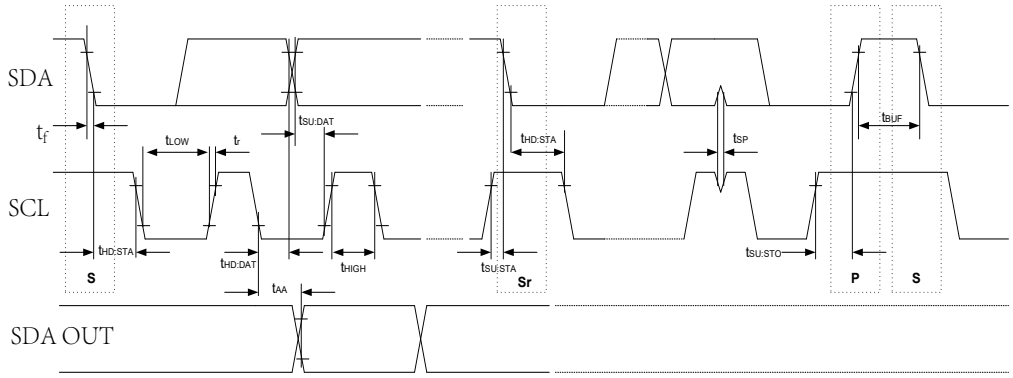
Frame Frequency

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
LCD Frame Frequency	f_{LCD1}	56	80	104	Hz	3.3V	80Hz,-40 ~ +85℃
LCD Frame Frequency	f_{LCD2}	49	71	93	Hz	3.3V	71Hz,-40 ~ +85℃
LCD Frame Frequency	f_{LCD3}	44	64	84	Hz	3.3V	64Hz,-40 ~ +85℃
LCD Frame Frequency	f_{LCD4}	37	53	69	Hz	3.3V	53Hz,-40 ~ +85℃

I2C parameter

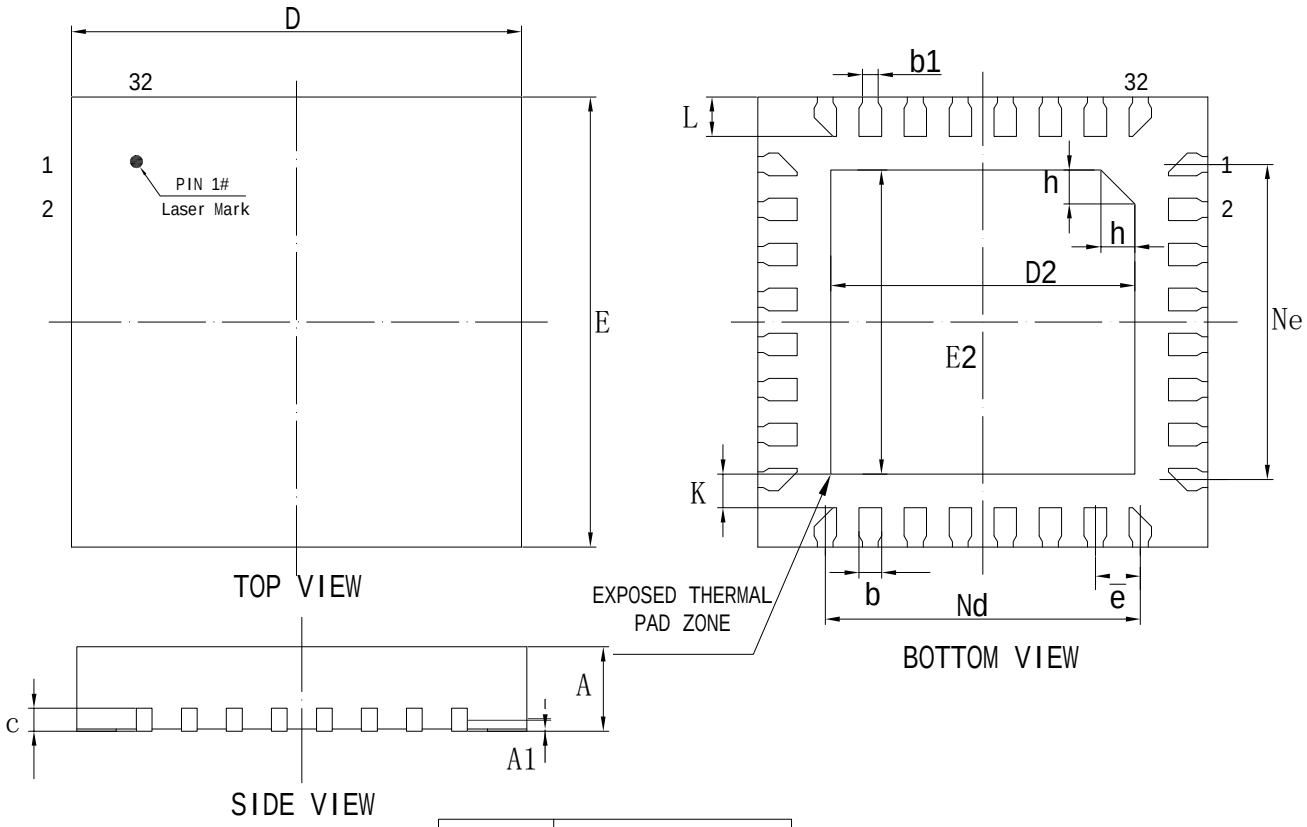
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Clock Frequency	f_{SCL}	—	—	400	kHz	3.0-5.5V	—
Bus Free Time	t_{BUF}	1.3	—	—	μs	3.0-5.5V	Time in which the bus must be free before a new transmission can start
Start Condition Hold Time	$t_{HD:STA}$	0.6	—	—	μs	3.0-5.5V	After this period, the first clock pulse is generated
SCL Low Time	t_{LOW}	1.3	—	—	μs	3.0-5.5V	—
SCL High Time	t_{HIGH}	0.6	—	—	μs	3.0-5.5V	—
Start Condition Setup Time	$t_{SU:STA}$	0.6	—	—	μs	3.0-5.5V	Only relevant for repeated START condition
Data Hold Time	$t_{HD:DAT}$	0	—	—	ns	3.0-5.5V	—
Data Setup Time	$t_{SU:DAT}$	100	—	—	ns	3.0-5.5V	—
SDA and SCL Rising Time	t_R	—	—	0.3	μs	3.0-5.5V	periodically sampled
SDA and SCL Falling Time	t_F	—	—	0.3	μs	3.0-5.5V	periodically sampled
Stop Condition Setup Time	$t_{SU:STO}$	0.6	—	—	μs	3.0-5.5V	—
Output Valid from Clock	t_{AA}	—	—	0.9	μs	3.0-5.5V	—
Input Filter Time Constant (SDA and SCL pin	t_{SP}	—	—	50	ns	3.0-5.5V	Noise suppression time

I²C Timing



7 Package Information

7.1 QFN32 (4.0mm x 4.0mm PP=0.4mm):



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1		0.14REF	
c		0.203REF	
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
e		0.40BSC	
Nd		2.80BSC	
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
Ne		2.80BSC	
L	0.30	0.35	0.40
h	0.25	0.30	0.35
K		0.30REF	

8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

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