Features

- Operating voltage:2.4-5.2V
- Built-in 256kHz RC oscillator（default）
- mode select by DS pin:
  mode0:Drive display point 116×2,dynamic,1/2bias 50%duty （DS=0）
  mode1:Drive display points116×1， static,no bias 100%duty（DS=1）
- Built-in 58×4 bit display RAM,Two ram mapping modes correspond to mode 0 and mode 1 respectively
- STANDBY mode（by Cmd LCD OFF,SYS DIS）
- 4 wire serial interface
- Software configuration LCD parameters
- Data mode and command mode instructions
- Read/Write address auto increment
- VLCD pin for adjusting LCD operating voltage（≤VDD）
- Three data accessing modes

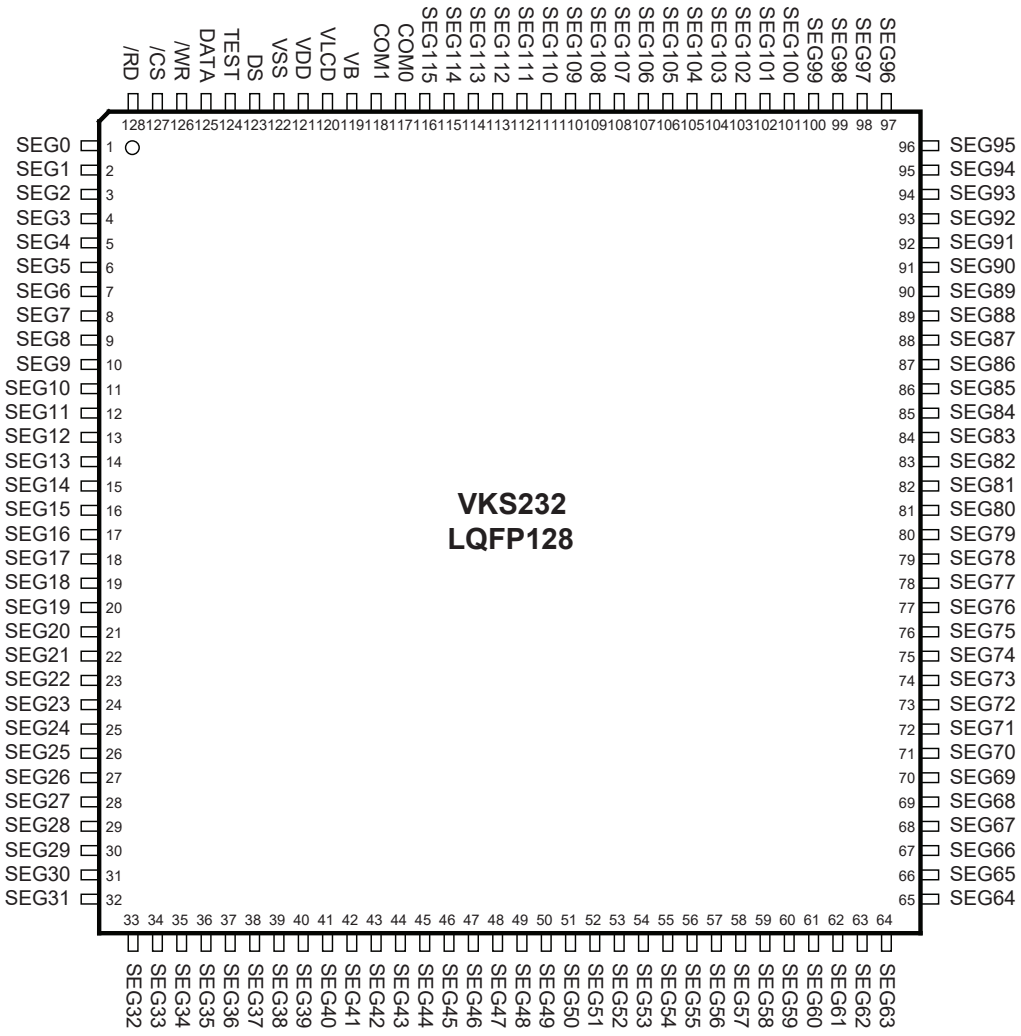
- Package:
  LQFP128(14.0mm x 14.0mm PP=0.4mm)

1 General Description

VKS232 is a RAM Mapping dual-mode LCD Driver,Select the display mode through the DS pin， It can support static LCD screens with a maximum of 116 pattern(116SEGx1COM), or dynamic LCD screens with a maximum of 232 pattern(116SEGx2COM), only 3 or 4 lines are required to communication interface with the VKS232,it is used to configure display parameters and transfer display data, and can also enter the standby mode through Power down command （by Cmd LCD OFF,SYS DIS）..It has the characteristics of good contrast, large viewing angle and no flicker. It is suitable for washing machine panels, automotive instruments, household appliances and other products requiring high display quality.

2. Pinouts and pin description

2.1 VKS232 LQFP128 Pin Assignment

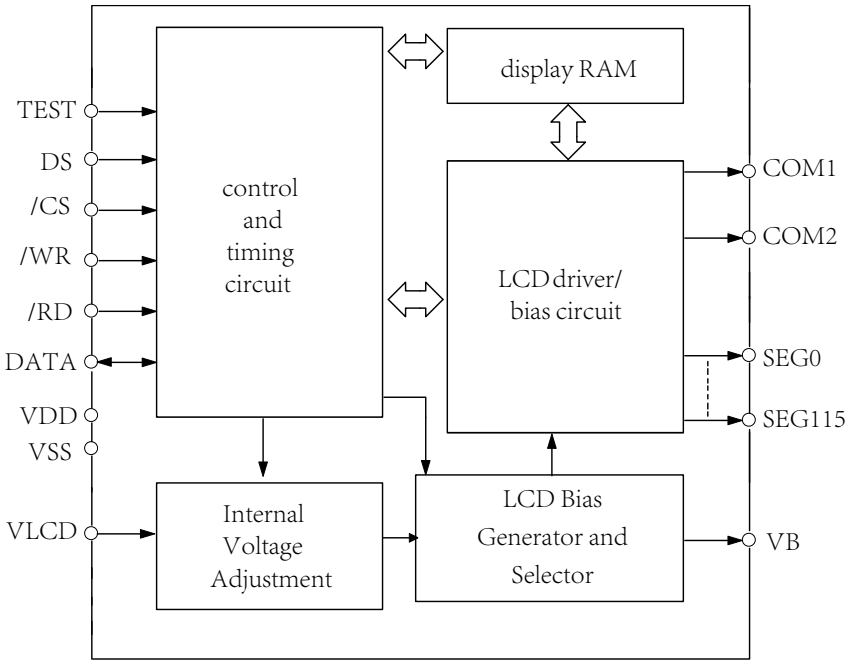


2.2 VKS232 LQFP128 Pin Description

No.	Name	I/O	Function
1-116	SEG0-SEG115	O	LCD SEG outputs
117-118	COM0,COM1	O	LCD COM outputs
119	VB	O	1/2 bias voltage output pin， connect 1uF capacitor
120	VLCD	I	LCD power input
121	VDD	VDD	Positive power supply
122	GND	GND	Negative power supply
123	DS	I	mode select: DS=“1”： Drive display points116×1， static,no bias 100%duty DS=“0”： Drive display point 116×2,dynamic,1/2bias 50%duty
124	TEST	I	TEST pin
125	DATA	I/O	Serial data input/output with pull-high resistor.
126	/WR	I	WRITE clock input with pull-up resistor, data latched on the rising edge of the /WR signal.
127	/CS	I	Chip selection input with pull-up resistor 1-disabe， 0-enable.
128	/RD	I	READ clock input with pull-up resistor, data out on the falling edge of the /RD signal.

3 Functional Description

3.1 Block diagram



3.2 Display RAM

The display memory (RAM) is organized into 58×4 bit sand stores the displayed data. the contents of the RAM are directly mapped to the contents of the LCD driver. Data in the RAM can be accessed by the READ, WRITE, and READ-MODIFY-WRITE commands.

The following is a mapping from the RAM to the LCD pattern:

mode0:Drive display point 116×2,dynamic,1/2bias 50%duty （DS=0）

COM1	COM0	COM1	COM0	Address	
SEG0		SEG1		0	address 6 bit （A5----A0）
SEG2		SEG3		1	
SEG4		SEG5		2	
SEG6		SEG7		3	
⋮		⋮		⋮	
SEG114		SEG115		57	
D3	D2	D1	D0	Data/Addr	

mode1:Drive display points116×1, static,no bias 100%duty （DS=1）

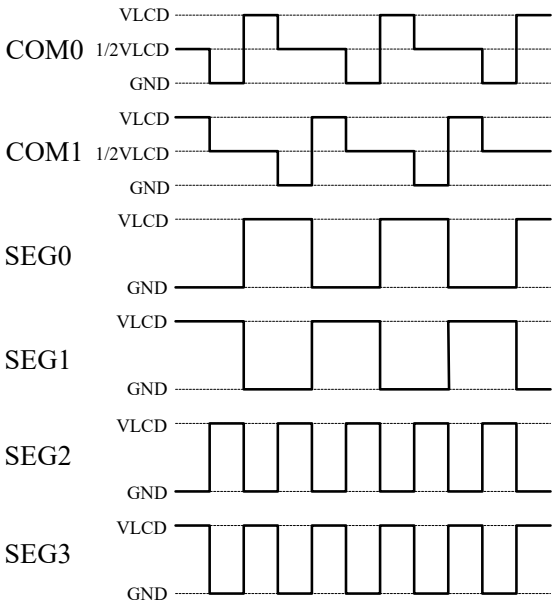
COM0				Address	
SEG0	SEG1	SEG2	SEG3	0	address 6 bit （A5----A0）
SEG4	SEG5	SEG6	SEG7	1	
SEG8	SEG9	SEG10	SEG11	2	
SEG12	SEG13	SEG14	SEG15	3	
⋮		⋮		⋮	
SEG112	SEG113	SEG114	SEG115	28	
D3	D2	D1	D0	Data/Addr	

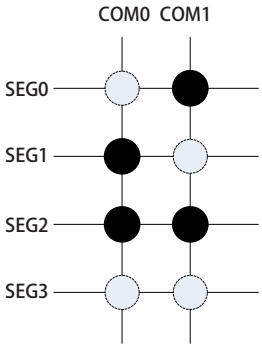
3.3 LCD Driver

VKS232 is a RAM Mapping dual-mode LCD Driver,Select the display mode through the DS pin:
mode0 - Drive display points116×2,dynamic display,1/2bias 50%duty （DS=0）
mode1 - Drive display points 116×1static display,no bias 100%duty（DS=1）

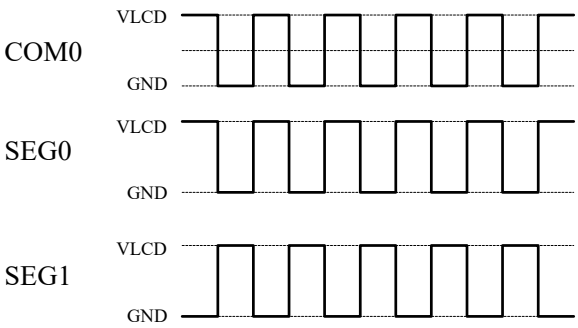
LCD driving waveform is as follows:

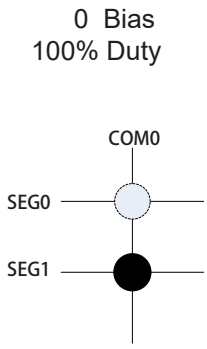
mode0 - 1/2 bias,50%duty:





mode1 - 0 bias, 100%duty:





3.3.1 Communication Interfacing

Four lines are required to interface with the VKS232.If only used for display, only 3 pins can be used.

The /CS pin is used to initialize the serial interface circuit and to terminate the communication with HOST.

. The DATA pin is the serial data input/output line. Data to be read or written or commands to be written have to be passed through the DATA line.

The /RD line is the READ clock input. Data in the RAM are clocked out on the falling edge of the /RD signal, and the clocked out data will then appear on the DATA line

The /WR line is the WRITE clock input. The data, address, and command on the DATA line are all clocked into theVKS232 on the rising edge of the WR signal.

The /IRQ pin can be selected as a timer output or a WDT overflow flag output by the software setting,it is a NMOS open drain output..

3.3.2 Command Format

VKS232 can be configured by the Software setting.There are two mode commands to configure the LCD parameters and to transfer the LCD display data,The configuration mode of the VKS232 is called command mode, and its command mode ID is 1 0 0. The data mode includes READ, WRITE, and READ-MODIFY-WRITE operations.

The following are the data mode IDs and the command mode ID:

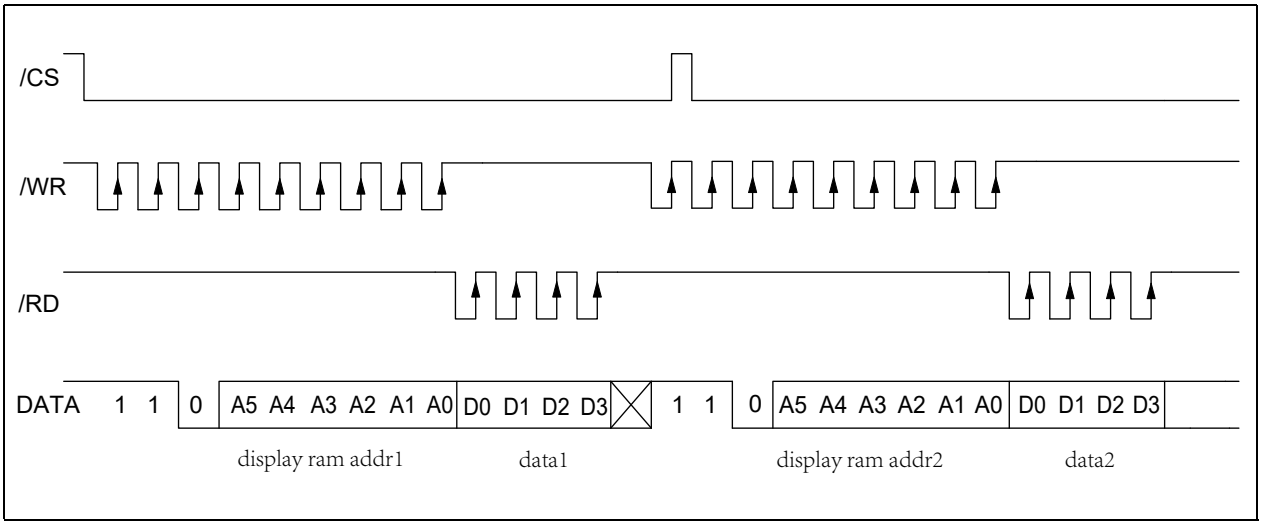
Operation	MODE	ID
READ	DATA	110
WRITE	DATA	101
Read-Modify-Write	DATA	101
COMMAND	COMMAND	100

3.3.3 Cmd/Data Timing Diagrams

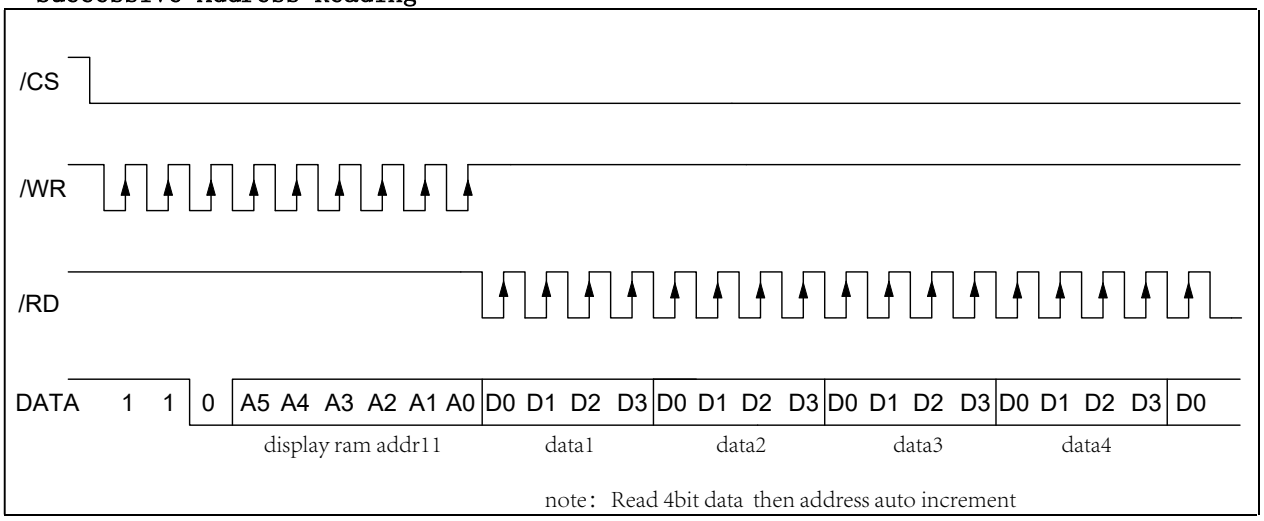
The following are the data mode IDs and the command mode ID Timing Diagrams。

3.3.3.1 READ Mode

Command Code : 110

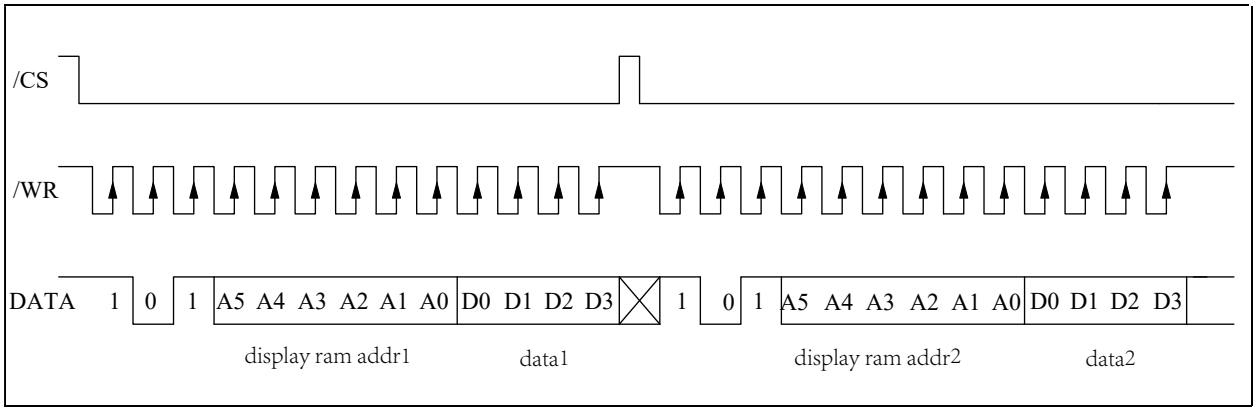


Successive Address Reading

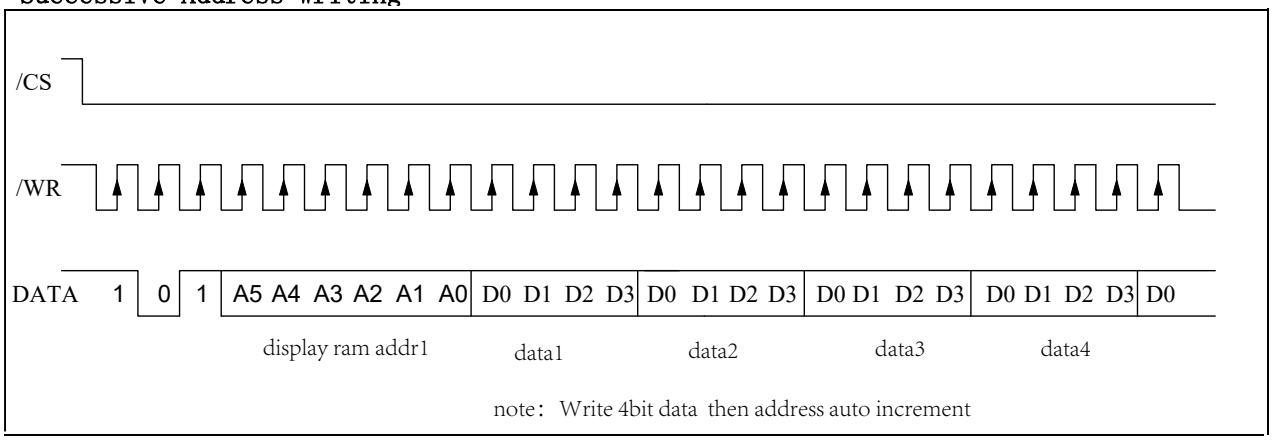


3.3.3.2 WRITE Mode

Command Code : 101

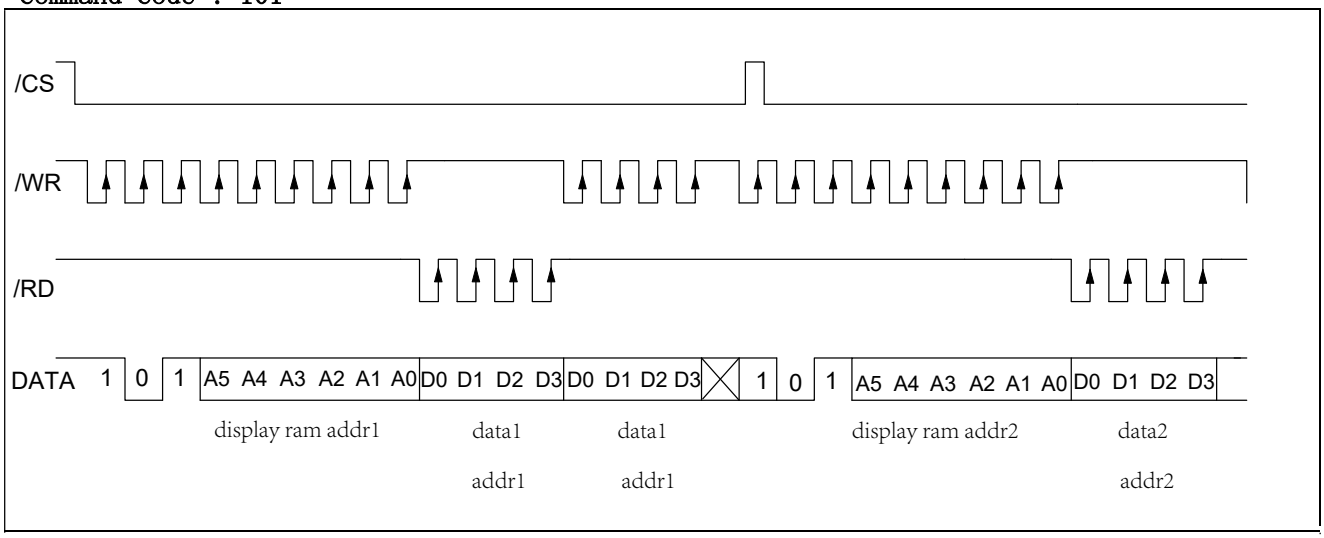


Successive Address Writing

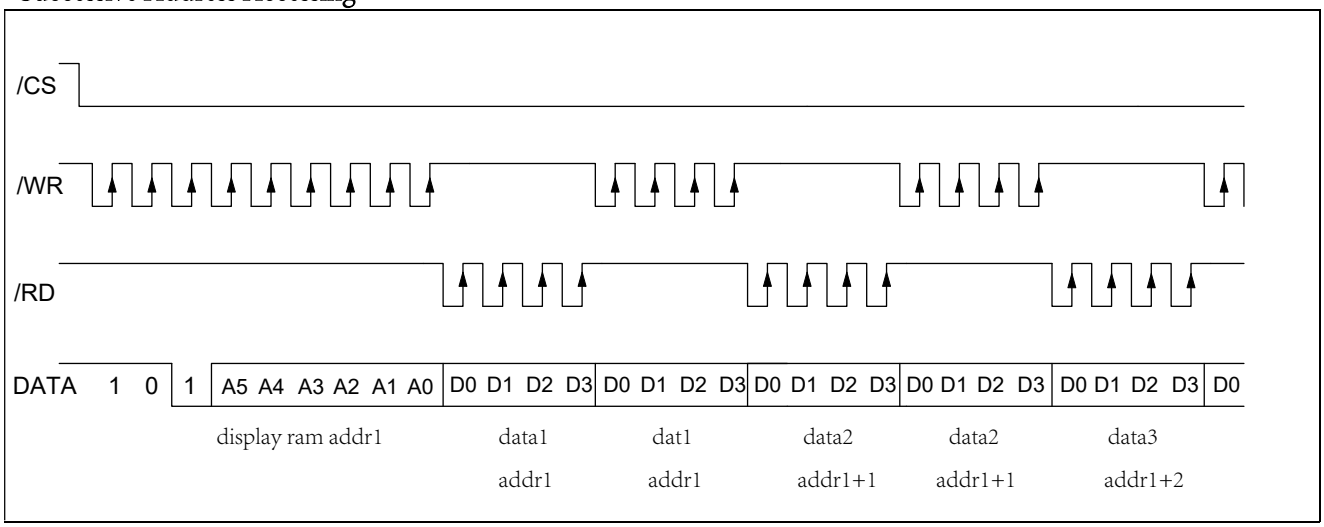


3.3.3.3 Read-Modify-Write Mode

Command Code : 101

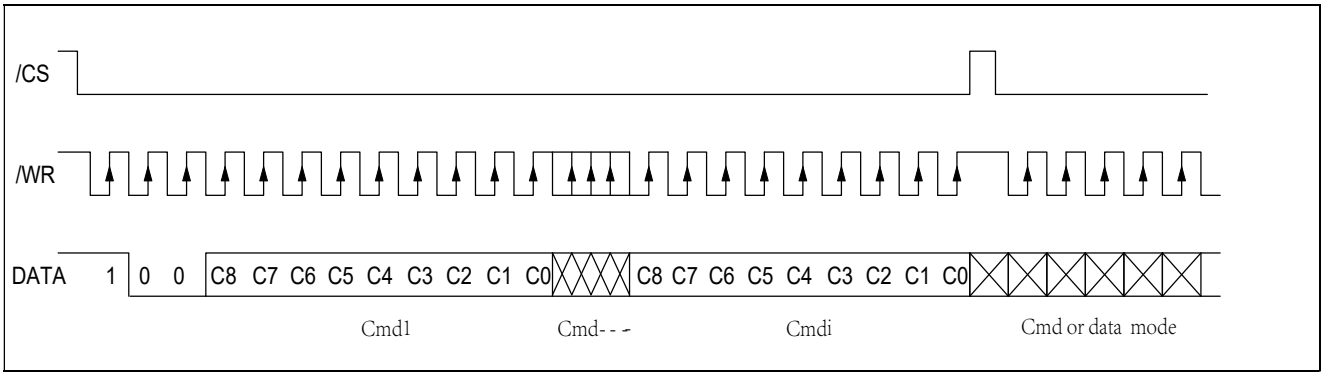


Successive Address Accessing



3.3.3.4 Command Mode

Command Code : 100

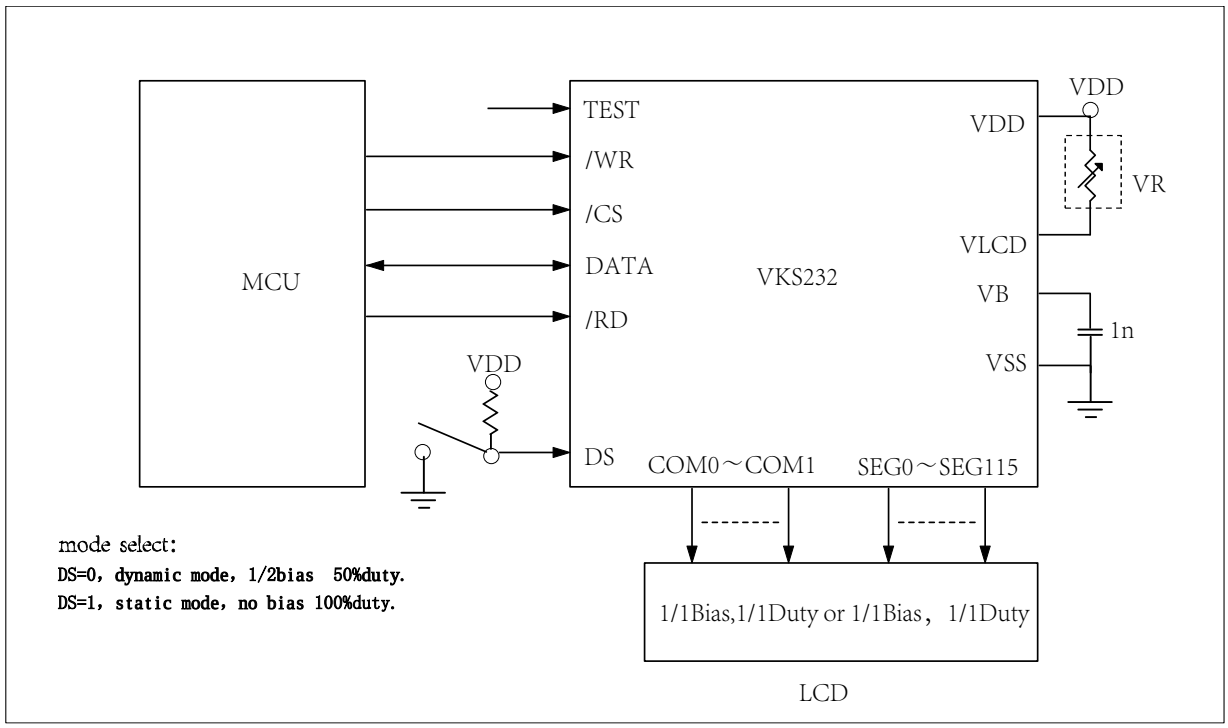


4 Command Summary

Name	ID	Command Code	D/C	Function	Def.
READ	110	A5A4A3A2A1A0D0D1D2D3	D	Read data from the RAM	
WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	Write data to the RAM	
READ-MODIFY-WRITE	101	A5A4A3A2A1A0D0D1D2D3	D	READ and WRITE to the RAM	
SYS DIS	100	0000- 0000-X	C	Turn off both system oscillator	YES
SYS EN	100	0000- 0001-X	C	Turn on system oscillator	
LCD OFF	100	0000- 0010-X	C	Turn off LCD bias generator	YES
LCD ON	100	0000- 0011-X	C	Turn on LCD bias generator	

note: X: 0 or 1
A5-A0: DIspaly RAM addresses
D3-D0:4bit DIspaly RAM data
D/C:Data/Command mode
Def.:Power on reset default
110,101和 100是Command ID

5 Dssolfdwlrq Flufxlwv



Note: Adjust VR(20K) to fit user's LCD panel display voltage (VLCD)

6 Electrical characteristics

6.1 Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power voltage	VDD	-0.3～5.5	V
Input Voltage	VIN	V_{SS}-0.3～V_{DD}+0.3	V
Storage Temperature	TSTG	-50～+125	℃
Operating Temperature	TOTG	-40～+85	℃

6.2 DC Characteristics

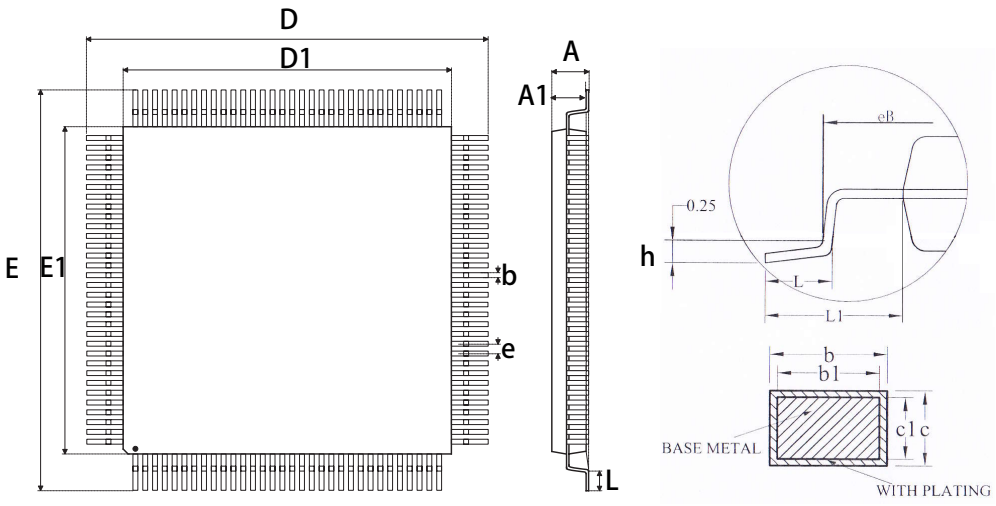
Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
Operating voltage	VDD	2.4	—	5.2	V	—	—
Operating current	I_{DD1}	—	150	300	μA	3V	No load/LCD ON On-chip RC oscillator
		—	300	600		5V	
Standby Current	I_{STB}	—	0.1	5	μA	3V	No load, Power down mode
		—	0.3	10		5V	
Input Low Voltage	V_{IL}	0	—	0.6	V	3V	DATA,/WR,/CS
		0	—	1.0		5V	
Input High Voltage	V_{IH}	2.4	—	3.0	V	3V	DATA,/WR,/CS
		4.0	—	5.0		5V	
DATA	I_{OL}	0.5	1.2	—	mA	3V	VOL=0.3V
		1.3	2.6	—		5V	VOL=0.5V
DATA	I_{OH}	-0.4	-0.8	—	mA	3V	VOL=2.7V
		-0.9	-1.8	—		5V	VOL=4.5V
LCD COM Sink Current	I_{OL1}	80	150	—	μA	3V	V_{OL}=0.3V
		150	250	—		5V	V_{OL}=0.5V
LCD COM Source Current	I_{OH1}	-80	-120	—	μA	3V	V_{OH}=2.7V
		-120	-200	—		5V	V_{OH}=4.5V
LCD SEG Sink Current	I_{OL2}	60	120	—	μA	3V	V_{OL}=0.3V
		120	200	—		5V	V_{OL}=0.5V
LCD SEG Source Current	I_{OH2}	-40	-70	—	μA	3V	V_{OH}=2.7V
		-70	-100	—		5V	V_{OH}=4.5V
Pull-UP Resistor	R_{PH}	40	80	150	KΩ	3V	DATA,/WR,/CS
		30	60	100		5V	

6.3 AC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
						VDD	Conditions
System Clock	f_{SYS1}	192	256	320	kHz	3V	On-chip RC oscillator
		—	256	—		5V	
LCD Clock	f_{LCD1}	—	f_{SYS1}/ 1024	—	Hz	—	On-chip RC oscillator
LCD Common Period	t_{COM}	—	N/f_{LCD}	—	sec	—	N： Number of COM
Serial Data Clock (/WR,/RD)	F_{CLK1}	—	—	150	kHz	3V	Duty cycle 50%
		—	—	300		5V	
Serial Interface Reset PW	t_{CS}	—	250	—	ns	—	/CS
/WR, /RD Input Pulse Width	t_{CLK}	3.34	—	—	μs	3V	Write mode
		1.67	—	—	μs	5V	Write mode
Rise/Fall Time Serial Data Clock Width	t_r, t_f	—	120	—	ns	3V	—
						5V	
Setup Time for DATA to /WR, /RD Clock Width	t_{su}	—	120	—	ns	3V	—
						5V	
Hold Time for DATA to /WR, /RD Clock Width	t_h	—	120	—	ns	3V	—
						5V	
Setup Time for /CS to /WR, /RD Clock Width	t_{su1}	—	100	—	ns	3V	—
						5V	
Hold Time for /CS to /WR, /RD Clock Width	t_{h1}	—	100	—	ns	3V	—
						5V	

7 Package Information

7.1 LQFP128(14.0mm x 14.0mm PP=0.4mm))



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	--	--	1.60
A1	1.35	1.40	1.45
b	0.14	--	0.23
b1	0.13	0.16	0.19
c	0.13	--	0.18
c1	0.12	0.127	0.134
D	15.80	16.00	16.20
D1	13.90	14.00	1410
E	15.80	16.00	15.20
E1	13.90	14.00	14.10
e	0.. 0BSC		
L	0.45	0.60	0.75
L1	1.00REF		

8 Revision history

No.	Version	Date	Modify the content	Check
1	1.0	2018-08-10	Original version	Yes
2	1.1	2018-10-11	Add Ref circuits	Yes
3	1.2	2019-03-21	Check para	Yes
4	1.3	2020-04-11	Update content	Yes

Disclaimers