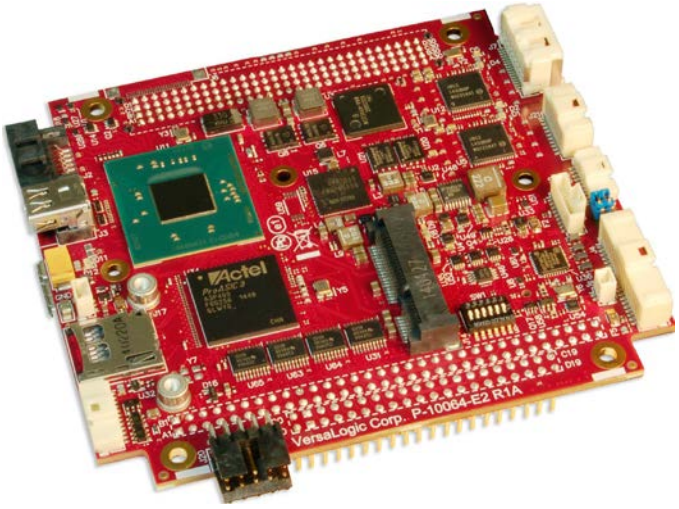
Hardware Reference Manual

REV. January 2019



BayCat

(VL-EPM-31)

Intel® Atom™-based Single Board Computer with Dual Ethernet, Video, USB, SATA, Serial I/O, Digital I/O, Trusted Platform Module security, Counter/Timers, Mini PCIe, mSATA, PCI/104-*Plus* Interface, and SPX.

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Product Release Notes

Release 1.0	January 2016	First production release
Release 1.1	April 2016	Added information regarding I^2C support to **Table 8**, **Table 19**, and **Table 20**.
Release 1.2	August 2016	Updated caption for Figure 23, Updated signal information for pins 6 and 14 in table 14.
Release 1.3	October 2016	Added ISA IRQ information.
Release 1.4	January 2017	Updated terminology for updating RTC registers
Release 1.5	July 2017	Updated Web links
Release 1.6	April 2018	Updated Boot Drive Selection Process
Release 1.7	August 2018	Updated LED Table in Figure 11
Release 1.8	October 2018	Updated Table 11
Release 1.9	January 2019	Updated the List of Figures

Technical Support

The EPM-31 support page contains additional information and resources for this product including:

- Reference Manuals (PDF format)
- Operating system information and software drivers
- Data sheets and manufacturers' links for chips used in this product
- BIOS information and upgrades
- Utility routines and benchmark software

This is a private page for EPM-31 users that can be accessed only be entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

If you have additional questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All non-warranty repairs are subject to diagnosis and labor charges, parts charges and return shipping fees. Specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Mark the RMA number clearly on the outside of the box before returning. Failure to do so can delay the processing of your return.

RoHS Compliance

The EPM-31 is RoHS-compliant.

About RoHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of poly-brominated biphenyls (PBB) and poly-brominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corporation is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Cautions

Electrostatic Discharge

Electrostatic discharge (ESD) can damage boards, disk drives and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic anti-static envelope during shipment or storage.

Note:

The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom-side of the EPM-31.

Lithium Battery

To prevent shorting, premature failure or damage to the lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The Lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of in fire. Dispose of used batteries promptly.

MOUNTING SUPPORT

The single board computer must be supported at all four mounting points to prevent excessive flexing when expansion modules are attached and removed. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty. See page 15 for more details.

EARTH GROUND REQUIREMENT

All mounting standoffs should be connected to earth ground (chassis ground). This provides proper grounding for EMI purposes. Figure 1 shows the locations of the board's mounting holes. All mounting holes identified in Figure 1 must be connected to earth ground.

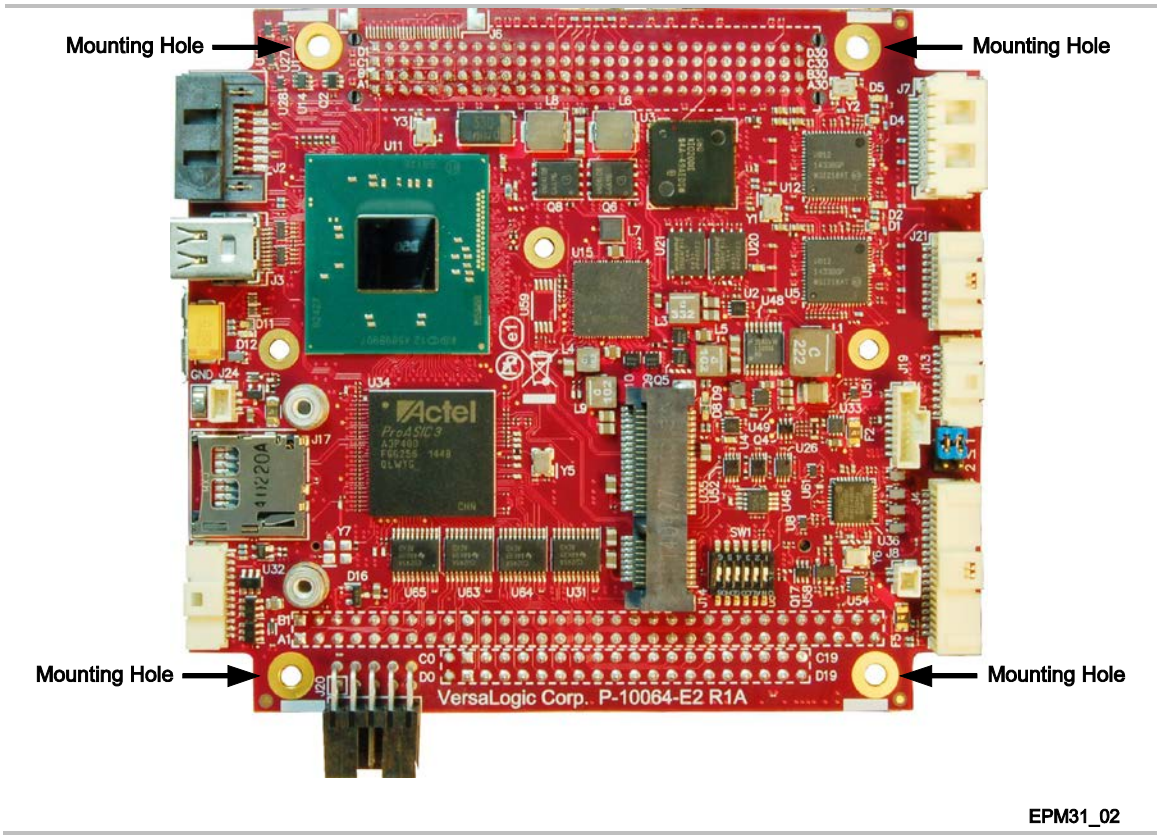


Figure 1. Attaching the EPM-31 to Earth Ground

Contents

Figures

Tables

1 Introduction

Description

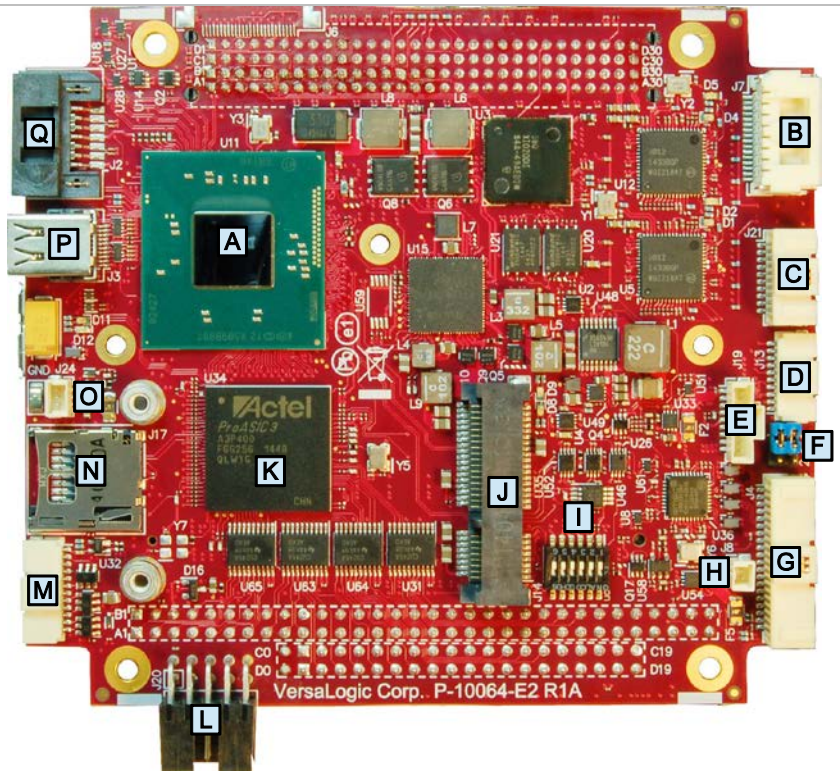
The EPM-31 BayCat is a feature-packed single board computer (SBC) designed to support OEM applications where high reliability and long-term availability are required. Its features include:

- Intel† Atom† "Bay Trail" processor, quad, dual, or single core with processor clock rates up to 1.91 GHz (Atom E3845)
- Integrated IntelGen7 graphics core, supports DirectX11, Open GL3, and H.264, MPEG-2 encoding/decoding
- Analog and Mini DisplayPort video outputs
- Up to 8 GB DDR3L memory, one SO-DIMM socket
- Two Intel I210-IT-based Ethernet ports, auto-detect 10Base-T / 100Base-TX / 1000Base-T
- One USB 3.0 port and four USB 2.0 ports
- Trusted Platform Module
- Two RS-232/422/485 serial ports
- Three 8254 timer/counters
- 24 digital I/O lines (16 on the EPM-31 board and an additional eight when using the VL-CBR-4005 paddleboard)
- SATA port, 3 Gb/s
- Mini PCIe / mSATA socket, supports Wi-Fi modems, GPS receivers, flash storage, and other modules
- SPX expansion
- PC/104 form factor with PC/104-*Plus* expansion
- Customization available

The EPM-31 is compatible with popular operating systems such as Microsoft† Windows†, Windows Embedded, Linux, VxWorks†, and QNX†.

EPM-31 boards are subjected to complete functional testing and are backed by a limited five-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional single-board computer (SBC).

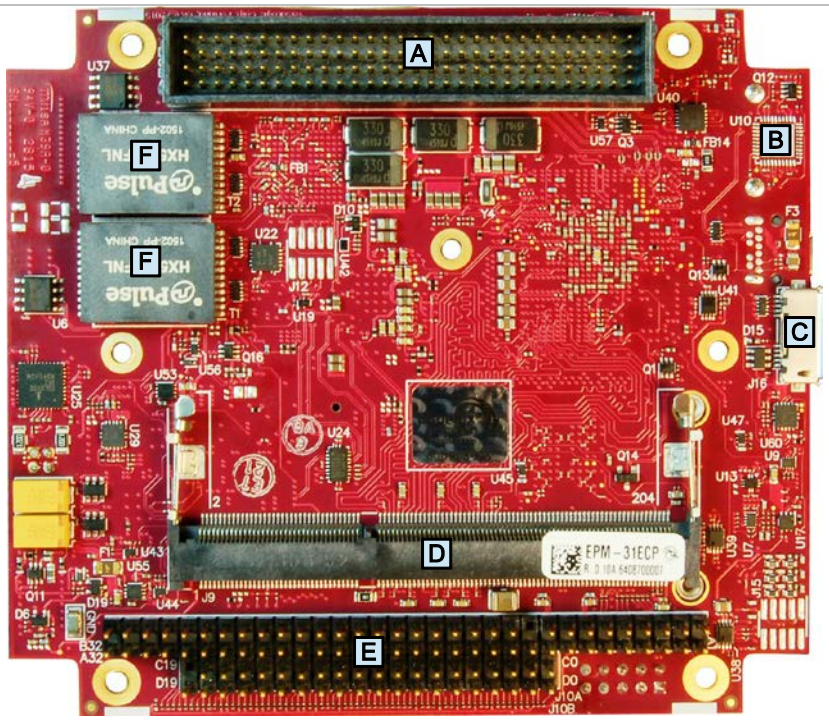
Figure 2 shows the connectors and major components on the top side of the board. Figure 3 shows the connectors and major components on the bottom side of the board.



EPM31_07

Item/ [Reference Designator]	Description	Item/ [Reference Designator]	Description
A	Intel Atom “Bay Trail” SoC	J [J14]	PCIe Minicard/mSATA connector
B [J7]	Ethernet port 0/1 connector	K	FPGA device
C [J21]	Digital I/O connector	L [J20]	Main power connector
D [J13]	COM1/COM2 Serial port connector	M [J5]	VGA connector
E [J19]	SPX connector	N [J17]	microSD card socket
F [V1]	Configuration jumpers	O [J24]	Fan connector
G [J4]	User I/O (CBR-4005B mating connector)	P [J3]	Mini DisplayPort connector
H [J8]	External battery connector	Q [J2]	SATA connector
I [SW1]	Configuration switches		

Figure 2. VL-EPM-31 BayCat Single Board Computer (Top Side)



EPM31_06

Item/ [Reference Designator]	Description
A [J11]	PC/104 Legacy PCI expansion connector
B	Trusted Platform Module (TPM) device
C [J16]	USB 3.0 port
D [J9]	SODIMM socket
E [J10A/J10B]	PC/104 Legacy ISA expansion connector
F	Ethernet transformers

Figure 3. VL-EPM-31 BayCat Single Board Computer (Bottom Side)

Technical Specifications

See the BayCat Data Sheet for complete specifications.

Thermal Considerations

The operating temperature for the EPM-31 is -40 °C to +85 °C, de-rated -1.1 °C per 305m (1,000 ft.) above 2,300m (7,500 ft.). All BayCat models include a rigid-mount heat plate thermal solution. Refer to the Chapter 13, beginning on page 67 for information on additional thermal solutions.

EPM-31 Block Diagram

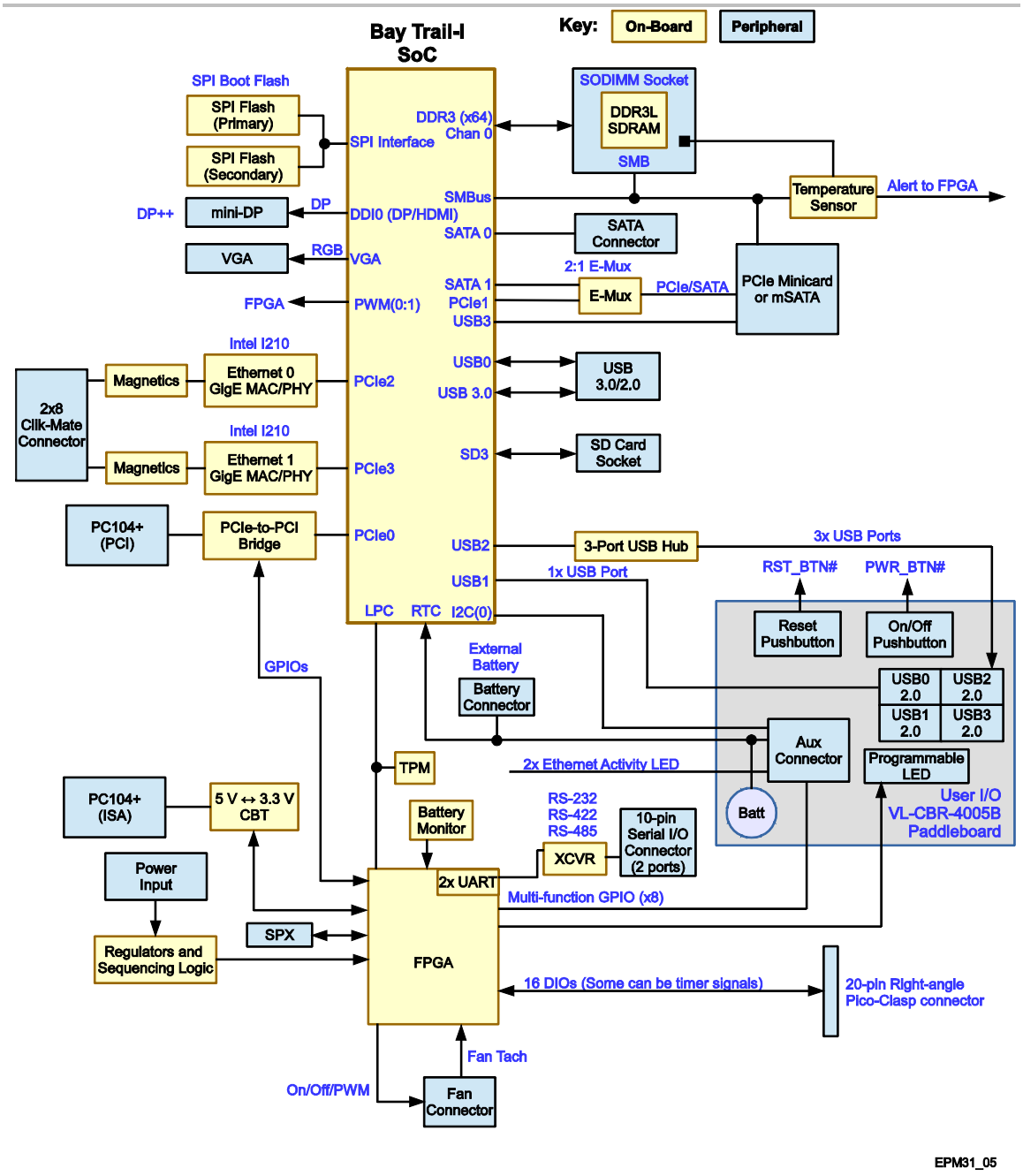


Figure 4. EPM-31 Block Diagram

Dimensions and Mounting

The EPM-31 complies with the PC/104 standard which provides for specific mounting hole and PC/104-*Plus* stack locations as shown in Figure 5.

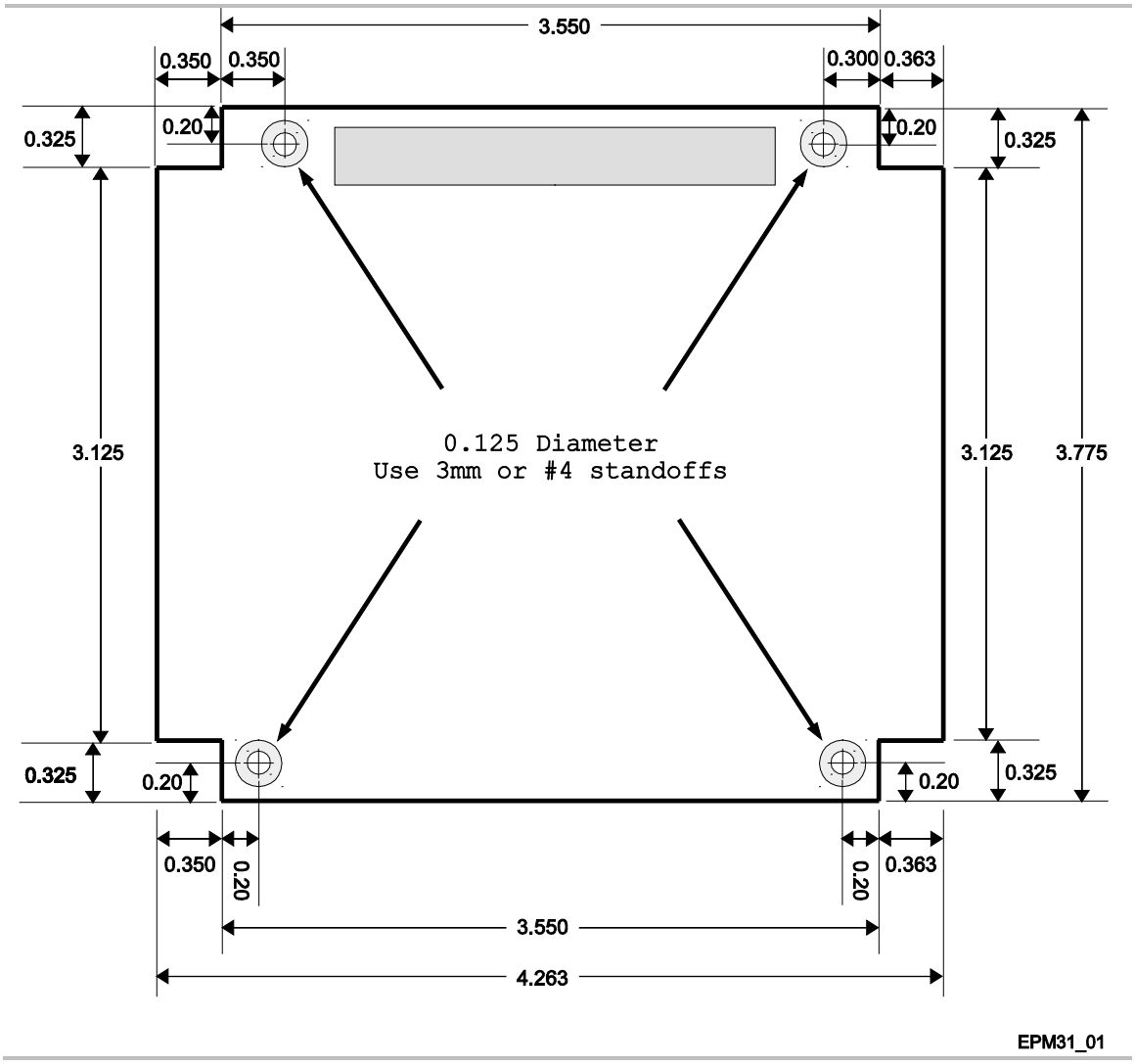


Figure 5. EPM-31 Dimensions and Mounting Holes
(Not to scale. All dimensions in inches.)

CAUTION:

The EPM-31 must be supported at all four mounting points to prevent excessive flexing when expansion modules are attached and removed. Flex damage caused by excessive force on an improperly mounted circuit board is not covered under the product warranty.

HARDWARE ASSEMBLY

The EPM-31 mounts on four hardware standoffs using the corner mounting holes. These standoffs are secured to the underside of the circuit board using pan head screws.

The entire assembly can sit on a table top or be secured to a base plate. When bolting the unit down, make sure to secure all standoffs to the mounting surface to prevent circuit board flexing.

An extractor tool is available (part number VL-HDW-201) to separate the PC/104 modules from the stack.

Related Documents

The following documents available are on the EPM-31 Product Support Web Page:

- *EPM-31 Programmer's Reference Manual* – provides information on the board's resources (memory, I/O, and IRQs), a description of the FPGA's registers, and programming information for the board's hardware interfaces.
- *EPM-31 BIOS Reference Manual* – provides information on accessing and configuring settings in the BIOS Setup utility. All BIOS menus, submenus, and configuration options are described.
- *VersaAPI Installation and Reference Guide* – describes the shared library of API calls for reading and controlling on-board devices on certain VersaLogic products.

Additional documents:

Processor Intel Atom E38xx (formerly "Bay Trail") System-on-Chip (SoC) Processor	Intel Atom Processor E3800 Product Family Datasheet
Ethernet Controller Intel I210-IT Gigabit Ethernet Controller	Intel I210-IT Datasheet
PC/104 Specification	http://www.versalogic.com/products/PC104/index.asp
PC/104-*Plus* Specification	http://www.versalogic.com/products/PC104/index.asp

Configuration and Setup

2

Initial Configuration

The following components are recommended for a typical development system.

- VL-EPM-31 single board computer
- VL-MM9-xxEBN DDR3 SO-DIMM module (see System RAM)
- ATX power supply with motherboard and disk drive connectors
- VGA video monitor
- USB Keyboard
- USB Mouse
- SATA hard drive

The following VersaLogic cables and accessories are recommended.

- VGA Video adapter cable (CBR-1204)
- User I/O cable (CBR-4005) and accompanying paddleboard (CBR-4005B)
- Power adapter cable (CBR-1008)
- VL-CBR-0702 – SATA data cable
- VL-CBR-0401 – ATX to SATA power adapter
- VL-CBR-1604 – 12-inch dual Ethernet RJ-45 adapter

You will also need a Windows (or other OS) installation CD/DVD and corresponding drive.

Basic Setup

The following steps outline the procedure for setting up a typical development system. The EPM-31 should be handled at an ESD workstation or while wearing a grounded antistatic wrist strap.

Before you begin, unpack the EPM-31 and accessories. Verify that you received all the items you ordered. Inspect the system visually for any damage that may have occurred in shipping. Contact Support@VersaLogic.com immediately if any items are damaged or missing.

Gather all the peripheral devices you plan to attach to the BayCat as well as their interface and power cables.

It is recommended that you attach standoffs to the board (see Hardware Assembly) to stabilize the board and make it easier to work with.

1. Install Memory

- Insert the DDR3L DRAM module into the SO-DIMM socket on the bottom side of the board and latch it into place.

2. Attach Cables and Peripherals

Note:
The instructions below refer to connector locations by the reference designators printed on the board's silkscreen. Figure 2 (page 12) and Figure 3 (page 13) show the locations of all the connectors along with their reference designators.

- Plug the VGA cable VL-CBR-1204 into socket J5. Attach the cable to a VGA display. (Alternatively, you can attach a DisplayPort-enabled display to the Mini DisplayPort connectors at J3. The VL-EPH-V6 video adapter card converts DisplayPort output to LVDS.)
- Plug the VL-CBR-4005B paddleboard into socket J4.
- Plug a USB CD-ROM drive, USB keyboard, and USB mouse into any of the USB connectors of the CBR-4005B paddleboard.
- Plug the SATA data cable VL-CBR-0702 into socket J2. Attach a hard drive to the connector on the cable.
- Attach the SATA power adapter cable VL-CBR-0401 to the ATX power supply and SATA drive.
- Optionally, attach a LAN cable to either of the Ethernet connectors at J7 on the EPM-31 using the VL-CBR-1604 RJ-45 adapter.

3. Attach Power

- Plug the power adapter cable VL-CBR-1008 into socket J20. Attach the motherboard connector of the ATX power supply to the adapter.

4. Review Configuration

- Before you power up the system, double-check all the connections. Make sure all cables are oriented correctly and that adequate power will be supplied to the VL-EPM-31 and peripheral devices.

5. Power On

- Turn on the ATX power supply and the video monitor. If the system is correctly configured, a video signal should be present.

6. Select a Boot Drive

- During startup, press the F5 function key to display the boot menu. Select the CDROM, and use the [+] and [-] keys to move the CDROM to the first boot device "1" in the boot order. Select Save and Exit or press [F10] and select [YES] to save changes and exit. Insert the OS installation CD in the CD-ROM drive and select to boot from the CD-ROM drive.

7. Install Operating System

- Install the operating system according to the instructions provided by the operating system manufacturer. (See Operating System Installation on page 22.)

Jumper Blocks

JUMPERS BLOCKS IN THE AS-SHIPPED CONFIGURATION

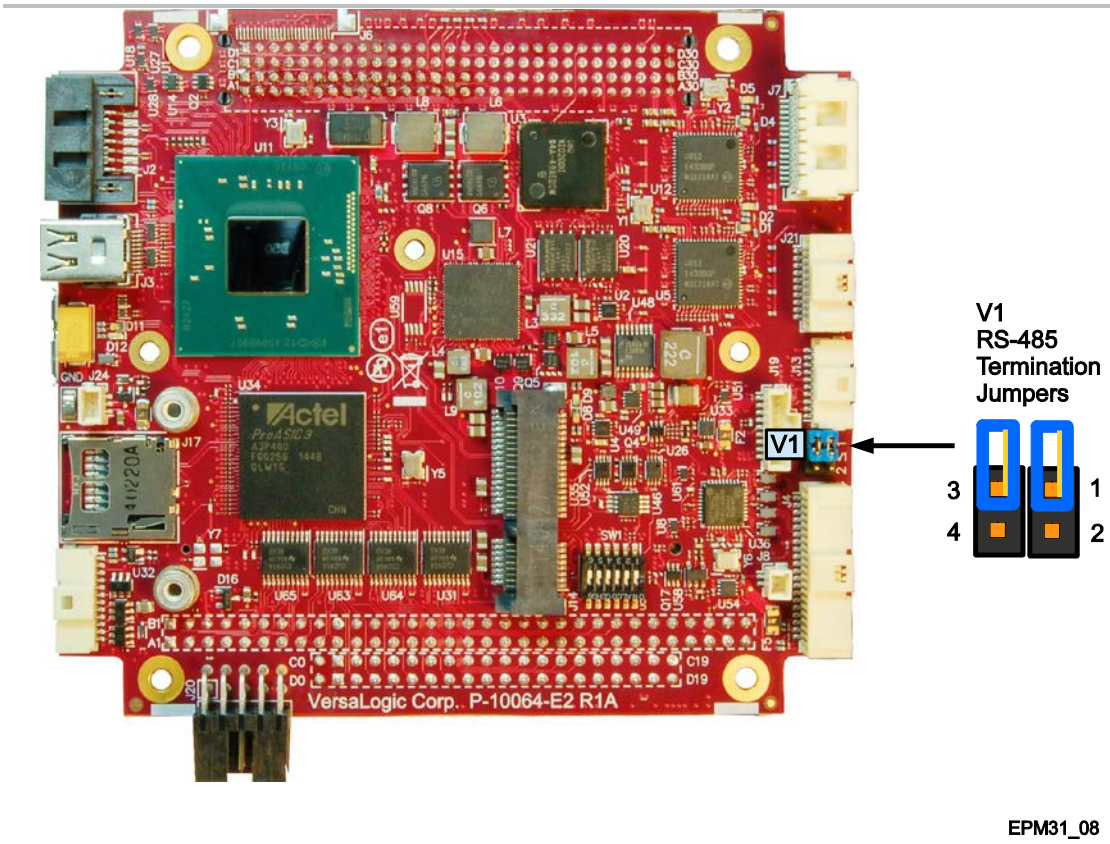


Figure 6. Jumper Block Locations

JUMPER SUMMARY

Table 1: Jumper Summary

Jumper Block	Description	Reference
V1 [1-2]	**COM1 Rx End-point termination** • In – COM1 terminator enabled for RS-485/RS-422 • Out – COM1 terminator disabled **(default)**	Table 11, page 45
V1 [3-4]	**COM4 Rx End-point termination** • In – COM2 terminator enabled for RS-485/RS-422 • Out – COM2 terminator disabled **(default)**	Table 11, page 45

Configuration Switches

Figure 7 shows the as-shipped switch configuration with all switches in the Off position. The Off position is toward the center of the board.

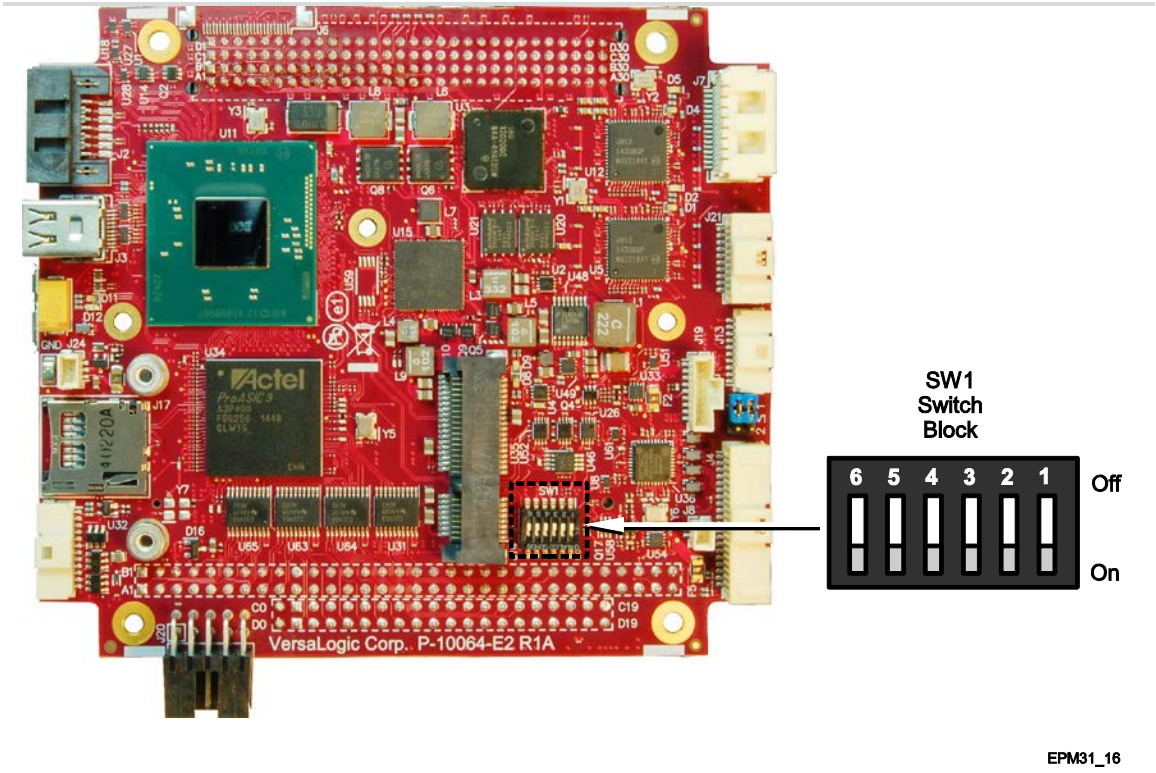


Figure 7. Location of SW1 Configuration Switch Block

Table 2: Switch Setting Summary

SW1 Switch Position	Description
Position 1	**Clears non-volatile RAM and clears resets real-time clock registers (see page 21)** **Off** – Normal operation (default) On – Clears battery backed up non-volatile memory bytes 0xE-0x7F and clears battery backed-up RTC registers
Position 2	**No Battery Switch** (see Integrator's Note below) **Off** – A battery is being used (default) On – A battery is not being used
Position 3	**Reset BIOS to factory defaults (see page 21)** **Off** – Normal operation (default) On – Resets BIOS to factory defaults when the board boots.
Position 4	**For factory use only. Always leave in the Off position.**
Position 5	**SPI Flash Security** – Not supported. Leave in the Off position.
Position 6	**BIOS select** **Off** – Primary BIOS (default) On – Backup BIOS

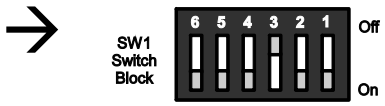
Integrator's Note:

- **If a battery is installed** (on the CBR-4005B paddleboard or externally using the J8 connector), switch position 2 must be set to the Off position. If it is set to On, the battery will discharge quickly.
- **If you don't use a battery**, switch position 2 should be set to the ON position. Otherwise, boot times could increase (by as much as 30 seconds in low temperature environments).

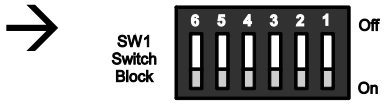
RESETTING THE BIOS TO FACTORY DEFAULTS

Reset the BIOS to default settings using the following the instructions:

1. Power off the EPM-31and set SW1 switch position 3 to the On position (toward the outer edge of the board).



2. Power on the EPM-31.
3. After the system boots, power off the EPM-31 and set the switch back to the Off position (toward the center of the board).

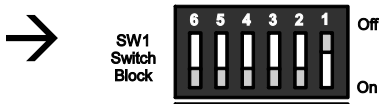


4. Power on the EPM-31.

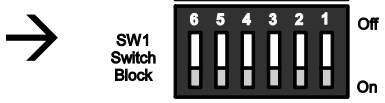
CLEARING RAM AND RTC REGISTERS

Clear RAM and RTC registers (which includes the date/time) using the following the instructions:

1. Power off the EPM-31.
2. Set SW1 switch position 1 to the On position (toward the outer edge of the board).



3. Wait at least two seconds and set the switch back to the Off position (toward the center of the board).



4. Power on the EPM-31.

BIOS Setup Utility

The EPM-31 permits users to modify the BIOS Setup utility defaults. Refer to the *EPM-31 BIOS Reference Manual* (available on the EPM-31 Product Support Web Page) for information on accessing and configuring settings in the BIOS Setup utility. All BIOS menus, submenus, and configuration options are described in the *EPM-31 BIOS Reference Manual.*

Operating System Installation

The standard PC architecture used on the EPM-31 makes the installation and use of most of the standard x86 processor-based operating systems relatively simple. The operating systems listed on the VersaLogic OS Compatibility Chart use the standard installation procedures provided by the maker of the OS. Special optimized hardware drivers for a particular operating system, or a link to the drivers, are available at the EPM-31 Product Support Web Page.

Board Features 3

CPU

The EPM-31 uses one of three Intel 4th Generation Atom (formerly “Bay Trail”) System-on-Chip (SoC) processors:

- E3845 (quad core)
- E3826 (dual core)
- E3815 (single core)

Each core contains a 512 KB L2 cache. These processors support Intel 64-bit instructions, AES Instructions, Execute Disable Bit, and Virtualization Technology.
See the Intel Atom Processor E3800 Product Family Datasheet for a complete description of the CPU.

Note:
If the above link to the datasheet becomes inactive, search the internet for “Intel Bay Trail” or “E3800” and follow the results to the Intel site and datasheet.

System RAM

The EPM-31 accepts one 204-pin SO-DIMM memory module (J9 connector on the bottom side of the board) with the following characteristics:

- Size Up to 8 GB, 1066 MHz or 1333 MHz, CPU dependent
- Voltage 1.35 V
- Type DDR3L (VersaLogic VL-MM9 Series modules)

I/O Interfaces

The EPM-31 board’s I/O interfaces and their associated connectors are described in later chapters as follows:

Power Delivery

MAIN POWER CONNECTOR

Figure 8 shows the location and pin orientation of the main power connector.

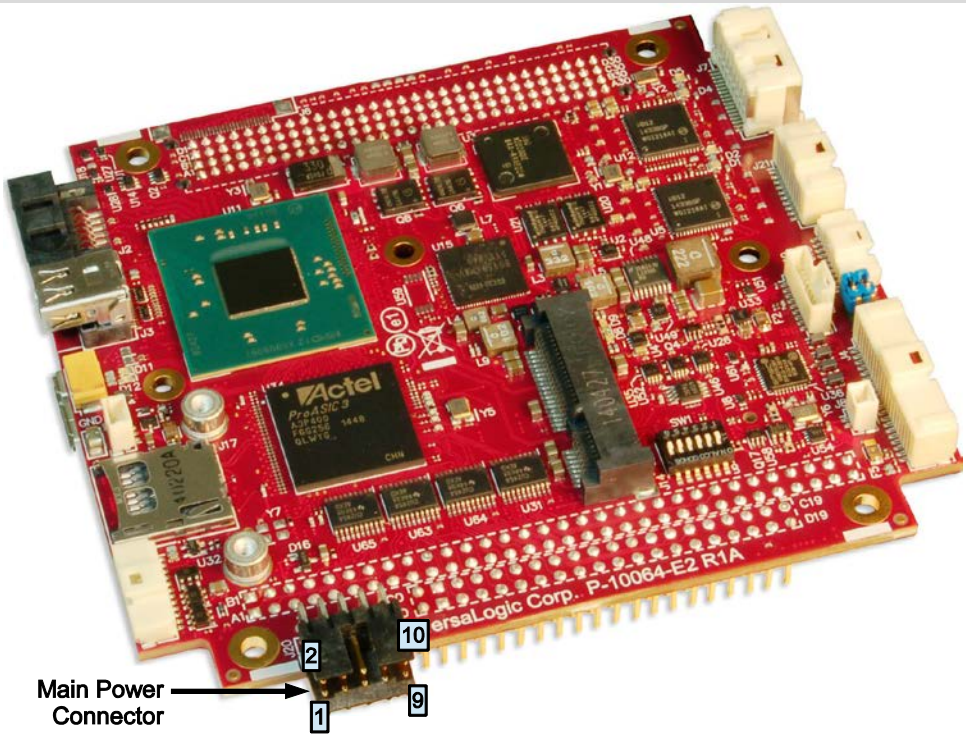


Figure 8. Location and Pin Orientation of the Main Power Connector

CAUTION:

To prevent severe and possibly irreparable damage to the system, it is critical that the power connector is wired correctly. Make use of all +5 VDC pins and all ground pins to prevent excess voltage drop.

Note:

The +3.3 VDC, +12 VDC and -12 VDC inputs on the power connector are only required for PC/104-*Plus* and PC/104 expansion modules that require these voltages.

Table 3 lists the pinout for the main power connector.

Table 3: J20 Main Power Connector Pinout

Pin	Signal	Pin	Signal
1	Ground	2	+5 VDC
3	Ground	4	+12 VDC
5	Ground	6	-12 VDC
7	+3.3 VDC	8	+5 VDC
9	Ground	10	+5 VDC

CABLING

An adapter cable, part number CBR-1008, is available for connecting the EPM-31 to an ATX power supply.

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
FCI 78207-110HLF	FCI 69176-010LF

POWER DELIVERY CONSIDERATIONS

Using the VersaLogic approved power supply (VL-PS200-ATX) and power cable (VL-CBR-1008) ensures high quality power delivery to the board. Customers who design their own power delivery methods should take into consideration the guidelines below to ensure good power connections.

In addition, the specifications for typical operating current do not include any off-board power usage that may be fed through the main power connector. Expansion boards and USB devices plugged into the board will source additional power through the main power connector.

- Do not use wire smaller than 22 AWG. Use high quality UL 1007 compliant stranded wire.
- The length of the wire should not exceed 18 inches.
- Avoid using any additional connectors in the power delivery system.
- The power and ground leads should be twisted together, or as close together as possible to reduce lead inductance.
- A separate conductor must be used for each of the power pins.
- All power input pins and all ground pins must be independently connected between the power source and the power connector.
- Use a high quality power supply that can supply a stable voltage while reacting to widely varying current draws.

Refer to Table 17: PCI/104-Plus Connector (PCI) Maximum Current on page 55 for information on the current ratings for the PCI/104-*Plus* connector.

POWER BUTTON

User I/O connector J4 includes an input for a push-button power switch. Shorting J4, pin 17 to ground causes the board to enter an S5 power state (similar to the Windows Shutdown state). Shorting it again returns the board to the S0 power state and reboots the board. The button can be configured in Windows to enter an S3 power state (Sleep, Standby, or Suspend-to-RAM), an S4 power state (Hibernate or Suspend-to-Disk), or an S5 power state (Shutdown or Soft-Off).

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 3.3 mA with a voltage drop that is less than 500 mV (there is a 1 kΩ resistor on the EPM-31 pulled up to 3.3 V). Do not add an external pull-up resistor to this signal.

A power button is provided on the CBR-4005B paddleboard. See Figure 27 on page 59 for the location of the reset button on the CBR-4005B paddleboard.

In configurations where a power button is not connected to the board, if the system is put into an S5 state, power can be restored by turning off the power supply and turning it back on. This behavior is set by default in the BIOS.

SUPPORTED POWER STATES

Table 4 lists the board's supported power states.

Table 4: Supported Power States

Power state	Description
S0 (G0)	Working
S1 (G1-S1)	All processor caches are flushed, and the CPUs stop executing instructions. Power to the CPUs and RAM is maintained. Devices that do not indicate they must remain on may be powered down.
S3 (G1-S3)	Commonly referred to as Standby, Sleep, or Suspend-to-RAM. RAM remains powered.
S4 (G1-S4)	Hibernation or Suspend-to-Disk. All content of main memory is saved to non-volatile memory, such as a hard drive, and is powered down.
S5 (G2)	Soft Off. Almost the same as G3 Mechanical Off, except that the power supply still provides power, at a minimum, to the power button to allow return to S0. A full reboot is required. No previous content is retained. Other components may remain powered so the computer can "wake" on input from the keyboard, clock, modem, LAN, or USB device.
G3	Mechanical off (ATX supply switch turned off).

BATTERY POWER OPTIONS

The battery circuit on the EPM-31 provides power for the Real-Time Clock (RTC) and power to store BIOS Setup utility settings in non-volatile RAM.

The EPM-31 has multiple options for providing battery power:

- Use an external battery, connected to the board through the J8 external battery connector.
- Use the battery supplied with the CBR-4005B paddleboard

Figure 9 shows the location and pin orientation of the external battery connector.

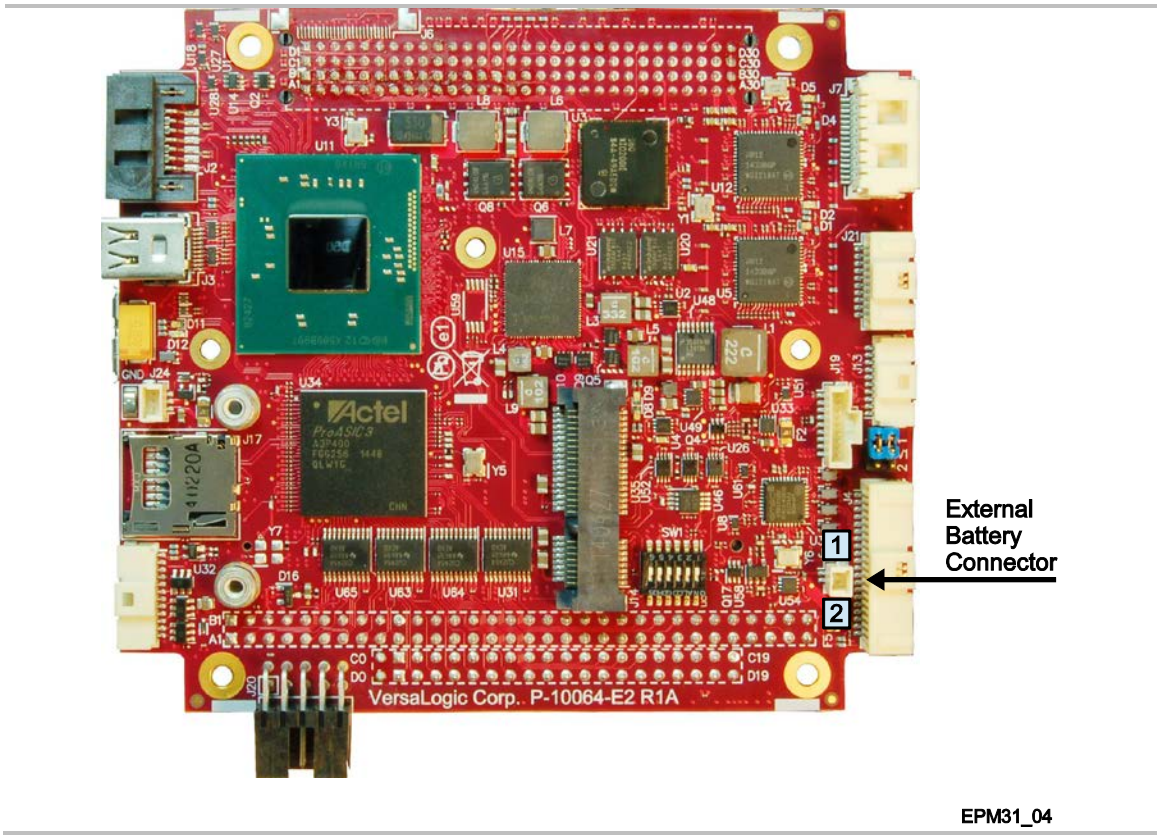


Figure 9. Location and Pin Orientation of the External Battery Connector

CABLING

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
Molex 501331-0207	Molex 501330-0200

VL-CBR-0203 External Battery Module

The VL-CBR-0203 external battery module is compatible with the EPM-31. For more information, contact Sales@VersaLogic.com.

Figure 10. VL-CBR-0203 Latching Battery Module

Real Time Clock (RTC)

The EPM-31 features a real-time clock/calendar (RTC) circuit. The RTC can be set using the BIOS Setup utility.

The EPM-31 supplies RTC voltage in S5, S3, and S0 states, but requires an external +2.75 V to +3.3 V battery to maintain RTC functionality and RTC CMOS RAM when the board is not powered. The battery connection can be made to either (but not both) of the following:

- J8 external battery connector
- J4 user I/O connector

Integrator's Note:

There is no on-board battery. The EPM-31 board will operate without a battery, but to save the date and time, use a VL-CBR-4005B paddleboard (which includes a battery) or connect an external battery to connector J8.

Push-Button Reset

User I/O connector J4 includes an input for a push-button reset switch. Shorting J4, pin 18 to ground causes the EPM-31 to reboot.

The input can be connected to ground using the normally open contacts of a pushbutton switch or a relay, or with a switching transistor (open-collector or open-drain) capable of sinking 3.3 mA with a voltage drop that is less than 500 mV (there is a 1 kΩ resistor on the EPM-31 pulled up to 3.3 V). Do not add an external pull-up resistor to this signal.

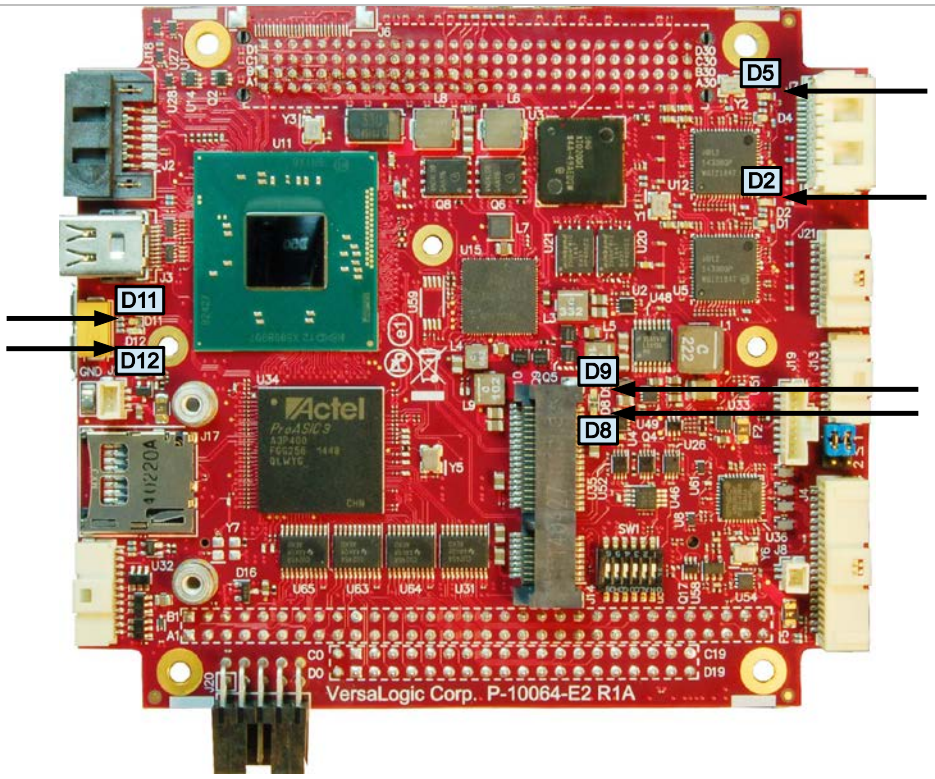
Integrator's Note:

The reset button has a switch de-bounce circuit in the FPGA that requires the button to be held asserted at least 125 ms (1/8 second) to reset the board. Holding the reset asserted on a Bay Trail processor does not continue to hold the processor in reset; it only resets on the edge of the assertion that follows the 125 ms de-bounce time interval).

A reset button is provided on the CBR-4005B paddleboard. See Figure 27 on page 59 for the location of the reset button on the CBR-4005B paddleboard.

LEDs/Indicators

Figure 11 shows the locations of the boards LEDs/indicators.



EPM31_19

LED	Description	For more information, see…
D5	Ethernet Port 0 status LED	Table 15, page 52
D2	Ethernet Port 1 status LED	Table 15, page 52
D9/D8	PCIe Mini Card LEDs	Table 7, page 37
D11	Power status LEDs	Figure 12, page 30
D12	SATA/mSATA Activity LED	Figure 16, page 36

Figure 11. Locations of the LEDs/Indicators

PROGRAMMABLE LED

User I/O connector J4 includes an output signal for attaching a software controlled LED. Connect the cathode of the LED to J4, pin 16; connect the anode to +3.3 V. An on-board 120 Ω resistor limits the current when the circuit is turned on. A programmable LED is provided on the CBR-4005B paddleboard. See Figure 27 on page 59 for the location of the Programmable LED on the CBR-4005B paddleboard.

For instructions on how to switch the Programmable LED on and off, refer to the *EPM-31 Programmer's Reference Manual* (available on the EPM-31 Product Support Web Page).

POWER LEDS

Figure 12 shows the location of the dual green/yellow LED. This dual LED indicates the following:

- The green LED illuminates when all power rails are within specified limits and indicates that the board is in the S0 power state. If any power rail is not within specified limits, the green LED will not illuminate. The green LED blinks at a slow rate when the processor is in a sleep or hibernate mode indicating that the sustain rail power is still within specified limits
- The yellow LED is a fault indicator that illuminates if there is a problem with the processor booting. (Software can also be used to turn on this LED to indicate a major software failure.)

The power LED on the VL-CBR-4005B5 indicates that the paddleboard is being powered by the +3.3 V supply (though it does not indicate that all S0 power supplies are within specified limits). The LED is lit only when the board is in the S0 power state. If the board enters a Sleep or Hibernate mode, the LED will not be lit.

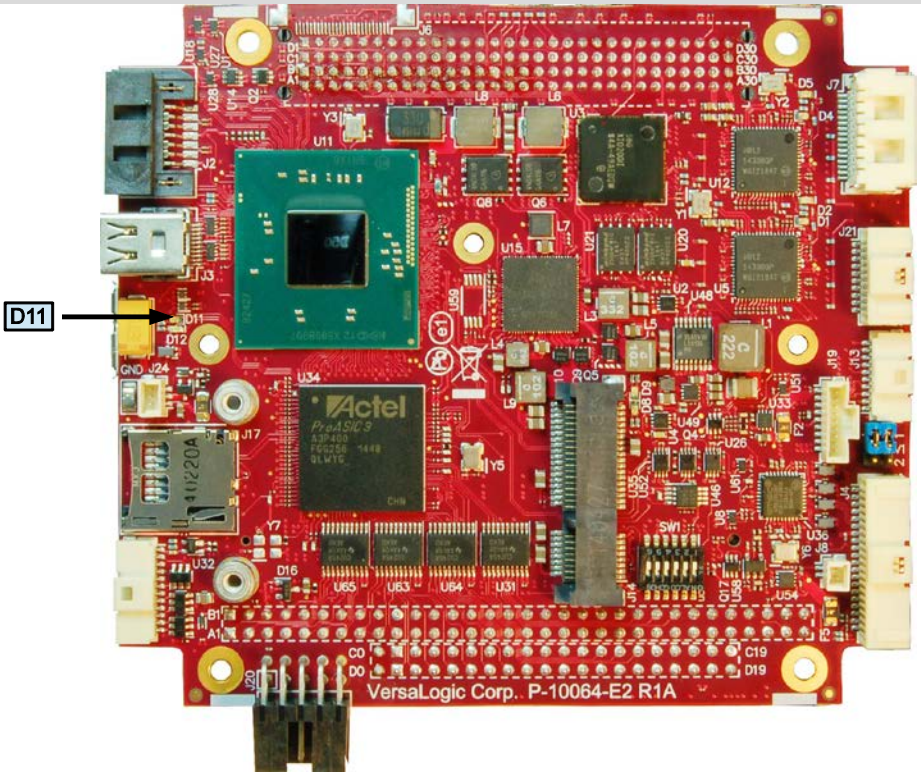


Figure 12. Location of the D11 Dual-color LED

External Speaker

A miniature 8 Ω speaker can be connected between user I/O connector J4, pin 15 (SPKR#) and J4, pin 13 (V3P3). A speaker is provided on the CBR-4005B paddleboard. See Figure 31 on page 64 for the location of the speaker on the CBR-4005B paddleboard.

SATA

The EPM-31 provides one 3 GB/s SATA port (J2). The SATA connector is a standard 7-pin right-angle connector with latching capability.

Power to the SATA drive is provided by the ATX power supply. Note that the standard SATA drive power connector is different from the typical 4-pin Molex connector used on IDE drives. Most current ATX power supplies provide SATA connectors, and many SATA drives provide both types of power connectors. If the power supply you are using does not provide SATA connectors, adapters are available.

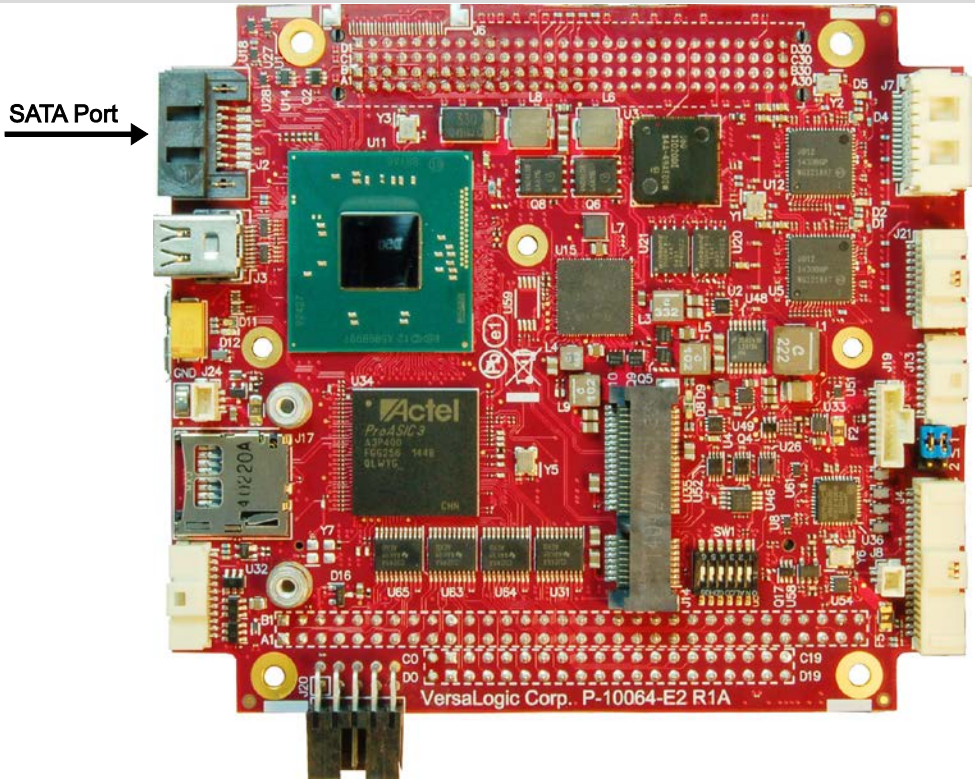


Figure 13. Location of the SATA Port

microSD Socket

Figure 14 shows the location of the microSD socket. The VL-F41 series of microSD cards provide solid-state storage of 2 GB, 4 GB, or 8 GB. The microSD socket accommodates cards with up to 32 GB of storage capacity. No drivers are needed, as the device interface is abstracted as a standard parallel IDE drive on the master IDE channel.

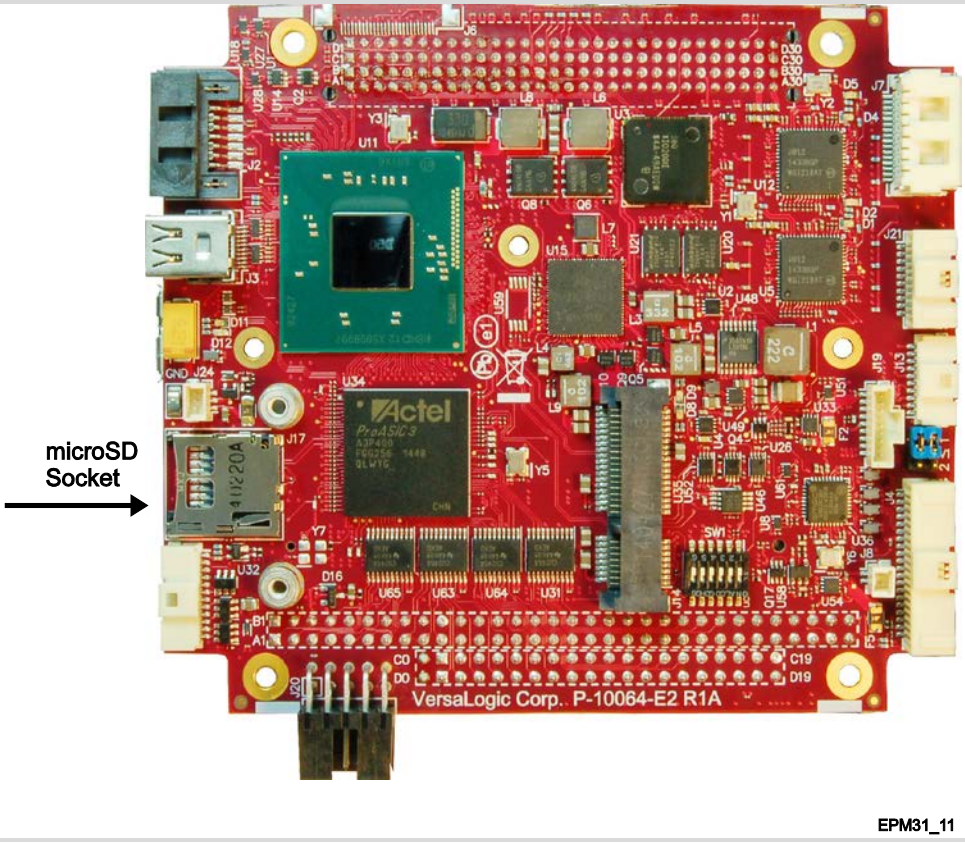


Figure 14. Location of the microSD Socket

USB Interfaces

The EPM-31 includes four USB 2.0 host ports and one USB 3.0 host port. The four USB 2.0 ports are incorporated into the J4 user I/O connector, with standard USB Type A connectors located on the VL-CBR-4005B paddleboard. Connector J16 on the bottom side of the board provides a USB 3.0 Micro-A (host) connector. Figure 15 shows the location of the USB 3.0 port.

This interface can operate using either the Atom processor's EHCI controller or its xHCI controller. To use the USB 3.0 Super Speed mode, the xHCI controller must be used. USB controller selection is set in the BIOS. By default, EHCI is used. Some older operating systems (such as MS-DOS) may not support xHCI.

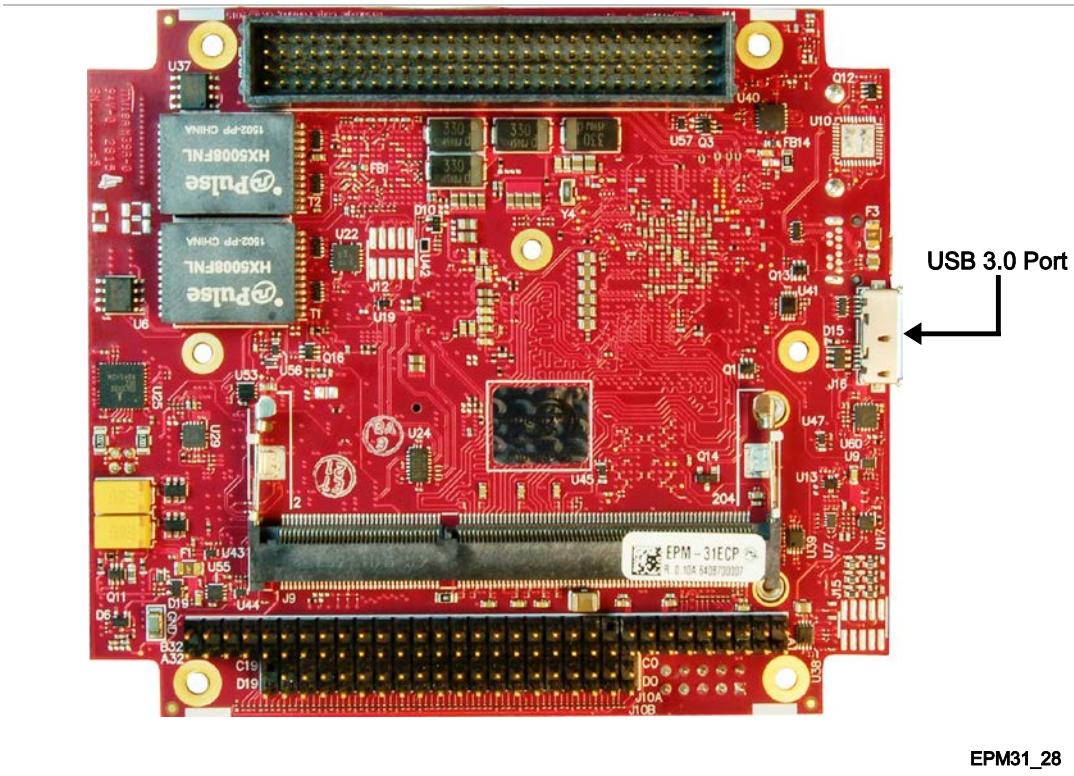


Figure 15. Location of the USB 3.0 Port (Bottom Side of the Board)

Table 5: USB 3.0 J16 Connector Pinout

J16 Pin	Signal Name	Direction	Function
1	+5V	Out	+5.0 volts
2	USB-	I/O	USB 2.0 differential pair negative
3	USB+	I/O	USB 2.0 differential pair positive
4	ID	In	Not used **(Note)**
5	GND	—	Ground
6	MICA_SSTX-	Out	USB 3.0 transmit differential pair negative
7	MICA_SSTX+	Out	USB 3.0 transmit differential pair positive
8	GND	—	Ground
9	MICA_SSRX-	In	USB 3.0 receive differential pair negative
10	MICA_SSRX+	In	USB 3.0 receive differential pair positive

Note: This signal is typically used for On-The-Go (OTG) mode. The BayCat does not support this mode.

CABLING

The VersaLogic VL-CBR-1015 cable is a USB 3.0 Micro-A to Micro-B adapter. The VL-CBR-1015 cable can be used to connect the BayCat to any certified USB 3.0 hubs.

PCIe Mini Card / mSATA

The socket at location J14 accepts a full-height PCI Express Mini Card or an mSATA module.

The PCIe Mini Card interface includes one PCIe x1 lane, one hubbed USB 2.0 channel, and the SMBus interface. The socket is compatible with plug-in Wi-Fi modems, GPS receivers, Flash data storage, and other cards for added flexibility. The VL-MPEs-F1E series of mSATA modules provide flash storage of 4 GB, 16 GB, or 32 GB.

For more information on PCIe Mini Cards offered by VersaLogic, contact Sales@VersaLogic.com.

To secure a Mini Card or mSATA module to the on-board standoffs, use two M2.5 x 6mm pan head Philips nylon screws. These screws are available in quantities of 10 in the VL-HDW-108 hardware kit from VersaLogic.

Table 6: PCIe Mini Card / mSATA Pinout

J14 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
1	WAKE#	Wake	Reserved	Not connected
2	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
3	NC	Not connected	Reserved	Not connected
4	GND	Ground	GND	Ground
5	NC	Not connected	Reserved	Not connected
6	1.5V	1.5V power	+1.5V	1.5V power
7	NC	Not connected	Reserved	Not connected
8	NC	Not connected	Reserved	Not connected
9	GND	Ground	GND	Ground
10	NC	Not connected	Reserved	Not connected
11	REFCLK-	Reference clock input –	Reserved	Not connected

J14 Pin	PCIe Mini Card Signal Name	PCIe Mini Card Function	mSATA Signal Name	mSATA Function
12	NC	Not connected	Reserved	Not connected
13	REFCLK+	Reference clock input +	Reserved	Not connected
14	NC	Not connected	Reserved	Not connected
15	GND	Ground	GND	Ground
16	NC	Not connected	Reserved	Not connected
17	NC	Not connected	Reserved	Not connected
18	GND	Ground	GND	Ground
19	NC	Not connected	Reserved	Not connected
20	W_DISABLE#	Wireless disable	Reserved	Not connected
21	GND	Ground	GND	Ground
22	PERST#	Card reset	Reserved	Not connected
23	PERn0	PCIe receive –	+B	Host receiver diff. pair +
24	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
25	PERp0	PCIe receive +	-B	Host receiver diff. pair –
26	GND	Ground	GND	Ground
27	GND	Ground	GND	Ground
28	1.5V	1.5V power	+1.5V	1.5V power
29	GND	Ground	GND	Ground
30	SMB_CLK	SMBus clock	Two Wire I/F	Two wire I/F clock
31	PETn0	PCIe transmit –	-A	Host transmitter diff. pair –
32	SMB_DATA	SMBus data	Two Wire I/F	Two wire I/F data
33	PETp0	PCIe transmit +	+A	Host transmitter diff. pair +
34	GND	Ground	GND	Ground
35	GND	Ground	GND	Ground
36	USB_D-	USB data –	Reserved	Not connected
37	GND	Ground	GND	Ground
38	USB_D+	USB data +	Reserved	Not connected
39	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
40	GND	Ground	GND	Ground
41	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source
42	LED_WWAN#	Wireless WAN LED	Reserved	Not connected
43	GND	mSATA detect (**Note 1**)	GND/NC	Ground/not connected (**Note 2**)
44	LED_WLAN#	Wireless LAN LED	Reserved	Not connected
45	NC	Not connected	Vendor	Not connected
46	LED_WPAN#	Wireless PAN LED	Reserved	Not connected
47	NC	Not connected	Vendor	Not connected
48	1.5V	1.5V power	+1.5V	1.5V power
49	Reserved	Reserved	DA/DSS	Device activity (**Note 3**)
50	GND	Ground	GND	Ground
51	Reserved	Reserved	GND	Ground (**Note 4)**
52	3.3VAUX	3.3V auxiliary source	+3.3V	3.3V source

Notes:

1. This pin is not grounded on the EPM-31 since it can be used to detect the presence of an mSATA module versus a PCIe Mini Card. Grounding this pin is available as an option on custom boards.
2. This pin is not grounded on the BayCat to make it available for mSATA module detection.
3. This signal drives the blue LED activity indicator at the location shown in Figure 16. This LED lights with mSATA disk activity, if supported by the mSATA module.
4. Some PCIe modules use this signal as a second Mini Card wireless disable input. On the BayCat, this signal is available for use for mSATA versus PCIe Mini Card detection. There is an option in BIOS setup for setting the mSATA detection method.

mSATA Activity LED

Figure 16 shows the location (D12) of the SATA/mSATA activity blue LED. This LED indicates activity on either the SATA or the mSATA interface. Not all mSATA drives provide this disk activity signal.

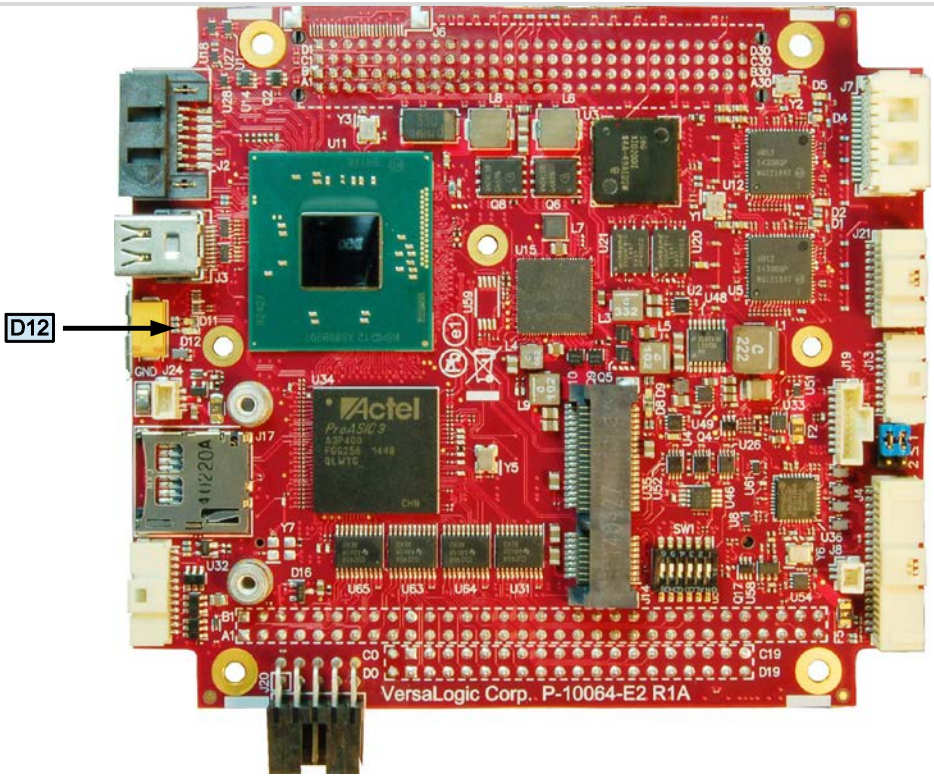


Figure 16. Location of the SATA/mSATA Activity LED

PCIe Mini Card LEDs

Two dual-colored PCIe Mini Card LEDs are provided on the EPM-31 at locations D9 and D8. Table 7 lists the states of the LEDs. Figure 17 shows the location of the PCIe Mini Card LEDs.

Table 7: PCIe Mini Card LED States

LED	Color	Status (when lit)
D9	Green	Activity on Wireless PAN (**Note**)
	Yellow	Illuminates when the 3.3 V power to the Mini Card is on. It alerts users to not hot-plug the Mini Card. By default, Mini Card power stays on when the processor is in sleep modes.
D8	Green	Activity on Wireless WAN (**Note**)
	Yellow	Activity on Wireless LAN (**Note**)

Note: These LEDs will illuminate when the associated device is installed and capable of transmitting. Their function is determined by the installed device.

Integrator's Note:

The 3.3 V power to the Mini Card can be controlled by the FPGA. By default, the power is always on, but there is a register setting that turns this power off in sleep modes. The Mini Card 1.5 V power is always turned off in sleep modes.

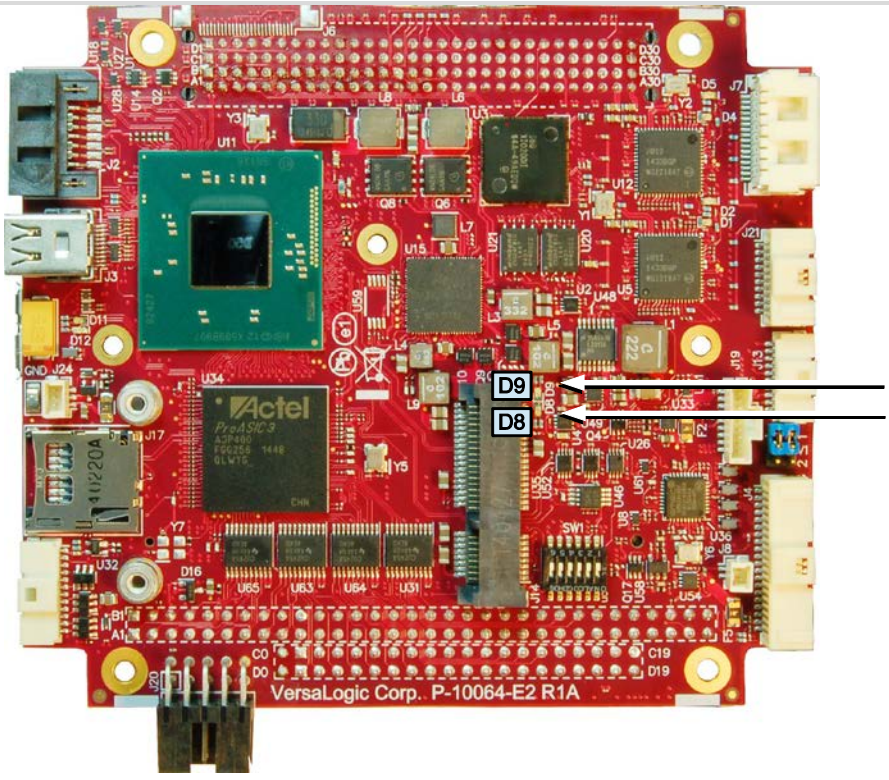


Figure 17. Location of PCIe Mini Card LEDs

User I/O Connector

The 40-pin J4 I/O connector incorporates the signals for the following:

- Four USB ports
- Eight GPIO lines (these are functionally muxed with six timer I/O signals per FPGA registers). There are eight timer signals and they share digital I/Os 16-9. The eight GPIO lines on the paddleboard each have an alternate mode, accessible using the FPGA's AUXMOD1 register. Refer to the *EPM-31 Programmer's Reference Manual* for more information on FPGA registers.
- Three LEDs (two Ethernet link status LEDs and a programmable LED)
- I^2C clock and data signals
- Push-button power switch
- Push-button reset switch
- Speaker output

This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

Figure 18 shows the location and pin orientation of the user I/O connector.

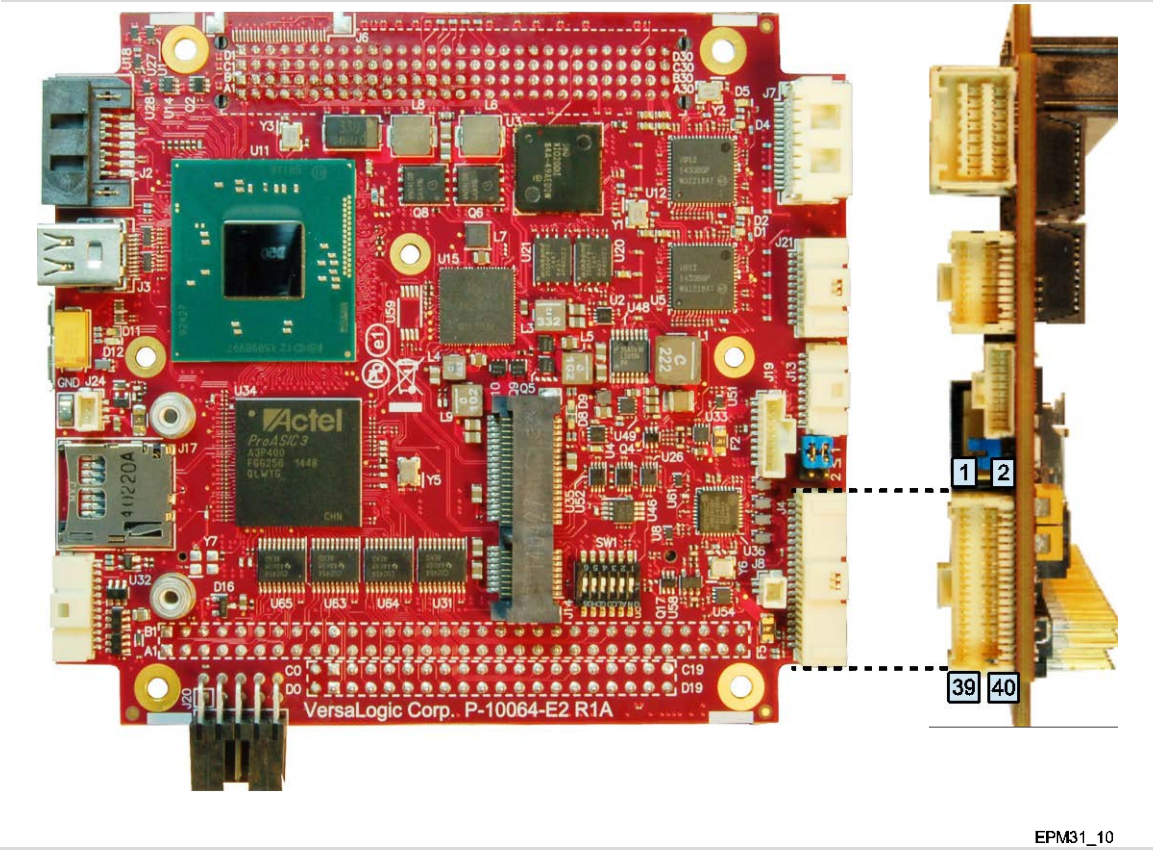


Figure 18. Location and Pin Orientation of User I/O Connector

Table 8 provides the pinout of the user I/O connector.

Table 8: J4 I/O Connector Pinout and Pin Orientation

Pin	Signal	Pin	Signal
1	+5 V	2	GND
3	USB0_P	4	USB1_P
5	USB0_N	6	USB1_N
7	+5V	8	GND
9	USB2_P	10	USB3_P
11	USB2_N	12	USB3_N
13	+3.3 V (**Note 1**)	14	GND
15	SPKR#	16	PLED#
17	PWR_BTN#	18	RST_BTN#
19	GND	20	GND
21	I2C Clock	22	V_BATT
23	I2C Data	24	RETURN_BATT
25	GND	26	GND
27	FPGA GPIO1	28	FPGA GPIO2
29	FPGA GPIO3	30	FPGA GPIO4
31	GND	32	GND
33	FPGA GPIO5	34	FPGA GPIO6
35	FPGA GPIO7	36	FPGA GPIO8
37	+3.3 V (**Note 2**)	38	GND
39	ETH0 LED	40	ETH1 LED

Notes:
1. This 3.3 V power goes off in sleep modes. The SPKR# uses this power as should the PLED# (there is no requirement for PLED# to use this power, but the CBR-4005 paddleboard does).
2. This 3.3 V power can be turned on our off similar to the 3.3V power to the Mini Card via the FPGA (can go off in sleep modes or always stay on; by default it goes off in sleep modes). It is used for the 10 kΩ pullup resistor power on the 8x GPIOs and usually for the 2x Ethernet LEDs, however, the Ethernet LEDs can be powered by a 3.3 V power source.

CABLING

An adapter cable, part number CBR-4005A, is available for connecting the CBR-4005B paddleboard to the EPM-31. This is a 12-inch, Pico-Clasp 40-pin to 40-pin cable

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
Molex 501571-4007	Molex 501189-4010

I^2C

Pins 21 and 23 of the J4 User I/O connector connect to the first of the seven I^2C ports on the Intel Atom "Bay Trail" processor. The EPM-31 has a 3.3 V I^2C interface. The required pullups for this interface are included in the EPM-31 design. The 3.3 V power for this interface is the same as that used for the digital I/O interface. By default, this power is turned off when the processor is in a sleep state.

Digital I/O (DIO)

The 20-pin I/O connector (J21) incorporates 16 Digital I/O (DIO) lines that are independently configurable as an input or output. DIO inputs can be set for normal or inverted level. DIO outputs can be set to be normal HIGH or LOW state. There are pull-up resistors to +3.3 V on all DIO lines. The pull-ups implemented — in the FPGA — can range in value from 20 kΩ to 40 kΩ. After reset, the DIO lines are set as inputs with pull-ups that will be detected as a HIGH state to external equipment.

VersaLogic provides a set of application programming interface (API) calls for managing the DIO lines. See the VersaAPI Support Page for information.

Figure 19 shows the location and pin orientation of the digital I/O connector. Table 9 lists the pin functions of the digital I/O connector and how the pins are routed to the VL-CBR-2004B paddleboard. Refer to page 64 for information on the VL-CBR-2004B paddleboard.

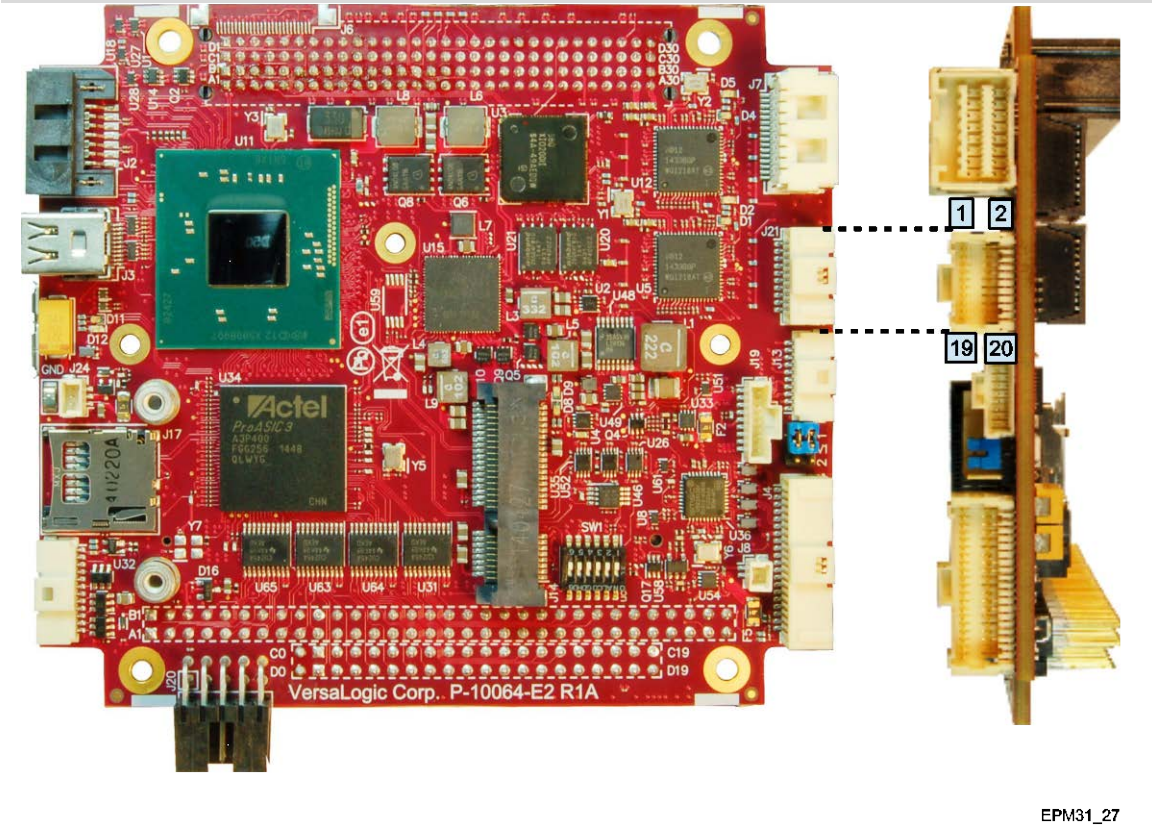


Figure 19. Location and Pin Orientation of Digital I/O Connector

Table 9: J21 I/O Connector Pinout

J21 Pin	Signal	VL-CBR-2004B Terminal Block	Terminal Block Pin
1	Digital I/O 1	J1	5
2	Digital I/O 2		4
3	Digital I/O 3		3
4	Digital I/O 4		1
5	Ground		2
6	Digital I/O 5	J2	5
7	Digital I/O 6		4
8	Digital I/O 7		2
9	Digital I/O 8		1
10	Ground		3
11	Digital I/O 9 (Optional Timer Channel 5 output)	J3	5
12	Digital I/O 10 (Optional Timer Channel 5 output)		3
13	Digital I/O 11 (Optional Timer Channel 4 Gate input)		2
14	Digital I/O 12 (Optional Timer Channel 3 Gate input)		1
15	Ground		4
16	Digital I/O 13 (Optional Timer 3 output)	J4	4
17	Digital I/O 14 (Optional Timer 3 input)		3
18	Digital I/O 15 (Optional Timer 4 output)		2
19	Digital I/O 16 (Optional Timer 4 input)		1
20	Ground		5

FPGA registers control the mode on pins 11-14 and 16-19. By default, they are DIOs. There are FPGA register settings to select the timer signals in 4-signal mode (pins 16-19) and 8-signal mode (11-15 and 16-19).

DIO Guidelines

Consider the following guidelines when using the DIO lines.

VOLTAGE

The DIO lines are 3.3 V Low-voltage TTL (LVTTL) compatible DIOs capable of sourcing/sinking up to 4 mA of current. Level shifting or current limiting is necessary when connecting signals with different voltage rails.

CAUTION:

Do not connect the DIO signals to external +5 V devices; doing so will damage the FPGA and void the warranty.

POWER STATES

CPU power states will affect voltage rails driving DIO circuits as described below:

- DIOs and their pull-up resistors will remain powered in all CPU power states (except when power is turned off). The DIO power (which includes the pullup voltage) can be controlled (the same power used for the 8x GPIOs on the CBR-4005 paddleboard) using an FPGA register setting. By default, they power-down in sleep modes but can be configured to always stay on.
- Power control during CPU power states on user devices connected to DIO lines is dependent on the application design. These external devices would likely remain powered unless a power-down mechanism is designed into the system.
- Care must be taken when powered DIO signals are connected to un-powered DIO signals. Significant voltage and current can be leaked from a powered system to an un-powered system causing unpredictable results. Current limiting and/or diode isolation can help.

CABLES

Cabling issues will affect the usable speed of DIO signals.

- These are single-ended drivers/receivers.
- Cabling crosstalk can be a problem with fast edge rates. The DIOs are slew-rate limited and have 50 Ω source terminators to minimize crosstalk and reflections.

Serial Ports

6

The EPM-31 features two on-board 16550-based serial communications channels located at standard PC I/O addresses. The serial ports can be operated in RS-232 4-wire, RS-422, or RS-485 modes. IRQ lines are chosen in the BIOS Setup utility. Each COM port can be independently enabled, disabled, or assigned a different I/O base address in the BIOS setup utility.

Serial Port Connectors

Figure 20 shows the location and pin orientation of the serial port connector.

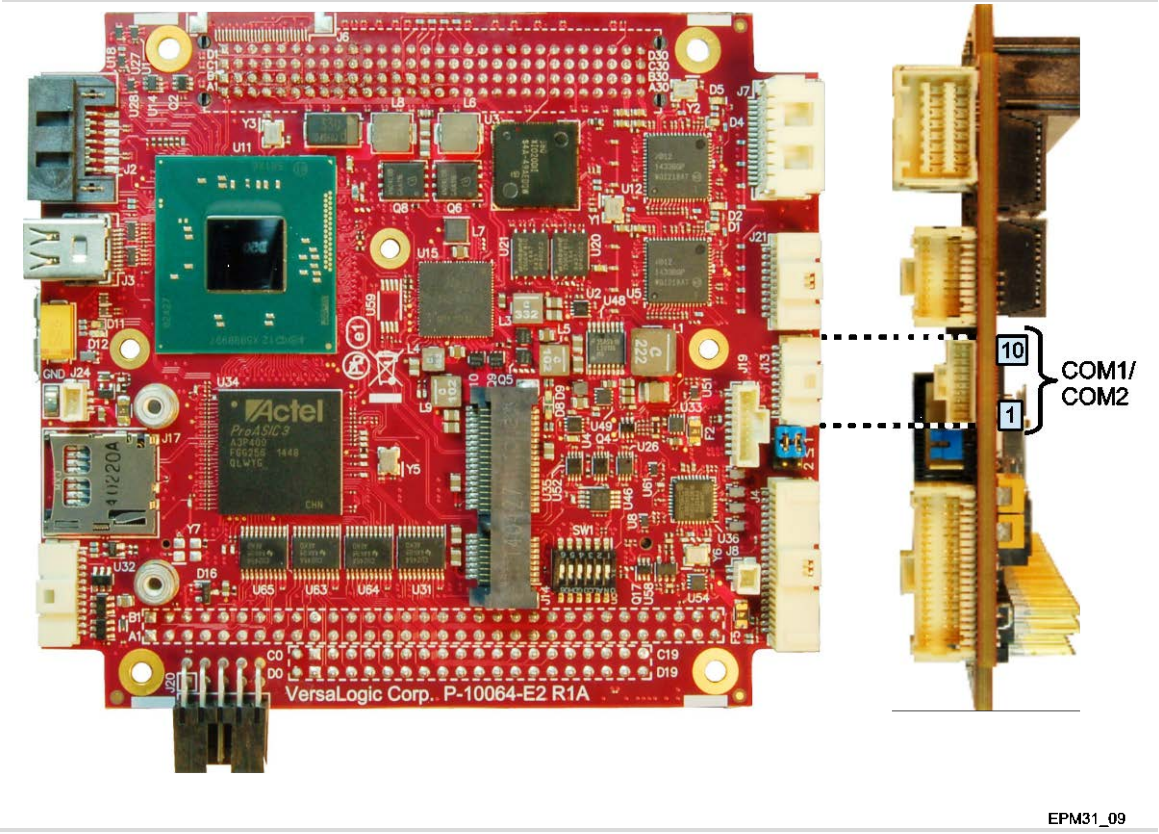


Figure 20. Location and Pin Orientation of Serial Port Connector

SERIAL PORT CONNECTOR PINOUTS

Table 10: J13 COM1/COM2 Connector Pinout

Pin	RS-232 Signal	RS-422/RS-485 Signal	Port
1	RTS1	TXD1_P	COM1
2	TXD1#	TXD1_N	
3	CTS1	RXD1_P	
4	RXD1#	RXD1_N	
5	GND	GND	—
6	RTS2	TXD2_P	COM2
7	TXD2#	TXD2_N	
8	CTS2	RXD2_P	
9	RXD2#	RXD2_N	
10	GND	GND	—

CABLING

An adapter cable, part number CBR-1014, is available for routing the J13 signals to 9-pin D-sub connectors. This is a 12-inch, Pico-Clasp 10-pin to two 9-pin D-sub connector cable.

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
Molex 501331-1007	Molex 501330-1000

RS-485 MODE LINE DRIVER CONTROL

The transmit line driver can be automatically turned on and off based on data availability in the UART output FIFO. This mode can be enabled in the BIOS setup utility. The transmit line driver can be enabled in the BIOS Setup utility.

COM1/COM2 Hardware Configuration

Jumper block V1[1-2] enables the RS-422/485 termination resistor for COM1. Jumper V1[3-4] enables the RS-422/485 termination resistor for COM2. The termination resistor should be enabled for an RS-422 or RS-485 endpoint station; it should be disabled for RS-232 and RS-485 non-endpoint receivers.

Table 11: COM1/COM2 Termination Jumpers

Jumper Position	Function	Jumper In	Jumper Out
1-2	COM1 Rx Termination	RS-485/RS-422 (**Note**)	RS-232 (default)
3-4	COM2 Rx Termination	RS-485/RS-422 (**Note**)	RS-232 (default)

Note: RS-485 non-endpoints do not require termination. If receivers are mid-line, remove this termination jumper.

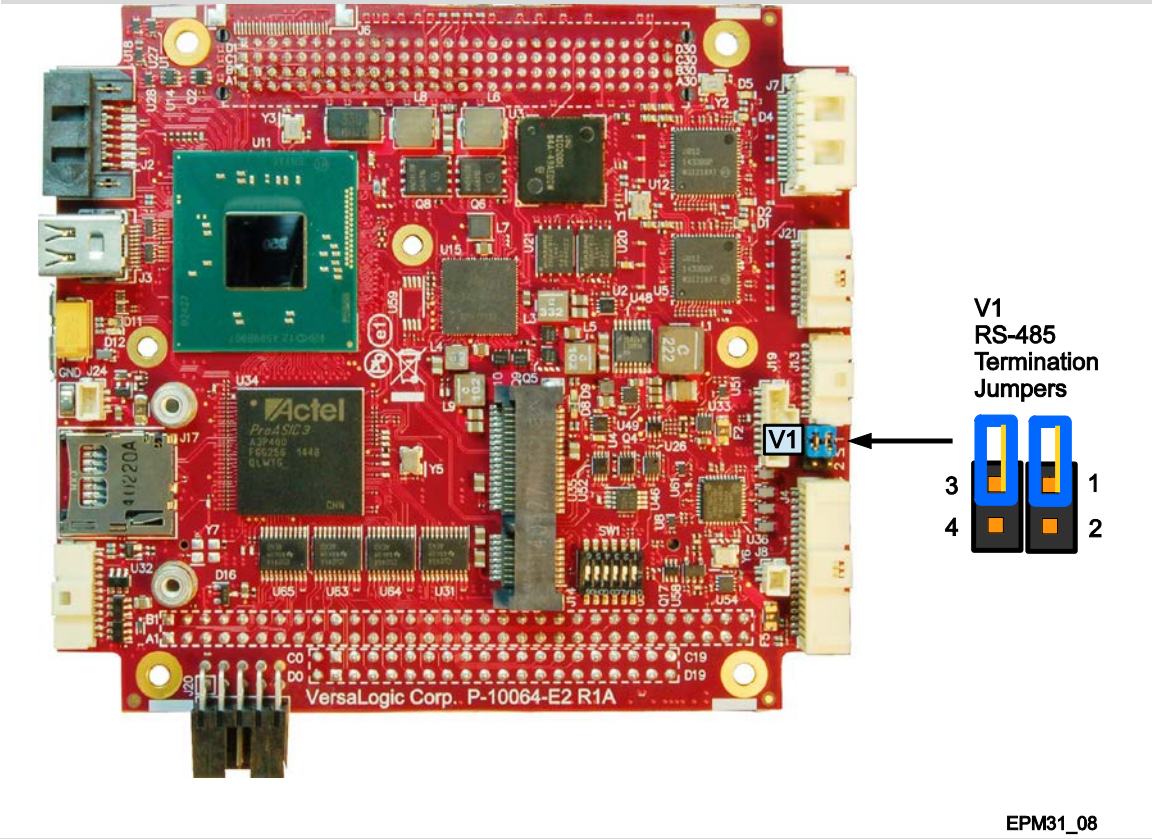


Figure 21. COM1/COM2 End-point Termination Jumpers

7 Video Interfaces

The EPM-31 incorporates the Intel Gen-7 graphics core with four Execution Units and Turbo Boost. It supports two independent displays. It also supported formats including DirectX 11, OpenGL 3, VP8, MPEG2, H.264, VC1, 2 HD streams (1080p@30fps), Flash and WMP support.

The analog (VGA) and Mini DisplayPort video interfaces support Extended Desktop, Clone, and Twin display modes.

The optional VL-EPH-V6 video adapter card converts DisplayPort output to LVDS for flat panel operation.

VGA Interface

The VGA port supports resolutions up to 2560 x 1600 at 60 Hz. This connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage.

When the EPM-31 board is booted, the BIOS tests for a video monitor attached to the VGA port. If a monitor is not detected during this test, the VGA signals are disabled.

Figure 22 shows the location and pin orientation of the J5 VGA video output connector.

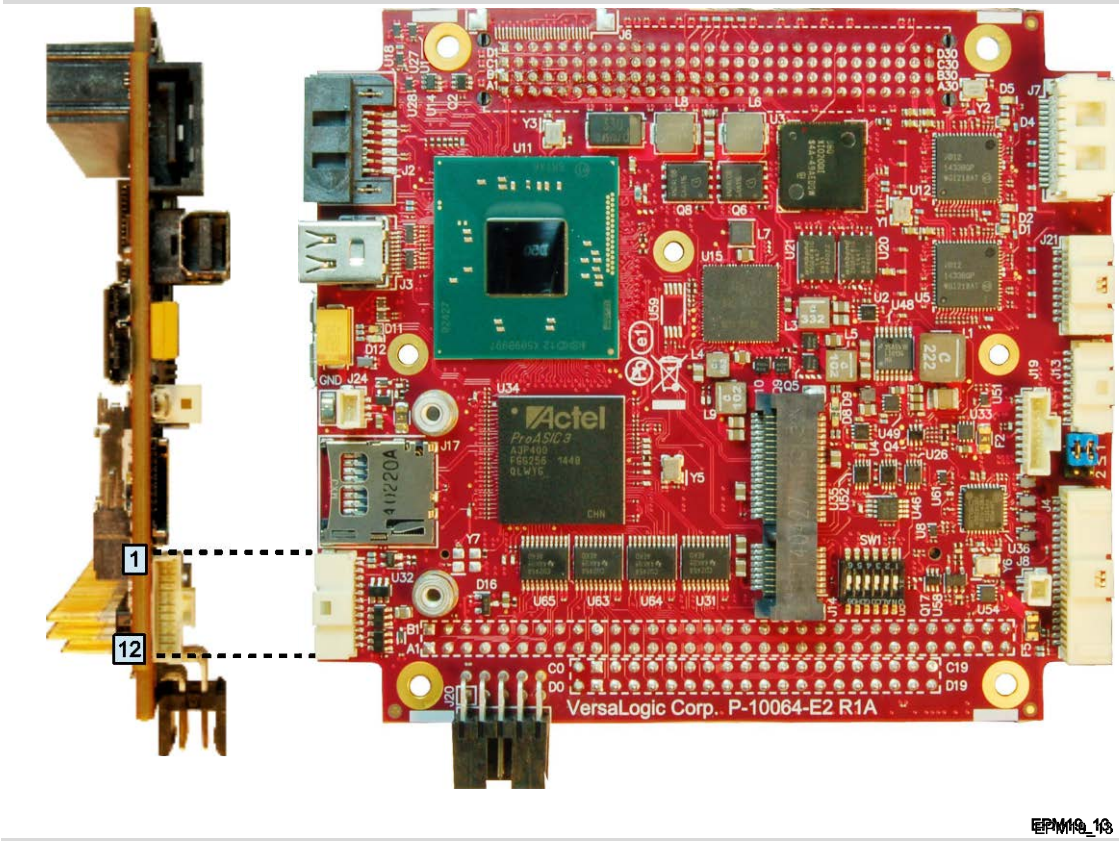


Figure 22. VGA Connector Location and Pin Configuration

Table 12 lists the signals of the VGA video output connector.

Table 12: J5 VGA Video Output Pinout

Pin	Signal (Function)	DB-15 Pin
1	Ground	6
2	RED (Red video)	1
3	Ground	7
4	GREEN (Green video)	2
5	Ground	8
6	BLUE (Blue video)	3
7	Ground	5
8	HSYNC (Horizontal sync)	13
9	Ground	10
10	VSYNC (Vertical sync)	14
11	CRT_SCL (DDC data clock line)	15
12	CRT_SDA (DDC serial data line)	12

CABLING

An adapter cable, part number CBR-1204, is available to translate J5 into a standard 15-pin D-Sub VGA connector. This is a 12-inch, 12-pin Pico-Clasp to 15-pin VGA cable.

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
Molex 501568-1207	Molex 501330-1200

Mini DisplayPort Connector

DisplayPort consists of three interfaces:

- Main Link – transfers high-speed isochronous video and audio data
- Auxiliary channel – used for link management and device control; the EDID is read over this interface
- Hot Plug Detect – indicates that a cable is plugged in

The DisplayPort interface supports:

- Audio signaling
- DP++ mode allowing connection to an HDMI device through a passive adapter. "Passive" means that the adapter does not require external power (because it uses the DP port's 3.3 V power) and it does not require software drivers.

Figure 23 shows the location of the 20-pin Mini DisplayPort connector. Table 13 lists the pinout of the J3 Mini DisplayPort connector.

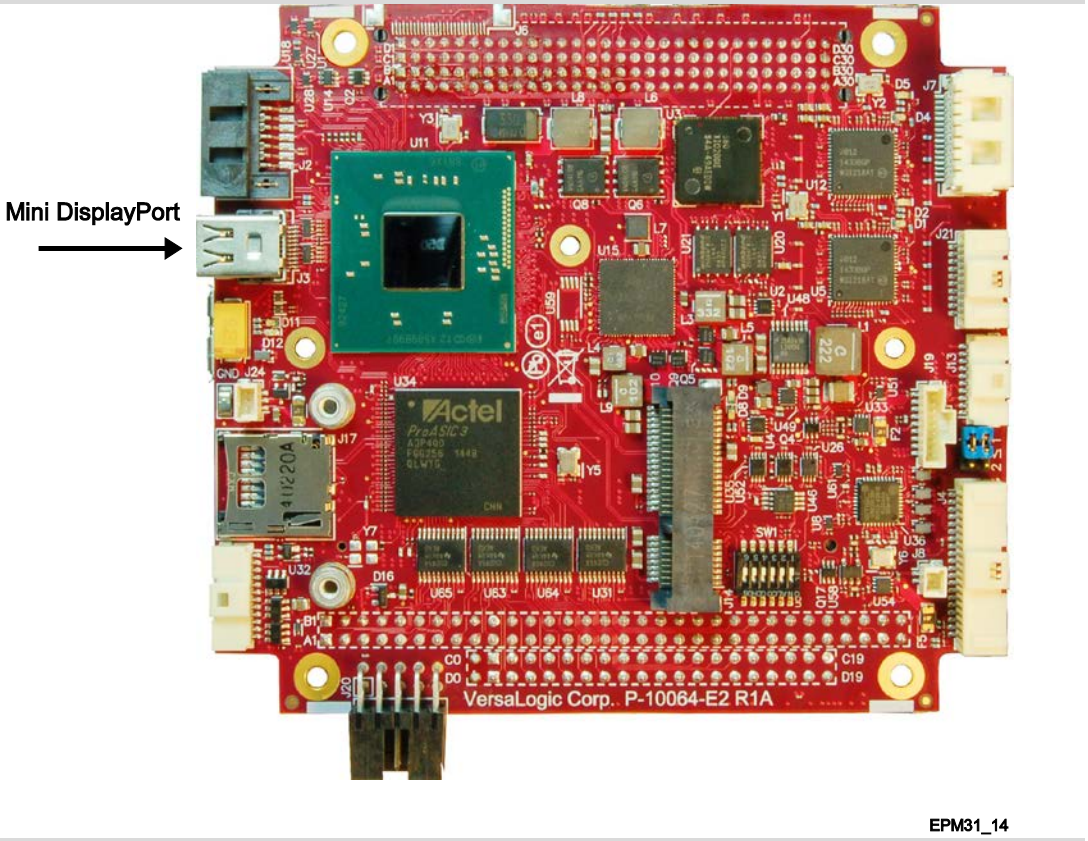


Figure 23. Location of the Mini DisplayPort Connector

Table 13: J3 Mini DisplayPort Connector Pinout

Pin	Signal	Pin	Signal
1	GND	2	HOT PLUG DETECT
3	ML_LANE0_P	4	CONFIG 1
5	ML_LANE0_N	6	CONFIG 2
7	GND	8	GND
9	ML_LANE1_P	10	ML_LANE3_P
11	ML_LANE1_N	12	ML_LANE3_N
13	GND	14	GND
15	ML_LANE2_P	16	AUX_CH_P
17	ML_LANE2_N	18	AUX_CH_N
19	RTN	20	DP_POWER

Console Redirection

The EPM-31 can be configured for remote access by redirecting the console to a serial communications port. The BIOS setup utility and some operating systems (such as MS-DOS) can use this console for user interaction. The default settings for the redirected console are as follows:

- 115,200 baud rate
- 8 data bits, no parity
- 1 stop bit)
- No parity
- No flow control

8 Network Interfaces

The EPM-31 provides two on-board Intel I210-IT Gigabit Ethernet controllers. The controllers provide a standard Ethernet interface for 1000Base-T, 100Base-TX, and 10Base-T applications. The I210-IT Ethernet controller auto-negotiates connection speed. Drivers are available to support a variety of operating systems.

ETHERNET CONNECTOR

The J7 connector provides access to the Ethernet ports 0 and 1. The J7 connector uses IEC 61000-4-2-rated TVS components to help protect against ESD damage. Figure 24 shows the location and pin orientation of the Ethernet connector.

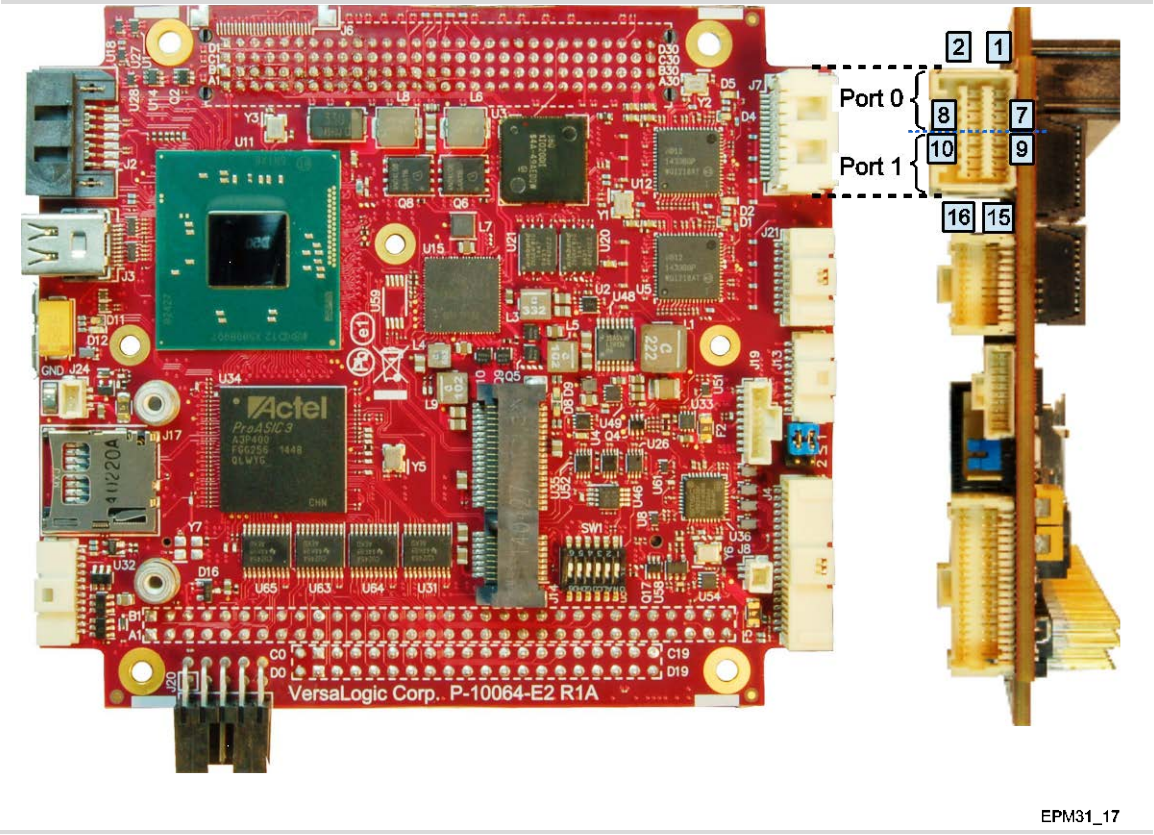


Figure 24. Location and Pin Orientation for the J7 Ethernet Connector

Table 14 lists the pinout of the Ethernet connector.

Table 14: Ethernet Connector Pinout

	Pin	10/100 Signals	10/100/1000 Signals	Pin	10/100 Signals	10/100/1000 Signals	
Port 0	1	- Auto Switch (Tx or Rx)	BI_DD-	2	+ Auto Switch (Tx or Rx)	BI_DD+	Port 0
	3	- Auto Switch (Tx or Rx)	BI_DB-	4	+ Auto Switch (Tx or Rx)	BI_DB+	
	5	- Auto Switch (Tx or Rx)	BI_DC-	6	+ Auto Switch (Tx or Rx)	BI_DC+	
	7	- Auto Switch (Tx or Rx)	BI_DA-	8	+ Auto Switch (Tx or Rx)	BI_DA+	
Port 1	9	- Auto Switch (Tx or Rx)	BI_DD-	10	+ Auto Switch (Tx or Rx)	BI_DD+	Port 1
	11	- Auto Switch (Tx or Rx)	BI_DB-	12	+ Auto Switch (Tx or Rx)	BI_DB+	
	13	- Auto Switch (Tx or Rx)	BI_DC-	14	+ Auto Switch (Tx or Rx)	BI_DC+	
	15	- Auto Switch (Tx or Rx)	BI_DA-	16	+ Auto Switch (Tx or Rx)	BI_DA+	

CABLING

An adapter cable, part number CBR-1604, is available. This is a 12-inch, 16-pin Click-Mate to two RJ-45 connector cables.

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
Molex 503148-1690	Molex 503149-1600

ON-BOARD ETHERNET STATUS LEDS

On-board status LEDs are provided for both Ethernet ports:

- D5 (green LED) provides status for Ethernet port 0
- D2 (green LED) provides status for Ethernet port 1

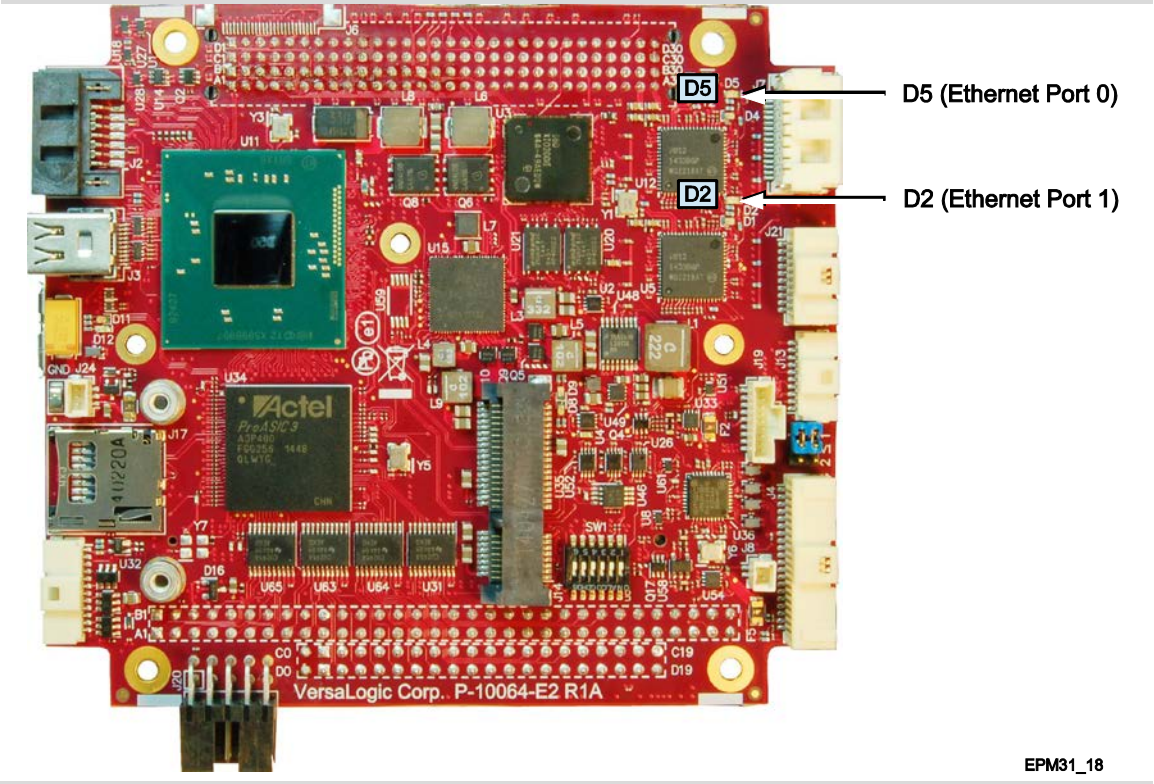


Figure 25. Location of Ethernet Status LEDs

Table 15: Ethernet Status LEDs

Ethernet Port	LED	State	Description
Port 0	D5	On	Cable connected (blinks with activity)
		Off	Cable not connected
Port 1	D2	On	Cable connected (blinks with activity)
		Off	Cable not connected

SPX™ Expansion Bus

Up to two serial peripheral expansion (SPX) devices can be attached to the EPM-31 at connector J19 using a CBR-0901 cable. The SPX interface provides the standard serial peripheral interface (SPI) signals: CLK, MISO, and MOSI, as well as two chip selects, SS0# and SS1#. The +5 V power provided to pin 1 of the SPX connector is protected by a 1 A resettable fuse.

Figure 26 shows the location and pin orientation of the SPX connector.

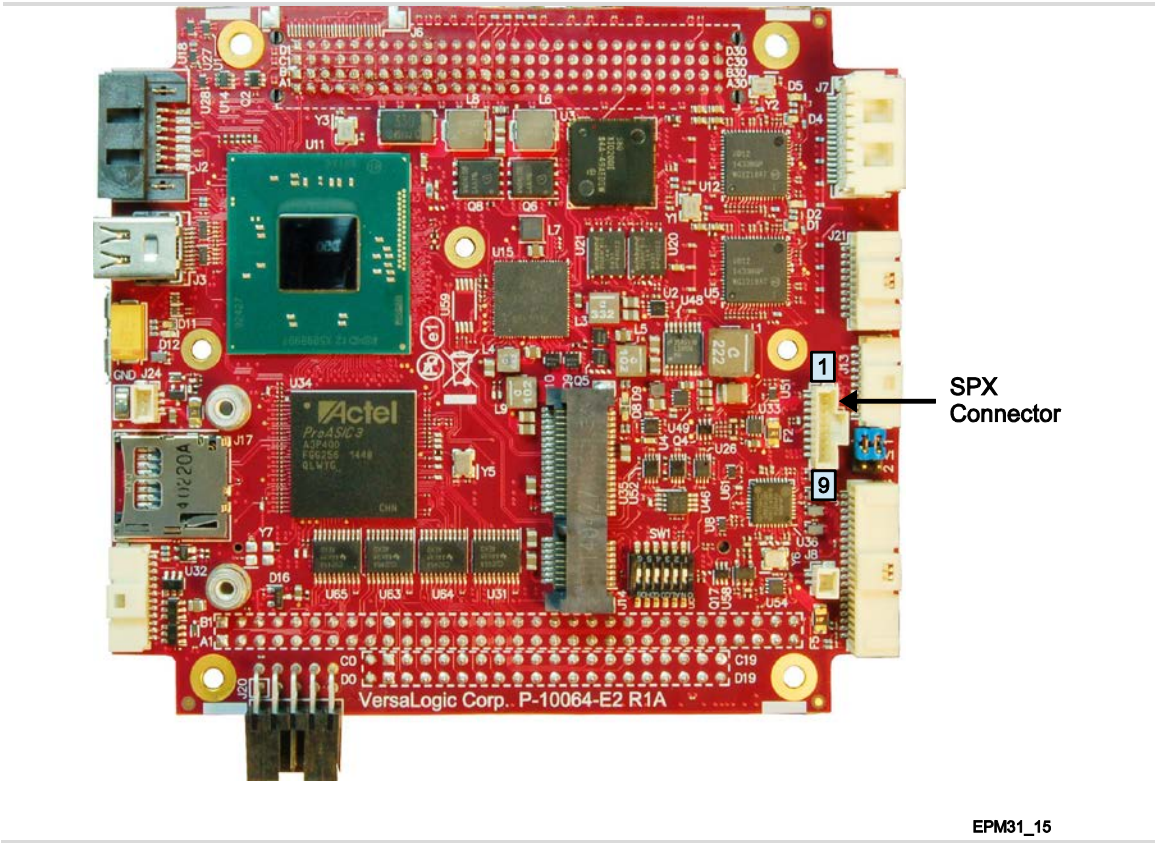


Figure 26. J19 SPX Connector Location and Pin Configuration

Table 16 lists the pinout of the SPX connector.

Table 16: SPX Connector Pinout

Pin	Signal	Function
1	V5_SPX	+5.0 V
2	CLK	SPX Clock
3	GND	Ground
4	MISO	Master input, Slave output
5	GND	Ground
6	MOSI	Master output, Slave input
7	GND	Ground
8	SS0#	Chip Select 0
9	SS1#	Chip Select 1

SPI is, in its simplest form, a three wire serial bus. One signal is a clock, driven only by the permanent master device on-board. The others are Data In and Data Out with respect to the master. The SPX implementation on the EPM-31 board supports chip selects. The master device initiates all SPI transactions. A slave device responds when its chip select is asserted and it receives clock pulses from the master. All four common SPI modes are supported through the use of clock polarity and clock idle state controls.

The SPI clock is derived from a 33 MHz PCI clock and can be software-configured to operate at the following frequencies:

- 8.25 MHz (33 MHz/4)
- 4.125 MHz (33 MHz/8)
- 2.0625 MHz (33 MHz/16)
- 1.03125 MHz (33 MHz/32)

CABLING

An adapter cable, part number CBR-0901, is available. This is a 9-inch, 9-pin Pico-Clasp to Dual SPX cable.

If your application requires a custom cable, the following information will be useful:

EPM-31 Board Connector	Mating Connector
Molex 501568-0907	Molex 501330-0900

VERSALOGIC SPX EXPANSION MODULES

VersaLogic offers several SPX modules that provide a variety of standard functions, such as analog input, digital I/O, CANbus controller, and others. These are small boards (1.2 inches x 3.775 inches) that can mount on the PC/104 and PC/104-*Plus* stack, using standard PC/104 stand-offs, or up to two feet away from the base board. For more information, contact VersaLogic at info@VersaLogic.com.

PC/104-*Plus* Expansion Bus

The EPM-31 provides a legacy stack-down PCI connector at locations J11 (for PCI) and J10 (for ISA) on the bottom side of the board for PC/104-*Plus* (PCI +ISA) as well as PCI-104 (PCI only) and PC/104 (ISA only) expansion modules. Figure 3 on shows the locations of these connectors.

Integrator's Notes:

- PC/104 ISA only modules (those that have no PCI connector) must not be positioned below the PC/104-Plus (PCI+ISA) modules in the stack.
- Modules with PCI interfaces must be above those with only ISA interfaces.
- PCI-104 PCI only modules (those with no ISA connector) must not be positioned below the PC/104-Plus (PCI+ISA) modules in the stack.
- In general, PC/104 (ISA only) and PCI-104 (PCI only) cards can never be used together in a stack.

Table 17 lists the maximum PC/104-*Plus* slot current rating on the EPM-31. This is the aggregate power available to both the PCI and ISA connectors. ISA does not use +3.3 V power, so all of the +3.3 V power is available for the PCI connector.

Table 17: PCI/104-*Plus* Connector (PCI) Maximum Current

Voltage	Maximum Current
+5 V	4.0 A
+3.3 V	3.0 A
+12 V	1.0 A
–12 V	0.5 A

ISA Bus (on PC/104-*Plus* and PC/104 Expansion Modules)

Refer to the ISA sections of the PC/104-Plus Specification for a complete description of this interface.

The EPM-31 implements the ISA bus on PC/104-*Plus* and PC/104 expansion modules using an LPC-to-ISA bridge implemented in the FPGA. This LPC-to-ISA bridge supports all features except the following:

- The ISA bus must not be mastered by an external module. The EPM-31 is always the bus master. The MASTER signal on pin D17 of J10 is not connected.
- The REFRESH output signal on B19 of J10 is not supported; it is pulled up to a high logic level.
- DMA is not supported. The seven DACKx outputs on pins B15, B17, B26, D8, D10, D12, and D14 on J10 are pulled up to a high logic level. The seven DRQx inputs on pins B6, B16, B18, D9, D11, D13, and D15 on J10 are not connected. The Terminal Count (TC) output on pin B27 of J10 is pulled low.
- –5.0V power is not provided on J10 pin B5. This pin is not connected.

Most PC/104-*Plus* (PCI +ISA) or PC/104 (ISA only) expansion modules will work, but be sure to check the requirements of your PC/104 card against the list above.

ISA I/O SUPPORT

Both 8-bit and 16-bit I/O cycles are supported, but for 16-bit cycles the PC/104 (ISA) module must be 16-bit capable and must assert IOCS16#.

Table 18 lists the I/O ranges available on the ISA bus unless there is a device claiming the range on the LPC or PCI bus. The FPGA on the EPM-31 uses I/O addresses 0xC80-0xCBF and, if enabled, the FPGA has two COM ports that can be configured in the BIOS Setup utility to map to various address ranges.

By default, the two COM ports in the FPGA are enabled and occupy the I/O address ranges of 0x3F8-0x3FF and 0x2F8-0x2FF. The following are the I/O address ranges available on the ISA bus when the BIOS is configured to factory defaults.

Table 18: Available ISA Bus I/O Ranges

▪ 0x0 – 0x1F	▪ 0x3E – 0x3F	▪ 0x93 – 0x9F	▪ 0x300 – 0x3AF
▪ 0x22 – 0x23	▪ 0x43 – 0x4F	▪ 0xA2 – 0xA3	▪ 0x3BC – 0x3BF
▪ 0x26 – 0x27	▪ 0x53 – 0x5F	▪ 0xA6 – 0xA7	▪ 0x3E0 – 0x3F7
▪ 0x2A – 0x2B	▪ 0x62	▪ 0xAA – 0xAB	▪ 0x480 – 0x4CF
▪ 0x2E – 0x2F	▪ 0x66	▪ 0xAE – 0xAF	▪ 0x4D2 – 0x4FF
▪ 0x32 – 0x33	▪ 0x68 – 0x70	▪ 0xB6 – 0xB7	▪ 0x600 – 0xC7F
▪ 0x36 – 0x37	▪ 0x78 – 0x7F	▪ 0xBA – 0xBB	▪ 0xCC0 – 0xCF8
▪ 0x3A – 0x3B	▪ 0x90 – 0x91	▪ 0xBE – 0x2F7	▪ 0xCFA – 0xCFB
▪	▪	▪	▪ 0xD00 – 0xFFF

Assuming the COM ports in the FPGA are disabled, the available I/O base addresses for COM ports on the ISA bus are as follows:

▪ 0x200	▪ 0x228	▪ 0x338
▪ 0x208	▪ 0x238	▪ 0x3E8
▪ 0x220	▪ 0x2E8	▪ 0x3F8

Each COM port in the FPGA that is enabled will use one of these I/O base addresses and, in that case, that 8 byte I/O range will not be available on the ISA bus. PCI devices may be assigned I/O space, but that usually occurs at I/O address 0x1000 or higher so as to not conflict with legacy I/O devices.

ISA MEMORY SUPPORT

The following memory addresses are available on the ISA bus:

- 0xA0000 – 0xB7FFF

▪

ISA IRQ SUPPORT

The following IRQs are supported on the ISA bus:

▪ IRQ3	▪ IRQ9[1]
▪ IRQ4	▪ IRQ10[1]
▪ IRQ5	▪ IRQ11
▪ IRQ6	▪ IRQ12
▪ IRQ7	▪ IRQ15

Each of the IRQs must be enabled in the BIOS Setup utility before they can be used. (All are disabled by default.)

Because ISA IRQ sharing is not supported,

[1]Some IRQs may not be available to the ISA bus due to operating system limitations.

- IRQ 9 is used by the ACPI SCI (System Control Interrupt) by default, and requires a custom BIOS for use on the ISA bus.
- IRQ 10 is used for PCI IRQ routing, and usually requires a custom BIOS for use on the ISA bus.

PCI BUS (ON PC/104-*PLUS* AND PCI-104 EXPANSION MODULES)

Refer to the PCI sections of the PC/104-Plus Specification for a complete description of this interface.

Make sure to correctly configure the PCI slot position jumpers on each PC/104-*Plus* or PCI-104 module appropriately.

The BIOS automatically allocates I/O, memory, and interrupt resources.

10 System Resources and Maps

Refer to the *EPM-31 Programmer's Reference Manual* for the following information:

- Memory map
- IRQ map
- I/O map
- FPGA register map
- FPGA register descriptions
- Programming information for certain hardware interfaces.

CBR-4005B Paddleboard

CBR-4005B Connectors and Indicators

Figure 31 shows the locations of the connectors, switches, and LEDs on the CBR-4005B paddleboard.

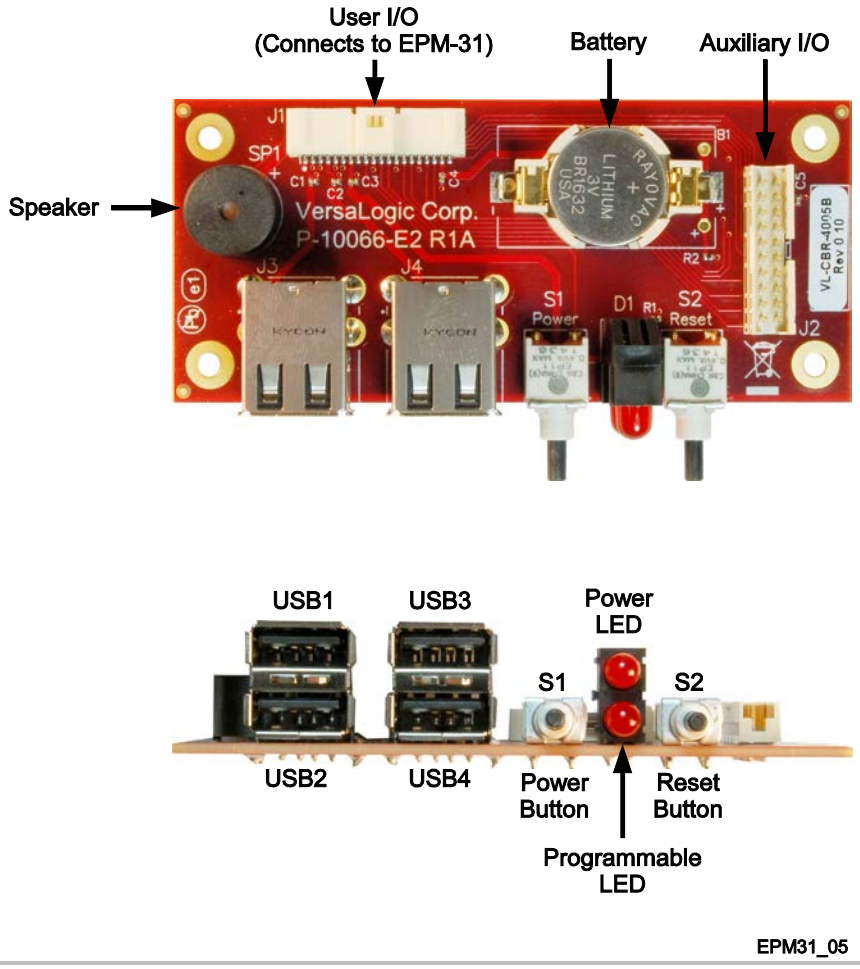


Figure 27. CBR-4005B Connectors, Switches, and LEDs

USER I/O CONNECTOR

Figure 31 shows the location and pin orientation of the user I/O connector.

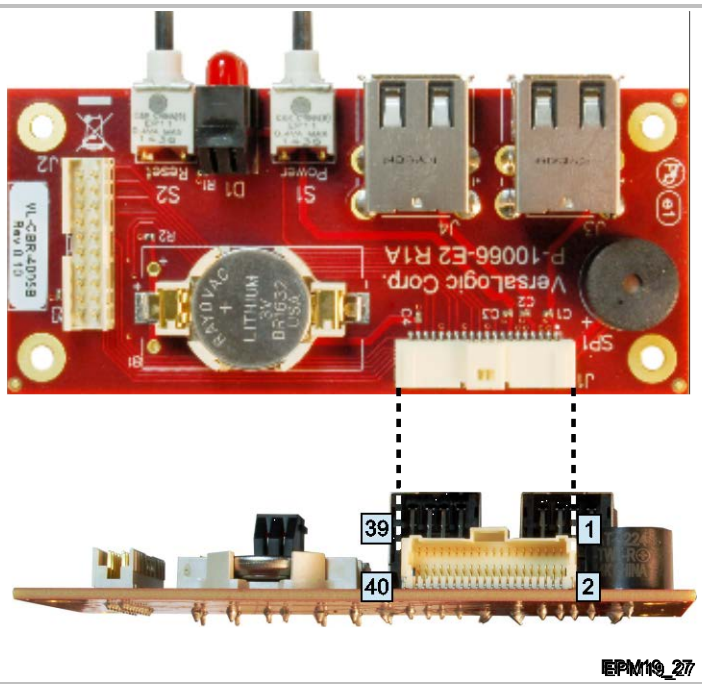


Figure 28. Location and Pin Orientation of the User I/O Connector

Table 19: User I/O Connector Pinout

Pin	Signal	Pin	Signal
1	+5 V	2	GND
3	USB1_P	4	USB2_P
5	USB1_N	6	USB2_N
7	+5V	8	GND
9	USB3_P	10	USB4_P
11	USB3_N	12	USB4_N
13	+3.3 V	14	GND
15	SPKR#	16	PLED#
17	PWR_BTN#	18	RST_BTN#
19	GND	20	GND
21	I2C Clock	22	V_BATT
23	I2C Data	24	V_BATT_RETURN
25	GND	26	GND
27	FPGA GPIO1	28	FPGA GPIO2
29	FPGA GPIO3	30	FPGA GPIO4
31	GND	32	GND
33	FPGA GPIO5	34	FPGA GPIO6
35	FPGA GPIO7	36	FPGA GPIO8
37	+3.3 V	38	GND
39	ETH0 LED	40	ETH1 LED

CABLING

An adapter cable, part number CBR-4005A, is available for connecting the CBR-4005B paddleboard to the EPM-31. This is a 12-inch, Pico-Clasp 40-pin to 40-pin cable

If your application requires a custom cable, the following information will be useful:

CBR-4005B Board Connector	Mating Connector
Molex 501571-4007	Molex 501189-4010

ON-BOARD BATTERY

CAUTION:

To prevent shorting, premature failure or damage to the Lithium battery, do not place the board on a conductive surface such as metal, black conductive foam or the outside surface of a metalized ESD protective pouch. The Lithium battery may explode if mistreated. Do not recharge, disassemble, or dispose of the battery in fire. Dispose of used batteries promptly.

Nominal battery voltage is 3.0 V. If the voltage drops below 2.7 V, contact the factory for a replacement. The life expectancy under normal use is approximately five years.

AUXILIARY I/O CONNECTOR

Figure 31 shows the location and pin orientation of the auxiliary I/O connector.

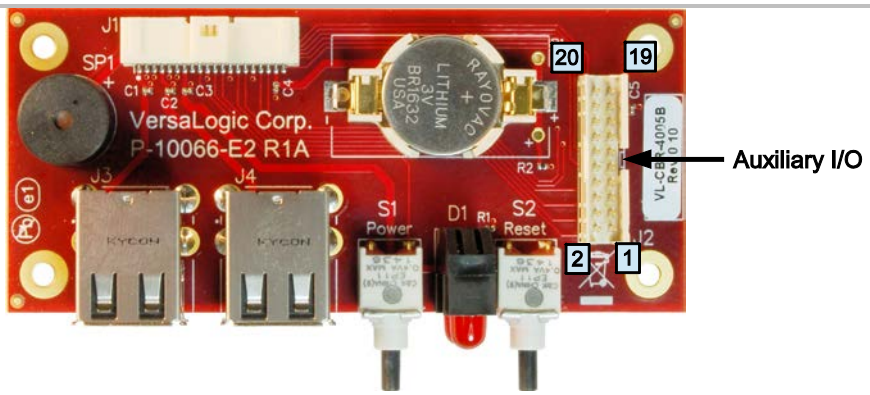


Figure 29. Location and Pin Orientation of Auxiliary I/O Connector

Table 20: Auxiliary I/O Connector Pinout

Pin	Signal	Pin	Signal
1	I2C Clock	2	V_BATT
3	I2C Data	4	V_BATT_RETURN
5	GND	6	GND
7	FPGA GPIO1	8	FPGA GPIO2
9	FPGA GPIO3	10	FPGA GPIO4
11	GND	12	GND
13	FPGA GPIO5	14	FPGA GPIO6
15	FPGA GPIO7	16	FPGA GPIO8
17	+3.3 V	18	GND
19	Ethernet Port 0 LED	20	Ethernet Port 1 LED

DIMENSIONS AND MOUNTING HOLES

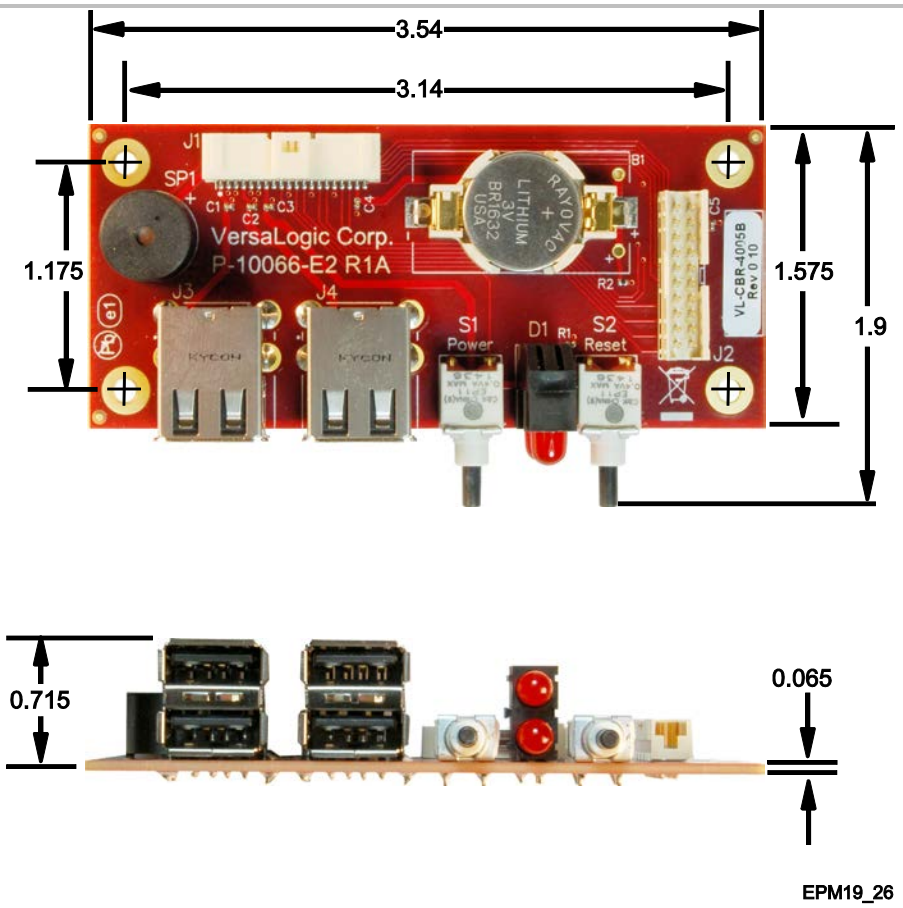
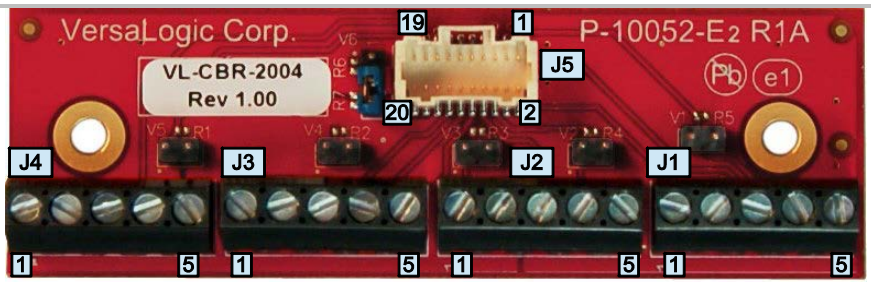


Figure 30. CBR-4005B Dimensions and Mounting Holes

To access the 16 digital I/O lines on the EPM-31 board, a paddleboard and 12-inch cable are available from VersaLogic, part number VL-CBR-2005.

CBR-2004B Connectors

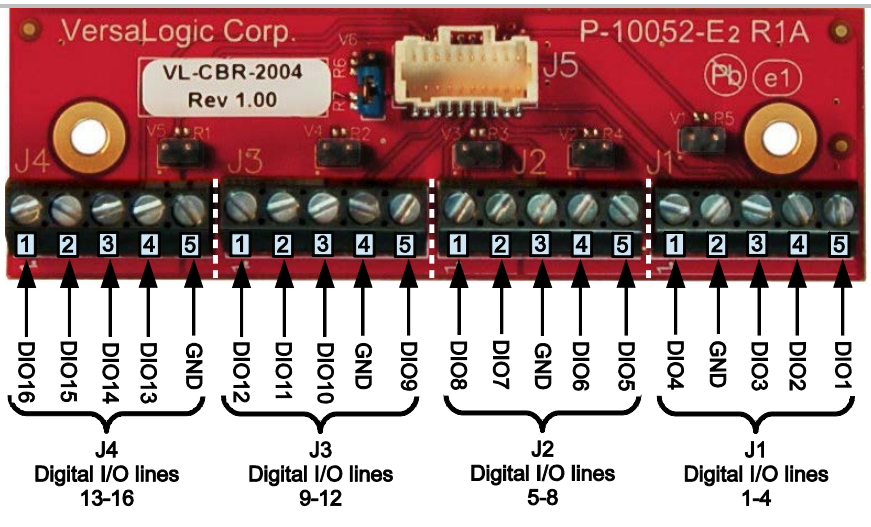
Figure 31 shows the locations and pin orientations of the connectors on the CBR-2004B paddleboard.



EPM31_23

Item	Description
J5	Main I/O connector (mates with the EPM-31 board's digital I/O connector)
J4	Digital I/O lines 13-16
J3	Digital I/O lines 9-12
J2	Digital I/O lines 5-8
J1	Digital I/O lines 1-4

Figure 31. CBR-2004B Connectors



EPM31_25

Figure 32. J4/J3/J2/J1 Digital I/O Terminal Block Pinouts

MAIN I/O CONNECTOR

Figure 31 shows the location and pin orientation of the main I/O connector.

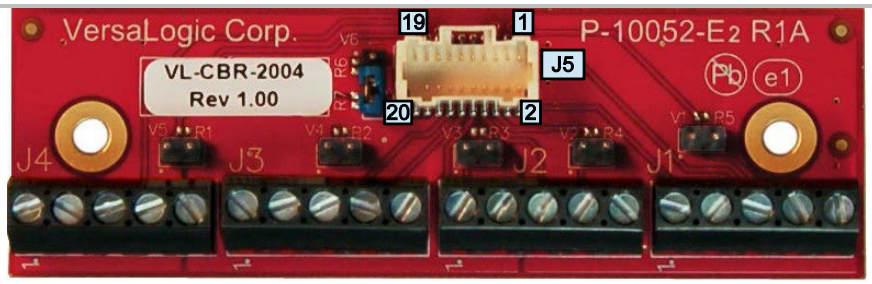


Figure 33. Location and Pin Orientation of the Main I/O Connector

Table 21: Main I/O Connector Pinout

Pin	Signal	Pin	Signal
1	Digital I/O 1	2	Digital I/O 2
3	Digital I/O 3	4	Digital I/O 4
5	GND	6	Digital I/O 5
7	Digital I/O 6	8	Digital I/O 7
9	Digital I/O 8	10	GND
11	Digital I/O 9	12	Digital I/O 10
13	Digital I/O 11	14	Digital I/O 12
15	GND	16	Digital I/O 13
17	Digital I/O 14	18	Digital I/O 15
19	Digital I/O 16	20	GND

CABLING

An adapter cable, part number CBR-4005A, is available for connecting the CBR-4005B paddleboard to the EPM-31. This is a 12-inch, Pico-Clasp 20-pin to 20-pin cable

If your application requires a custom cable, the following information will be useful:

CBR-4005B Board Connector	Mating Connector
Molex 501571-2007	Molex 501189-4010

Dimensions and Mounting Holes

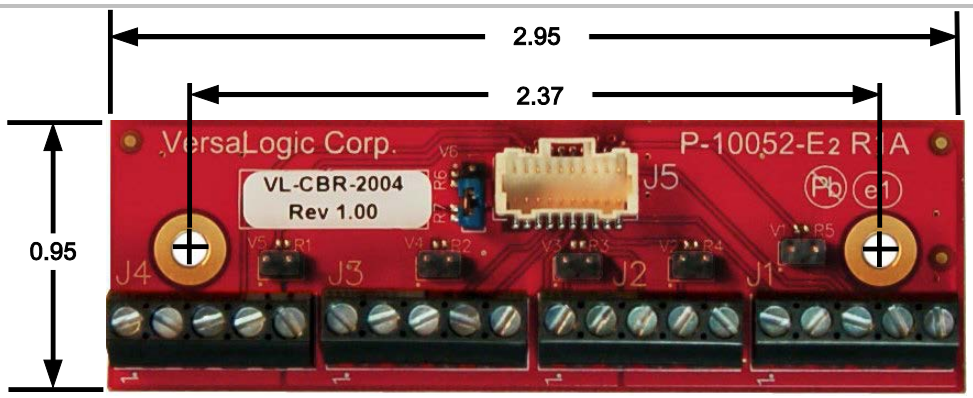


Figure 34. CBR-2004B Dimensions and Mounting Holes

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Thermal Considerations 13

This chapter discusses the following topics related to thermal issues:

- Selecting the correct thermal solution for your application (begins below)
- EPM-31 thermal characterization (begins on page 71)
- Installing the passive (HDW-412 heat sink) and active (HDW-407 fan) thermal solutions available from VersaLogic (begins on page 75)

Selecting the Correct Thermal Solution for Your Application

This section provides guidelines for the overall system thermal engineering effort.

HEAT PLATE

The heat plate supplied with the BayCat is the basis of the thermal solution. The heat plate draws heat away from the CPU chip as well as other critical components such as the power supply / management unit, the PCIe-to-PCI Bridge, and the Ethernet interfaces. Other components rely on the ambient air temperature being maintained at or below the maximum specified 85 ºC.

The heat plate is designed with the assumption that the user's thermal solution will maintain the top surface of the heat plate at 90 ºC or less. If that temperature threshold is maintained, the CPU (and the other noted components) will remain safely within their operating temperature limits.

CAUTION:

By itself, the heat plate is not a complete thermal solution. Integrators should either implement a thermal solution using the accessories available from VersaLogic or develop their own thermal solution that attaches to the heat plate, suitable for environments in which the EPM-31 will be used. As stated above, any thermal solution must be capable of keeping the top surface of the heat place at or below 90 ºC and the air surrounding the components in the assembly at or below 85 ºC.

The heat plate is permanently affixed to the BayCat and must not be removed. Removal of the heat plate voids the product warranty. Attempting to operate the BayCat without the heat plate voids the product warranty and can damage the CPU.

SYSTEM-LEVEL CONSIDERATIONS

The EPM-31 thermal solutions – either the HDW-412 heat sink alone or with the HDW-407 fan – are part of the larger thermal system of the application. Other PC/104 boards stacked under the BayCat and any other nearby heat sources (power supplies or other circuits), all contribute to how the EPM-31 will perform from a thermal standpoint.

The ambient air surrounding the EPM-31 needs to be maintained at 85 ºC or below. This can prove to be challenging depending on how and where the EPM-31 is mounted in the end user system. Standard methods for addressing this requirement include the following:

- Provide a typical airflow of 100 linear feet per minute (LFM) / 0.5 linear meters per second (as described in the section titled EPM-31 Thermal Characterization, beginning on page 71) within the enclosure
- Position the EPM-31 board to allow for convective airflow
- Lower the system level temperature requirement as needed

The decision as to which thermal solution to use can be based on several factors including (but not limited to) the following:

- Number of CPU cores in the SoC (single, dual, or quad)
- CPU core program utilization
- Temperature range within which the EPM-31 will be operated
- Air movement (or lack of air movement)
- Video processing intensity
- Memory access demands
- High speed I/O usage (PCIe, USB 3.0, SATA usage)

Most of these factors involve the demands of the user application on the EPM-31 and cannot be isolated from the overall thermal performance. Due to the interaction of the user application, the BayCat thermal solution, and the overall environment of the end system, thermal performance cannot be rigidly defined.

CPU THERMAL TRIP POINTS

The CPU cores in the BayCat have their own thermal sensors. Coupled with these sensors are specific reactions to four thermal trip points. Table 22 describes the four thermal trip points.

Table 22: CPU Thermal Trip Points

Trip Point	Description
Active (Note 1)	The fan is turned on when this temperature is reached
Passive (Note 2)	At this temperature, the CPU cores throttle back to a lower speed. This reduces the power draw and the temperature.
Critical (Note 3)	At this temperature, the operating system typically puts the board into a sleep or other low-power state.
Maximum core temperature	The CPU turns itself off when this temperature is reached. This is a fixed trip point and cannot be adjusted.

Notes:

1. The default value in the BIOS Setup program for this trip point is 55 ºC.
2. The default value in the BIOS Setup program for this trip point is 105 ºC.
3. The default value in the BIOS Setup program for this trip point is 110 ºC.

These trip points allow maximum CPU operational performance while maintaining the lowest CPU temperature possible. The long-term reliability of any electronic component is degraded when it is continually run near its maximum thermal limit. Ideally, the CPU core temperatures would be kept well below 100 ºC with only brief excursions above.

CPU temperature monitoring programs are available to run under both Windows and Linux. Table 23 lists some of these hardware monitoring programs.

Table 23: Temperature Monitoring Programs

Operating System	Program Type	Description
Windows	Core Temperature	http://www.alcpu.com/CoreTemp/
	Hardware Monitor	http://www.cpuid.com/softwares/hwmonitor.html
	Open Hardware Monitor	http://openhardwaremonitor.org/
Linux	lm-sensors	http://en.wikipedia.org/wiki/Lm_sensors

THERMAL SPECIFICATIONS, RESTRICTIONS, AND CONDITIONS

Graphical test data is in the section titled EPM-31 Thermal Characterization, beginning on page 71. Refer to that section for the details behind these specifications. These specifications are the thermal limits for using the EPM-31 with one of the defined thermal solutions.

Due to the unknown nature of the entire thermal system, or the performance requirement of the application, VersaLogic cannot recommend a particular thermal solution. This information is provided for user guidance in the design of their overall thermal system solution.

Table 24: Absolute Minimum and Maximum Air Temperatures

Board	With Heat Plate	With Heat Sink (HDW-412)	With Heat Sink + Fan (HDW-412 + HDW-407)
VL-EPM-31EAP	-40 ° to +85 °C	-40 ° to +85 °C	-40 ° to +85 °C
VL-EPM-31EBP	-40 ° to +85 °C	-40 ° to +85 °C	-40 ° to +85 °C
VL-EPM-31ECP	-40 ° to +85 °C	-40 ° to +85 °C	-40 ° to +85 °C

OVERALL RESTRICTIONS AND CONDITIONS

- Ranges shown assume less than 90% CPU utilization.
- Keep the maximum CPU core temperature below 100ºC.
- The ambient air surrounding the EPM-31 needs to be maintained at 85 ºC or below. This includes the space between this CPU board and any board it is stacked on top of it. Included is the space beneath an installed Mini PCIe expansion board and the installed SODIMM. A recommended overall air flow of 100 Linear Feet per Minute (LFM) / 0.5 Linear Meters per Second (LMS) addresses this requirement. If this air flow is not provided, other means to keep the adjacent air at 85 ºC or below must be implemented.

HEAT PLATE ONLY RESTRICTIONS AND CONDITIONS:

- The heat plate must be kept below 90 °C. This applies to a heat plate mounted directly to another surface.

HEAT SINK ONLY CONSIDERATIONS:

- At 85°C air temperature and 90% CPU utilization, there will be little – if any – thermal margin to a CPU core temperature of 100 °C or the passive trip point (see test data). If this is the use case, consider adding a fan or other additional air flow.

HEAT SINK WITH FAN CONSIDERATIONS:

- The heat sink and fan combination cools the CPU when it is running in high temperature environments, or when the application software is heavily utilizing the CPU or video circuitry. The fan assists in cooling the heat sink and provides additional air movement within the system.

Integrator's Note:

The ambient air surrounding the EPM-31 needs to be maintained at 85 ºC or below.

EPM-31 Thermal Characterization

The EPM-31 board underwent the following thermal characterization tests:

- Test Scenario 1: Single core EPM-31EAP + HDW-412 heat sink
- Test Scenario 2: Dual core EPM-31EBP + HDW-412 heat sink, with/without HDW-407 fan
- Test Scenario 3: Quad core EPM-31ECP + HDW-412 heat sink, with/without HDW-407 fan

Table 25 describes the thermal testing setup for the board.

Table 25: EPM-31 Thermal Testing Setup

Hardware configuration	EPM-31 (BayCat) single/dual/quad core CPU with: ▪ 4 GB of DDR3 DRAM (VersaLogic part number VL-MM9-4EBN) ▪ HDW-412 (passive heat sink) ▪ HDW-407 (heat sink fan) ▪ One attached DisplayPort device ▪ Two RS-232 ports in loopback configuration ▪ Two active Ethernet ports ▪ Three USB 2.0 ports in loopback configuration
BIOS	▪ ID string: BayCat_3.1.0.334.r1.101 ▪ Passive thermal trip point setting: 105 ºC ▪ Critical thermal trip point setting: 110 ºC
Operating system	Microsoft Windows 8.1 Enterprise
Test software	▪ Passmark BurnIn Test v7.1 b1017 - CPU utilization ~90% ▪ Intel Thermal Analysis Tool (TAT) v5.0.1014 - Primarily used to read the CPU core temperature
Test environment	Thermal chamber

The test results reflect the test environment within the temperature chamber used. This particular chamber has an airflow of about 0.5 meters per second (~100 linear feet per minute). Thermal performance can be greatly enhanced by increasing the overall airflow beyond 0.5 meters per second.

The system power dissipation is primarily dependent on the application program; that is, its use of computing or I/O resources. The stress levels used in this testing are considered to be at the top of the range of a typical user's needs.

TEST RESULTS

Test Scenario 1: Single Core EPM-31EAP + HDW-412 Heat Sink

At 90% CPU utilization, this single core unit operates within the CPU's core temperature safe operating range all the way up to +85 ºC using only a heat sink.

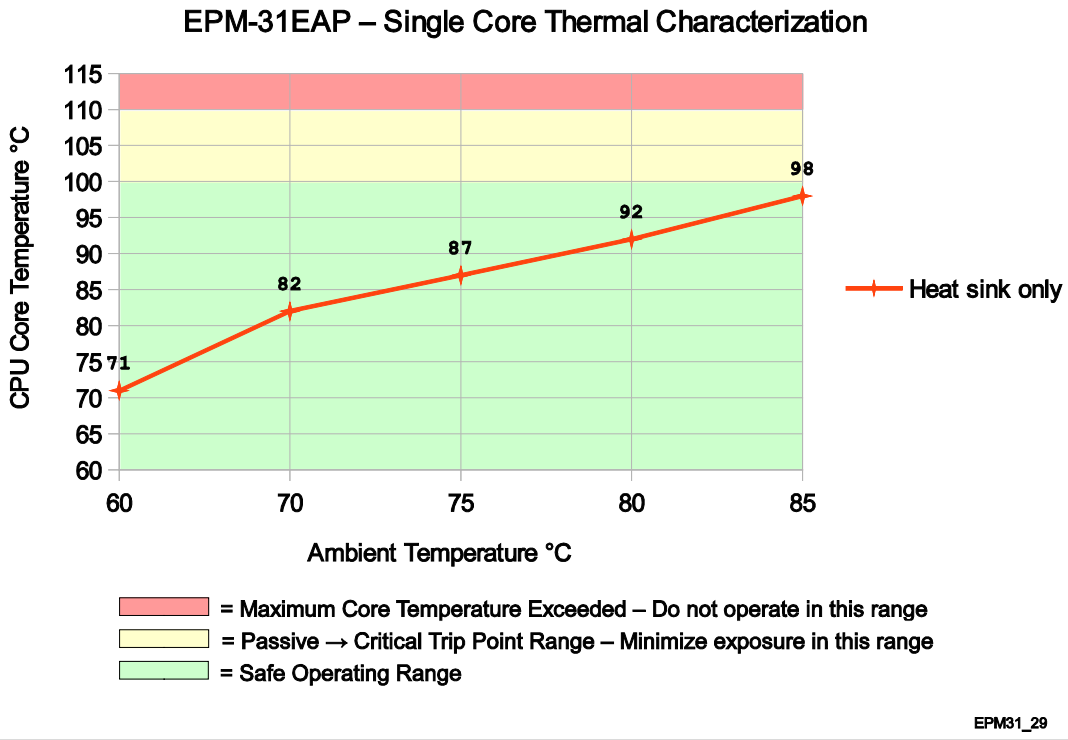

Figure 35. EPM-31EAP CPU Core Temperature Relative to Ambient Temperature

Test Scenario 2: Dual Core EPM-31EBP + HDW-412 Heat Sink, with/without HDW-407 fan

As shown in Figure 36, running the test scenario with just the heat sink, the core temperature is slightly above 100 ºC at maximum ambient temperature. This will be less in most applications that require less than 90% CPU utilization. Adding the fan provides an additional 5-6 ºC of margin. For long-term reliability, ensure the CPU cores are predominately running with their temperatures below 100 ºC.

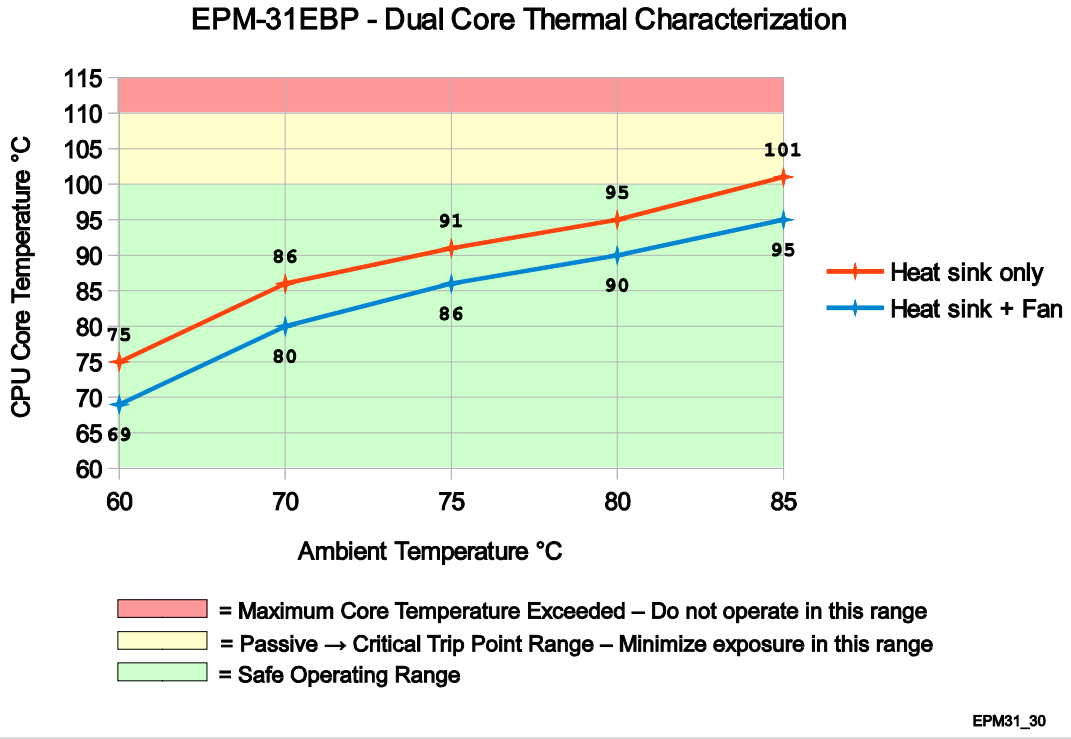

Figure 36. EPM-31EBP CPU Core Temperature Relative to Ambient Temperature

Test Scenario 3: Quad Core EPM-31ECP + HDW-412 Heat Sink, with/without HDW-407 Fan

As shown below, the quad core version of the BayCat will typically require a heat sink + fan for operation above 80 ºC, at >90% CPU utilization.

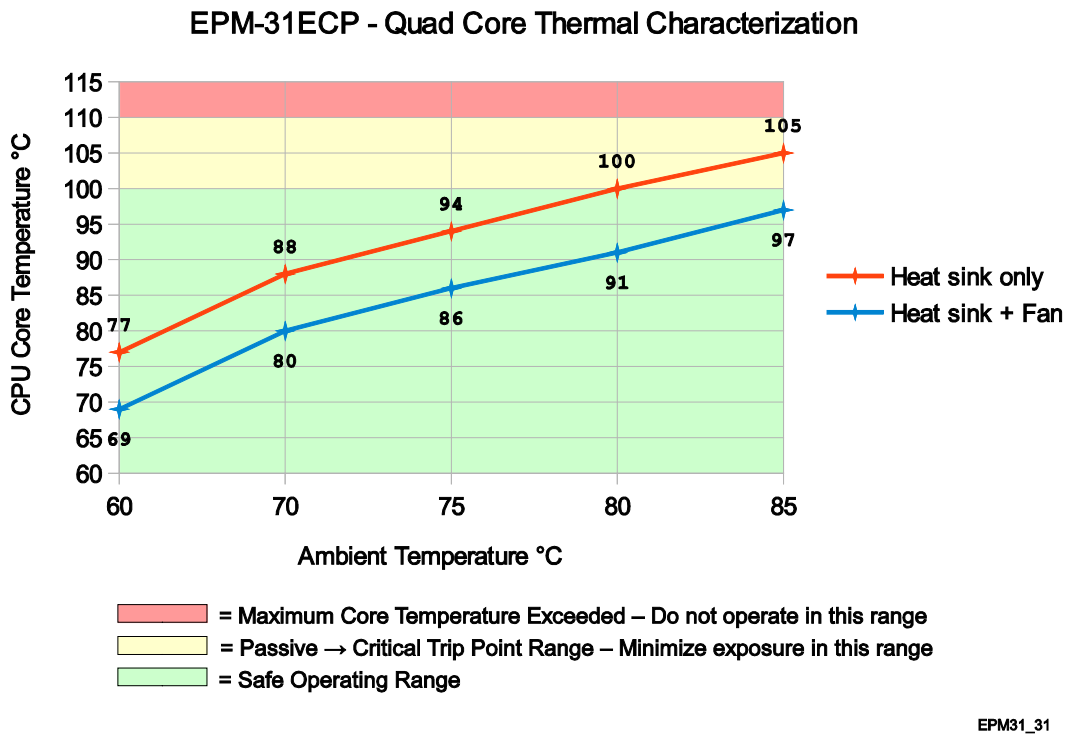

Figure 37. EPM-31ECP CPU Core Temperature Relative to Ambient Temperature

Installing the VersaLogic Thermal Solutions

The following thermal solution accessories are available from VersaLogic:

- VL-HDW-401 Thermal Compound Paste - used to mount the heat sink to the heat plate
- VL-HDW-412 Passive Heat Sink – mounts to standard product.
- VL-HDW-407 Fan Assembly – mounts to HDW-412 Heat Sink.

INSTALLING THE PASSIVE HEAT SINK

Install the passive heat sink (VL-HDW-412) using these steps:

1. **Apply the Arctic Silver† Thermal Compound**
   - Apply the thermal compound to the heat plate using the method described on the Arctic Silver website - http://www.arcticsilver.com/
2. **Position the passive heat sink**
   - Using Figure 38 as a guide, align the six mounting holes of the heat sink with the heat plate.
3. **Secure the passive heat sink to the heat plate**
   - Affix the passive heat sink to the heat plate using six M2.5 pan head screws.
   - Using a torque screwdriver, tighten the screws to 4.0 inch-pounds.

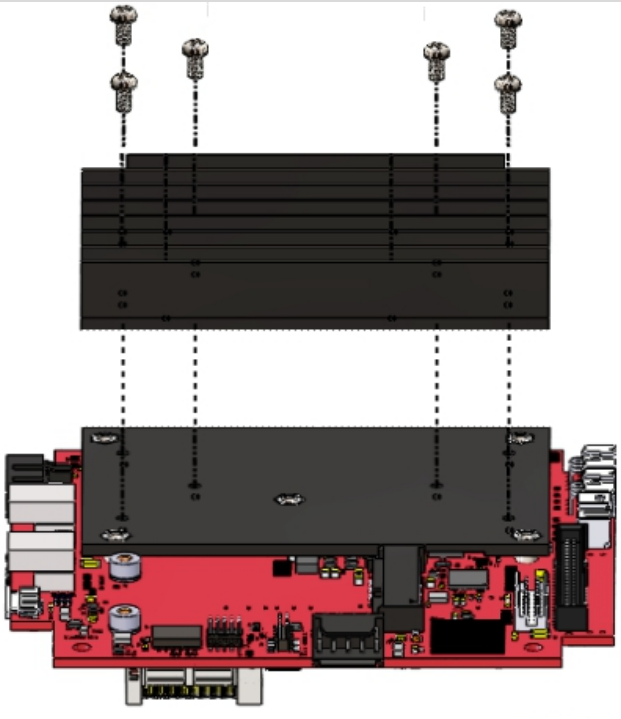

Figure 38. Installing the Passive Heat Sink

INSTALLING THE HEAT SINK FAN

Install the heat sink fan (VL-HDW-407) using these steps:

1. **Position the fan assembly**
   - Using Figure 39 as a guide, align the mounting holes of the heat sink fan with the four holes in the passive heat sink. Position the fan so that its power cable is on the side nearest the J24 CPU fan connector. The CPU fan connector is located between the Mini DisplayPort connector and the microSD socket (see Figure 2 on page 12).
2. **Secure the fan to the heat sink**
   - Affix the heat sink fan using four M3 pan head screws.
   - Using a torque screwdriver, tighten the screws to 4.0 inch-pounds.
3. **Connect power to the fan**
   - Connect the fan's power cable to the J24 CPU fan connector on the BayCat board.

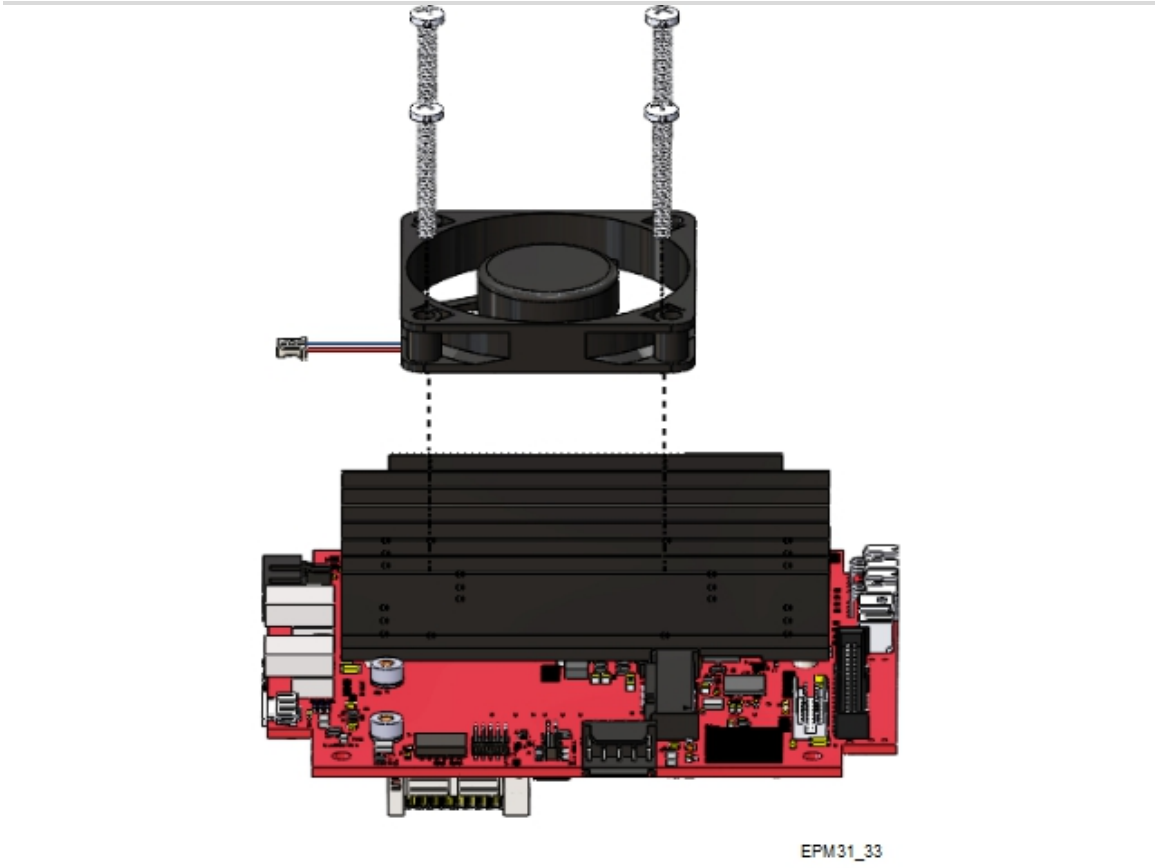

Figure 39. Installing the Heat Sink Fan

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