DOCUMENT NUMBER AND REVISION

VL-FS-MDLS12433P-01 REV. A

(MDLS12433P-LV-S)

DOCUMENT TITLE:

SPECIFICATION

OF

LCD MODULE TYPE

MODEL NUMBER: MDLS12433P-01

DEPARTMENT	NAME	SIGNATURE	DATE
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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2004.03.16	First Release. Based on a.) Test Specification: VL-TS-MDLS12433P-XX Rev. B 2003-08-26. b.) VL-QUA-012A-S, REV. P, APR/2003 (English version). According to VL-QUA-012A-S, LCD size is small because Unit Per Laminate=21 which is more than 6pcs/Laminate.	CHEN HUI JUAN	SUNNY LEE

CONTENTS

VARITRONIX LIMITED

Specification
of
LCD Module Type
Item No.: MDLS12433P-01

1. General Description

- 12 characters x 4 lines (5 x 8 dots) STN Positive Silver Reflective LCD character module.
- Driving scheme: 1:32 multiplexed drive, 1/6 bias.
- Optimal view direction: 6 O'clock.
- 'PHILIPS' PCF2116AU/10 die form LCD controller / driver.
- Data interface: I^2C-bus.
- Built in character generator with the standard character set.
- Flexible Flat Cable (FFC) (length=70mm).

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	49.0(W) x 44.0(H) x 2.0 max.(D) (Excluded FFC and RTV). 49.0(W) x 108.5(H) x 2.0 max.(D) (Included FFC. Excluded RTV).	mm
Viewing area	41.0(W) x 19.1(H)	mm
Display format	12 characters X 4 lines (5 x 8 dots)	-
Character size	2.05(W) x 3.55(H) (5 x 8 dots)	mm
Character spacing	0.96(W) x 0.96(H)	mm
Character pitch	3.01(W) x 4.51(H)	mm
Dot size	0.37(W) x 0.40(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.42(W) x 0.45(H)	mm
Weight:	TBD	grams

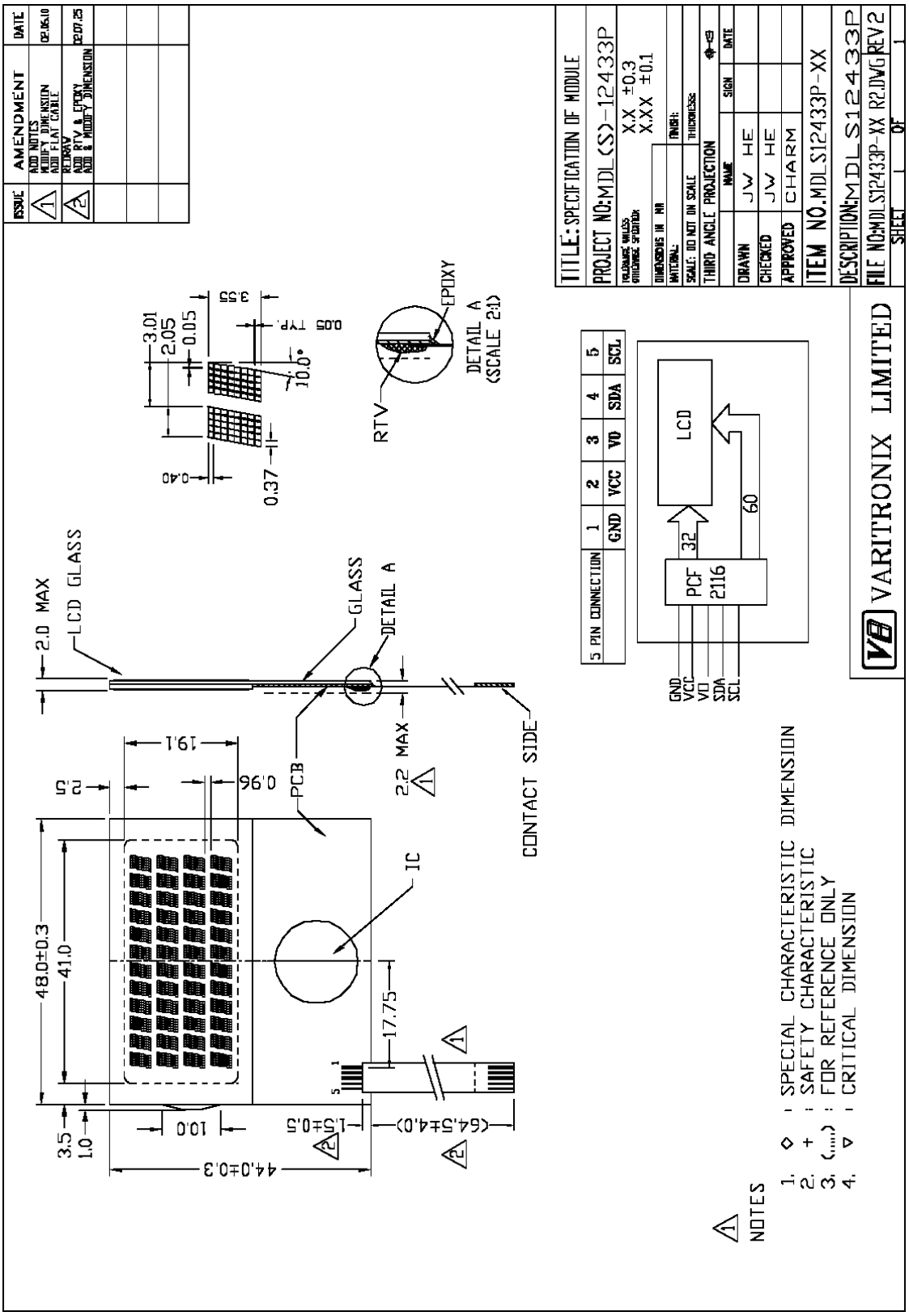

Figure 1: Specification Drawing

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = 25 ºC)

Table 2

Parameter	Condition	Symbol	Min.	Max.	Unit
Power supply voltage (Logic)	-	VCC - GND	-0.5	+8.0	V
Power supply voltage (LCD)		V_{LCD}	0	11.0	V
Input voltage range	OSC,SCL,SDA	Vin	GND-0.50	VCC +0.5	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to GND = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

4. Electrical Specifications

4.1 Interface signals

Table 4

Pin No.	Symbol	Description
1	GND	Ground (0V) and cathode of LED backlight.
2	VCC	Power supply for logic (+5V).
3	V0	Control input for V_{LCD}.
4	SDA	I^2C serial data input/output.
5	SCL	I^2C serial clock input.

4.2 Typical Electrical Characteristics

Ta = 25 °C,VCC = 5.0V ±5%,GND=0V.

Conditions: GND=0V, VCC=$VCC_{(}$typ.), Tamb=+25°C, Vop=Vop(typ.),
Rosc=Rosc(typ.), unless otherwise stated.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VCC-GND		4.75	5.00	5.25	V
Supply voltage (LCD)	VLCD =VCC-V0	Note 1	3.0	3.3	3.6	V
Input signal voltage low	Vil		GND	-	0.1 VCC	V
Input signal voltage high	Vih		0.9 VCC	-	VCC	V
LCD operating current	ICC	Character mode, Note 1	-	0.4	0.6	mA
		Checker board mode, Note 1	-	0.5	0.8	mA

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

4.3 Timing Specifications

Ta = 0 °C to +50 °C, VCC =5V±5%, GND=0V; V_{LCD}= VCC-3.5V to VCC-9V.

Refer to Fig.2, I^2C Bus Timing Diagram of 'PHILIPS' PCF2116; rise and fall times referring to V_{IL} and $V_{IH.}$

Table 6

Parameters	**Symbol**	**Min.**	**Typ.**	**Max.**	**Unit**
LCD frame frequency (internal clock) (note 1)	f_{FR}	40	65	100	Hz
External clock frequency	f_{OSC}	90	150	225	kHz
Timing characteristics: I^2C-bus interface; note 2					
SCL clock frequency	f_{SCL}	-	-	100	kHz
Tolerable spike width on bus	t_{SW}	-	-	100	ns
Bus free time	t_{BUF}	4.7	-	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	-	µs
Start condition hold time	$t_{HD;STA}$	4	-	-	µs
SCL LOW time	t_{LOW}	4.7	-	-	µs
SCL HIGH time	t_{HIGH}	4	-	-	µs
SCL and SDA rise time	t_r	-	-	1	µs
SCL and SDA fall time	t_f	-	-	0.3	µs
Data set-up time	$t_{SU;DAT}$	250	-	-	ns
Data hold time	$t_{HD;DAT}$	0	-	-	ns
Set-up time for Stop condition	$t_{SU;STO}$	4	-	-	µs

Notes:

1 VCC=5.0V.

2. All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing to GND to VCC.

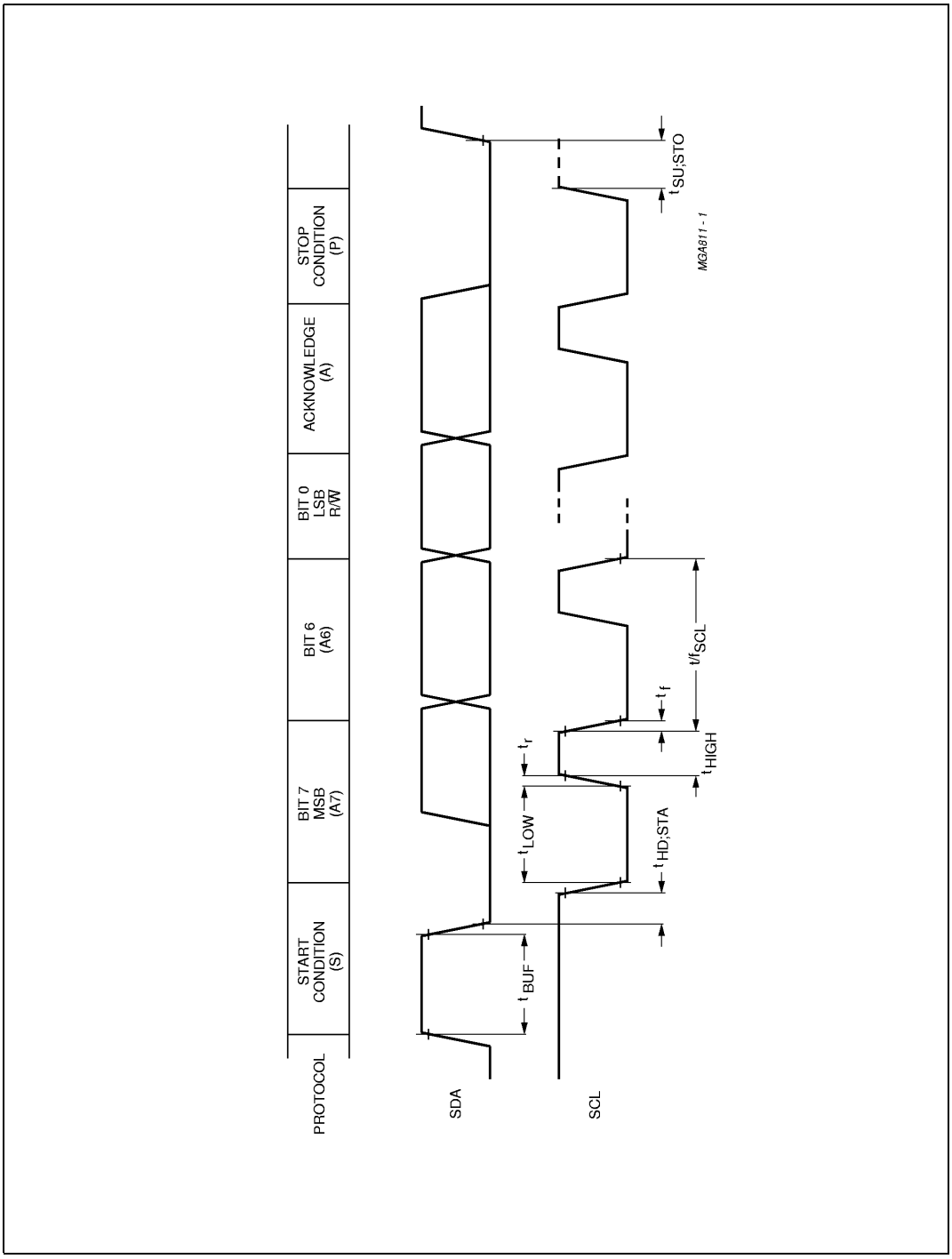

Figure 2: I^2C Bus Timing Diagram of 'PHILIPS' PCF2116;
rise and fall times referring to V_{IL} and V_{IH}

5. LCD Cosmetic Conditions

Refer to VL-QUA-012A-S.

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