Reference Manual

DOC. REV. 10/20/2016

VL-MPEe-A1/A2

Mini PCIe Analog Input Module
with Digital I/O

VERSALOGIC CORPORATION

WWW.VERSALOGIC.COM

12100 SW Tualatin Road
Tualatin, OR 97062-7341
(503) 747-2261
Fax (971) 224-4708

Notice:

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VersaLogic reserves the right to revise this product and associated documentation at any time without obligation to notify anyone of such changes.

Product Revision Notes

Revision 1.01 – *Updated tables 6 and 7*

Revision 1.00 – Commercial release.

Support

The VL-MPEe-A1/A2 support page, at **http://www.versalogic.com/private/mpeeaxsupport.asp**, contains additional information and resources for this product including:

- Reference Manual (PDF format)
- Device drivers
- Data sheets and manufacturers' links for chips used in this product
- Photograph of the circuit board

This is a private page for VL-MPEe-A1/A2 users that can be accessed only by entering this address directly. It cannot be reached from the VersaLogic homepage.

The VersaTech KnowledgeBase is an invaluable resource for resolving technical issues with your VersaLogic product.

VersaTech KnowledgeBase

Contents

Introduction 1

Description

Features and Construction

The VL-MPEe-A1 is an extremely small and rugged analog input module based on the industry-standard Mini PCIe module format. This analog board provides eight single-ended or four differential input channels. The VL-MPEe-A1 model provides 12-bit resolution, while the VL-MPEe-A2 model provides 16-bit resolution. Operating at up to 100,000 samples per second, each input channel is individually configurable for an input range of 0 to 5V, 0 to +10V, -5 to +5V, and -10 to +10V. In addition, the board provides three general purpose digital I/O lines which are independently configurable for input, output, or interrupts. The board's features include:

- Eight single or four differential analog input channels, 12-bit (A1) or 16-bit (A2) resolution
- Three general purpose digital I/O (GPIO) lines
- RoHS-compliant
- Industrial temperature operation
- Customization available

The VL-MPEe-A1/A2 features high reliability design and construction. VL-MPEe-A1/A2 boards undergo 100% functional testing and are backed by a limited two-year warranty. Careful parts sourcing and US-based technical support ensure the highest possible quality, reliability, service, and product longevity for this exceptional board.

Technical Specifications

Specifications are subject to change without notification.

Board Size:
30.00 mm x 50.95 mm (Mini PCIe standard)

Storage Temperature:
-40° to +85°C

Operating Temperature:
-40° to +85°C

Power Requirements: *at +25°C*
3.3V ± 5% @ 0.45W
(supplied by the Mini PCIe socket; 1.5V on the MiniCard connector not used)

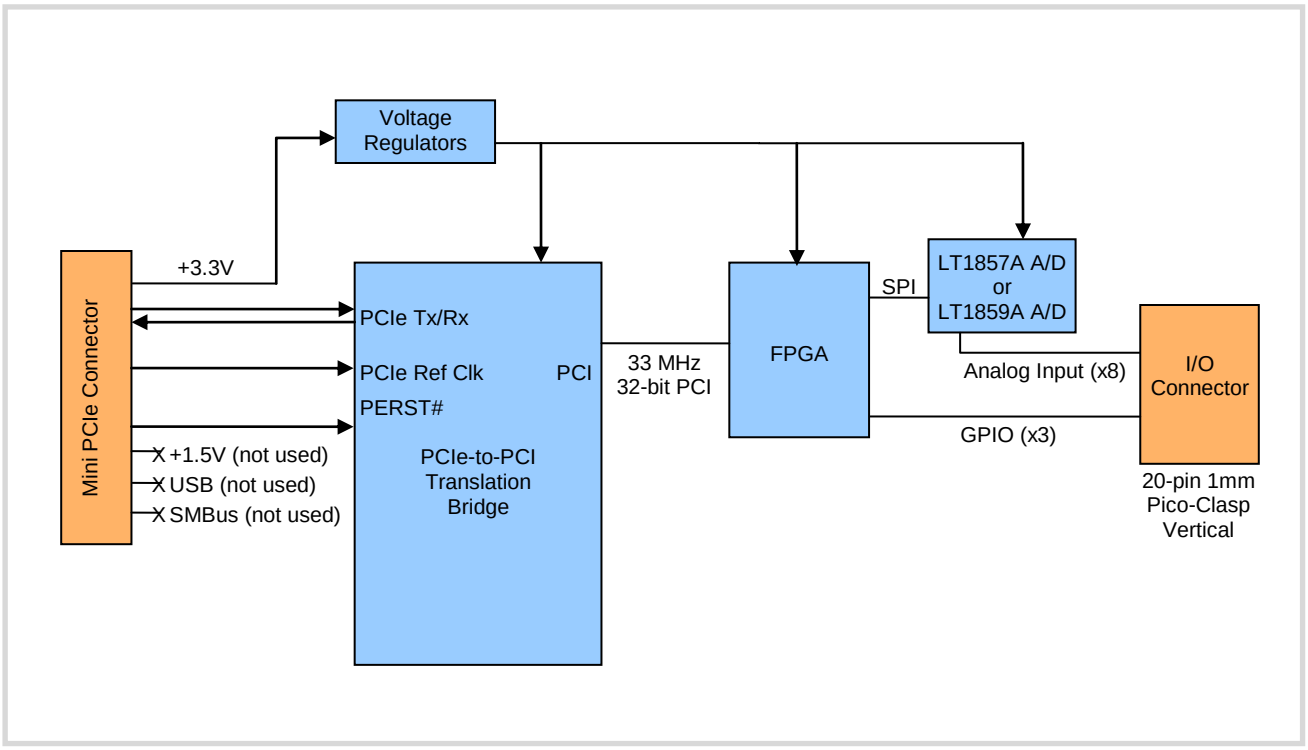
Analog Input:
8-channel, 12-bit (A1) or 16-bit (A2), single-ended or differential, 100 Ksps, channel independent input range: bipolar ±5, ±10, or unipolar 0 to +5V or 0 to +10V

GPIOs:
Three 3.3V general purpose I/O lines; each configurable as input or output, normal or inverted level, HIGH or LOW state

Bus Requirements:
PCIe 1.1 signals from PCIe MiniCard bus (USB and SMBus not used)

Weight:
0.012 lbs (0.006 kg)

Block Diagram



RoHS Compliance

The VL-MPEe-A1/A2 is RoHS-compliant.

ABOUT ROHS

In 2003, the European Union issued Directive 2002/95/EC regarding the Restriction of the use of certain Hazardous Substances (RoHS) in electrical and electronic equipment.

The RoHS directive requires producers of electrical and electronic equipment to reduce to acceptable levels the presence of six environmentally sensitive substances: lead, mercury, cadmium, hexavalent chromium, and the presence of polybrominated biphenyls (PBB) and polybrominated diphenyl ethers (PBDE) flame retardants, in certain electrical and electronic products sold in the European Union (EU) beginning July 1, 2006.

VersaLogic Corp. is committed to supporting customers with high-quality products and services meeting the European Union's RoHS directive.

Warnings

ELECTROSTATIC DISCHARGE

Warning! Electrostatic discharge (ESD) can damage circuit boards, disk drives, and other components. The circuit board must only be handled at an ESD workstation. If an approved station is not available, some measure of protection can be provided by wearing a grounded antistatic wrist strap. Keep all plastic away from the board, and do not slide the board over any surface.

After removing the board from its protective wrapper, place the board on a grounded, static-free surface, component side up. Use an antistatic foam pad if available.

The board should also be protected inside a closed metallic antistatic envelope during shipment or storage.

Note: The exterior coating on some metallic antistatic bags is sufficiently conductive to cause excessive battery drain if the bag comes in contact with the bottom side of the board.

HANDLING CARE

Warning! Care must be taken when handling the board not to touch the exposed circuitry with your fingers.

Technical Support

If you are unable to solve a problem after reading this manual, please visit the VL-MPEe-A1/A2 product support page below. This page provides links to component datasheets and device drivers.

VL-MPEe-A1/A2 Support Page

The VersaTech KnowledgeBase contains a wealth of technical information about VersaLogic products, along with product advisories. Click the link below to see all KnowledgeBase articles related to the VL-MPEe-A1/A2.

VersaTech KnowledgeBase

If you have further questions, contact VersaLogic Technical Support at (503) 747-2261. VersaLogic support engineers are also available via e-mail at Support@VersaLogic.com.

REPAIR SERVICE

If your product requires service, you must obtain a Returned Material Authorization (RMA) number by calling (503) 747-2261.

Please provide the following information:

- Your name, the name of your company, your phone number, and e-mail address
- The name of a technician or engineer that can be contacted if any questions arise
- Quantity of items being returned
- The model and serial number (barcode) of each item
- A detailed description of the problem
- Steps you have taken to resolve or recreate the problem
- The return shipping address

Warranty Repair All parts and labor charges are covered, including return shipping charges for UPS Ground delivery to United States addresses.

Non-warranty Repair All approved non-warranty repairs are subject to diagnosis and labor charges, parts charges, and return shipping fees. Please specify the shipping method you prefer and provide a purchase order number for invoicing the repair.

Note: Please mark the RMA number clearly on the outside of the box before returning.

Board Layout and Connectors

VL-MPEe-A1/A2 Mounting

The VL-MPEe-A1/A2 is a full size Mini PCIe card and needs to be mounted into a full size Mini PCIe site. On VersaLogic CPU boards, the module is secured using two nylon screws. VersaLogic offers 2 mm nylon screws (VL-HDW-110) and 2.5 mm nylon screws (VL-HDW-108). On non-VersaLogic CPU boards, mounting might be accomplished using a latching system.

Note: Be careful not to over tighten the nylon mounting screws. Optimum tightness is 1 lbf·in (0.1 N·m).

VL-MPEe-A1/A2 Dimensions and Connectors

The VL-MPEe-A1/A2 complies with Mini PCIe card (full size) dimensional standards. Dimensions are given below to help with pre-production planning and layout.

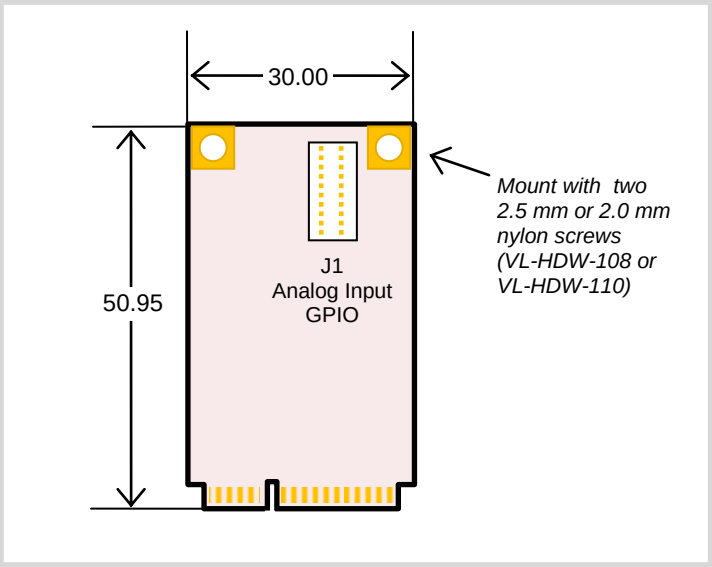


Figure 1. VL-MPEe-A1/A2 Dimensions and Connectors

(Not to scale. All dimensions in millimeters.)

Table 1 provides information about the function, mating connectors, and transition cables for the VL-MPEe-A1/A2 connector. Page numbers indicate where a detailed pinout or further information is available.

Table 1: Connector Functions and Interface Cables

Connector[1]	Function	Mating Connector	Transition Cable	Cable Description	Page
J1	Analog input, GPIO	Molex 501189-2010 2x10 1 mm “pico-clasp” receptacle	VL-CBR-2004A	20 position screw terminal, 12” latching cable to VL-CBR-2004B I/O board	7

1. Connector J2 is not installed.

VL-CBR-2004 Dimensions and Connectors

The VL-CBR-2004 I/O connector provides a screw terminal interface for all analog inputs and GPIO lines.

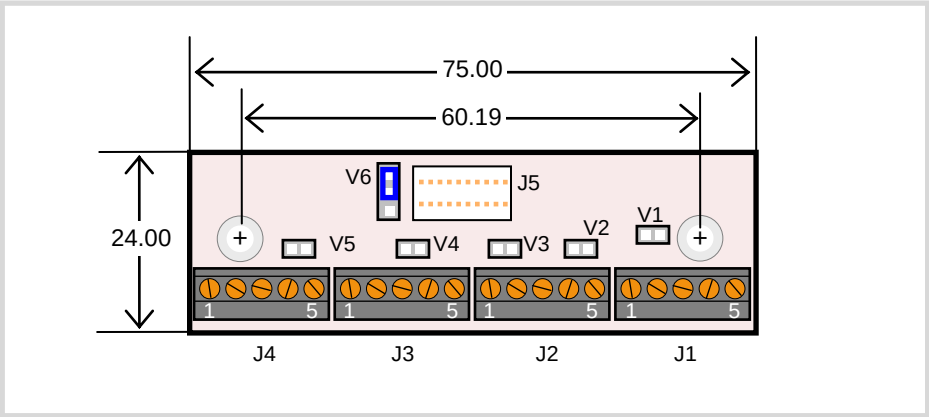


Figure 2. VL-CBR-2004 Dimensions, Connectors, Jumper Blocks

Note: The jumpers on the VL-CBR-2004B must not be removed or moved. Leave all jumpers in the positions shown in the above figure.

Table 2 provides information about the function, mating connectors, and transition cables for VL-MPEe-A1/A2 connectors. Page numbers indicate where a detailed pinout or further information is available.

Table 2: Connector Functions and Interface Cables

Connector	Function	Mating Connector	Transition Cable	Cable Description	Page
J1	Analog inputs 1-3	Bare wire, 18–30 AWG	—	—	10
J2	Analog inputs 4-5	Bare wire, 18–30 AWG	—	—	10
J3	Analog inputs 6-8	Bare wire, 18–30 AWG	—	—	10
J4	GPIO 1-3	Bare wire, 18–30 AWG	—	—	10
J5	Interface to Mini PCIe board	Molex 501189-2010 2x10 1 mm “pico-clasp” receptacle	VL-CBR-2004A	20 position screw terminal, 12” latching cable to VL-CBR-2004B I/O board	—

J1 I/O Connector

The J1 I/O connector incorporates the analog input and GPIO interfaces. The table below shows the function of each pin.

Table 3: J1 I/O Connector Pinout

J1 Pin	Signal Name	Function	Signal Direction	J1 Pin	Signal Name	Function	Signal Direction
1	ADC_CH1	Analog Input 1	In	2	ADC_CH2	Analog Input 2	In
3	AGND	Analog ground	–	4	AGND	Analog ground	–
5	ADC_CH3	Analog Input 3	In	6	ADC_CH4	Analog Input 4	In
7	AGND	Analog ground	–	8	AGND	Analog ground	–
9	ADC_CH5	Analog Input 5	In	10	ADC_CH6	Analog Input 6	In
11	AGND	Analog ground	–	12	AGND	Analog ground	–
13	ADC_CH7	Analog Input 7	In	14	ADC_CH8	Analog Input 8	In
15	AGND	Analog ground	–	16	AGND	Analog ground	–
17	DGND	Ground	–	18	GPIO1	GPIO Channel 1	In/Out
19	GPIO2	GPIO Channel 2	In/Out	20	GPIO3	GPIO Channel 3	In/Out

Analog Input

The VL-MPEe-A1/A2 uses a multi-range, 12-bit or 16-bit Linear Technology LTC185xA A/D converter with eight single-ended input signals (even and odd analog channels, for example inputs 1 and 2, can also be combined as differential inputs). The converter has a 100 kilo-samples-per-second (Ksps) sampling rate, with a 4 µs acquisition time, with per-channel input ranges of 0 to +5V or 0 to +10V unipolar, and ±5V or ±10V bipolar.

See the Linear Technology LTC185x Datasheet for detailed information.

VersaLogic provides a set of API calls for managing the analog input lines. See Application Programming Interface (API) for information.

Analog Input Characteristics

The analog input resistance for the LTC185xA A/D converter is typically 42K ohms (singled-ended) or 31K ohms (differential) and requires low resistance sources in order to achieve the 12-bit or 16-bit accuracies. This input impedance and the driving source resistance determine the actual analog source voltage. The driving source impedance also includes cable wire and PC board trace resistances. The cable wire resistance for the 28 gauge wire in the 12 inch CBR-4004 cable is approximately 0.064 ohms. The trace impedance on the VL-MPEe-A1/A2 boards is approximately 0.10 ohms. Note that the ground return path on single ended signals contribute to the overall resistance though it is typically much less than the signal path resistance.

It is very difficult to obtain low enough drive source impedances to meet 16-bit accuracies without compensating for the A/D input resistance and the maximum driving source impedances. The following relation should be used to estimate the input source voltage (V_{in}) given the A/D voltage reading (V_a), the A/D input resistance (Ra) and the driving source resistance (R_s) … which also includes the cable wire and PC board trace resistances). In general, typical values should be used for the A/D input resistance R_a and the driving source resistance R_s for compensation since actual values are not known.

$$V_{in} = V_a \times (1 + R_s/R_a)$$

The A/D input resistance Ra can vary ±20%, and the lower range impacts the maximum source resistance R_s that is allowed even when compensating. The following relation can be used to determine the maximum source resistance allowed when compensating at the typical input A/D resistance.

$$R_s < R_a \times (4 / N)$$

where N = 4096 for the 12-bit A/D converter and 65536 for the 16-bit A/D converter, and R_a is the minimum A/D input resistance.

The following table specifies the driving source resistance requirements to meet 1 LSB accuracy with and without compensation for the typical A/D input resistance. The general rule though is that a lower driving source resistance is always better to minimize the impacts of source and A/D resistances on overall accuracy.

Table 4: A/D Converter Driving Source Resistance Requirements

Converter Accuracy	Input Mode	Minimum A/D Input Resistance	Driving Source Resistance (No Compensation)	Driving Source Resistance (with Compensation)
12-Bit (LTC1857A on MPEe-A1E)	Single-Ended	33.6K (42K typical)	< 8 ohms	< 33 ohms
	Differential	24.8K (31K typical)	< 6 ohms	< 24 ohms
16-Bit (LTC1859A on MPEe-A2E)	Single-Ended	33.6K (42K typical)	< 0.5 ohms	< 2 ohms
	Differential	24.8K (31K typical)	< 0.4 ohms	< 1.6 ohms

General Purpose I/O (GPIO) Lines

The VL-MPEe-A1/A2 provides three GPIO (digital I/O) lines that are independently configurable as an input or output. GPIO inputs can be set for normal or inverted level. GPIO outputs can be set to be normal HIGH or LOW state. There are pull-up resistors to +3.3V on all GPIO lines. The pull-ups, which are implemented in the FPGA, can range in value from 20K to 40K. After reset, the GPIO lines are set as inputs with pull-ups, which will be detected as a HIGH state to external equipment.

VersaLogic provides a set of API calls for managing the GPIO lines. See Application Programming Interface (API) for information.

GPIO GUIDELINES

Consider the following guidelines when using the VL-MPEe-A1/A2 GPIO lines.

Voltage

The VL-MPEe-A1/A2 GPIO lines are 3.3V LVTTL compatible DIOs capable of sourcing/sinking up to 4mA of current. Level shifting or current limiting is necessary when connecting signals with different voltage rails.

Caution: Do not connect the GPIO signals to external +5V devices.

Host Board CPU Power States

Host board CPU power states may or may not turn off voltage rails driving GPIO circuits.

- Mini PCIe based GPIOs and their pull-up resistors (each with a resistance that can range from 20K to 40K ohms) will remain powered in all CPU power states (except when power is turned off).
- Power control during CPU power states on user devices connected to GPIO lines is dependent on the application design. These external devices would likely remain powered unless a power-down mechanism is designed into the system.
- Care must be taken when powered GPIO signals are connected to un-powered GPIO signals. Significant voltage and current can be leaked from a powered system to an un-powered system causing unpredictable results. Current limiting and/or diode isolation can help.

Cables

Cabling issues will affect the usable speed of GPIO signals.

- These are single-ended drivers/receivers.
- Cabling cross-talk can be a problem with fast edge rates. The GPIO outputs on the MPEe-A1/A2 are slew limited (using 3.3nsec RC filters) to minimize crosstalk and signal reflections.

VL-CBR-2004 I/O Board

The VersaLogic VL-CBR-2004 I/O board provides four terminal blocks for accessing the VL-MPE-A1/A2 analog input and GPIO channels.

Note: The correct cable must be used to connect the VL-CBR-2004 to the VL-MPE-A1/A2. Make sure to use the VL-CBR-2004A cable.

Table 5: VL-CBR-2004 Terminal Block Pinouts

J1 Pin	Signal Name	Function	Signal Direction
5	ADC_CH1	Analog Input 1	In
4	AGND	Analog ground	–
3	ADC_CH2	Analog Input 2	In
2	AGND	Analog ground	–
1	ADC_CH3	Analog Input 3	In
J2 Pin			
5	AGND	Analog ground	–
4	ADC_CH4	Analog Input 4	In
3	AGND	Analog ground	–
2	ADC_CH5	Analog Input 5	In
1	AGND	Analog ground	–
J3 Pin			
5	ADC_CH6	Analog Input 6	In
4	AGND	Analog ground	–
3	ADC_CH7	Analog Input 7	In
2	AGND	Analog ground	–
1	ADC_CH8	Analog Input 8	In
J4 Pin			
5	AGND	Analog ground	–
4	DGND	Ground	–
3	GPIO1	GPIO Channel 1	In/Out
2	GPIO2	GPIO Channel 2	In/Out
1	GPIO3	GPIO Channel 3	In/Out

4 Application Programming Interface (API)

About VersaAPI

The VersaLogic Application Programming Interface (VersaAPI) is a shared library of API calls for reading and controlling on-board devices on certain VersaLogic products. In Microsoft Windows they are presented as a dynamically linked library interface plus associated header file, and under Linux as a shared library with an associated header file.

Visit the VL-MPEe-Ax support page to download the VersaAPI package, which includes drivers for the VL-MPEe-A1/A2.

Open and Close Calls

The library interface must be opened by every application that wishes to make calls into the API and also must be closed by that same application when exiting.

VSL_Open();

Opens the VersaAPI library.

Syntax: VL_OSALIB_API unsigned long VSL_Open();

Inputs: none

Outputs: unsigned long
This call returns 0 if the open was a success and nonzero if no useable drivers were found by the DLL.

VSL_Close();

Closes the VersaAPI library.

Syntax: VL_OSALIB_API void VSL_Close();

Inputs: none

Outputs: none

VSL_GetVersion()

Gets the version number of the VersaAPI library

Syntax: VL_OSALIB_API void VSL_GetVersion(unsigned char *Major, unsigned char *Minor, unsigned char *Revision);

Inputs: unsigned char *Major
A pointer to the unsigned character to receive the Version Major number.

unsigned char *Minor
A pointer to the unsigned character to receive the Version Minor number.

unsigned char *Revision
A pointer to the unsigned character to receive the Version Revision number.

Outputs: none
While this function is void, the Major, Minor, and Revision versions are returned in their respective input fields.

GPIO Calls

API calls can be made to control or interrogate specific GPIO channels. The following table lists the channel, level, and direction parameter definitions used in DIO calls.

Table 6: DIO API Parameter Definitions

Parameters	Value	
Channel	DIO_AX_CHANNEL_1	0x90
	DIO_AX_CHANNEL_2	0x91
	DIO_AX_CHANNEL_3	0x92
Level*	DIO_CHANNEL_LOW	0x00
	DIO_CHANNEL_HIGH	0x01
Direction	DIO_INPUT	0x01
	DIO_OUTPUT	0x00

*Level values are also the return results for VSL_DIOGetChannelLevel.

VSL_DIOGetChannelLevel

Reads the signal level of the specified channel.

Syntax: VL_OSALIB_API unsigned char VSL_DIOGetChannelLevel(unsigned char Channel);

Inputs: unsigned char Channel
The DIO channel number to be interrogated.

Outputs: unsigned char
Returns the state of the channel as either high (DIO_CHANNEL_HIGH) or low (DIO_CHANNEL_LOW).

VSL_DIOSetChannelLevel

Sets the signal level of the specified channel.

Syntax: VL_OSALIB_API void VSL_DIOSetChannelLevel(unsigned char Channel, unsigned char Level);

Inputs: unsigned char Channel
The DIO channel number to be set.

unsigned char Level
The DIO level to be set: DIO_CHANNEL_HIGH or DIO_CHANNEL_LOW.

Outputs: none

VSL_DIOSetChannelDirection

Sets the signal direction of the specified channel.

Syntax: VL_OSALIB_API void VSL_DIOSetChannelDirection(unsigned char Channel, unsigned char Direction);

Inputs: unsigned char Channel
The DIO channel number to be set.

unsigned char Direction
The DIO direction to be set: DIO_INPUT or DIO_OUTPUT.

Outputs: none

Analog-to-Digital (ADC) Calls

API calls can be made to control specific analog input channels. The following table lists the channel, range, and format parameter definitions used in ADC calls.

Table 7: ADC API Parameter Definitions

Parameters	Value	
Channel	PCI_AI_CHANNEL_1	0x0E
	PCI_AI _CHANNEL_2	0x4E
	PCI_AI _CHANNEL_3	0x1E
	PCI_AI _CHANNEL_4	0x5E
	PCI_AI _CHANNEL_5	0x2E
	PCI_AI _CHANNEL_6	0x6E
	PCI_AI _CHANNEL_7	0x3E
	PCI_AI _CHANNEL_8	0x7E
Range	SPI_RANGE_PM5V	0x00
	SPI_RANGE_PM10V	0x04
	SPI_RANGE_0_5V	0x08
	SPI_RANGE_0_10V	0x0C
Format	AI_RAW	0x00
	AI_VOLTS	0x01

VSL_ADCSetAnalogInputRange

Sets the analog input channel and range for a selected channel.

Syntax: VL_OSALIB_API void VSL_ADCSetAnalogInputRange(unsigned char Channel, unsigned char Range);

Inputs: unsigned char Channel
The analog input channel.

unsigned char Range
The analog input range for the channel.

Outputs: void

VSL_ADCGetAnalogInput

Returns the value of the selected analog input channel.

Syntax: VL_OSALIB_API double VSL_ADCGetAnalogInput(unsigned char Channel, unsigned char Format);

Inputs: unsigned char Channel
The analog input channel to be read.

unsigned char Format
How the data is returned. Either in its raw format or formatted into volts.

Outputs: double
The value read from the selected analog channel. This value will resolve to either 12 or 16 bits of accuracy depending on the accuracy of the channel.

VSL_GetADCType

Returns the model of Analog Input card installed.

Syntax: VL_OSALIB_API unsigned char VSL_GetADCType();

Inputs: void

Outputs: unsigned char
The type of MPEe-Ax card: Either VSL_ADC_TYPE_A1 or VSL_ADC_TYPE_A2.