VL82C37A

CMOS DIRECT MEMORY ACCESS (DMA) CONTROLLER

FEATURES

- Low-power CMOS version of popular 8237A DMA controller
- Four DMA channels
- Individual enable/disable control of DMA requests
- Directly expandable to any number of channels
- Independent auto-initialize feature for all channels
- High performance 8 MHz version available
- Transfers may be terminated by end-of-process input
- Software controlled DMA requests
- Independent polarity control for DREQ and DACK signals

DESCRIPTION

The VL82C37A Direct Memory Access (DMA) Controller serves as a peripheral interface circuit for microprocessor systems, and is designed to improve system performance by allowing external devices to directly transfer information from the system memory. Memory-to-memory transfer capability is also provided. The VL82C37A DMA Controller offers many programmable control features that enhance data throughput and system performance. Dynamic reconfiguration is permitted under program control.

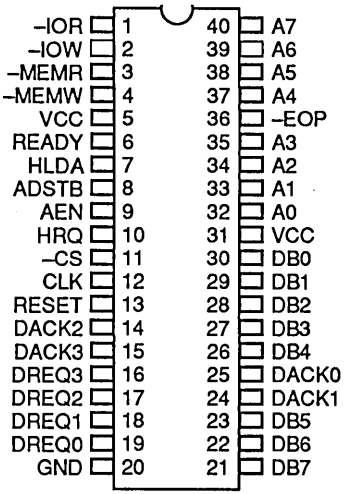
The VL82C37A is designed to be used with an external 8-bit address register such as the 8282. In addition to the four independent channels, the VL82C37A is expandable to any number of channels by cascading additional controller devices.

Three basic transfer modes allow the user to program the types of DMA service. Each channel can be individually programmed to auto-initialize to its original condition following an end-of-process (EOP) input. Each channel also has a 64K address and word count handling ability.

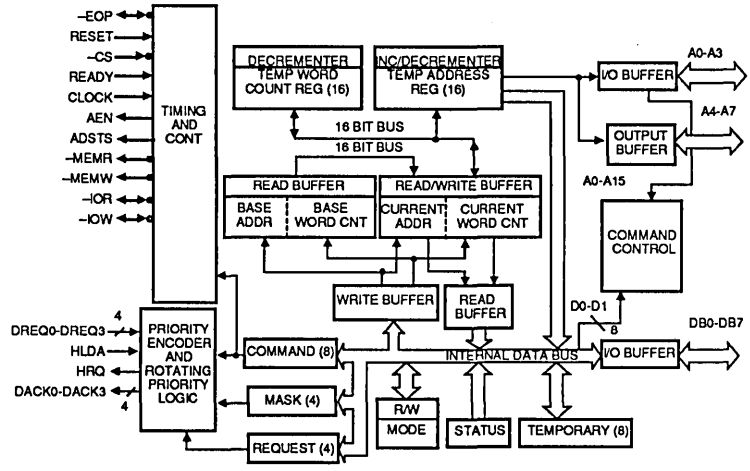
The VL82C37A DMA Controller is available in 5 MHz and 8 MHz clock frequencies.

PIN DIAGRAM

VL82C37A



BLOCK DIAGRAM

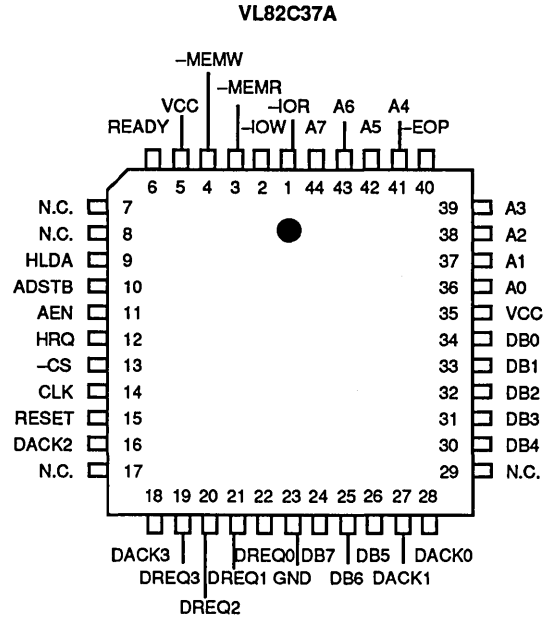


ORDER INFORMATION

Part Number	Clock Frequency	Package
VL82C37A-05PC	5 MHz	Plastic DIP
VL82C37A-05CC		Ceramic DIP
VL82C37A-05QC		Plastic Leaded Chip Carrier (PLCC)
VL82C37A-08PC	8 MHz	Plastic DIP
VL82C37A-08CC		Ceramic DIP
VL82C37A-08QC		Plastic Leaded Chip Carrier (PLCC)

Note: Operating temperature range is 0°C to +70°C.

PIN DIAGRAM


VL82C37A
-MEMW
-MEMR
VCC
-IOR
A6
A4
READY
-IOW
A7
A5
-EOP
6 5 4 3 2 1 44 43 42 41 40
N.C. 7
N.C. 8
HLDA 9
ADSTB 10
AEN 11
HRQ 12
-CS 13
CLK 14
RESET 15
DACK2 16
N.C. 17
39 A3
38 A2
37 A1
36 A0
35 VCC
34 DB0
33 DB1
32 DB2
31 DB3
30 DB4
29 N.C.
18 19 20 21 22 23 24 25 26 27 28
DACK3
DREQ3
DREQ2
DREQ1
GND
DREQ0
DB7
DB6
DB5
DACK1
DACK0

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
CLK	12	Clock Input: Controls the internal operations of the VL82C37A DMA Controller and its rate of data transfers. This input may be driven at up to 4 MHz for the standard VL82C37A-04 and up to 8 MHz for the VL82C37A-08.
–CS	11	Chip Select: An active low input used to select the VL82C37A as an I/O device during the idle cycle, allows CPU communication on the data bus.
RESET	13	Reset: An active high input that clears the Command, Request, and Temporary Registers, clears the first/last flip-flop, and sets the Mask Register. The device is in the idle cycle following a Reset signal.
READY	6	Ready: An input that extends the memory read and write pulses from the VL82C37A accommodating slow memories or I/O peripheral devices. During its specified setup/hold time, READY must not make transitions.
HLDA	7	Hold Acknowledge: This active high signal from the CPU indicates that it has relinquished control of the system busses.
DREQ0-DREQ3	19 - 16	DMA Request: These lines are individual asynchronous channel request inputs. Peripheral circuits use these lines to obtain DMA service. In fixed Priority, DREQ0 has the highest priority and DREQ3 has the lowest priority. Activating the DREQ line of a channel generates a request. DACK then acknowledges the recognition of DREQ signal. Polarity of DREQ is programmable. Reset initializes these lines to active high. DREQ must be sustained until the corresponding DACK becomes active.
DB0 - DB7	30 - 26, 23 - 21	Data Bus: These lines are bidirectional, three-state signals that connect to the system data bus. The outputs are enabled in the program condition during the I/O read to output the contents of an Address Register, a Status Register, the Temporary Register, or a Word Count Register to the CPU. The outputs are disabled and the inputs are read during an I/O Write cycle when the CPU is programming the VL82C37A control registers. During DMA cycles the most significant eight bits of the address are sent onto the data bus and are strobed into an external latch by ADSTB. In memory-to-memory operations, data from the memory comes into the VL82C37A on the data bus during the read-from-memory transfer. In the write-to-memory transfer, the data bus outputs determine the placement of the data, not the new memory location.
–IOR	1	I/O Read: This is a bidirectional, active low, three-state line. In the idle cycle, it is an input control signal used by the CPU to read the control registers. In the active cycle, it is an output control signal used by the VL82C37A to access data from a peripheral during a DMA Write transfer.
–IOW	2	I/O Write: This signal is a bidirectional active ow, three-state line. It is used by the CPU to load information into the VL82C37A DMA Controller. In the active cycle, it is used as an output control signal used by the VL82C37A to load data to the peripheral during a DMA read transfer.
–EOP	36	End of Process: This is an active low bidirectional signal, which provides data on the completion of DMA services and is available at the bidirection –EOP pin. The VL82C37A allows an external signal to terminate an active DMA service, by pulling the –EOP input low with an external –EOP signal. The VL82C37A also generates a pulse when the terminal count (TC) for any channel is achieved. This generates an –EOP signal that is active on the –EOP Line. When –EOP is received, either internally or externally, it will cause the VL82C37A to terminate the service, reset the request, and, if auto-initialize is enabled, to write the base registers to the current registers of that channel. The mask bit and TC bit in the status word will be set for the currently active channel by –EOP, unless the channel is programmed for auto-initialize. In that case, the mask bit remains unchanged. During memory-to-memory transfers, –EOP will be output when the TC for channel 1 occurs. To prevent erroneous end-of-process inputs, –EOP should be tied high with a pull-up resistor if it is not used.

SIGNAL DESCRIPTIONS (CONT.)

Signal Name	Pin Number	Signal Description
A0 - A3	32 - 35	The four least significant address lines: These lines are bidirectional three-state signals. In the idle cycle, they are inputs used by the CPU to address the register to be loaded or read. In the active cycle they are outputs that provide the lower four bits of the output address to the system.
A4 - A7	37 - 40	The four most significant address lines: These lines are three-state outputs that provide four bits of address. They are enabled only during the DMA service.
HRQ	10	Hold Request: This is the hold request to the CPU. It is used to request control of the system bus. If the corresponding mask bit is clear, the presence of any valid DREQ causes the VL82C37A to issue the HRQ signal. After HRQ is asserted, at least one clock cycle (TCY) must occur before HLDA can be valid.
DACK0 - DACK3	25, 24, 14, 15	DMA Acknowledge: This signal is used to notify an individual peripheral when it has been granted a DMA cycle. The sense of these lines is programmable; Reset initializes them to an active low.
AEN	9	Address Enable: This active high line enables the 8-bit latch containing the upper eight address bits onto the system address bus. It can also be used to disable other system bus drivers during DMA transfers.
ADSTB	8	Address Strobe: This active high is used to strobe the upper address byte into an external latch.
–MEMR	3	Memory Read: This active low signal is a three-state output used to access data from a selected memory location during a DMA read or memory-to-memory transfer.
–MEMW	4	Memory Write: This signal is an active low three-state output used to write data to a selected memory location during a DMA write or memory-to-memory transfer.
VCC	5, 31	+5 V ±5% power supply.
GND	20	Ground.

TABLE 1. INTERNAL REGISTERS

Name	Size	Number
Base Address Registers	16 bits	4
Base Word Count Registers	16 bits	4
Current Address Registers	16 bits	4
Current Word Count Registers	16 bits	4
Temporary Address Register	16 bits	1
Temporary Word Count Register	16 bits	1
Status Register	8 bits	1
Command Register	8 bits	1
Temporary Register	8 bits	1
Mode Registers	6 bits	4
Mask Register	4 bits	1
Request Register	4 bits	1

FUNCTIONAL DESCRIPTION

The internal registers and major logic blocks of the VL82C37A are shown in the block diagram. Data interconnection paths are also shown, but the various control signals between the blocks are not. The VL82C37A contains 344 bits of internal register memory. Figure 3 describes these registers and shows them by size. A complete description of the registers and their functions can be found in the Register Descriptions section.

The VL82C37A contains three basic control logic blocks. The Timing Control block generates internal timing and external control signals for the VL82C37A. The program command control block decodes the various commands given to the VL82C37A by the microprocessor before servicing a DMA Request. Further, it decodes the mode control word used to select the type of DMA during the servicing. The priority encoder block settles priority contention between DMA channels requesting service at the same time.

The external clock drives the timing control block. In most VL82C37A systems, this clock will usually be the Ø2 TTL clock from an VL82C84A. For 8085AH-2 systems above 3.9 MHz, the 8085 CLK(OUT) will not meet VL82C37A-05 (5 MHz) clock low and high time requirements. In this case, an external clock should be used to drive the VL82C37A-05.

DMA OPERATION

The VL82C37A is designed to operate in two major cycles: the idle and active . Several states are contained in each device cycle. The VL82C37A supports seven separate states, each being one full clock period. State I (SI), the inactive state, is entered when the VL82C37A has no valid DMA requests pending. While in SI, the DMA controller is inactive but may be in the program condition, being programmed by the processor. State 0 (S0) is the first state of a DMA service. The VL82C37A has requested a hold, but the processor has not yet responded with an acknowledge. The VL82C37A may still be programmed until it receives HLDA from the CPU. An acknowledge from the CPU signals that DMA transfers may begin. S1, S2, S3 and S4 are the functional states of the DMA service. If more time is needed to complete a transfer than is available with normal timing, wait states (WS) can be placed between S2 or S3 and S4 by using the Ready line on the VL82C37A. The data is transferred directly from the I/O device to memory (or vice versa) with –IOR and –MEMW (or –MEMR and –IOW) being active simultaneously. The data is not read into or driven out of the VL82C37A during I/O-to-memory or memory-to-I/O DMA transfers.

To complete memory-to-memory transfers requires a read-from and a write-to-memory. The states, which resemble the normal working states, use two-digit numbers for identification. Eight states are needed for each transfer: the first four states (S11, S12, S13, S14), are used for read-from-memory and the last four states (S21, S22, S23, S24), for the write-to-memory of the transfer.

IDLE CYCLE

When no channels are requesting service, the VL82C37A enters the idle cycle and performs SI states, sampling the DREQ lines every clock cycle to determine if any channel is requesting a DMA service. The device also samples –CS, looking for an attempt by the microprocessor to write or read to the internal registers of the VL82C37A. When –CS is low and HLDA is low, the VL82C37A initiates the program condition. The CPU now establishes, changes or inspects the internal definition of the part by reading from or writing to the internal register. Address lines A0-A3 are inputs to the device. They select registers that will be read or written. The –IOR and –IOW lines are used to select and time reads or writes. Because of the number and size of the internal registers, an internal flip-flop is used to generate one more bit of address. This bit is used to determine the upper or lower byte of the 16-bit address and Word Count Registers. This flip-flop can be reset by a separate software command.

Special software commands executed in the VL82C37A during the program condition are decoded as sets of addresses with the –CS and –IOW signals. The commands do not use the data bus. Clear First/Last Flip-Flop and Master Clear instructions are included.

ACTIVE CYCLE

When the VL82C37A is in the idle cycle and a nonmasked channel requests a DMA service, the device outputs an HRQ to the microprocessor and then enters the active cycle. During this cycle the DMA service takes place, in one of four modes.

In the single transfer mode, the device is programmed to make only one transfer. The word count is decremented and the address decremented or incremented, following each transfer. When the word count is completed from zero to FFFFH, a Terminal Count (TC) causes an auto-initialize if the channel has been so programmed.

The DREQ signal must be held active until DACK becomes active, in order to be recognized. If DREQ is held active for the entire single transfer, HRQ will become inactive and release the bus to the system. It again goes active and, upon receipt of a new HLDA, another single transfer is performed. In 8080A, 8085AH, 8088, or 8086 systems this insures one full machine cycle execution between DMA transfers. Details of timing between the VL82C37A and other bus control protocols depends upon the characteristics of the microprocessor involved.

In the block transfer mode, the device is activated by the DREQ signal to continue making transfers during the service until a TC, caused by word count going to FFFFH, or an external end of process (–EOP) is encountered. DREQ need only be held active until DACK becomes active. An auto-initialization will occur at the end of the service, if the channel has been programmed for it.

In the demand transfer mode the device is programmed to continue making transfers until a TC or external –EOP is encountered or until the DREQ signal goes inactive. Transfers may continue

until the I/O device has exhausted its data capacity. After the I/O device has caught up, the DMA service is re-established by a DREQ signal. During the interval between services, when the microprocessor is operating, the intermediate values of address and word count are stored in the VL82C37A Current Address and Current Word Count Registers. Only an –EOP can cause an auto-initialize at the end of the service. EOP is generated either by TC or by an external signal.

The fourth mode cascades multiple VL82C37As together for easy system expansion. The HRQ and HLDA signals from additional VL82C37As are connected to the DREQ and DACK signals of a channel of the primary VL82C37A. This permits the DMA requests of the additional device to propagate through the priority network circuitry of the preceding device. The priority chain is not broken, and the new device waits for its turn to acknowledge requests. As the cascade channel of the primary VL82C37A is used only to prioritize the additional device, it does not produce any address or control signals of its own, which could conflict with the outputs of the active channel in the added device. The VL82C37A responds to the DREQ and DACK signal, but all other outputs except HRQ are disabled.

Figure 8 shows two devices cascaded into a primary device using two of the previous channels. This forms a two-level DMA system. More VL82C37A's could be added at the second level by using the remaining channels of the first level. More devices can also be cascaded into the channels of the second-level devices, forming a third level.

TRANSFER TYPES

Each of the three modes of active transfer can perform three different types of transfers: read, write and verify. Write transfers move data from an I/O device to the memory by activating –MEMW and –IOR; read transfers move data from memory to an I/O device by activating –MEMR and –IOW.

Verify transfers are pseudo routines: the VL82C37A DMA Controller operates as in read or write transfers generating addresses, and responding to –EOP, and other operations.The memory and I/O control lines remain inactive. The verify mode is not permitted during memory-to-memory operation.

To perform block moves of data from one memory address space to another with a minimum of programming, the VL82C37A includes a memory-to-memory transfer feature. Programming a bit in the Command Register selects channels 0 and 1 to operate as memory-to-memory transfer channels. The transfer is initiated by setting the software DREQ for channel 0. The VL82C37A requests a DMA device as usual. After HLDA is true, the device, using eight-state transfers in block transfer mode, reads data from the memory. The channel 0 Current Address Register is the source for the address, and is decremented or incremented as usual. The data byte read from the memory is then stored in the VL82C37A internal Temporary Register. Channel 1 writes the data from the Temporary Register to memory using the address in its Current Address Register and incrementing or decrementing it as usual. The channel 1 current word count is decremented. When the word count goes to FFFFH, a TC is generated causing an –EOP output terminating the service.

Channel 0 may be programmed to hold the same address for all transfers, which permits a single word to be written to a block of memory.

The VL82C37A responds to external –EOP signals during memory-to-memory transfers. In block search schemes data comparators may use this input on finding a match. The timing of memory-to-memory transfers is shown in Figure 10. Memory-to-memory operations can be detected as an active AEN signal with no DACK outputs.

A channel may be set up to auto-initialize by setting a bit in the Mode Register. During initialization, the original values of the Current Address and Current Word Count Registers are automatically restored from the Base Address and Base Word Count Registers of that channel following –EOP. The base registers and the current registers are loaded at the same time. They remain unchanged thoughout the DMA service. The mask bit is not set when the channel is in auto-initialize. Following auto-initialize, the channel is prepared to perform another DMA service, without CPU action, as soon as a valid DREQ is detected.

The VL82C37A has two types of priority encoding available as software-selectable options. The fixed priority option sets the channels in priority order based upon the descending value of their number. The channel with the lowest priority is 3, then 2,1 and the highest priority channel is 0. After recognizing any one channel for service, the other channels are prevented from interferring with that service until it is completed.

In the rotating priority option, the last channel to get service becomes the lowest priority channel with the others rotating in order.

Rotating priority allows a single chip DMA system. Any device requesting service is guaranteed to be recognized after no more than three higher priority services have occurred. This prevents any one channel from dominating the system.

To achieve even greater throughput where system characteristics permit, the VL82C37A DMA Controller can compress the transfer time to two clock cycles. State S3 is used to extend the access time of the read pulse. By removing state S3, the read pulse width is made equal to the write pulse width, and a transfer consists only of state S2 to change the address and state S4 to perform the read/write. S1 state still occurs when A8-A15 need updating (see the Address Generation section.)

To reduce pin count, the VL82C37A multiplexes the eight higher order address bits on the data lines. State S1 is used to output the higher order address bits to an external latch, where they may be placed on the address bus. The falling edge of the Address Strobe (ADSTB) is used to load these bits from the data lines to the latch. Address Enable (AEN) is used to enable the bits onto the address bus through a three-state enable. The lower order address bits are directly sent by the VL82C37A . Lines A0-A7 are connected to the address bus.

During block and demand transfer mode services, including multiple transfers, the addresses generated will be in order. During a large number of transfers the data held in the external address latch will not change. This data will change when a carry or borrow from A7 to A8 takes place in the normal order of addresses. To expedite transfers, the VL82C37A DMA Controller executes S1 states only when needed to update A8-A15 in the latch. For long services, S1 states and address strobes may occur only once every 256 transfers, a savings of 255 clock cycles for each 256 transfers.

REGISTER DESCRIPTION

Current Address Register: Each channel has a 16-bit Current Address Register. This register holds the value of the address used during DMA transfers. The address is automatically incremented or decremented after each transfer and the intermediate values of the address are stored in the Current Address Register throughout the transfer. The microprocessor reads this register in successive 8-bit bytes. It may also be reinitialized by an auto-initialize to its original value which takes place only after an –EOP.

Current Word Register: Each channel has a 16-bit Current Word Count Register that determines the number of transfers to be performed. The actual number of transfers is one more than the number programmed in the Current Word Count Register; programming a count of 100 will result in 101 transfers. The word count is decremented after each transfer; the intermediate value of this word count is stored in the register during the transfer. When the value in the register goes from 0 to FFFFH, a TC is generated. The register is then loaded or read in successive 8-bit bytes by the microprocessor in the program condition. Following the end of a DMA service, it may also be reinitialized by an auto-initialization to its original value which occurs only on –EOP. If it is not auto-initialized, this register has a count of FFFFH after TC.

Base Address and Base Word Count Registers: Each channel has a pair of 16-bit Base Address and Base Word Count Registers that store the original value of their associated current registers. Throughout auto-initialization these values are used to restore the current registers to their original values. The base registers are written at the same time with their corresponding current register in 8-bit bytes in the program condition by the microprocessor. These registers cannot be read by the microprocessor.

Command Register: This 8-bit register controls the operation of the VL82C37A, is programmed by the microprocessor in the program condition and is cleared by reset or a master clear instruction. Figure 2 lists and describes the function of the command bits.

Mode Register: All channels have a 6-bit Mode register. When the register is being written to by the microprocessor in the program condition, bits 0 to 1 determine which channel the Mode Register is to be written.

Request Register: The VL82C37A can responds to requests for DMA service that are initiated by software as well as by a DREQ signal. Each channel has a request bit associated with it in the 4-bit Request Register. These are non-maskable and can be prioritized by the priority encoder network.

Each register bit is set or reset separately under software control, or is cleared upon generation of a TC or external –EOP. The entire register is cleared by a Reset. To set or reset a bit, the software loads the correct form of the data word. Table 2 shows register address coding. To make a software request, the channel must be in block mode.

Mask Register: Each channel has an associated mask bit that can be set to disable the incoming DREQ signal. A mask bit is set when its associated channel produces an –EOP, if the channel is not programmed for auto-initialize. Any bit of the 4-bit Mask register may also be set or cleared separately under software control. The entire register is set by a reset, which disables all DMA requests until a clear Mask Register instruction allows them to occur. This instruction to separately set or clear the mask bits is similar in form to that used with the Request Register.

Status Register: The Status Register is available to be read out of the VL82C37A DMA Controller by the microprocessor and contains information about the status of the devices at this point. This information includes which channels have reached a terminal count and which channels have pending DMA requests.

Bits 0-3 are set each time a TC is reached by that channel or an external –EOP is applied and are cleared upon reset and on every status read. Bits 4 through 7 are set whenever their corresponding channel is requesting service.

Temporary Register: The Temporary Register is used to hold data during memory-to-memory transfers. The last word moved can be read by the microprocessor in the Program Condition following the completion of the transfers. The Temporary Register always contains the last byte transferred in the previous memory-to-memory operation, unless cleared by a reset.

Software Commands: These additional special software commands can be executed in the program condition and do not depend on any specific bit pattern on the data bus.

The clear first/last flip-flop command is executed prior to writing or reading new address or word count information to the VL82C37A. This initializes the flip-flop to a known state so that subsequent accesses to register contents by the microprocessor will address upper and lower bytes in the correct sequence.

The Master Clear software instruction has the same effect as the hardware reset. The Command, Status, Request, Temporary, and Internal First/Last Flip-Flop Registers are cleared and the Mask Register is set. The VL82C37A enters an idle cycle.

The Clear Mask Register command clears the mask bits of all four channels, enabling them to accept DMA requests.

PROGRAMMING

The VL82C37A DMA Controller accepts programming from the host processor any time that HLDA is inactive, even if the HRQ signal is active. The host must assure that programming and HLDA are

mutually exclusive. A problem can occur if a DMA request occurs, on an unmasked channel while the VL82C37A is being programmed.

For example, the CPU may be starting to reprogram the two-byte Address Register of a channel when that channel receives a DMA request. If the VL82C37A is enabled (bit 2 in the command register is 0) and that channel is unmasked, a DMA service will occur after one byte of the Address Register has been reprogrammed. This can be avoided by disabling the controller - setting bit 2 in the command register - or masking the channel before programming another registers. Once the programming is complete, the controller can be enabled (unmasked).

After power-up all internal locations, including the Mode registers, should be loaded with a valid value. This should be done to unused channels as well.

APPLICATION

Figure 1 shows a convenient method for configuring a DMA system with the VL82C37A DMA Controller and an 8080A/8085AH microprocessor system. Whenever there is at least one valid DMA request from a peripheral device, the multimode VL82C37A DMA Controller issues a HRQ to the processor.

When the processor replies with a HLDA signal, the VL82C37A takes control of the address, data, and control buses. The address for the first transfer operation is output in two bytes - the least significant eight bits on the eight address outputs, and the most significant eight bits on the data bus. The contents of the data bus are then latched into the 8282 8-bit latch to complete the full 16 bits of the address bus. The 8282 is a high-speed, 8-bit, three-state latch in a 20-pin DIP package. After the initial transfer takes place, the latch is updated only after a carry or borrow is generated in the least significant address byte. Four DMA channels are available when one VL82C37A DMA Controller is used.

FIGURE 1. SYSTEM INTERFACE

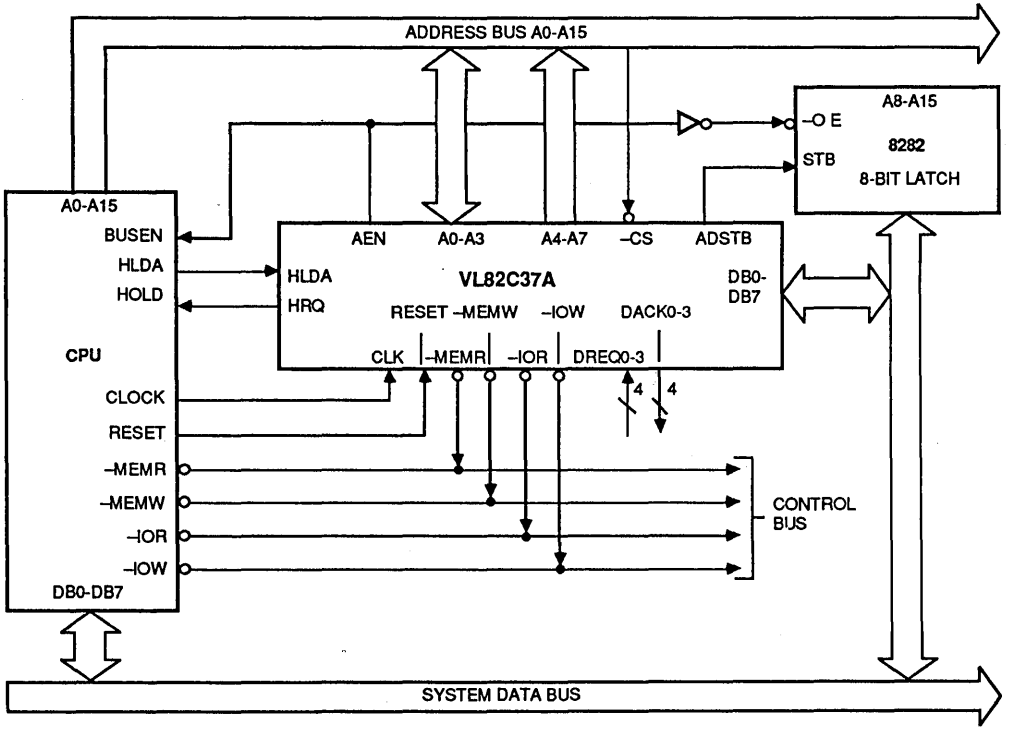


FIGURE 2. COMMAND REGISTER

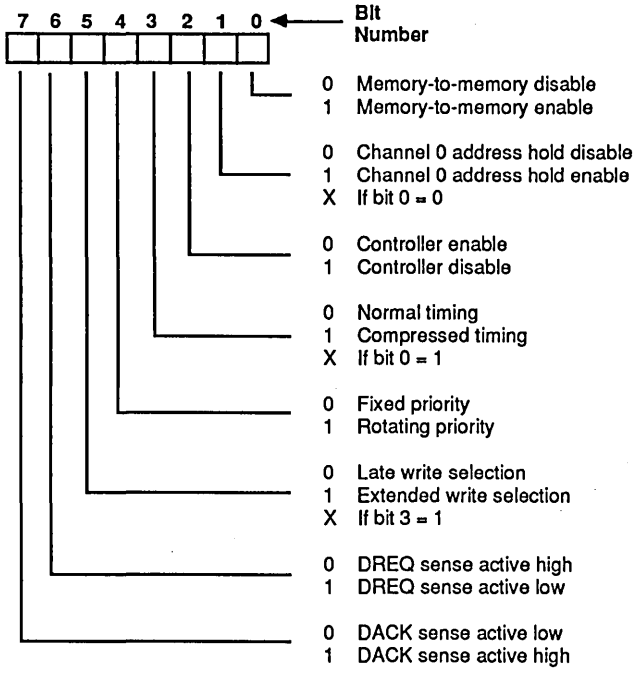


FIGURE 3. MODE REGISTER

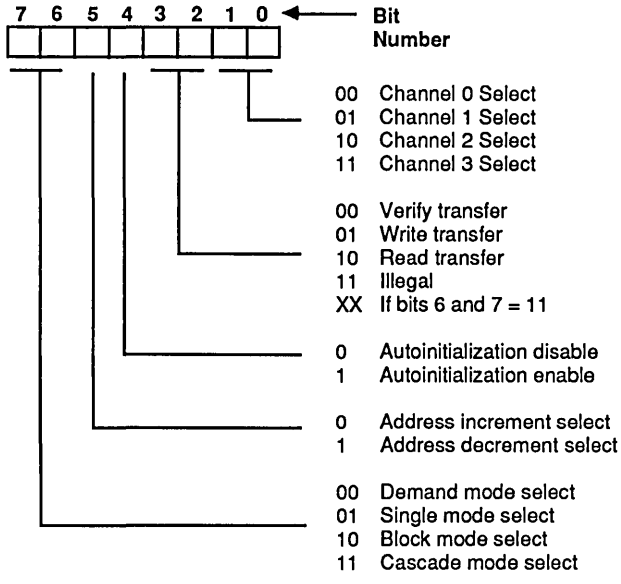


FIGURE 4. REQUEST REGISTER

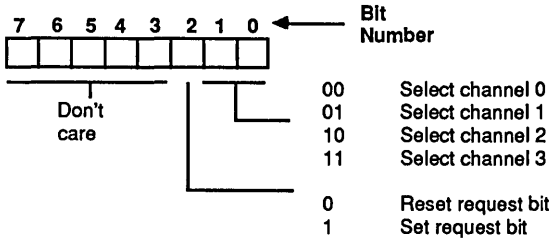


FIGURE 6. MASK REGISTER (SELECT MODE)

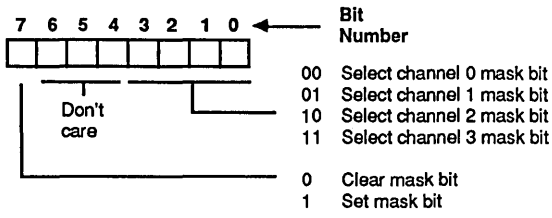


FIGURE 5. STATUS REGISTER

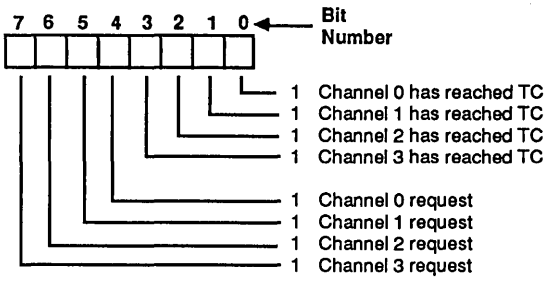


FIGURE 7. MASK REGISTER (MASK MODE)

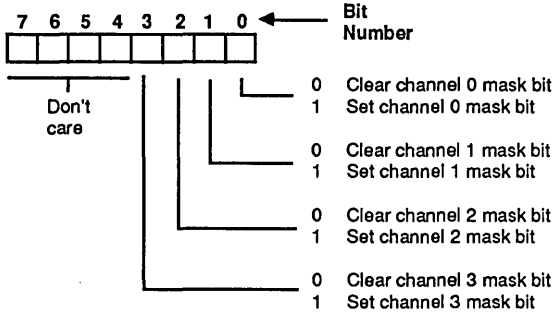


TABLE 2. REGISTER CODES

Register	Operation	Signals						
		–CS	–IOR	–IOW	A3	A2	A1	A0
Command	Write	0	1	0	1	0	0	0
Mode	Write	0	1	0	1	0	1	1
Request	Write	0	1	0	1	0	0	1
Mask	Set/Reset	0	1	0	1	0	1	0
Mask	Write	0	1	0	1	1	1	1
Temporary	Read	0	0	1	1	1	0	1
Status	Read	0	0	1	1	0	0	0

TABLE 3. SOFTWARE COMMAND CODES

Signals						Operation
A3	A2	A1	A0	–IOR	–IOW	
1	0	0	0	0	1	Read Status Register
1	0	0	0	1	0	Write Command Register
1	0	0	1	0	1	Illegal
1	0	0	1	1	0	Write Request Register
1	0	1	0	0	1	Illegal
1	0	1	0	1	0	Write Single Mask Register Bit
1	0	1	1	0	1	Illegal
1	0	1	1	1	0	Write Mode Register
1	1	0	0	0	1	Illegal
1	1	0	0	1	0	Clear Byte Pointer Flip/Flop
1	1	0	1	0	1	Read Temporary Register
1	1	0	1	1	0	Master Clear
1	1	1	0	0	1	Illegal
1	1	1	0	1	0	Clear Mask Register
1	1	1	1	0	1	Illegal
1	1	1	1	1	0	Write All Mask Register Bits

FIGURE 8. CASCADED VL82C37A CONTROLLERS

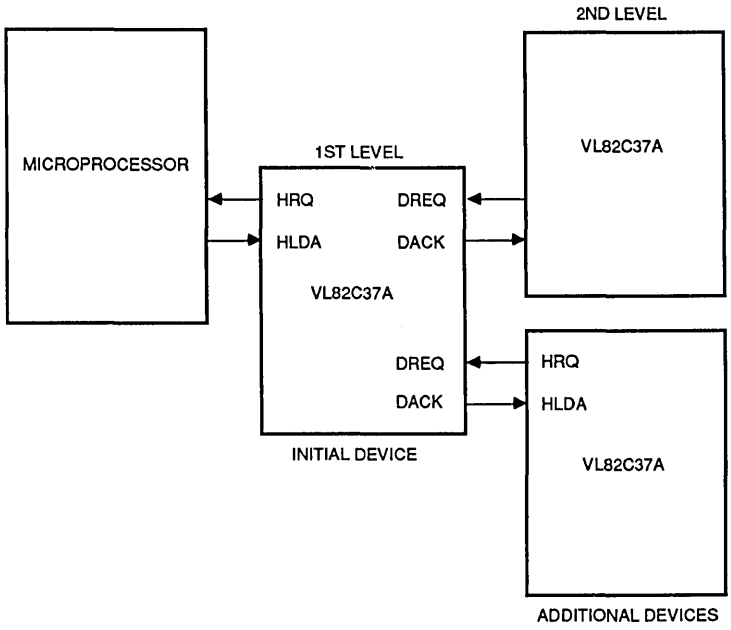


TABLE 4. WORD COUNT AND ADDRESS REGISTER COMMAND CODES

Channel	Register	Operation	Signals							Internal Flip-Flop	Data Bus DB0-DB7
			–CS	–IOR	–IOW	A3	A2	A1	A0		
0	Base and Current Address	Write	0	1	0	0	0	0	0	0	A0-A7
			0	1	0	0	0	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	0	0	0	A0-A7
			0	0	1	0	0	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	0	1	0	W0-W7
			0	1	0	0	0	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	0	1	0	W0-W7
			0	0	1	0	0	0	1	1	W8-W15
1	Base and Current Address	Write	0	1	0	0	0	1	0	0	A0-A7
			0	1	0	0	0	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	0	1	0	0	A0-A7
			0	0	1	0	0	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	0	1	1	0	W0-W7
			0	1	0	0	0	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	0	1	1	0	W0-W7
			0	0	1	0	0	1	1	1	W8-W15
2	Base and Current Address	Write	0	1	0	0	1	0	0	0	A0-A7
			0	1	0	0	1	0	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	0	0	0	A0-A7
			0	0	1	0	1	0	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	0	1	0	W0-W7
			0	1	0	0	1	0	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	0	1	0	W0-W7
			0	0	1	0	1	0	1	1	W8-W15
3	Base and Current Address	Write	0	1	0	0	1	1	0	0	A0-A7
			0	1	0	0	1	1	0	1	A8-A15
	Current Address	Read	0	0	1	0	1	1	0	0	A0-A7
			0	0	1	0	1	1	0	1	A8-A15
	Base and Current Word Count	Write	0	1	0	0	1	1	1	0	W0-W7
			0	1	0	0	1	1	1	1	W8-W15
	Current Word Count	Read	0	0	1	0	1	1	1	0	W0-W7
			0	0	1	0	1	1	1	1	W8-W15

TABLE 5. DMA MODE AC CHARACTERISTICS

Symbol	Parameter	VL82C37A-04		VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	Min	Max	
TAEL	AEN High from CLK Low (S1) Delay Time		225		200		105	ns
TAET	AEN Low from CLK High (S1) Delay Time		150		130		80	ns
TAFAB	ADR Active to Float Delay from CLK High		120		90		55	ns
TAFC	Read or Write Float from CLK High		120		120		75	ns
TAFDB	DB Active Float Delay from CLK High		190		170		135	ns
TAHR	ADR from Read High Hold Time	TCY-100		TCY-100		TCY-75		ns
TAHS	DB from ADSTB Low Hold Time	40		30		20		ns
TAHW	ADR from Write High Hold Time	TCY-50		TCY-50		TCY-50		ns
TAK	DACK Valid from CLK Low Delay Time (Note 7)		220		170		105	ns
	–EOP High from CLK High Delay Time (Note 10)		190		170		105	ns
	–EOP Low from CLK High Delay Time		190		170		105	ns
TASM	ADR Stable from CLK High		190		170		105	ns
TASS	DB to ADSTB Low Setup Time	100		100		65		ns
TCH	Clock High Time (Transitions ≤ 10 ns)	100		80		55		ns
TCL	Clock Low Time (Transitions ≤ 10 ns)	110		68		43		ns
TCY	CLK Cycle Time	250		200		125		ns
TDCL	CLK High to Read or Write Low Delay (Note 4)		200		190		120	ns
TDCTR	Read High from CLK High (S4) Delay Time (Note 4)		210		190		115	ns
TDCTW	Write High from CLK High (S4) Delay (Note 4)		150		130		80	ns
TDQ1	HRQ Valid from CLK High Delay Time (Note 5)		120		120		75	ns
TDQ2			190		120		75	ns
TEPS	–EOP Low from CLK Low Setup Time	45		40		25		ns
TEPW	–EOP Pulse Width	225		220		135		ns
TFAAB	ADR Float to Active Delay from CLK High		190		170		100	ns
TFAC	Read or Write Active from CLK High		150		150		90	ns
TFADB	DB Float to Active Delay from CLK High		225		200		110	ns
THS	HLDA Valid to CLK High Setup Time	75		75		45		ns
TIDH	Input Data from –MEMR High Hold Time	0		0		0		ns
TIDS	Input Data to –MEMR High Setup Time	190		170		90		ns
TODH	Output Data from –MEMW High Hold Time	20		10		10		ns
TODV	Output Data Valid to –MEMW High	125		125		90		ns
TQS	DREQ to CLK Low (S1,S4) Setup Time	0		0		0		ns
TRH	CLK to READY Low Hold Time	20		20		20		ns
TRS	READY to CLK Low Setup Time	60		60		35		ns
TSTL	ADSTB High from CLK High Delay Time		150		130		110	ns
TSTT	ADSTB Low from CLK High Delay Time		110		90		65	ns

Explanatory notes follow DC Characteristics Table.

FIGURE 9. DMA TRANSFER TIMING (SEE TABLE 5.)

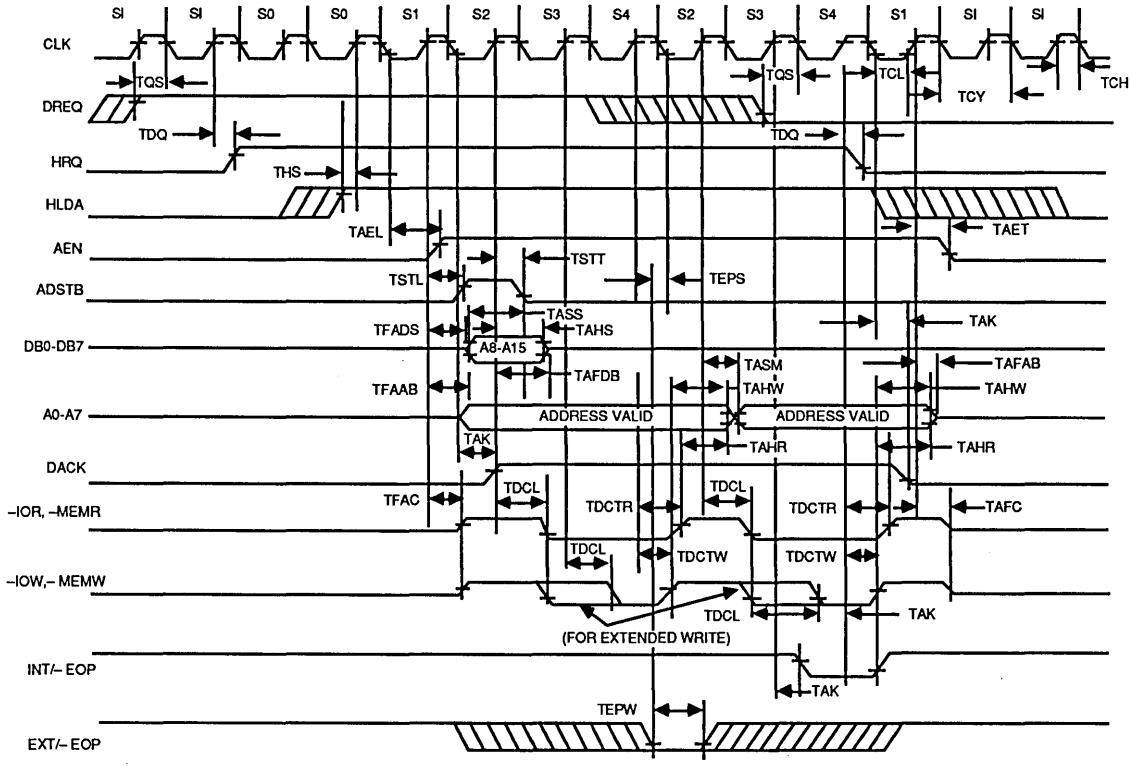


FIGURE 10. MEMORY-TO-MEMORY TRANSFER TIMING (SEE TABLE 5)

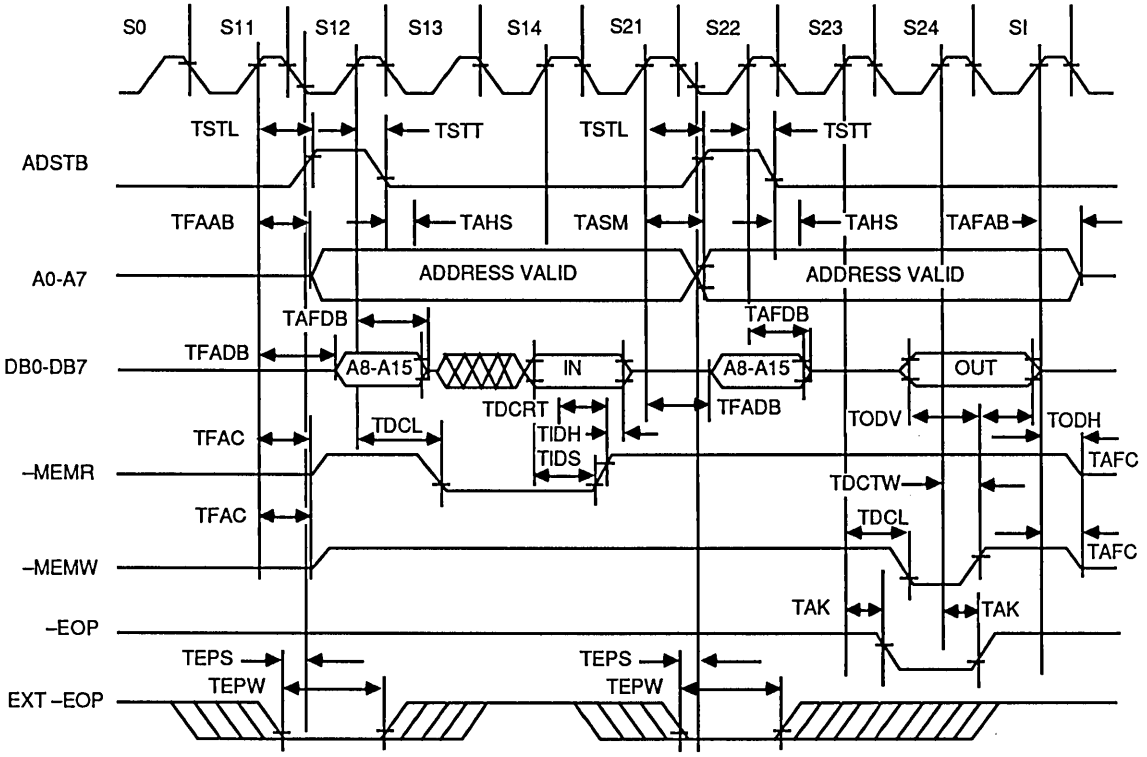


TABLE 6. PERIPHERAL MODE AC CHARACTERISTICS

Symbol	Parameter	VL82C37A-04		VL82C37A-05		VL82C37A-08		Unit
		Min	Max	Min	Max	Min	Max	
TAR	ADR Valid or –CS Low to Read Low	50		50		30		ns
TAW	ADR Valid to Write High Setup Time	150		130		80		ns
TCW	CS Low to Write High Setup Time	150		130		80		ns
TDW	Data Valid to Write High Setup Time	150		130		80		ns
TRA	ADR or CS Hold from Read High	0		0		0		ns
TRDE	Data Access from Read Low (Note 3)		200		140		120	ns
TRDF	DB Float Delay from Read High	20	100	0	70	0	70	ns
TRSTD	Power Supply High to RESET Low Setup Time	500		500		500		ns
TRSTS	RESET to First –IOW	2TCY		2TCY		2TCY		ns
TRSTW	RESET Pulse Width	300		300		300		ns
TRW	Read Width	250		200		155		ns
TWA	ADR from Write High Hold Time	20		20		10		ns
TWC	CS High from Write High Hold Time	20		20		10		ns
TWD	Data from Write High Hold Time	30		30		20		ns
TWWS	Write Width	200		160		100		ns

Explanatory notes follow DC Characteristics Table.

FIGURE 11. SLAVE MODE WRITE TIMING (SEE TABLE 6)

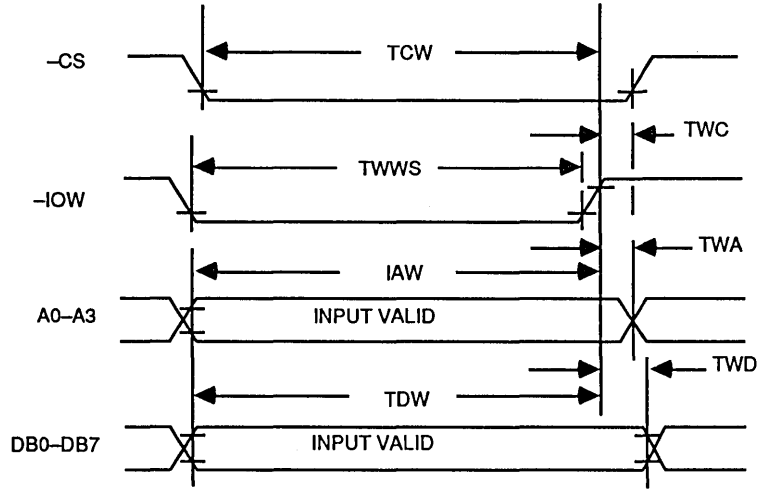


FIGURE 12. SLAVE MODE READ TIMING (SEE TABLE 6)

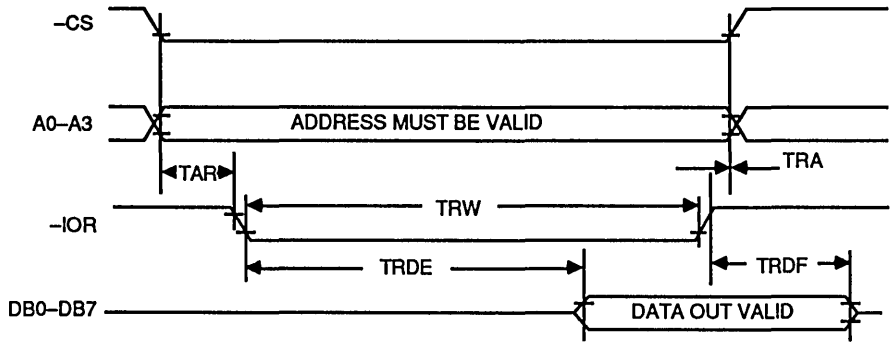


FIGURE 13. READY TIMING (SEE TABLE 5)

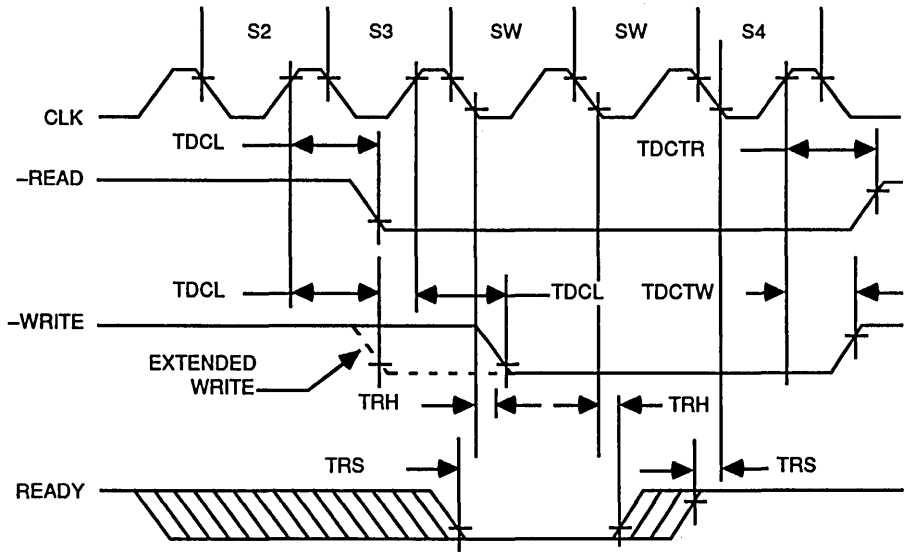


FIGURE 14. COMPRESSED TRANSFER TIMING (SEE TABLE 5)

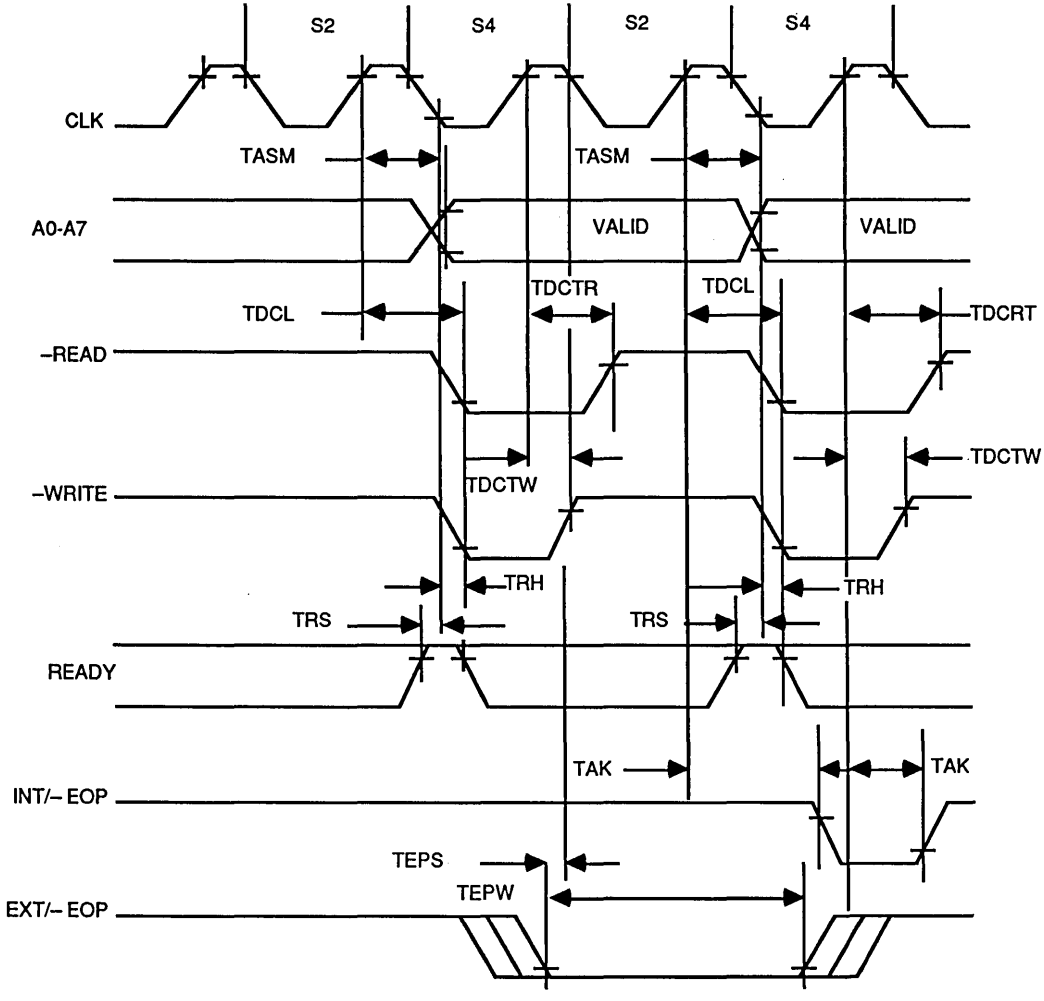
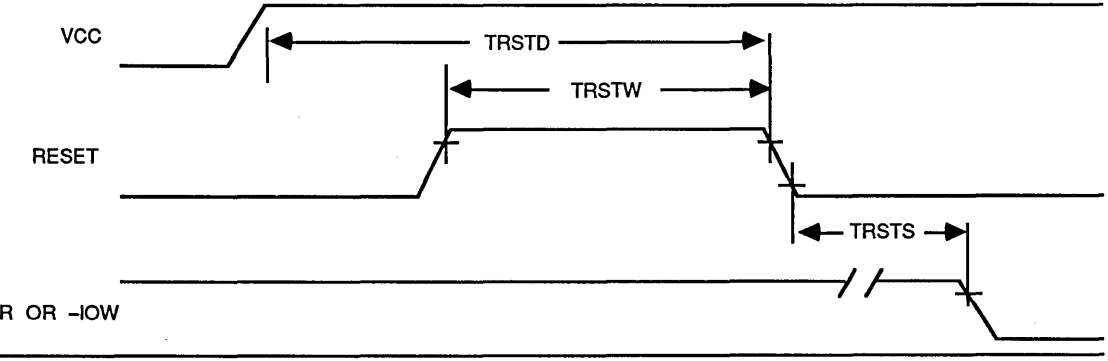


FIGURE 15. RESET TIMING (SEE TABLE 6)



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	−0.5 to 7.0 V
Input Voltage	−0.5 to 5.5 V
Output Voltage	−0.5 to 5.5 V
Operating Temperature	0 °C to +150°C
Storage Temperature	−65°C to +150°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS:

Symbol	Parameter	Min	Typ (1)	Max	Unit	Test Conditions
VOH	Output High Voltage	2.4			V	IOH = −200 µA
		3.3			V	IOH = −100 µA (HRQ Only)
VOL	Output Low Voltage			450	mV	IOL = 2.0 mA (data bus) −EOP IOL = 3.2 mA (other outputs) (8) IOL = 2.5 mA (ADSTB) (8)
VIH	Input High Voltage	2.2		VCC + 0.5	V	
VIL	Input Low Voltage	−0.5		0.8	V	
ILI	Input Load Current			±10	µA	0 V ≤ VIN ≤ VCC
ILO	Output Leakage Current			±10	µA	0.45 V ≤ VOUT ≤ VCC
ICC	VCC Supply Current			30	mA	Clk. Freq. = 5 MHz, 8MHz
C0	Output Capacitance		4	8	pF	fC = 1.0 MHz, Inputs = 0 V
C1	Input Capacitance		8	15	pF	
C10	I/O Capacitance		10	18	pF	

AC and DC Characteristics Notes:

1. Typical values are for TA = 25°C, nominal supply voltage, and nominal processing parameters.
2. Input timing parameters assume transition times of 20 ns or less. Waveform measurement points for both input and output signals are 2.0 V for high and 0.8 V for low, unless otherwise noted.
3. Output loading is 1 TTL gate plus 150 pF capacitance, unless otherwise noted.
4. The net −IOW or −MEMW pulse width for normal write will be TCY-100 ns and for extended write will be 2TCY-100 ns. The net −IOR or −MEMR pulse width for normal read will be 2TCY-50 ns and for compressed read will be TCY-50 ns.
5. TDQ is specified for two different output high levels: TDQ1 is measured at 2.0 V, TDQ2 is measured at 3.3 V. The value for TDQ2 assumes an external 3.3 Kohm pull-up resistor connected from HRQ to VCC.
6. DREQ should be held active until DACK is returned.
7. DREQ and DACK signals may be active high or active low. Timing diagrams assume the active high mode.
8. Successive read and/or write operations, by the external processor, to program or examine the controller must be timed to allow at least 400 ns for the VL82C37A-05 and at least 250 ns for the VL82C37A-08, as recovery time between active read or write pulses.
9. −EOP is an open-collector output. This parameter assumes the presence of a 2.2 kΩ pull-up resistor to VCC.
10. Pin 5 is an input that should always be at a logic high level. An internal pull-up resistor will establish a logic high when the pin is left floating. It is recommended, however, that pin 5 be tied to VCC.