VIA Labs, Inc.

Data Sheet

VL830
USB4 Endpoint Device Controller

October 6th, 2021

Revision 0.60

VLI

VL830

USB4
Endpoint Device Controller

FCCSP

Revision History

Rev	Date	Note	Initial
0.50	05/13/2021	Preliminary Draft Release	EC
0.60	10/06/2021	Production Candidate Update	EC/TS

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Product Features

VL830
USB4 Endpoint Device Controller

■ **USB Specification Compliant**
- Compliant to Universal Serial Bus 4 Specification
  - Supports Gen 2 & Gen 3 Operation (20Gbps & 40Gbps)
  - Supports USB and DisplayPort Tunneling
- Compliant to Universal Serial Bus 3.2 Specification
  - Meets all USB 3.2 ECN & Compliance Testing Updates to date
- Compliant to Universal Serial Bus 2.0 Specification
  - Integrated USB 2.0 Hub supports MTT

■ **DisplayPort Specification Compliant**
- Compliant to DisplayPort version 1.4a
  - 1x Dedicated DP Output
- DisplayPort alternate mode (Sink) support
  - 1.62Gbps/2.7Gbps/5.4Gbps/8.1Gbps signal rates
  - 2-Ln/4-Ln Firmware Configurable

■ **Security Feature Support**
- Hardware Support for Digitally Signed Firmware (256-bit ECDSA)
- Integrated SHA256 Hash Engine
- Configurable for Verity-On-Update or Verify-On-Boot

■ **USB Functions**
- Integrated USB 3.2 SuperSpeed 10Gbps Hub
  - Supports up to 5x DFP (4x USB SS, 1x USB HS)
- Integrated USB Billboard Class 1.2.2 Device
  - Implemented as a USB2 Virtual Device
  - Configurable by supported USB PD Controllers (Such as VL10X-series PD Controllers)
- Supports firmware update over USB

■ **Full Sideband Signal Support**
- Supports both Individual and Ganged Port Power Control Operation for All USB Ports
- Supports PWM LED Status Lights
- SPI Interface for Firmware. Firmware Upgradable over USB or I2C.
- Management Interface for Specialized Applications

■ **Comprehensive USB Battery Charging Support**
- Supports USB Battery Charging Specification v1.2 (SDP, CDP, DCP)
- Support for Vendor Specific Charging Modes eg. Apple 2.4A, Samsung, etc.
- Supports YD/T 1591-2009
- Supports Stand-Alone Charging when System is Suspend, Shut Down, or Disconnected
- Any Combination of DFPs can be Configured to Support USB Battery Charging

■ **Power and Package**
- In-house PHY employs advanced CMOS process for low power consumption
- Requires 3.3V/1.05V/0.9V Inputs
- 25MHz Xtal
- FCCSP green package (10x10x1.03 mm, 19x19 Grid with 328Balls)

VL830 System Overview

VIA Lab's VL830 is a USB4 Endpoint device controller, featuring an optimized cost-structure and full compliance with the USB4 specification. VL830 supports the full 40Gbps bandwidth of USB4 and offers both USB and DisplayPort functionality. VL830 operates at full performance when used with Thunderbolt™ 4 or USB4 systems, and is also backward compatible with systems that support DisplayPort Alternate Mode over USB Type-C.

VL830 features a highly-integrated design, with built-in USB 3.2 SuperSpeed USB 10Gbps Hub, USB 2.0 hub with Multiple Transaction Translator Support, and a DisplayPort 1.4a output with up to 4-Lane HBR3 (32.4 Gbit/s) support. Any combination of USB SuperSpeed (10Gbps), SuperSpeed (5Gbps), High Speed (480Mbps), Full Speed (12Mbps), and Low Speed (1.5Mbps) devices are supported. VL830 also features an optionally configurable USB Billboard Device when used with supported PD Controllers such as the VL10x Series, and an optionally configurable USB HID endpoint to support button functions.

VL830 utilizes a 10x10x1.03 mm Flip Chip-Chip Scale Package with 0.5mm ball pitch for ease of manufacturability and small board size. Two of the downstream USB ports also feature integrated 10Gbps muxes for board area savings and improved signal integrity for data-only USB Type-C applications. VL830 requires the use of an external USB PD controller for both upstream and downstream USB Type-C ports. If paired with the VL10X Series USB PD Controller, VL830 can share a single SPI flash and offer improved integration without consuming an additional USB port.
VL830 features flexible firmware architecture, providing a framework for custom functions in addition to in-field updates. Various parameters including USB configuration, PD configuration, Tx equalization setting, and GPIO behavior are changeable via firmware. VL830 also features an optionally configurable USB Charging Controller for charging various devices such as smartphones and tablets that can be configure on a per-port basis.

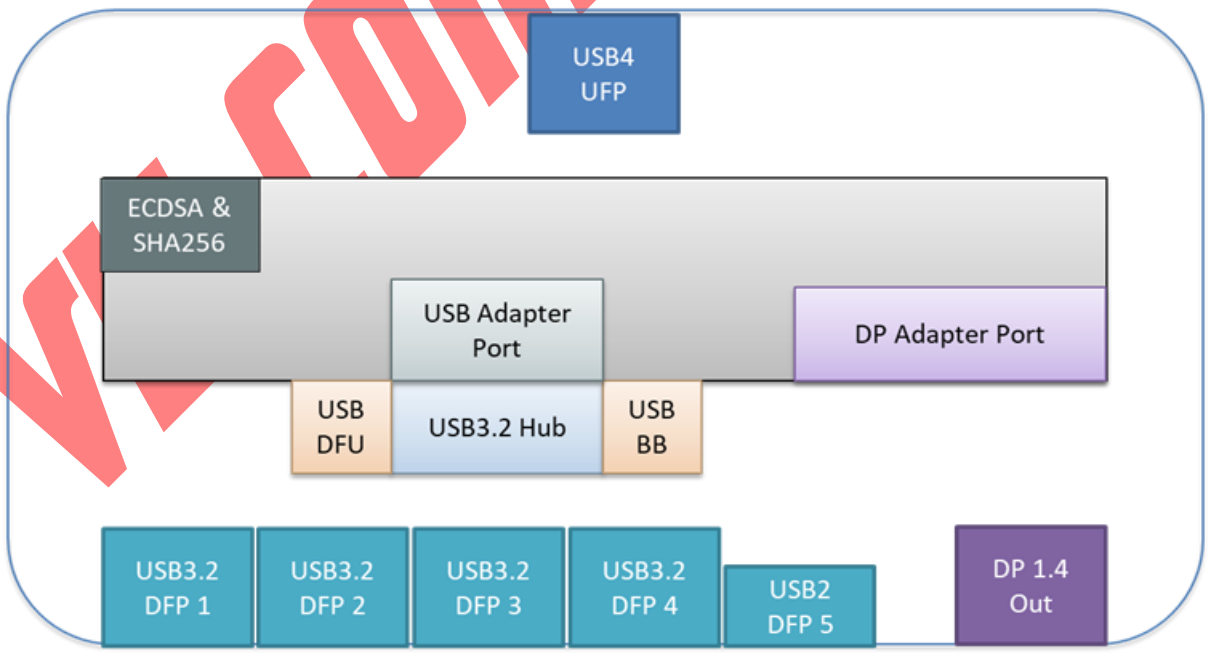

Figure 1 – VL830 Block Diagram

USB Battery Charging Behavior

3 Concepts of Rapid Charging over USB:

■Rapid Charging over USB enables charging of devices at rates in excess of baseline USB standards.

The current limit of USB 2.0 is 500mA for configured devices, and the current limit of USB 3.2 is 900mA for configured devices. Depending on the device, Rapid Charging implementations typically feature current limits between 1000mA to 2400mA.

■It is the Host/Hub's responsibility to advertise Rapid Charging capabilities, and it is the Device's responsibility to recognize and determine those capabilities.

Rapid Charging over USB enables charging at rates in excess of baseline USB specifications, so in order to prevent a situation where a device sinks more current than what a port is rated for, different manufacturers employ various charging schemes in an attempt to ensure safe and reliable operation with their respective device and charger. It goes without saying that Rapid Charging will only occur when both Host/Hub and Device supports it.

■The rate at which a device charges is dependent upon the device.

This means that the device must determine the host/hub port's capabilities to determine which charging mode to use. Also, the rate at which a device charges can vary depending on the status of the device. For example, some devices only charge at their maximum rate when the battery is nearly depleted. When the battery is nearly full, they may switch to a trickle-charge mode. The Host/Hub rapid-charging port has no control over this behavior.

Supported USB Charging Modes

SDP – Standard Downstream Port
This is a typical USB 2.0 or USB 3.2 port and does not explicitly support Rapid USB Charging. SDP is constrained to the current limits as defined in the USB 2.0 or USB 3.2 spec which are 500mA and 900mA respectively. While the actual current limit is enforced by the polyfuse or power-switch providing current-limiting functionality for the downstream port, most USB devices will not draw more than 500mA or 900mA under USB 2.0 or USB 3.2 modes.

CDP – Charging Downstream Port
CDP is defined in the USB Battery Charging Specification 1.2 and enables devices that are able to correctly recognize CDP to simultaneously function as a USB device while drawing up to 1.5A for Rapid Charging when connected to the downstream port of a USB Host or Hub that advertises CDP capability.

DCP – Dedicated Charging Port
DCP is defined in the USB Battery Charging Specification 1.2 and has been in use on an unofficial basis prior to the official USB Battery Charging Specification. DCP is a dedicated charging mode, so when a device is charging under DCP, regular USB operations such as data transfer to the device are not supported.

Special Modes
Various vendors such as Apple, RIM, Motorola, etc. may employ different detection mechanisms compared to other USB devices and thus, may enter Rapid Charging under the previously mentioned charging modes. VL830 supports an auto detection mechanism that provides charging for the majority of devices.

Ball Out (VL830)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	
A	ALT_AUX N	AUXN_DP	VSSA	USB4RN0 _B	VSSA	USB4RP0 _A	VSSA	USB4TN0 _B	VSSA	USB4TP0 _A	VSSA	TX0N_DP	VSSA	TX1N_DP	VSSA	TX2N_DP	VSSA	TX3N_DP	VSSA	A
B	ALT_AUX P	AUXP_DP	VSSA	USB4RP0 _B	VSSA	USB4RN0 _A	VSSA	USB4TP0 _B	VSSA	USB4TN0 _A	VSSA	TX0P_DP	VSSA	TX1P_DP	VSSA	TX2P_DP	VSSA	TX3P_DP	VSSA	B
C	USB4SBU 1	USB4SBU 2	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	HPD_DP	C
D	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA		GDBGO0 2	GPIO01	GPIO00	D
E	USB3XO	USB3XI	VSSA		VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA			GDBGO1 2	USBPE0	USBOC0	E
F	VSSA	VSSA		USB3REX TP	VSSA	VSSA	VSSA	VCCA10_ U4	VCCA10_ U4			VCCA_DP	VSSA	VSSA	GDBGO1 1		GDBGO0 1	USBPE3	USBOC3	F
G	DP	DM	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VCCA_DP	VSSA	VSSA	GDBGO0 0		GDBGO0 3	USBPE4	USBOC4	G
H	DP_E	DM_E	VSSA	VCCAH_M	VSSA	VSSA	VCCA09_ M	VCCA09_ U4	VCCA09_ U4		VCCA09_ DP	VSSA	VSSA	VCCAH_D P			GDBGO0 4	USBPE5	USBOC5	H
J	DP_D	DM_D	VSSA	VCCAH_U 4	VSSA	VCCA10_ M	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA				GDBGO0 5	USBLED2 /SPICK	USBLED1 /SPISI	J
K	VSSA	VSSA			VSSA	VCCA10_ U2	VSSA	VDD	VDD	VDD	VDD	VSSA	VCC33		GDBGO1 3		GDBGO0 6	SPICS	USBLED3 /SPISO	K
L	DP_C	DM_C	VSSA	VCCAH_U 2	VSSA		VSSA	VDD	VDD	VDD	VDD	VSSA	VCC33	VSSA	GDBGO1 4		GPI	VSSA	VSSA	L
M	DP_B	DM_B	VSSA	VCCAH_L 34	VSSA			VSSA	VSSA	VSSA	VSSA		VSSA	VSSA	GDBGO1 5		VBUSDET 0	RESET_	TESTEN	M
N	DP_A	DM_A	VSSA	VSSA	VSSA	VCCA10_L 34	VSSA	VCCA09_ U2	VCCA09_L 34	VCCA09_L 12	VCCA09_L 12	VSSA	VCCA10_L 12	VCCA10_L 12	VSSA		GDBGO0 7	GPIO02	GPIO03	N
P	VSSA	VSSA	VSSA	VSSA	VSSA	VCCA10_L 34	VSSA		VCCA09_L 34		VSSA	VSSA		VSSA			GDBGO0 8	USBPE1	USBOC1	P
R	USB3TN4	USB3TP4	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VCCAH_L 12		GDBGO0 9	USBPE2	USBOC2	R
T	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA		GDBGO1 0	GPIO05	GPIO04	T
U	USB3RP4	USB3RN4	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA	GPIO07	GPIO06	U
V	VSSA	VSSA	VSSA	USB3RN3	VSSA	USB3RP2 _A	USB3RP2 _B	VSSA	USB3TP2 _A	USB3TP2 _B	VSSA	USB3TP1 _A	USB3TP1 _B	VSSA	USB3RP1 _A	USB3RP1 _B	VSSA	USBLED4	GPIO08	V
W	USB3TN3	USB3TP3	VSSA	USB3RP3	VSSA	USB3RN2 _A	USB3RN2 _B	VSSA	USB3TN2 _A	USB3TN2 _B	VSSA	USB3TN1 _A	USB3TN1 _B	VSSA	USB3RN1 _A	USB3RN1 _B	VSSA	USB4TM U_CLKO	USB4TM U_CLKI	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	

Figure 2 – VL830 Ball Diagram

Ball List (VL830)

Ball#	Ball Name	Ball#	Ball Name
A1	ALT_AUXN	C1	USB4SBU1
A2	AUXN_DP	C2	USB4SBU2
A3	VSSA	C3	VSSA
A4	USB4RN0_B	C4	VSSA
A5	VSSA	C5	VSSA
A6	USB4RP0_A	C6	VSSA
A7	VSSA	C7	VSSA
A8	USB4TN0_B	C8	VSSA
A9	VSSA	C9	VSSA
A10	USB4TP0_A	C10	VSSA
A11	VSSA	C11	VSSA
A12	TX0N_DP	C12	VSSA
A13	VSSA	C13	VSSA
A14	TX1N_DP	C14	VSSA
A15	VSSA	C15	VSSA
A16	TX2N_DP	C16	VSSA
A17	VSSA	C17	VSSA
A18	TX3N_DP	C18	VSSA
A19	VSSA	C19	HPD_DP
B1	ALT_AUXP	D1	VSSA
B2	AUXP_DP	D2	VSSA
B3	VSSA	D3	VSSA
B4	USB4RP0_B	D4	VSSA
B5	VSSA	D5	VSSA
B6	USB4RN0_A	D6	VSSA
B7	VSSA	D7	VSSA
B8	USB4TP0_B	D8	VSSA
B9	VSSA	D9	VSSA
B10	USB4TN0_A	D10	VSSA
B11	VSSA	D11	VSSA
B12	TX0P_DP	D12	VSSA
B13	VSSA	D13	VSSA
B14	TX1P_DP	D14	VSSA
B15	VSSA	D15	VSSA
B16	TX2P_DP	D16	NC
B17	VSSA	D17	GDBGO02
B18	TX3P_DP	D18	GPIO01
B19	VSSA	D19	GPIO00

Ball List (VL830)

Ball#	Ball Name	Ball#	Ball Name
E1	USB3XO	G1	DP
E2	USB3XI	G2	DM
E3	VSSA	G3	VSSA
E4	NC	G4	VSSA
E5	VSSA	G5	VSSA
E6	VSSA	G6	VSSA
E7	VSSA	G7	VSSA
E8	VSSA	G8	VSSA
E9	VSSA	G9	VSSA
E10	VSSA	G10	VSSA
E11	VSSA	G11	VSSA
E12	VSSA	G12	VCCA_DP
E13	VSSA	G13	VSSA
E14	VSSA	G14	VSSA
E15	NC	G15	GDBGO00
E16	NC	G16	NC
E17	GDBGO12	G17	GDBGO03
E18	USBPE0	G18	USBPE4
E19	USBOC0	G19	USBOC4
F1	VSSA	H1	DP_E
F2	VSSA	H2	DM_E
F3	NC	H3	VSSA
F4	USB3REXTP	H4	VCCAH_M
F5	VSSA	H5	VSSA
F6	VSSA	H6	VSSA
F7	VSSA	H7	VCCA09_M
F8	VCCA10_U4	H8	VCCA09_U4
F9	VCCA10_U4	H9	VCCA09_U4
F10	NC	H10	NC
F11	NC	H11	VCCA09_DP
F12	VCCA_DP	H12	VSSA
F13	VSSA	H13	VSSA
F14	VSSA	H14	VCCAH_DP
F15	GDBGO11	H15	NC
F16	NC	H16	NC
F17	GDBGO01	H17	GDBGO04
F18	USBPE3	H18	USBPE5
F19	USBOC3	H19	USBOC5

Ball List (VL830)

Ball#	Ball Name	Ball#	Ball Name
J1	DP_D	L1	DP_C
J2	DM_D	L2	DM_C
J3	VSSA	L3	VSSA
J4	VCCAH_U4	L4	VCCAH_U2
J5	VSSA	L5	VSSA
J6	VCCA10_M	L6	NC
J7	VSSA	L7	VSSA
J8	VSSA	L8	VDD
J9	VSSA	L9	VDD
J10	VSSA	L10	VDD
J11	VSSA	L11	VDD
J12	VSSA	L12	VSSA
J13	VSSA	L13	VCC33
J14	NC	L14	VSSA
J15	NC	L15	GDBGO14
J16	NC	L16	NC
J17	GDBGO05	L17	GPI
J18	USBLED2 / SPICK	L18	VSSA
J19	USBLED1 / SPISI	L19	VSSA
K1	VSSA	M1	DP_B
K2	VSSA	M2	DM_B
K3	NC	M3	VSSA
K4	NC	M4	VCCAH_L34
K5	VSSA	M5	VSSA
K6	VCCA10_U2	M6	NC
K7	VSSA	M7	NC
K8	VDD	M8	VSSA
K9	VDD	M9	VSSA
K10	VDD	M10	VSSA
K11	VDD	M11	VSSA
K12	VSSA	M12	NC
K13	VCC33	M13	VSSA
K14	NC	M14	VSSA
K15	GDBGO13	M15	GDBGO15
K16	NC	M16	NC
K17	GDBGO06	M17	VBUSDET0
K18	SPICS	M18	RESET_
K19	USBLED3 / SPISO	M19	TESTEN

Ball List (VL830)

Ball#	Ball Name	Ball#	Ball Name
N1	DP_A	R1	USB3TN4
N2	DM_A	R2	USB3TP4
N3	VSSA	R3	VSSA
N4	VSSA	R4	VSSA
N5	VSSA	R5	VSSA
N6	VCCA10_L34	R6	VSSA
N7	VSSA	R7	VSSA
N8	VCCA09_U2	R8	VSSA
N9	VCCA09_L34	R9	VSSA
N10	VCCA09_L12	R10	VSSA
N11	VCCA09_L12	R11	VSSA
N12	VSSA	R12	VSSA
N13	VCCA10_L12	R13	VSSA
N14	VCCA10_L12	R14	VSSA
N15	VSSA	R15	VCCAH_L12
N16	NC	R16	NC
N17	GDBGO07	R17	GDBGO09
N18	GPIO02	R18	USBPE2
N19	GPIO03	R19	USBOC2
P1	VSSA	T1	VSSA
P2	VSSA	T2	VSSA
P3	VSSA	T3	VSSA
P4	VSSA	T4	VSSA
P5	VSSA	T5	VSSA
P6	VCCA10_L34	T6	VSSA
P7	VSSA	T7	VSSA
P8	NC	T8	VSSA
P9	VCCA09_L34	T9	VSSA
P10	NC	T10	VSSA
P11	VSSA	T11	VSSA
P12	VSSA	T12	VSSA
P13	NC	T13	VSSA
P14	VSSA	T14	VSSA
P15	NC	T15	VSSA
P16	NC	T16	NC
P17	GDBGO08	T17	GDBGO10
P18	USBPE1	T18	GPIO05
P19	USBOC1	T19	GPIO04

Ball List (VL830)

Ball#	Ball Name	Ball#	Ball Name
U1	USB3RP4	W1	USB3TN3
U2	USB3RN4	W2	USB3TP3
U3	VSSA	W3	VSSA
U4	VSSA	W4	USB3RP3
U5	VSSA	W5	VSSA
U6	VSSA	W6	USB3RN2_A
U7	VSSA	W7	USB3RN2_B
U8	VSSA	W8	VSSA
U9	VSSA	W9	USB3TN2_A
U10	VSSA	W10	USB3TN2_B
U11	VSSA	W11	VSSA
U12	VSSA	W12	USB3TN1_A
U13	VSSA	W13	USB3TN1_B
U14	VSSA	W14	VSSA
U15	VSSA	W15	USB3RN1_A
U16	VSSA	W16	USB3RN1_B
U17	VSSA	W17	VSSA
U18	GPIO07	W18	USB4TMU_CLKO
U19	GPIO06	W19	USB4TMU_CLKI
V1	VSSA		
V2	VSSA		
V3	VSSA		
V4	USB3RN3		
V5	VSSA		
V6	USB3RP2_A		
V7	USB3RP2_B		
V8	VSSA		
V9	USB3TP2_A		
V10	USB3TP2_B		
V11	VSSA		
V12	USB3TP1_A		
V13	USB3TP1_B		
V14	VSSA		
V15	USB3RP1_A		
V16	USB3RP1_B		
V17	VSSA		
V18	USBLED4		
V19	GPIO08		

Ball Descriptions (VL830)

Signal Type Definition

Name	Type	Signal Description
Input	I	A logic input-only signal
Output	O	A logic output only signal
Input/ Output	I/O	A logic bi-directional signal
Power	PWR	Power
Ground	GND	Ground
NC	-	No Connection

USB4 Interface

Ball Name	Ball #	I/O	Signal Description
USB4RP0_A	A6	I	USB4 UFP Differential RX+; Side A
USB4RN0_A	B6	I	USB4 UFP Differential RX–; Side A
USB4TP0_A	A10	O	USB4 UFP Differential TX–; Side A
USB4TN0_A	B10	O	USB4 UFP Differential TX+; Side A
USB4RP0_B	B4	I	USB4 UFP Differential RX+; Side B
USB4RN0_B	A4	I	USB4 UFP Differential RX–; Side B
USB4TP0_B	B8	O	USB4 UFP Differential TX–; Side B
USB4TN0_B	A8	O	USB4 UFP Differential TX+; Side B
USB4SBU1	C1	I/O	USB4 UFP Sideband use signal
USB4SBU2	C2	I/O	USB4 UFP Sideband use signal

USB 2.0 Interface

Ball Name	Ball#	I/O	Signal Description
DP	G1	I/O	USB 2.0 UFP Differential D+
DM	G2	I/O	USB 2.0 UFP Differential D–
DP_A	N1	I/O	USB 2.0 DFP1 Differential D+
DM_A	N2	I/O	USB 2.0 DFP1 Differential D–
DP_B	M1	I/O	USB 2.0 DFP2 Differential D+
DM_B	M2	I/O	USB 2.0 DFP2 Differential D–
DP_C	L1	I/O	USB 2.0 DFP3 Differential D+
DM_C	L2	I/O	USB 2.0 DFP3 Differential D–
DP_D	J1	I/O	USB 2.0 DFP4 Differential D+
DM_D	J2	I/O	USB 2.0 DFP4 Differential D–
DP_E	H1	I/O	USB 2.0 DFP5 Differential D+
DM_E	H2	I/O	USB 2.0 DFP5 Differential D–

Display Port Interface

Ball Name	Ball#	I/O	Signal Description
TX0P	B12	O	Display Port 1.4 Differential TX0+
TX0N	A12	O	Display Port 1.4 Differential TX0-
TX1P	B14	O	Display Port 1.4 Differential TX1+
TX1N	A14	O	Display Port 1.4 Differential TX1-
TX2P	B16	O	Display Port 1.4 Differential TX2+
TX2N	A16	O	Display Port 1.4 Differential TX2-
TX3P	B18	O	Display Port 1.4 Differential TX3+
TX3N	A18	O	Display Port 1.4 Differential TX3-
ALT_AUXP	B1	I/O	Display Port AUX Channel Positive (Alt-Mode)
ALT_AUXN	A1	I/O	Display Port AUX Channel Negative (Alt-Mode)
AUXP_DP	B2	I/O	Display Port AUX Channel Positive (USB4)
AUXN_DP	A2	I/O	Display Port AUX Channel Negative (USB4)
HPD_DP	C19	I	Display Port Hot Plug Detect

Test Pin

Ball Name	Ball#	I/O	Signal Description
TESTEN	M19	I	Test Mode Enable Low: Normal mode. High: Test mode.
USB4TMU_CLKI	W19	I	USB4 TMU Clock Input for TMU test.
USB4TMU_CLKO	W18	O	USB4 TMU Clock Output for TMU test.

Power and Ground

Ball Name	Ball#	I/O	Signal Description
VSSA	A3, A5, A7, A9, A11, A13, A15, A17, A19, B3, B5, B7, B9, B11, B13, B15, B17, B19, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, D1, D2, D3, D4, D5, D6, D7, D8, D9, D10, D11, D12, D13, D14, D15, E3, E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, F1, F2, F5, F6, F7,F13, F14, G3, G4, G5, G6, G7, G8, G9, G10, G11, G13, G14, H3, H5, H6, H12, H13, J3, J5, J7, J8, J9, J10, J11, J12, J13, K1, K2, K5, K7, K12, L3, L5, L7, L12, L14, L18, L19, M3, M5, M8, M9, M10, M11, M13, M14, N3, N4, N5, N7, N12, N15, P1, P2, P3, P4, P5, P7, P11, P12, P14, R3, R4, R5, R6, R7, R8, R9, R10, R11, R12, R13, R14, T1, T2, T3, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, U3, U4, U5, U6,U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, V1, V2, V3, V5, V8, V11, V14, V17, W3, W5, W8, W11, W14, W17	GND	Ground
VDD	K8, K9, K10, K11, L8, L9, L10, L11	PWR	0.9V Core Power
VCCA09	H7, H8, H9, H11, N8, N9, N10, N11, P9	PWR	0.9V Analog Power
VCCA10	F8, F9, J6, K6, N6, N13, N14, P6	PWR	1.05V Analog Power
VCCA	F12, G12	PWR	1.05V DP Block Analog Power
VCC33	K13, L13	PWR	3.3V Logic I/O Power
VCCAH	H4, H14, J4, L4, M4, R15	PWR	3.3V Analog Power

Analog Command Block

Ball Name	Ball#	I/O	Signal Description
USB3XO	E1	O	25M Crystal Output
USB3XI	E2	I	25M Crystal Input
USB3REXTP	F4	I	Connect to External Reference Resistor (20K+/- 1%)

USB 3.2 Interface

Ball Name	Ball #	I/O	Signal Description
USB3RP1_A	V15	I	USB 3.2 DFP1 Differential RX+; Side A
USB3RN1_A	W15	I	USB 3.2 DFP1 Differential RX−; Side A
USB3TP1_A	V12	O	USB 3.2 DFP1 Differential TX+; Side A
USB3TN1_A	W12	O	USB 3.2 DFP1 Differential TX−; Side A
USB3RP1_B	V16	I	USB 3.2 DFP1 Differential RX+; Side B
USB3RN1_B	W16	I	USB 3.2 DFP1 Differential RX-; Side B
USB3TP1_B	V13	O	USB 3.2 DFP1 Differential TX+; Side B
USB3TN1_B	W13	O	USB 3.2 DFP1 Differential TX-; Side B
USB3RP2_A	V6	I	USB 3.2 DFP2 Differential RX+; Side A
USB3RN2_A	W6	I	USB 3.2 DFP2 Differential RX−; Side A
USB3TP2_A	V9	O	USB 3.2 DFP2 Differential TX+; Side A
USB3TN2_A	W9	O	USB 3.2 DFP2 Differential TX−; Side A
USB3RP2_B	V7	I	USB 3.2 DFP2 Differential RX+; Side B
USB3RN2_B	W7	I	USB 3.2 DFP2 Differential RX-; Side B
USB3TP2_B	V10	O	USB 3.2 DFP2 Differential TX+; Side B
USB3TN2_B	W10	O	USB 3.2 DFP2 Differential TX-; Side B
USB3RP3	W4	I	USB 3.2 DFP3 Differential RX+
USB3RN3	V4	I	USB 3.2 DFP3 Differential RX−
USB3TP3	W2	O	USB 3.2 DFP3 Differential TX+
USB3TN3	W1	O	USB 3.2 DFP3 Differential TX−
USB3RP4	U1	I	USB 3.2 DFP4 Differential RX+
USB3RN4	U2	I	USB 3.2 DFP4 Differential RX−
USB3TP4	R2	O	USB 3.2 DFP4 Differential TX+
USB3TN4	R1	O	USB 3.2 DFP4 Differential TX−

Side Band Signal and Miscellaneous

Ball Name	Ball#	I/O	Signal Description
USBPE0	E18	O	UFP USB PE / I2C Shared Pin (Firmware Programmable) USB Power Enable Mode High: Enable Low: Off I2C Master Mode: SCL
USBOC0	E19	I or I/O	UFP USB OC / I2C Shared Pin (Firmware Programmable) Must be pulled high if NC. (3.3V Max) High: Normal Low: Port Over Current Event I2C Master Mode: SDA
USBPE1	P18	O	DFP1 USB PE / I2C Shared Pin (Firmware Programmable) USB Power Enable Mode High: Enable Low: Off I2C Master Mode: SCL
USBOC1	P19	I or I/O	DFP1 USB OC / I2C Shared Pin (Firmware Programmable) Must be pulled high if NC. (3.3V Max) High: Normal Low: Port Over Current Event I2C Master Mode: SDA
USBPE2	R18	O	DFP2 USB PE / I2C Shared Pin (Firmware Programmable) USB Power Enable Mode High: Enable Low: Off I2C Master Mode: SCL
USBOC2	R19	I or I/O	DFP2 USB OC / I2C Shared Pin (Firmware Programmable) Must be pulled high if NC. (3.3V Max) High: Normal Low: Port Over Current Event I2C Master Mode: SDA
USBPE3	F18	O	DFP3 USB PE / I2C Shared Pin (Firmware Programmable) USB Power Enable Mode High: Enable Low: Off I2C Master Mode: SCL
USBOC3	F19	I or I/O	DFP3 USB OC / I2C Shared Pin (Firmware Programmable) Must be pulled high if NC. (3.3V Max) High: Normal Low: Port Over Current Event I2C Master Mode: SDA
USBPE4	G18	O	DFP4 USB PE / I2C Shared Pin (Firmware Programmable) USB Power Enable Mode High: Enable Low: Off I2C Master Mode: SCL
USBOC4	G19	I or I/O	DFP4 USB OC / I2C Shared Pin (Firmware Programmable) Must be pulled high if NC. (3.3V Max) High: Normal Low: Port Over Current Event I2C Master Mode: SDA
USBPE5	H18	O	DFP5 USB PE USB Power Enable Mode

			High: Enable Low: Off
USBOC5	H19	I	DFP5 USB OC Must be pulled high if NC. (3.3V Max) High: Normal Low: Port Over Current Event
RESET_	M18	I	Reset Input of Controller Low: Reset High: Normal Operation
VBUSDET0	M17	I	UFP Vbus Detection (3.3V Max)
LED1/SPISI	J19	I/O	DFP1 LED Indicator / SPISI shared pin. Active High Output for LED Use.
LED2/SPICK	J18	I/O	DFP2 LED Indicator / SPISCLK shared pin. Active High Output for LED Use.
LED3/SPISO	K19	I/O	DFP3 LED Indicator / SPISO shared pin. Active High Output for LED Use.
SPICS	K18	I/O	SPICS Active Low Output for SPI CS# Use
LED4	V18	O	DFP4 LED Indicator Active High Output for LED Use
GPI	L17	I	GPI Input only for Security option
GPIO00	D19	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO01	D18	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO02	N18	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO03	N19	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO04	T19	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO05	T18	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO06	U19	I/O	GPIO Available for GPIO Use, Config via Firmware Setting.
GPIO07	U18	I/O	GPIO Available for GPIO Use, Config via Firmware Setting. I2C Slave mode: SDA
GPIO08	V19	I/O	GPIO Available for GPIO Use, Config via Firmware Setting. I2C Slave mode: SCL
GDBGO00	G15	I/O	Internal Debug Reserved.
GDBGO01	F17	I/O	Internal Debug Reserved.
GDBGO02	D17	I/O	Internal Debug Reserved.
GDBGO03	G17	I/O	Internal Debug Reserved.
GDBGO04	H17	I/O	Internal Debug Reserved.
GDBGO05	J17	I/O	Internal Debug Reserved.
GDBGO06	K17	I/O	Internal Debug Reserved.
GDBGO07	N17	I/O	Internal Debug Reserved.
GDBGO08	P17	I/O	Internal Debug Reserved.
GDBGO09	R17	I/O	Internal Debug Reserved.
GDBGO10	T17	I/O	Internal Debug Reserved.
GDBGO11	F15	I/O	Internal Debug Reserved.
GDBGO12	E17	I/O	Internal Debug Reserved.
GDBGO13	K15	I/O	Internal Debug Reserved.
GDBGO14	L15	I/O	Internal Debug Reserved.
GDBGO15	M15	I/O	Internal Debug Reserved.

Electrical Specification

Absolute Maximum Rating

Symbol	Parameter	Min	Max	Unit	Note
T_{STG}	Storage Temperature	-55	125	°C	—
V_{33}	3.3V Power Supply Voltage	-0.5	3.63	V	—
V_{105}	1.05V Input Voltage	-0.5	1.1	V	—
V_{09}	0.9V Input Voltage	-0.5	0.99	V	—
V_{IN}	Input voltage at I/O pins	-0.5	(≦ 3.63) and (≦ V_{33}+0.3)	V	—
V_{ESD}	Electrostatic Discharge	-2000	2000	V	Human Body Model
θ_{ja}	Thermal resistance between junction and ambient	FCCSP For 6-layer PCB: 25.5		°C/W	PCB definitions follow JESD51-7
θ_{jb}	Thermal resistance between junction and board	FCCSP For 6-layer PCB: 11.2		°C/W	
θ_{jc}	Thermal resistance between junction and case	FCCSP For 6-layer PCB: 7.8		°C/W	
P_D	Power dissipation	—	2	W	

Note: Stress above conditions may cause permanent damage to the device.
Functional operation of this device should be restricted to the conditions described.

Note: About thermal factors, T_a is the concerned ambient temperature, and
$\theta_{ca} = \theta_{ja} - \theta_{jc}$
$T_J = \theta_{ja} * P_D + T_a$
$T_c = \theta_{ca} * P_D + T_a$

Operating Conditions

Symbol	Parameter	Min	Max	Unit	Note
T_A	Ambient Temperature	0	65	°C	—
T_j	Junction Temperature	0	105	°C	—
V_{33}	3.3V Power Supply Voltage	3.0	3.465	V	—
V_{105}	1.05V Input Voltage	1.0	1.1	V	—
V_{09}	0.9V Input Voltage	0.81	0.99	V	—
V_{IL}	Input Low Voltage	—	0.8	V	—
V_{IH}	Input High Voltage	2.3	—	V	—
V_{OL}	Output Low Voltage	—	0.4	V	I_{OL}=4mA
V_{OH}	Output High Voltage	2.4	—	V	I_{OH}=4mA
I_{IL}	Input Leakage Current	—	+/-10	µA	$0<V_i<V_{33}$
I_{OZ}	Tristate Leakage Current	—	+/-20	µA	$0<V_o<V_{33}$

Note: The solution using VL830 should guarantee meeting one of the operating conditions.

i.e. either Ta is lower than 65C or Tj is lower than 105C.

Power consumption

The following consumption value applies up to typical condition.

TBD

Note: T_A=25°C, V_{33}=3.3V, V_{105}=1.05V, V_{09}=0.9V
SSP: Super Speed Plus (USB3.2 10Gbps) Device
SS: Super Speed (USB3.2 5Gbps) Device
HS: High Speed (USB2.0) Device

Timing Requirements for SPI Flash

SPI flash ROM is used to store the FW data for VL830. This section specifies the SPI timing requirements for the device

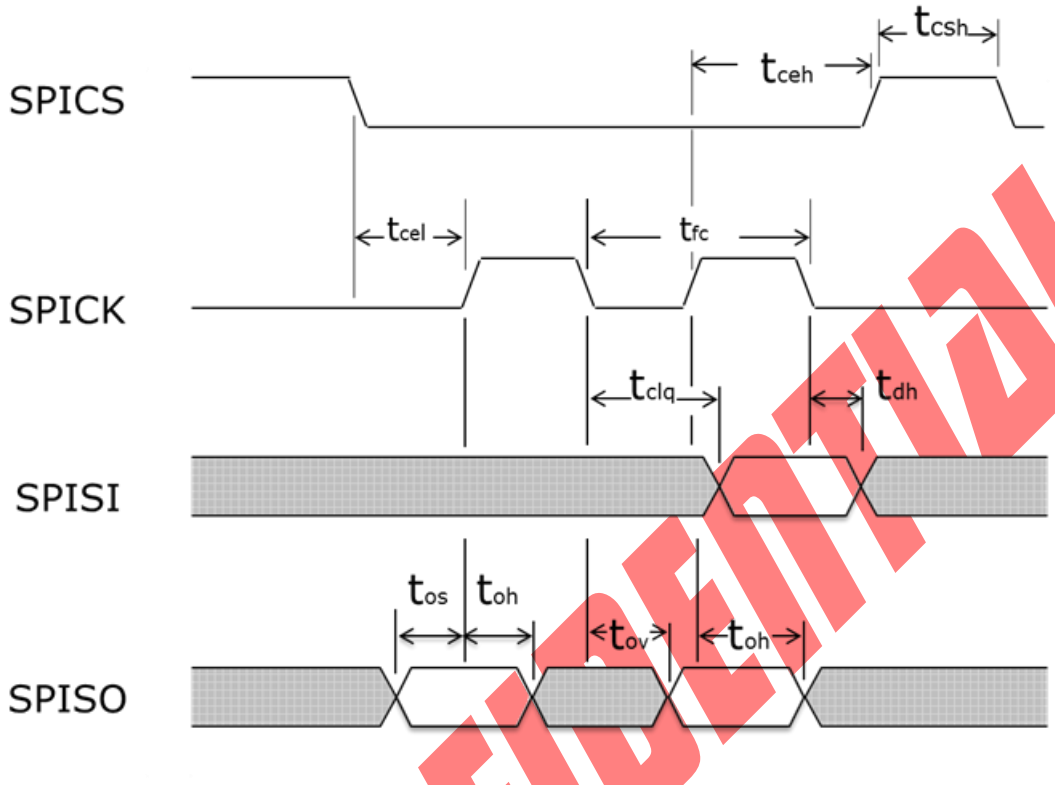

Figure 3 – SPI Timing

SPI Timing (7.8125 MHZ Operation)

Symbol	Parameters	Min	Typ	Max	Units
f_{CT}	Clock frequency		7.8125		MHz
t_{csh}	Chip enable (**SPICS**) high time	800			ns
t_{clq}	Clock to input data			20	ns
t_{dh}	Input data hold time	0			ns
t_{os}	Output setup time	20			ns
t_{oh}	Output hold time	10			ns
t_{ov}	Clock to output valid	5			ns
t_{cel}	Chip enable (**SPICS**) low to first clock	72			ns
t_{ceh}	last clock to chip enable (**SPICS**) high	72			ns

*Fast read mode must be supported.

General Reflow Profile Guidelines

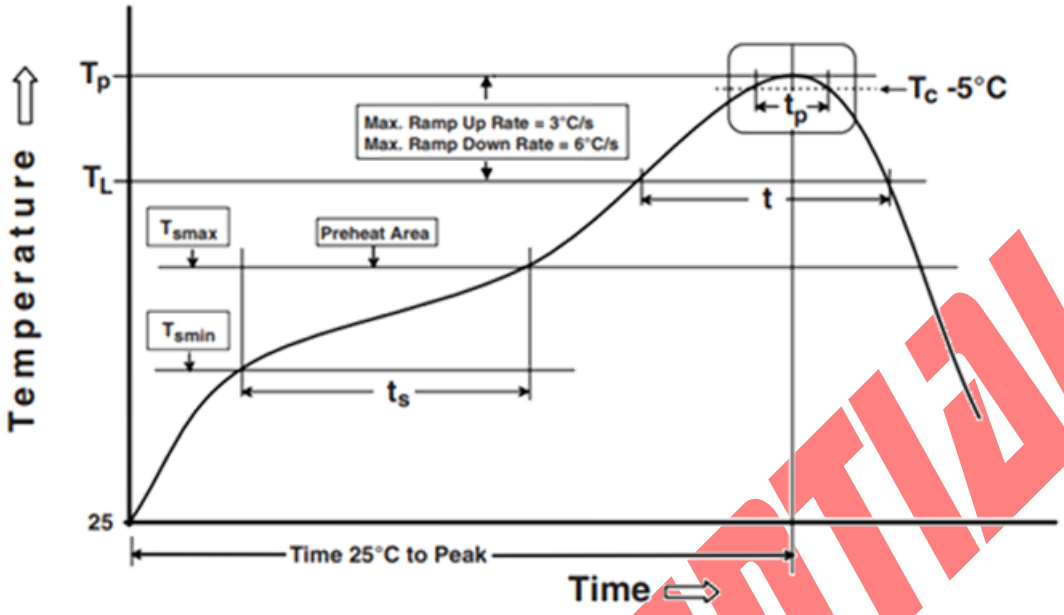

Figure 4 – Reflow

Classification Profiles

Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217 °C 60-150 seconds
Peak package body temperature (T_p)	260 °C
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

Reference: JSTD-020E

***Note 1:** All temperatures refer to the center of package, measured on package body surface
***Note 2:** The reflow condition may vary with PCB design; pitch; size; reflow; condition; solder and supplier, please contact your solder, reflow and vendors.

Package Mechanical Specifications (VL830)

Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.95	1.03	1.11
A1	0.11	0.16	0.21
A2	0.81	087	0.93
A3	0.42	0.45	0.48
c	0.37	0.42	0.47
D	9.90	10.00	10.10
E	9.90	10.00	10.10
D1	---	9.00	---
E1	---	9.00	---
e	---	0.50	---
b	0.22	0.27	0.32
aaa		0.15	
ccc		0.20	
ddd		0.08	
eee		0.15	
fff		0.05	

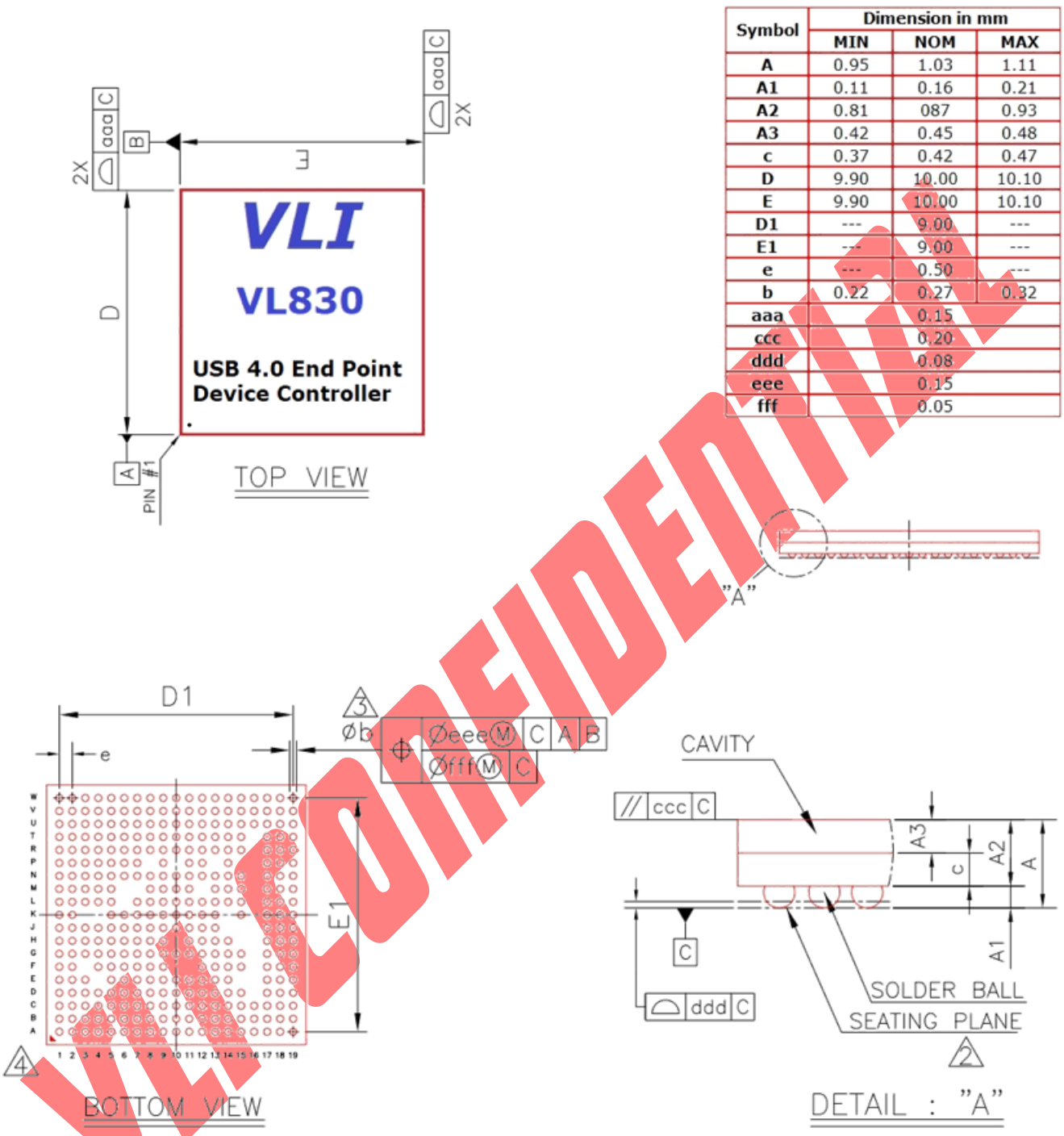

Figure 5 – Mechanical Specification – FCCSP (10x10x1.03 mm) Package

Package Top Side Marking & Ordering Information

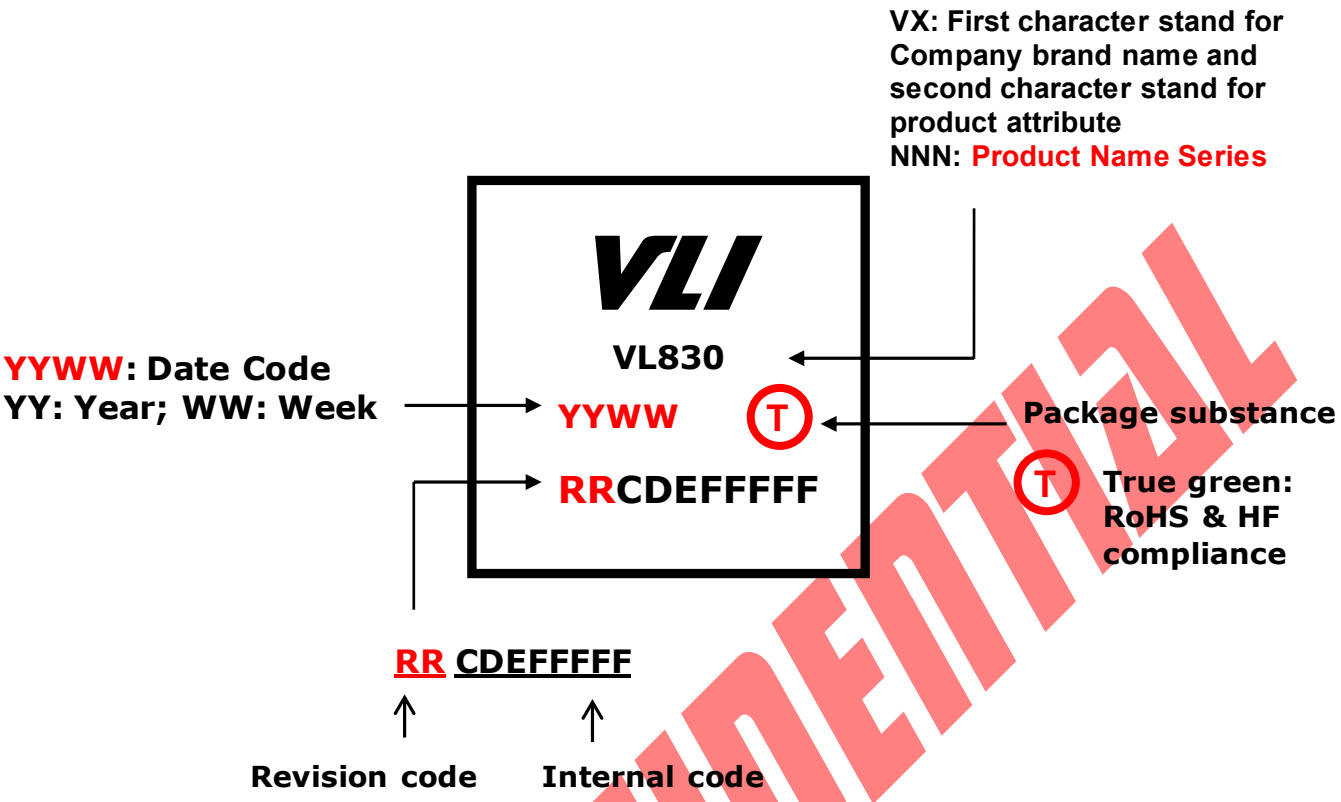

Figure 6 – Package Top Side Marking

Ordering Information

Please contact VIA Labs sales representative or distributor in your region for ordering part number details.

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