



## N-Channel Enhancement-Mode Vertical DMOS Power FETs

### Ordering Information

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
450V	4Ω	2A	VN0345N1	VN0345N2	VN0345N5	VN0345ND
500V	4Ω	2A	VN0350N1	VN0350N2	VN0350N5	VN0350ND

### Features

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

### Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

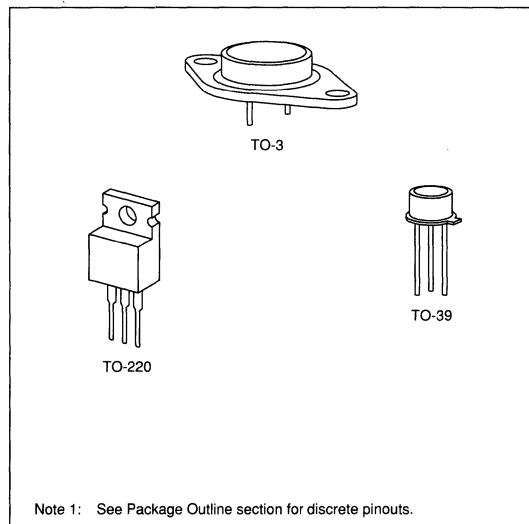
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

### Package Options

(Note 1)



Note 1: See Package Outline section for discrete pinouts.

### Absolute Maximum Ratings

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\*Distance of 1.6 mm from case for 10 seconds.

## Thermal Characteristics

Package	$I_D$ (continuous)*	$I_D$ (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	$\theta_{jC}$ $^\circ\text{C/W}$	$\theta_{jA}$ $^\circ\text{C/W}$	$I_{DR}$	$I_{DRM}^*$
TO-3	2.5A	5.0A	100W	1.25	30	2.5A	5.0A
TO-39	0.35A	4.5A	6W	20.8	125	0.35A	4.5A
TO-220	1.5A	5.0A	50W	2.5	40	1.5A	5.0A

\* $I_D$  (continuous) is limited by max rated  $T_J$ .

## Electrical Characteristics (@ 25°C unless otherwise specified)

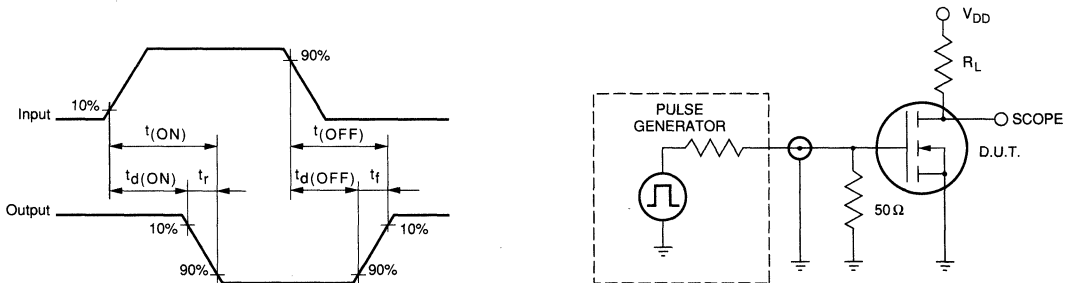
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
$BV_{DSS}$	Drain-to-Source Breakdown Voltage	VN0350	500		V	$V_{GS} = 0, I_D = 10\text{mA}$
		VN0345	450			
$V_{GS(th)}$	Gate Threshold Voltage	2		4	V	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-7	-9	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 10\text{mA}$
$I_{GSS}$	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
$I_{DSS}$	Zero Gate Voltage Drain Current			100	$\mu\text{A}$	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				2	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current		3.5		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
		2	4.5			$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		3.5		$\Omega$	$V_{GS} = 5\text{V}, I_D = 0.5\text{A}$
			2.8	4		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		1	1.5	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
$G_{FS}$	Forward Transconductance	500	1000		m $\Omega$	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$
$C_{ISS}$	Input Capacitance		550	650	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
$C_{OSS}$	Common Source Output Capacitance		50	75		
$C_{RSS}$	Reverse Transfer Capacitance		15	25		
$t_{d(ON)}$	Turn-ON Delay Time		8	15	ns	$V_{DD} = 25\text{V}$ $I_D = 1\text{A}$ $R_S = 50\Omega$
$t_r$	Rise Time		8	15		
$t_{d(OFF)}$	Turn-OFF Delay Time		65	100		
$t_f$	Fall Time		15	25		
$V_{SD}$	Diode Forward Voltage Drop		1.3	1.8		
$t_{rr}$	Reverse Recovery Time		450		ns	$V_{GS} = 0, I_{SD} = 0.5\text{A}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 $\mu\text{s}$  pulse, 2% duty cycle.)

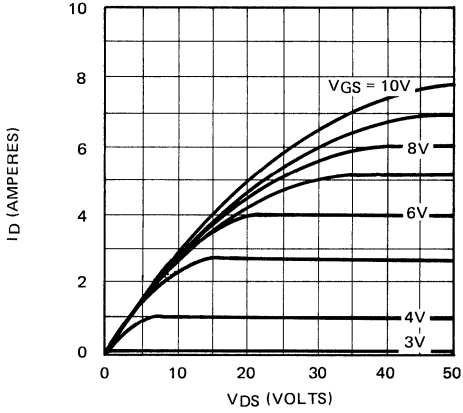
Note 2: All A.C. parameters sample tested.

## Switching Waveforms and Test Circuit

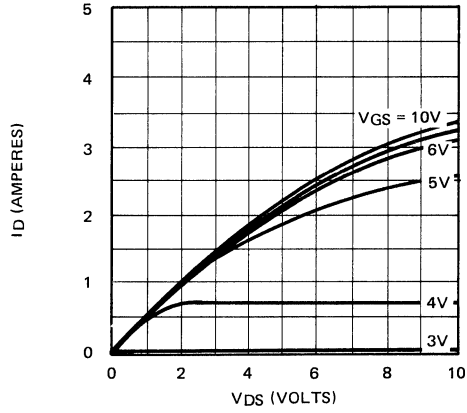


# Typical Performance Curves

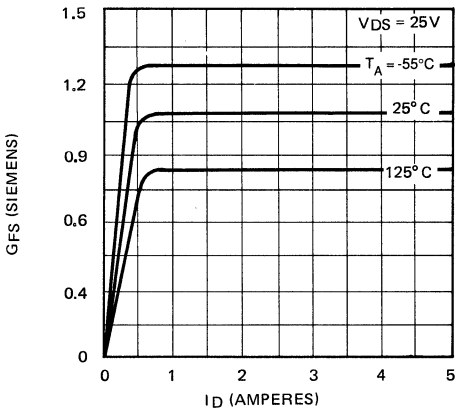
Output Characteristics



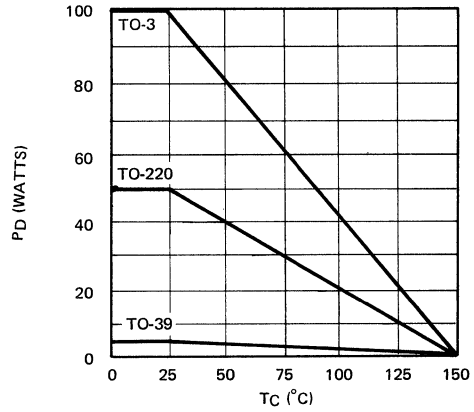
Saturation Characteristics



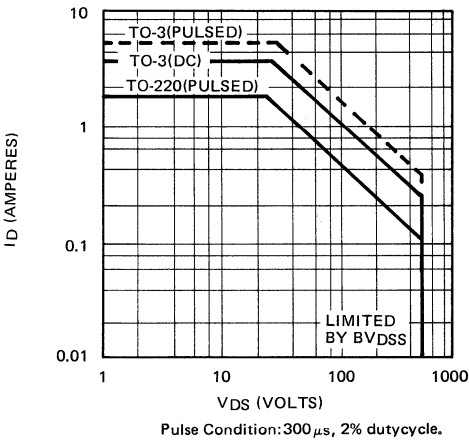
Transconductance Vs. Drain Current



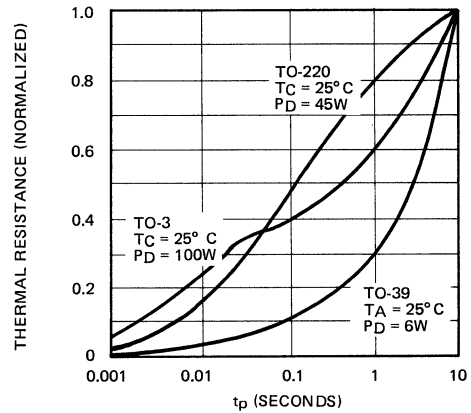
Power Dissipation Vs. Case Temperature



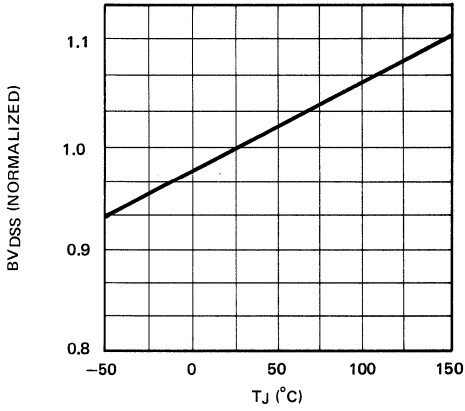
Maximum Rated Safe Operating Area



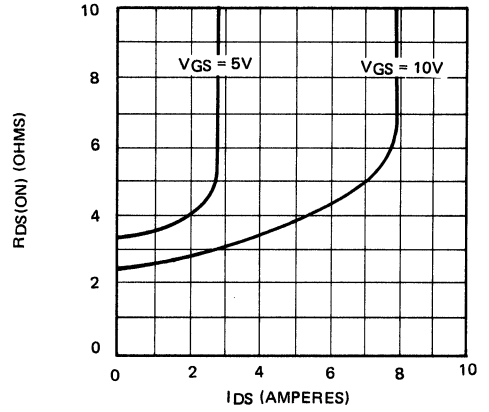
Thermal Response Characteristics



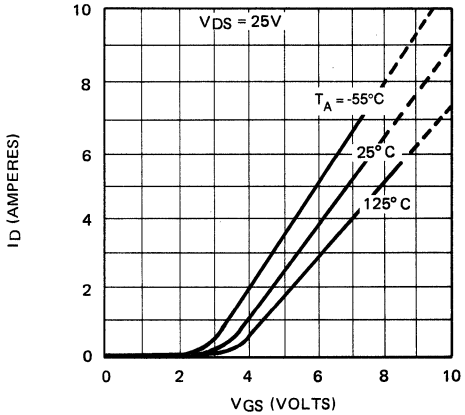
**BVDSS Variation with Temperature**



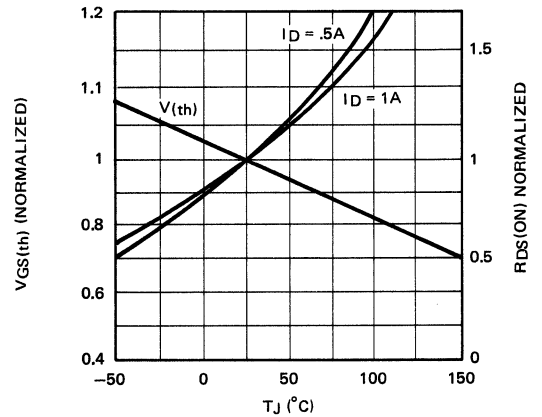
**ON - Resistance Vs. Drain Current**



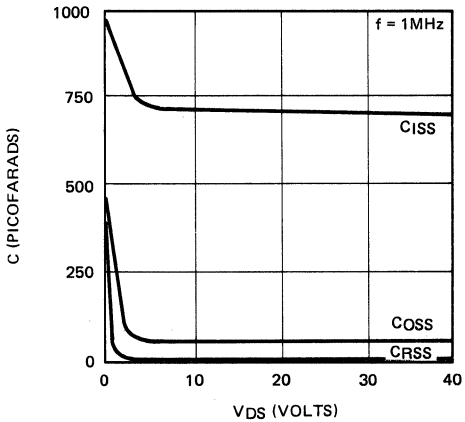
**Transfer Characteristics**



**V(th) and RDS Variation with Temperature**



**Capacitance Vs. Drain-to-Source Voltage**



**Gate Drive Dynamic Characteristics**

