Supertex inc.

VN03F

T-39-11

N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-3	TO-220	Dice
550V	6Ω	1.5A	VN0335N1	VN0335N5	VN0335ND
600V	6Ω	1.5A	VN0360N1	VN0360N5	VN0360ND

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

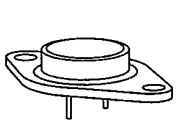
These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

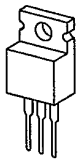
Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options (Note 1)



TO-3



TO-220

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

T-39-11

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ T_C = 25°C	θ_{jc} °C/W	θ_{ja} °C/W	I_{DR}	I_{DRM}*
TO-3	2.5A	6A	100W	1.25	30	2.5A	6A
TO-220	1.5A	6A	50W	40	40	1.5A	6A

*I_D (continuous) is limited by max rated T_j.

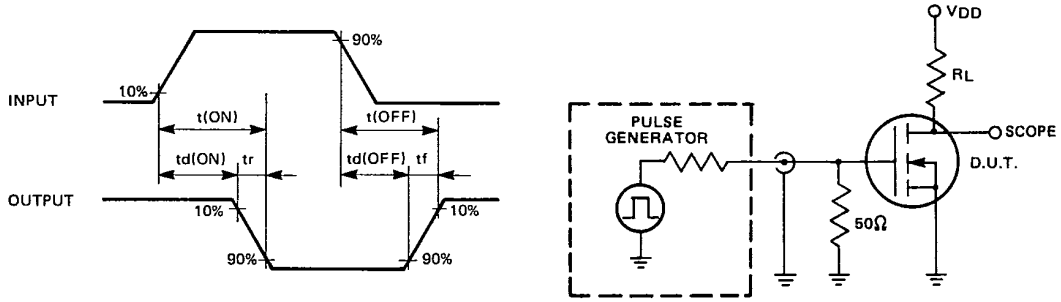
Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BVDSS	Drain-to-Source Breakdown Voltage	VN0360	600			V	VGS= 0, ID = 10mA
		VN0355	550				
VGS(th)	Gate Threshold Voltage		2		4	V	VGS = VDS, ID = 10mA
ΔVGS(th)	Change in VGS(th) with Temperature			-4.8	-6.0	mV/°C	VGS = VDS, ID = 10mA
IGSS	Gate Body Leakage				100	nA	VGS = ±20V, VDS = 0
IDSS	Zero Gate Voltage Drain Current				100	μA	VGS = 0, VDS = Max Rating
					2	mA	VGS = 0, VDS = 0.8 Max Rating, TA = 125°C
ID(ON)	ON-State Drain Current			1.3		A	VGS = 5V, VDS = 25V
			1.5	3.0			VGS = 10V, VDS = 25V
RDS(ON)	Static Drain-to-Source ON-State Resistance			5.5		Ω	VGS = 5V, ID = 0.25A
				4.5	6.0		VGS = 10V, ID = 0.5A
ΔRDS(ON)	Change in RDS(ON) with Temperature			1	2	%/°C	VGS = 10V, ID = 0.5A
GFS	Forward Transconductance		0.5	1		℧	VDS = 25V, ID = 0.5A
CISS	Input Capacitance			550	650	pF	VGS = 0, VDS = 25V, f = 1MHz
COSS	Common Source Output Capacitance			75	125		
CRSS	Reverse Transfer Capacitance			25	50		
td(ON)	Turn-ON Delay Time			8	15	ns	VDD = 25V, ID = 0.5A, RS = 50Ω
tr	Rise Time			8	15		
td(OFF)	Turn-OFF Delay Time			65	100		
tf	Fall Time			12	25		
VSD	Diode Forward Voltage Drop			1.1	1.5	V	VGS = 0, ISD = 5A
trr	Reverse Recovery Time			450		ns	VGS = 0, ISD = 5A

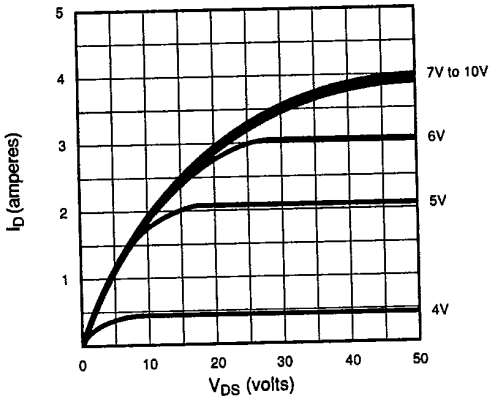
Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

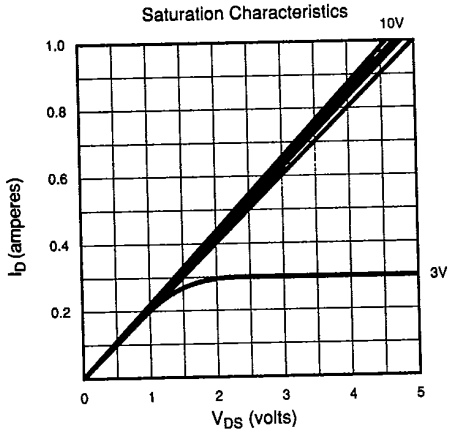


Typical Performance Curves

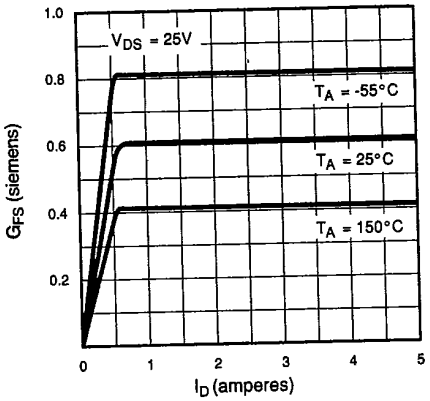
Output Characteristics



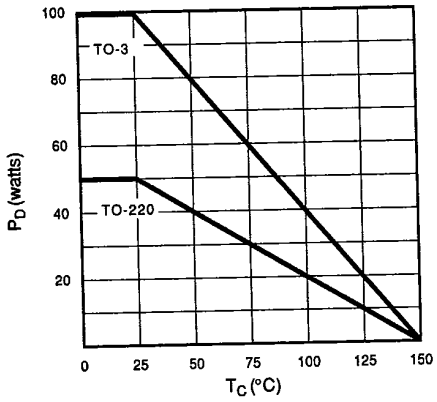
Saturation Characteristics



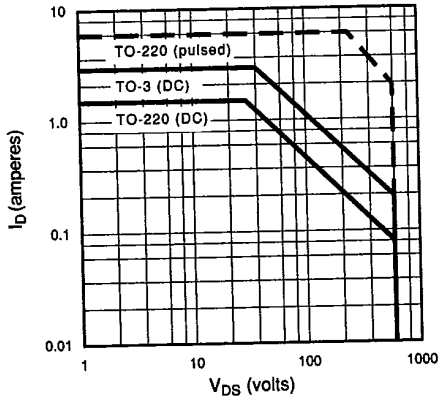
Transconductance vs. Drain Current



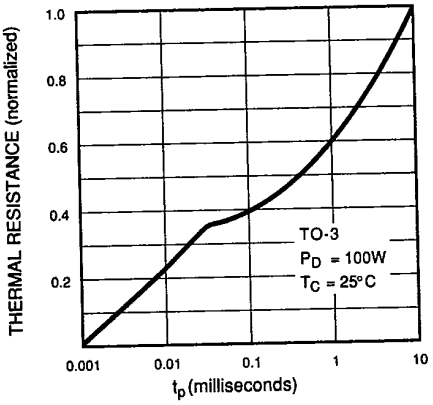
Power Dissipation vs. Case Temperature



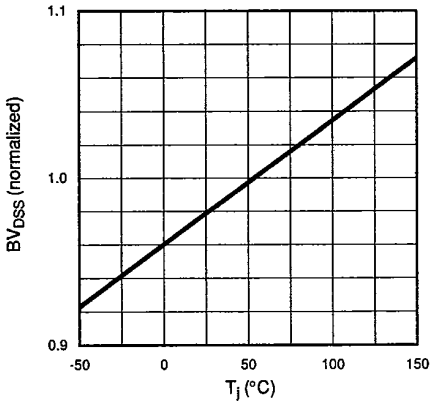
Maximum Rated Safe Operating Area



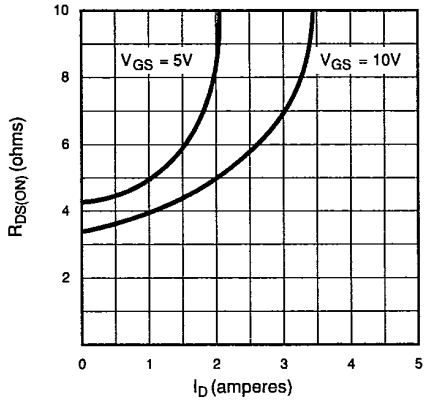
Thermal Response Characteristics



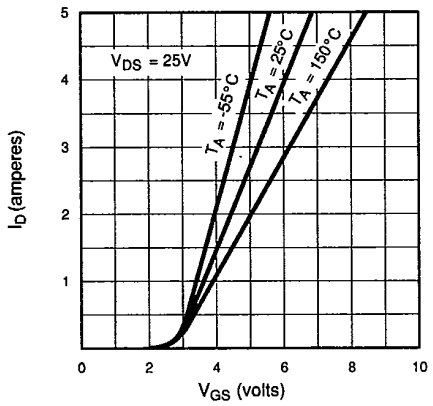
BV$_{DSS}$ Variation with Temperature



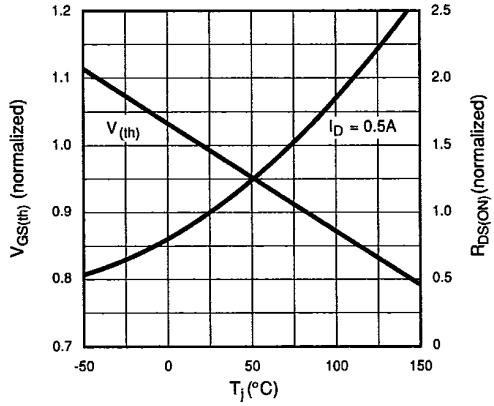
On-Resistance vs. Drain Current



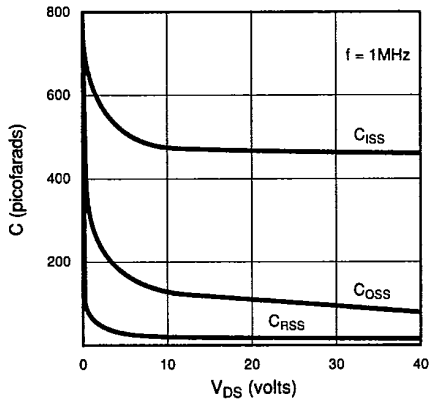
Transfer Characteristics



$V_{(th)}$ and R_{DS} Variation with Temperature



Capacitance vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics