N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package
			TO-92
60V	3Ω	1.5A	VN0606L
60V	5Ω	0.75A	VN0610LL

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{ISS} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

Package Options

(Note 1)

TO-92

Note 1: See Package Outline section for discrete pinouts.

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	±40V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ T_C = 25°C	θ_{ja} °C/W	θ_{jc} °C/W
TO-92	0.3A	2.0A	.4W	312.5	51

*I_D (continuous) is limited by max rated T_j.

Electrical Characteristics (@ 25°C unless otherwise specified)

(Notes 1 and 2)

Symbol	Parameter		Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0610	60			V	I_D = 100μA, V_{GS} = 0
		VN0606	60			V	I_D = 10μA, V_{GS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	VN0610	0.8		2.5	V	V_{GS} = V_{DS}, I_D = 1mA
		VN0606	0.8		2.0	V	V_{GS} = V_{DS}, I_D = 1mA
I_{GSS}	Gate Body Leakage				100	nA	V_{GS} = ±15V, V_{DS} = 0
I_{DSS}	Zero Gate Voltage Drain Current				10	μA	V_{GS} = 0V, V_{DS} = Max Rating
					500		V_{GS} = 0V, V_{DS} = Max Rating, T_A = 125°C
$I_{D(ON)}$	ON-State Drain Current	VN0610	0.75			A	V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
		VN0606	1.5				V_{GS} = 10V, V_{DS} ≥ 2 $V_{DS(ON)}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance	VN0610			7.5	Ω	V_{GS} = 5V, I_D = 0.2A
		VN0610			5		V_{GS} = 10V, I_D = 0.5A
		VN0606			3		V_{GS} = 10V, I_D = 1A
G_{FS}	Forward Transconductance		170			m℧	V_{DS} ≥ 2 $V_{DS(ON)}$, I_D = 0.5A
C_{ISS}	Input Capacitance				50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1MHz
C_{OSS}	Common Source Output Capacitance				25		
C_{RSS}	Reverse Transfer Capacitance				5		
$t_{(ON)}$	Turn-ON Time				10	ns	V_{DD} = 25V, I_D = 1A, R_S = 50Ω
$t_{(OFF)}$	Turn-OFF Time				10		
V_{SD}	Diode Forward Voltage Drop	VN0610		−1.2		V	I_{SD} = −0.47A, V_{GS} = 0
		VN0606		−.85			I_{SD} = −0.2A, V_{GS} = 0

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit