



**N-Channel Enhancement-Mode Vertical DMOS Power FETs**

**Ordering Information**

BV <sub>DSS</sub> / BV <sub>DGS</sub>	R <sub>DS(ON)</sub> (max)	I <sub>D(ON)</sub> (min)	Order Number / Package			
			TO-3	TO-39	TO-220	Dice
160V	3Ω	2.0A	VN1116N1	VN1116N2	VN1116N5	VN1116ND
200V	3Ω	2.0A	VN1120N1	VN1120N2	VN1120N5	VN1120ND

**Features**

- Freedom from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C<sub>ISS</sub> and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-Channel devices

**Advanced DMOS Technology**

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

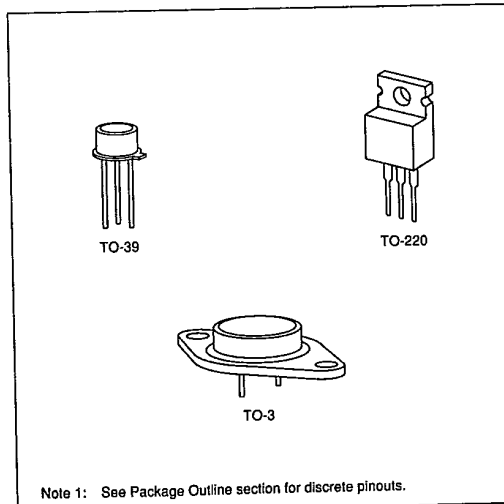
Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

**Applications**

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

**Package Options**

(Note 1)



Note 1: See Package Outline section for discrete pinouts.

**Absolute Maximum Ratings**

Drain-to-Source Voltage	BV <sub>DSS</sub>
Drain-to-Gate Voltage	BV <sub>DGS</sub>
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

\*Distance of 1.6 mm from case for 10 seconds.

T-39-11

**Thermal Characteristics**

Package	I <sub>D</sub> (continuous)*	I <sub>D</sub> (pulsed)*	Power Dissipation @ T <sub>C</sub> = 25°C	θ <sub>JA</sub> °C/W	θ <sub>JC</sub> °C/W	I <sub>DR</sub>	I <sub>DRM</sub> *
TO-3	3A	4.5A	100W	9.1	1.25	3A	4.5A
TO-39	1A	2.5A	4W	33	31	1A	2.5A
TO-220	2A	3.5A	45W	11.4	2.7	2A	3.5A

\*I<sub>D</sub> (continuous) is limited by max rated T<sub>J</sub>.

**Electrical Characteristics (@ 25°C unless otherwise specified)**

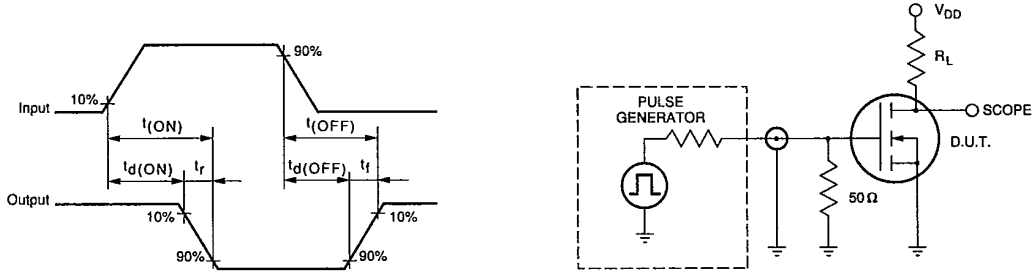
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	VN1116	160		V	V <sub>GS</sub> = 0, I <sub>D</sub> = 5mA
		VN1120	200			
V <sub>GS(th)</sub>	Gate Threshold Voltage	1		3	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 5mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with Temperature		-3.5	-6	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 5mA
I <sub>GSS</sub>	Gate Body Leakage			100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			50	μA	V <sub>GS</sub> = 0, V <sub>DS</sub> = Max Rating
				5	mA	V <sub>GS</sub> = 0, V <sub>DS</sub> = 0.8 Max Rating T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	ON-State Drain Current	1	1.5		A	V <sub>GS</sub> = 5V, V <sub>DS</sub> = 25V
		2	2.5			V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance		3.5	4	Ω	V <sub>GS</sub> = 5V, I <sub>D</sub> = 0.5A
			2.5	3		V <sub>GS</sub> = 10V, I <sub>D</sub> = 1A
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with Temperature		0.6	1	%/°C	V <sub>GS</sub> = 10V, I <sub>D</sub> = 1A
G <sub>FS</sub>	Forward Transconductance	0.2	0.4		∅	V <sub>DS</sub> = 25V, I <sub>D</sub> = 0.5A
C <sub>ISS</sub>	Input Capacitance		300	350	pF	V <sub>GS</sub> = 0, V <sub>DS</sub> = 25V f = 1 MHz
C <sub>OSS</sub>	Common Source Output Capacitance		75	150		
C <sub>RSS</sub>	Reverse Transfer Capacitance		20	30		
t <sub>d(ON)</sub>	Turn-ON Delay Time		20	30		
t <sub>r</sub>	Rise Time		3	10	ns	V <sub>DD</sub> = 25V I <sub>D</sub> = 2A R <sub>S</sub> = 50Ω
t <sub>d(OFF)</sub>	Turn-OFF Delay Time		32	40		
t <sub>f</sub>	Fall Time		8	15		
V <sub>SD</sub>	Diode Forward Voltage Drop		0.7	1.0	V	V <sub>GS</sub> = 0, I <sub>SD</sub> = 100mA
t <sub>rr</sub>	Reverse Recovery Time		400		ns	V <sub>GS</sub> = 0, I <sub>SD</sub> = 0.1A

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)

Note 2: All A.C. parameters sample tested.

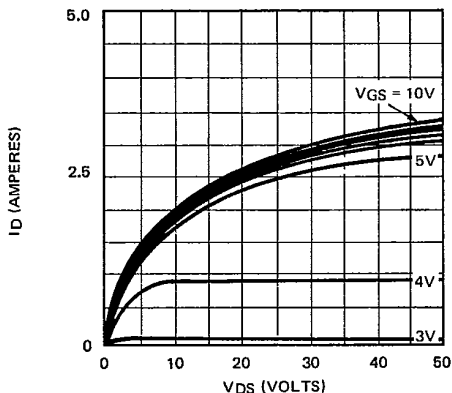
**Switching Waveforms and Test Circuit**



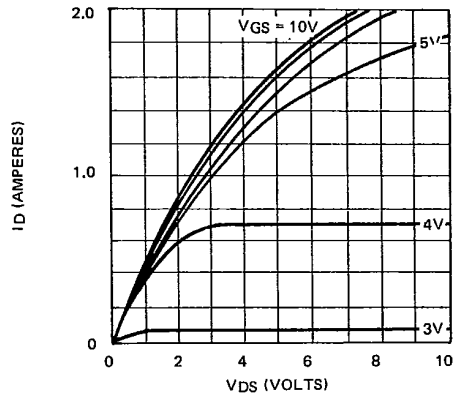
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Typical Performance Curves

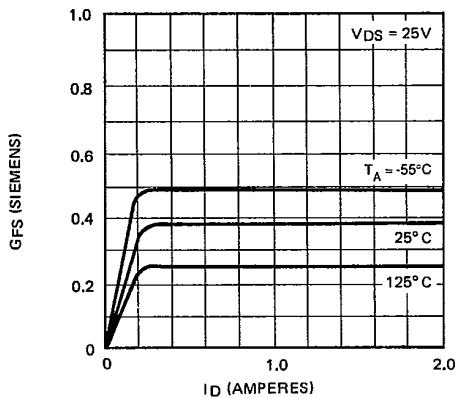
Output Characteristics



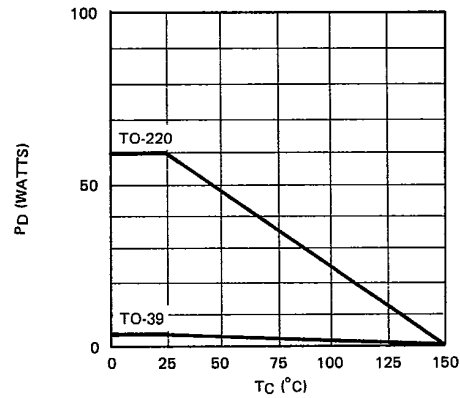
Saturation Characteristics



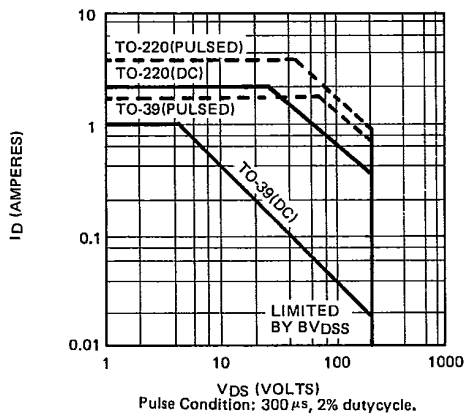
Transconductance Vs. Drain Current



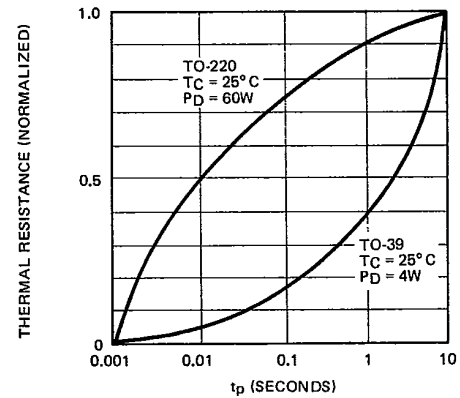
Power Dissipation Vs. Case Temperature



Maximum Rated Safe Operating Area

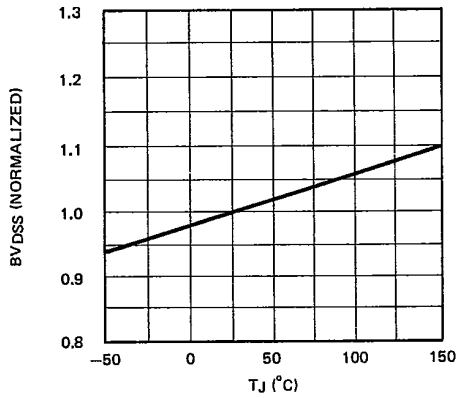


Thermal Response Characteristics

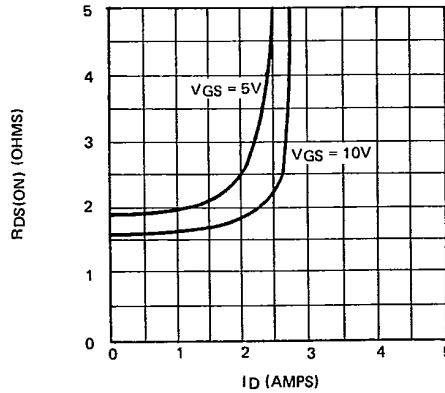


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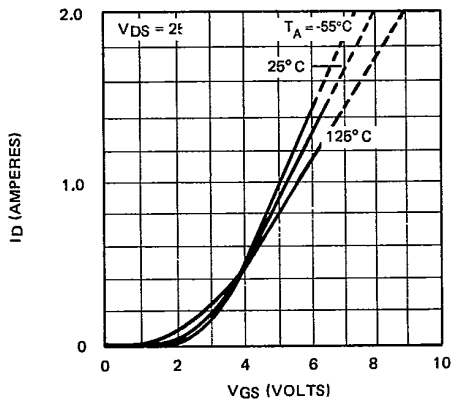
BVDSS Variation with Temperature



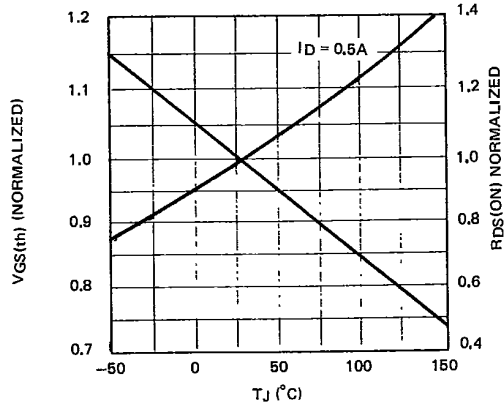
ON-Resistance Vs. Drain Source Current



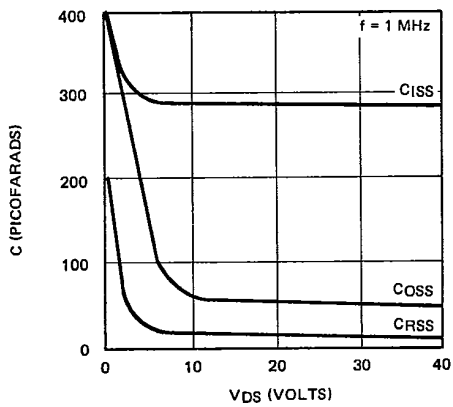
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

